FINGERPRINTS

CONFIDENTIAL

Product Specification

FPC1020

Revision PB3

Contents

1 Overview

The FPC1020 is a capacitive touch fingerprint sensor with low energy consumption, specifically developed and optimized for mobile devices. The FPC1020 sensor offers smartphone, tablet and PC OEMs unprecedented performance, along with the opportunity to relieve consumers from the burden of using PIN codes and passwords for user verification.

The FPC1020 sensor includes the following features:

- Fingerprint area sensor
- Superior 3D image quality
- 508 dpi resolution
- 192 x 192 pixels with 8 bit depth
- High-speed SPI interface
- Ultra-low energy consumption
- 1.8 Volt operation
- Extended ESD range 30kV
- Wake-up functionality

The FPC1020 enables smartphone and tablet OEMs to offer consumers a compelling user experience combining great convenience and security with excellent performance and appealing design.

1.1 Technical features

The following table gives an overview of the technical features of an FPC1020 sensor.

Parameter	Description	Value	Unit
Size sensing array		192*192	Pixel
Pixel resolution	256 gray scale levels	8	Bit
Interface	Serial SPI + interrupt	4+1	Pin
Supply voltage	VDD, typical	1.8	V
TX Supply voltage	Internal generated	<3.3	V
Supply current image	Typical	~5	mA
Supply current sleep mode	Typical when detecting finger	10	µA
Supply current deep sleep	Typical	<10	µA
Clock frequency	Serial SPI communication	<12	MHz
Operating temperature		- 40 … + 85	°C
Storage temperature		- 40 … + 85	°C
Resolution		508	DPI

Table 1: Technical features

Note: Dimensional data is based on nominal values. Tolerance ranges are defined in the corresponding mechanical drawing.

2 Functional description

This chapter includes a functional description of an FPC1020 sensor.

2.1 Pad assignment

This section gives an overview of pad assignment for inputs and outputs for an FPC1020 sensor.

No.	Name	Description
1	VDDIO	IO power supply
2	VSSIO	IO ground
3	SPICLK	SPI clock
4	CS_N	SPI chip select
5	MISO	SPI Data out
6	MOSI	SPI Data in
7	-	-
8	RST_N	System reset
9	VSS	Ground
10	VDD	Power supply

No.	Name	Description
11	IRQ	Interrupt request
12	TEST	Digital test
13	-	-
14	VDDA	Analog power supply
15	-	-
16	-	-
17	VSSA	Analog ground
18	TXOUT	Drive signal
19	VDDTX	Power Supply TXOUT

Table 2: I/O Pad assignment

2.2 Absolute maximum ratings

The following table describes the absolute maximum ratings for an FPC1020 sensor.

Parameter	Absolute maximum value	Unit
Supply voltage VDD	1.8	V
Input voltage	1.8 - 3.3	V
Output voltage	< 3.3	V
Total power dissipation	50 mW	mW

Table 3: Absolute maximum ratings

Stress beyond the absolute maximum ratings values listed in Table 3 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods, may affect device reliability.

Operation of the device conditions beyond those indicated as normal operation in this specification, is not supported.

3 Electrical characteristics

The following tables show the electrical characteristics of an FPC1020 sensor.

3.1 1.8 V I/O Applications

The following tables show the recommended operating conditions for 1.8V I/O applications measured at room temperature (RT).

3.1.1 Power Supply

The following table gives an overview of power supplies for 1.8V I/O applications.

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
VDD	Voltage supply (Core)		1.62	1.8	1.98	V
VDDIO	Voltage supply (IOs)		1.62	1.8	1.98	V
VDDA	Voltage supply (Analog)		1.62	1.8	1.98	V
IDD	Current supply, total	VDDIO = 1.8V, Image		6.2		mA
		VDDIO = 1.8V, Sleep		2.6		µA
		VDDIO = 1.8V, Deep Sleep		1.3		µA

Table 4: Power Supply for 1.8V I/O applications

The values for total current supply correspond to the average value measured during image readout, with default parameter settings.

3.1.2 Digital Inputs

The following table gives an overview of the digital inputs for 1.8V I/O applications.

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
VIL	Logic '0' voltage	-	-0.3	-	0.35*VDD	V
VIH	Logic '1' voltage	-	0.65*VDD	-	VDD+0.3	V
IIL	Input leakage current	-	-	-	±10	µA

Table 5: Digital Inputs for 1.8 V I/O applications

3.1.3 Digital Outputs

The following table gives an overview of the digital outputs for 1.8V I/O applications.

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
VOL	Logic '0' output voltage	-	-	-	0.45	V
VOH	Logic '1' output voltage	-	VDDIO-0.45	-	-	V

Table 6: Digital Outputs for 1.8 V I/O applications

3.2 3.3V I/O Applications

The following tables show the Recommended Operating Conditions for 3.3V I/O applications measured at room temperature (RT).

3.2.1 Power Supplies

The following table gives an overview of power supplies for 3.3V I/O applications.

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
VDD	Voltage supply (Core)		1.62	1.8	1.98	V
VDDIO	Voltage supply (IOs)		2.97	3.3	3.63	V
VDDA	Voltage supply (Analog)		1.62	1.8	1.98	V
IDD	Total current supply	VDDIO = 3.3V, Image		6.2		mA
		VDDIO = 3.3V, Sleep		2.6		µA
		VDDIO = 3.3V, Deep Sleep		1.3		µA

Table 7: Recommended operating conditions for power supplies for 3.3 V I/O applications

Total current supply corresponds to the average value measured during image readout, with default parameter settings.

3.2.2 Digital Inputs

The following table gives an overview of the digital inputs for 3.3V I/O applications.

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VIL	Logic '0' voltage	-0.3	-	0.8	V
VIH	Logic '1' voltage	2.0	-	3.6	V
IIL	Input leakage current	-	-	±10	µA

Table 8: Recommended operating conditions for digital inputs for 3.3 V I/O applications

3.2.3 Digital Outputs

The following table gives an overview of the digital outputs for 3.3V I/O applications.

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VOL	Logic '0' output voltage	-	-	0.4	V
VOH	Logic '1' output voltage	2.4	-	-	V

Table 9: Recommended operating conditions for digital outputs for 3.3 V I/O applications.

4 Functionality

This chapter describes the main functionality of the FPC1020 sensor chip, including:

- Analog to Digital conversion
- Command Interpretation
- Finger detection logic
- Host Interface
- Image properties
- Pixel Matrix Control
- Pixel Sensing Matrix
- Power Reset
- Voltage Boost

4.1 Sensor Chip Principal Block Diagram

The principal block diagram for the sensor chip is shown in Figure 1.

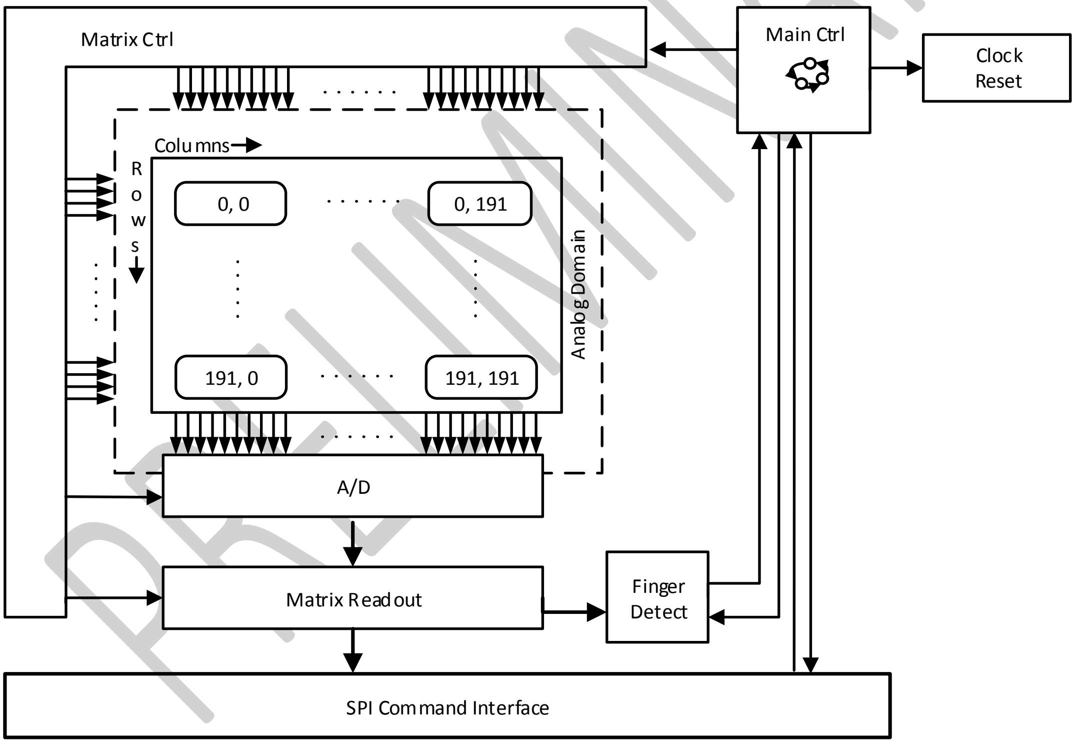

Figure 1: Sensor block diagram.

Key features of the pixel grid sensor include:

- Size: 192 columns x 192 rows
- Resolution: 508dpi (pixel area: 50µm x 50µm)

4.2 Power-on reset

The FPC1020 sensor requires a reset signal after power-up in order to reach a defined state. This occurs when the external signal, RST_N, is connected to the host, and released by the system after the sensor power-up.

Alternatively, an external capacitor, C, may be added and connected to ground, when used in conjunction with an internal pull-up resistance, R, as indicated in Figure 2.

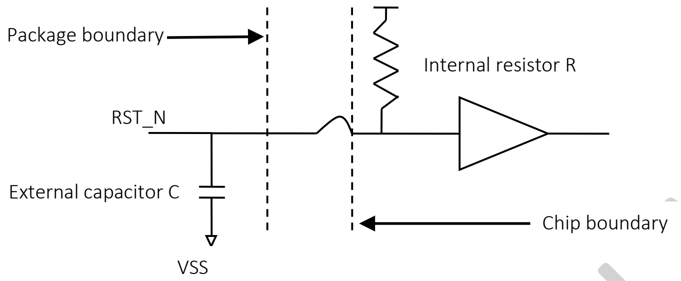

Figure 2: Power-on reset

The chip remains in reset state (RST_N low) by delaying the rise of the RST_N signal after VDD is turned on. Internal resistance depends on IO voltage and process variation.

The transition level from low to high for the RST_N IO for 1.8V VDDIO is shown in Table 10.

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VT+	Schmitt trigger Low to High threshold point	0.95	0.99	1.00	V
RPU	Pull- up Resistor	94	148	261	kohm

Table 10: Operating Conditions for RST_N I/O for 1.8V VDDIO

The transition level from low to high for the RST_N IO for 3.3V VDDIO is shown in Table 11.

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VT+	Schmitt trigger Low to High threshold point	0.95	0.99	1.00	V
RPU	Pull- up Resistor	94	148	261	kohm

Table 11: Operating Conditions for RST_N I/O for 3.3V VDDIO

4.3 Voltage Boost

The finger drive circuitry includes a voltage booster, which increases the internal voltage signal from 1.8V to a maximum of 3.3V. The voltage boost block requires an external decoupling on VDDTX. It recommended to supply this pin with external power (1.8V – 3.3V) instead of using the internally generated power.

4.4 Pixels

The pixels in the sensor matrix can be configured with host-controlled characteristics.

Default values enable basic operation without configuration.

4.5 ADC

The Analogue Digital Converter (ADC) has 8-bit resolution with programmable gain and shift for optimal operation range. Default values are set to enable basic operation without configuration.

4.6 Signal-to-noise Ratio

To verify the image quality and establish a proper signal-to-noise ratio (SNR), internal test functionality based on test patterns is implemented; Checkerboard and Inverted Checkerboard. To ensure conformity of the results, tests are always performed on these two internal test patterns.

4.7 Finger Detection

Reduced size sub-area sets are captured to detect if and where a finger is placed on the sensor, without doing a full image capture. This decreases capture response time and improves performance. The illustration in Figure 3 represents the sub-area distribution for finger detection.

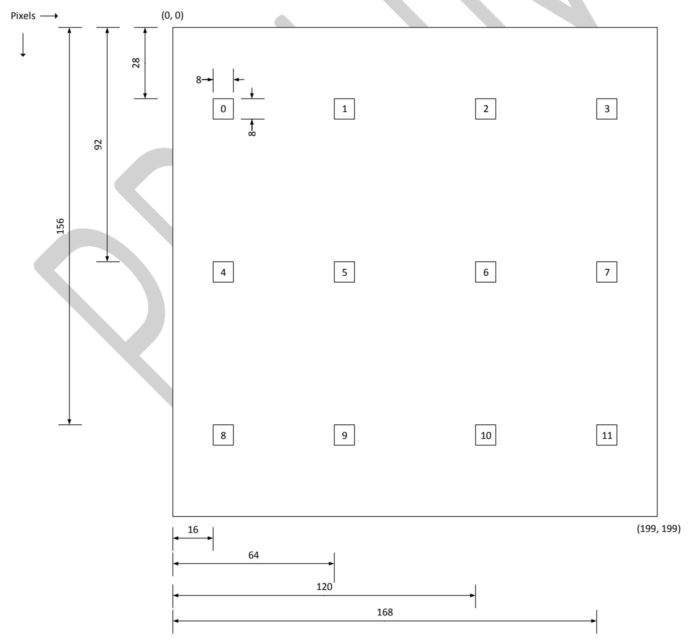

Figure 3: Finger detection sub-area distribution

Finger detection functionality includes the following areas:

- enhanced image capture
- optimally reduced power consumption
- response time and performance

The sensor uses 12 pre-defined sub-areas of 8x8 pixels each. These sub-areas are arranged in three evenly distributed rows. Each row has four areas evenly distributed horizontally.

4.7.1 Sensor Modes

Depending on the current sensor mode, finger detection will be performed differently:

Finger Query

A single snapshot of all 12 sub-areas is taken. The status register (*fngrPresentStatus*) is updated to indicate which areas are covered by a finger at that moment.

See section 5.4 for more information on the *fngrPresentStatus* register.

Wait for Finger

The Finger Query procedure is repeated until at least one sub-area is covered in one of the snapshots and no new covered areas are registered in the next snapshot. The *fngrPresentStatus* register is updated to indicate which areas are covered by a finger at that moment, and an interrupt is set. The idle period between repeated queries is configurable.

For more information on the *fngrPresentStatus* register, see section 5.4.

Sleep

The sensor wakes up at cyclic intervals, performing reduced measurement that only checks if areas 5 and 6 are covered. If a finger is detected on the sensor, the system will wake up and an interrupt is set. The idle period between wake-ups is configurable. For more information on sleep mode, see section 5.5.

4.8 Power Modes

Power modes for the FPC1020 sensor include:

- Idle mode (default)
- Image Capture
- Sleep mode
- Deep Sleep mode

An overview of the average, and peak current for each powermode is shown in Table 12.

Mode	Average current	Peak current
Idle Mode	0.63mA	< 7 mA
Image capture	6.2mA	< 7 mA
Sleep mode with finger detect	2.6µA	6.2 mA
Deep sleep mode	1.3µA	1.3 µA

Table 12: Current consumption for FPC1020 sensor power modes

The current is defined as the sum of the core voltages - analog and digital supply voltages - IDDA+IDD. The I/O current is not included.

4.9 Clock signals

The system clock is designed to generate 10MHz(+/-20%). The frequency is configurable in order to obtain (+/-20%) accuracy. The reset value of the trim register gives a frequency of 7.5 Mhz (+/-20%).

For more informaton on clock calibration, see section 5.7.

The low frequency oscillator is always active in order to support Sleep Mode and Deep Sleep Mode. The low frequency oscillator operates at a default frequency of 16 kHz(+/-60%). The frequency is adjustable to obtain the desired frequency with (+/-20%) accuracy. The frequency can also be lowered further in order to reduce power consumption during Sleep Mode even more.

4.9.1 Sleep Mode

In sleep mode, the system is not clocked. The system is awoken and clocked at regular intervals controlled by the low frequency oscillator.

4.9.2 Deep Sleep Mode

In deep sleep mode the system is not clocked at all and only the low frequency oscillator is running.

4.9.3 Shutdown Mode

In software controlled authentication systems, where all capture image tasks are initiated by software it is recommended to disconnect the power supply when sensor is not in use. This procedure will improve life time and overall reliability. All communication signals should also be set to low (GND) to avoid feeding the CMOS circuitry through the I/Os. This especially applies to active low signals.

Stand by procedure for FPC1020APA:

1. Disconnect sensor power supply VDD.
   Indicated as switch S10 in the reference layout.
2. Set SPI communication pins low.
   (SPI_DO, SPI_DI, SPI_CK)
   Set SPI_CS_N and RST_N low.

The start-up procedure is the reverse.

Start-up procedure

1. Connect sensor power supply VDD.
   Indicated as switch S10 in the reference layout.
2. Set SPI communication pins high.
   (SPI_DO, SPI_DI, SPI_CK)
   Set SPI_CS_N and RST_N high.

4.10 Host Communication Interface

For host control and fast image data readout, the sensor circuit includes a 4-wire Serial Peripheral Interface (SPI) and an interrupt signal. The sensor is designed to act as an SPI slave with CPHA = '0' and CPOL = '0'.

- When the internal clocks are calibrated, the SPI interface supports speeds of up to 12 Mbit/s.
- If internal clocks are not calibrated, data speeds up to 8 Mbit/s are supported.

The read-out time for reading a full image (36864 pixels) at 12 Mbit/s is approximately 30ms.

For more informaton on clock calibration, see section 5.7.

4.11 Command/address bytes

The FPC1020 sensor has an interpreter that processes host commands and writes to registers. Such operations typically consist of one command byte and one or more value bytes. Some basic commands only require a command byte, and some readout operations require a dummy value byte before the actual data is presented.

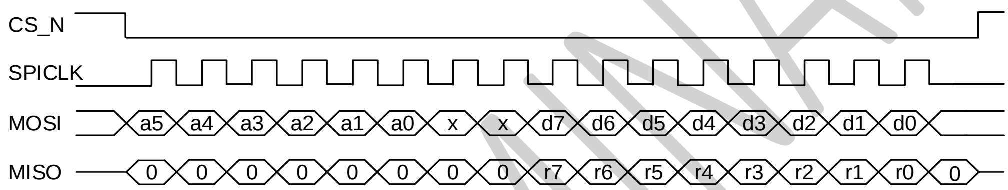

Figure 4: Principal SPI interface command/address with a command byte and one data byte.

The negative edge of CS_N indicates the start of a command or access to the register. Any command or register access must start with CS_N low and staying low throughout the command and data sequence.

For more information on supported commands, see section 6.1.

4.11.1 SPI Slave

The FPC1020 sensor is an SPI slave. The host must provide a SPICLK in order to read data. To keep the sensor active and transmitting data, the host must send dummy data on MOSI while reading data.

4.11.2 Configuration Register

A configuration register can be both read and write. Reading a configuration register alters values in the sensor and requires that suitable data be written back.

Configuration register changes are not allowed while the sensor is active.

4.12 System Interrupts signals

The following interrupt signals are produced by the sensor in different scenarios:

4.12.1 Reset interrupt

A reset interrupt signal is produced at reset release, for both soft reset, and power-up. The interrupt register is set to 0xFF.

4.12.2 Error interrupt

When an error is detected an error interrupt signal is produced. The error status register contains information on the type of error that occurred.

4.12.3 Image data ready

The image data ready signal indicates that the image capture data is ready to be read in the SPI buffer.

4.12.4 Finger Down

When a finger is detected, a finger down signal is sent. The Finger Status register contains more data.

4.12.5 Command Done

When a command is completed or aborted, a Command done signal is produced.

For more information on the interupt register, see section 7.2.1.

5 Use Case Scenarios

This chapter describes typical use case scenarios for a complete system, comprising a host and a sensor. In order to perform these operations, configuration registers must first be set up.

For a more detailed description on how to configure the sensor, see chapter 7.

5.1 Write to Setup Register

Writing to setup registers must be done before a sensor command can be performed. No changes can be made during the execution of any command sequence. A typical command sequence is shown in Figure 5.

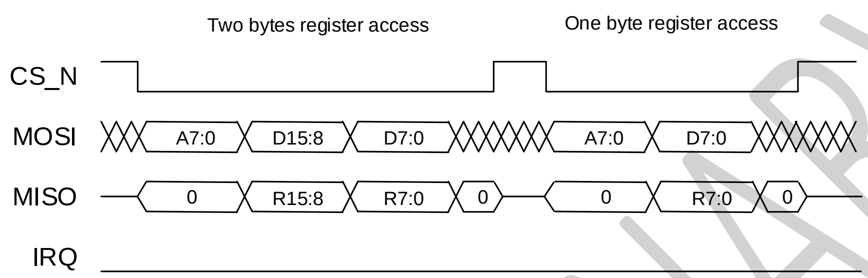

Figure 5: Principal SPI sequence for writing to a setup register

5.2 Image Capture

Image capture is the main functionality for the sensor. When captured image data is ready to be read, an interrupt is set. A typical image capture command sequence is outlined in Figure 6.

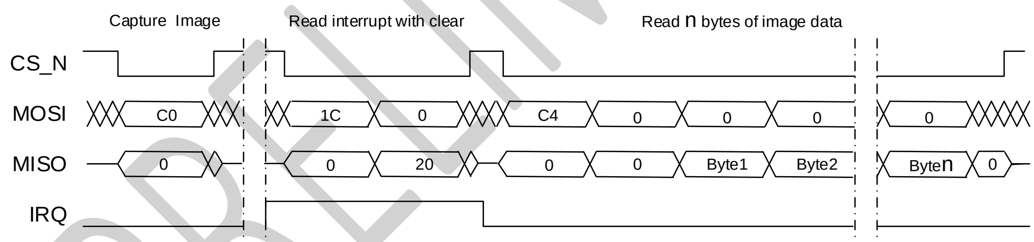

Figure 6: Principal SPI sequence for Image Capture

The *Read Image Data* command consists of the command byte, a dummy byte and the 192 *192 = 36 864 bytes of image data. The command may be interrupted at any time between data bytes. It is not a requirement that all data bytes must be read in one sequence.

This command may be cancelled at any time by sending an ACTIVATE_ACTIVATE_IDLE_MODE command.

A number of registers affect the captured image and must be configured in advance. See chapter 7 for more information on how to configure registers.

5.3 Finger present query

A finger present query is used to determine if a finger is present on the sensor. Captured pixel values are divided by 8 before being compared to the adjustable threshold value that is set in the register. See chapter 7 for more information on register configuration.

When the sensor is covered by a finger, the status register indicates which of the twelve sub-areas have surpassed the threshold value. A typical finger present query command sequence is outlined in Figure 7.

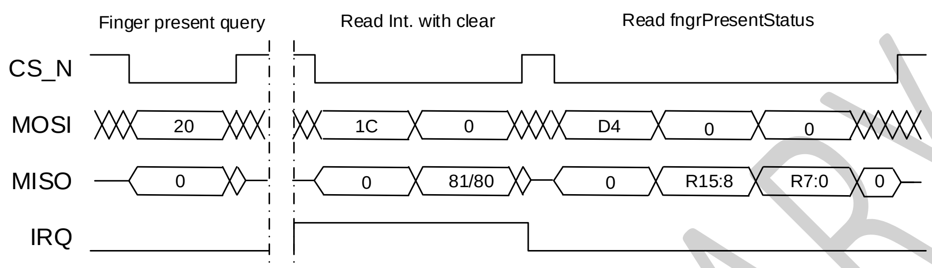

Figure 7: Principal SPI sequence for Finger Present Query

5.4 Wait for Finger

During the wait for finger command sequence, the sensor monitors changes to sensor coverage and determines the best instance to perform a full image capture. A typical wait for finger command sequence is outlined in Figure 8.

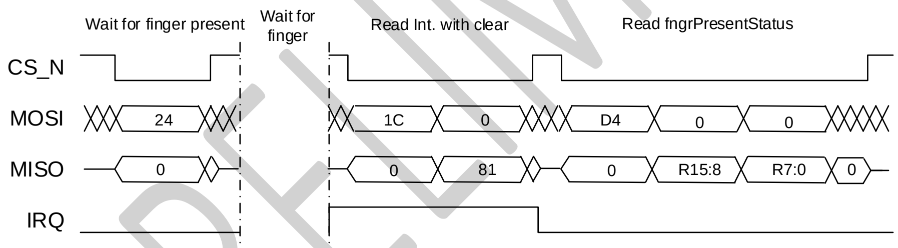

Figure 8: Principal SPI sequence for Wait for finger

The Wait for Finger command sequence may be cancelled at any time by sending an ACTIVATE_IDLE_MODE command. When returning to idle mode, an interrupt is set.

The sensor performs a finger present query at a fixed interval until a finger is placed on the sensor. See section 5.4.1 for more information on the time interval between queries.

5.4.1 Waiting Time Between Queries

When a finger present query is performed, up to 6.2 mA of current is consumed. Less current is used during the waiting time between queries approximately 0.63 mA. The *fngrDetCntr* register determines the waiting time between repeated finger queries, as indicated in Figure 9.

The adjustable range for the time is between 0 and 2 µs, approximately.

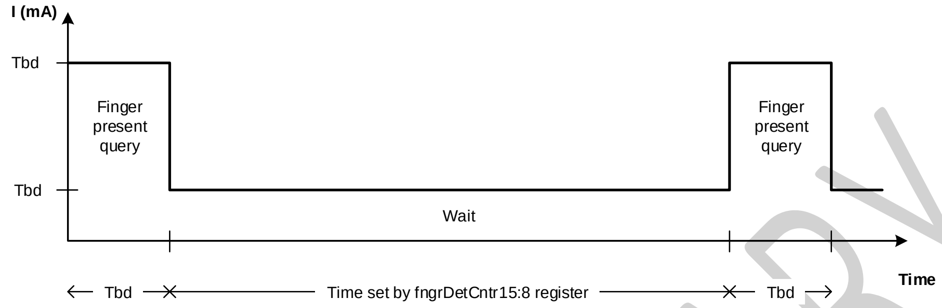

Figure 9: The fngrDetCntr register sets waiting time between finger present queries

5.5 Sleep Mode

Sleep mode is an essential element of the FPC1020 sensor for efficient system power usage. Sleep mode keeps the sensor in a low-power mode, periodically waking up to perform reduced finger present queries. If a finger is detected on the sensor, the sensor is brought out of sleep mode and into idle mode. When returning to idle mode, an interrupt is set.

Sleep mode may be cancelled by the host at any time by sending the ACTIVATE_IDLE_MODE command. When returning to idle mode, an interrupt is set. After sending the ACTIVATE_IDLE_MODE command, the host must wait until it receives the interrupt before issuing a new command sequence. Otherwise the ACTIVATE_IDLE_MODE command may be cancelled and the sensor remains in sleep mode.

A typical sleep mode command sequence is outlined in Figure 10.

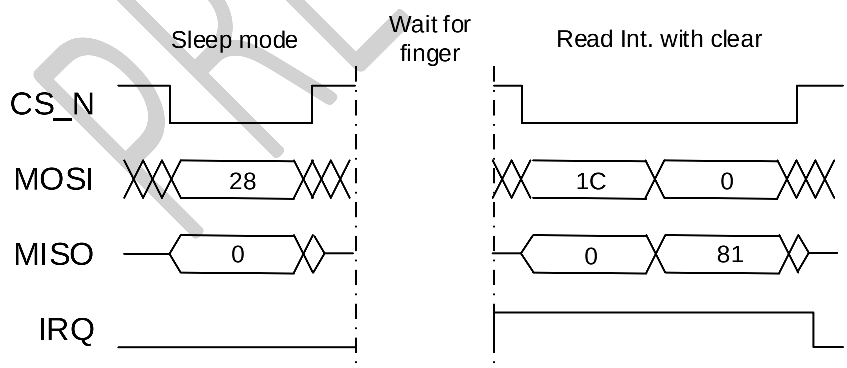

Figure 10: Principal SPI sequence for Sleep mode

5.5.1 Reduced Finger Queries

When the sensor is in sleep mode it draws less current than when performing a finger present query. Approximately 1.3 mA of current is consumed when the sensor is in sleep mode. Current drawn when performing a reduced finger query is approximately 6.2 mA. The *SleepCntr* paramter determines the time between reduced finger queries in sleep mode, as illustrated in Figure 11.

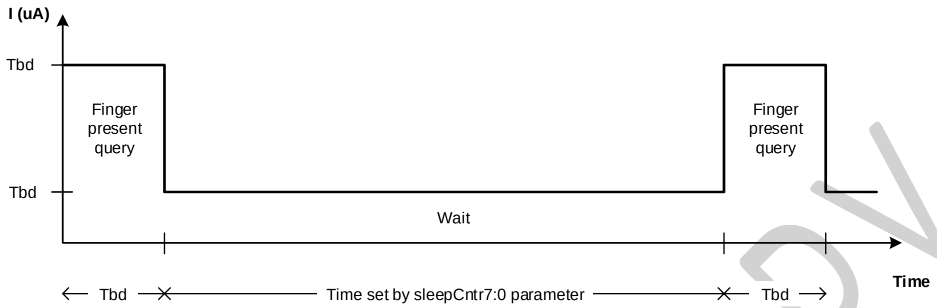

Figure 11: The sleepCntr parameter sets sleeping time between finger present queries in sleep mode.

The nominal value for 8 kHz is approximately 2 s and the corresponding value for 16 kHz is approximately 1 s. The precise value depends on the following:

- SleepCntr register settings
- Oscillator trimming to 8 or 16 kHz
- Oscillator calibration.

These settings offer a compromise between power consumption and reaction time when a finger placed on the sensor.

5.6 Deep Sleep Mode

Deep sleep mode is a vital aspect of efficient system power usage and can be used when a finger is not expected. Deep sleep mode is similar to sleep mode in that it keeps the sensor in a low power consumption mode, except that no finger detection is activated.

Deep sleep mode can be exited by sending an ACTIVATE_IDLE_MODE command which brings the sensor into idle mode. When returning to idle mode, an interrupt is set. After sending the ACTIVATE_IDLE_MODE command, the host must wait for the interrupt signal before issuing a new command sequence. The ACTIVATE_IDLE_MODE command may be cancelled at any time in the sequence and the sensor will remain in deep sleep mode.

A typical deep sleep mode command sequence is outlined in Figure 12.

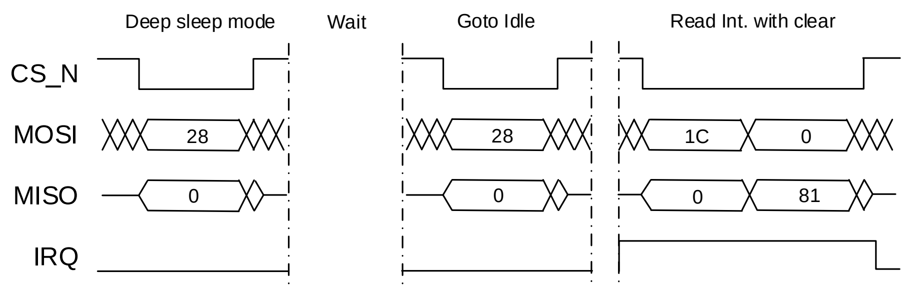

Figure 12: Principal SPI sequence for Deep sleep mode

5.7 Oscillator calibration

An internal system clock presents process variations between individual sensor chips. The oscillator should be calibrated for optimal SPI performance. Oscillator calibration can be performed if an application requires precise cycle times, such as the time between finger present queries during sleep mode.

A typical oscillator (clock) calibration mode command sequence is illustrated in Figure 13.

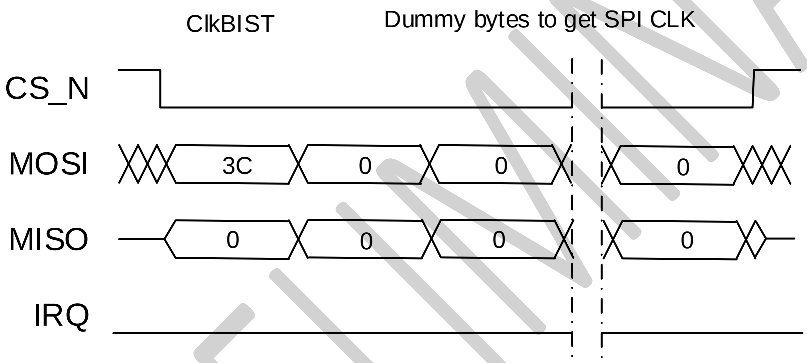

Figure 13: Principal SPI sequence for clock calibration

The lowest clock oscillation, clkOscLo, is 16kHz, and is used as reference for two other clocks. A test is performed by sending the ClkBist command, followed by a number of SPICLK cycles with a known frequency.

A counter measures the number of SPICLK cycles that appear between the two rising edges of clkOscLo. Another counter will measure the number of clkSys cycles that appear between two rising edges of clkOscLo.

The results are saved in the ClkBistResult register and can be read with an SPI sequence as outlined in Figure 14.

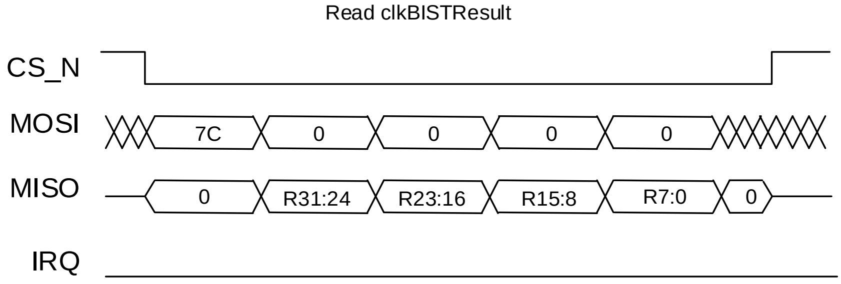

Figure 14: Principal SPI sequence for reading clock calibration result

5.7.1 Calculating clock frequencies

The following registers contain data which can be used to calculate clock frequencies:

- SPI register - contains SPI_{count} data
- clkSys register – contains $OscHi_{count}$ data

The clock frequencies can be calculated as follows:

Lowest oscillating frequency

$clkOscLo_{freq} = SPI_{freq} / SPI_{count}$

System clock

$clkSys_{freq} = OscLo_{freq} * OscHi_{count}$

6 Address Mapping

This chapter describes the address mapping for commands and registers which can be used to calibrate and operate the FPS1020 sensor. For more information on registers, see chapter 7.

6.1 Commands

This following table describes available commands and corresponding address mapping. See Table 13 for more information.

Command	Code / Address			Description
	Hex	Dec	Bin	
Capture image	C0	192	11000000	Capture new image. One byte access. Only the command is transmitted.
Read image data	C4	196	11000100	Valid data is first received following a command with a dummy byte. The read continues until csN is de-asserted. It is possible to split the reading of an image into several requests. In this case, new commands (all but the first) should be issued without the dummy byte.
Read interrupt with no clear	18	24	00011000	Read interrupt register. The register is not cleared. Two byte access, command and interrupt data.
Read interrupt with clear	1C	28	00011100	Read the interrupt register and clear it. Two byte access, command and interrupt data.
Finger present query	20	32	00100000	Checks if a finger is present. One byte access, only the command is transmitted.
Wait for finger present	24	36	00100100	Continue to check for a finger until a finger is present. One byte access, only the command is transmitted.
Activate sleep mode	28	40	00101000	Go to Sleep Mode. One byte access, only the command is transmitted.
Activate deep sleep mode	2C	44	00101100	Go to Deep Sleep Mode .One byte access, only the command is transmitted.
Activate idle mode	34	52	00110100	Go to Idle Mode. One byte access, only the command is transmitted.
Soft reset	F8	248	11111000	Performs a software controlled reset of the chip. One byte access, only the command is transmitted.
ClkBIST	3C	60	11000000	The command is used to measure the two internal oscillators' frequency in relation to a known SPICLK frequency. The command is done with one byte access plus a number of SPICLK cycles which is decided by the frequency of the OscLo oscillator. The measurement needs to run between two rising edges of the OscLo oscillator. Sending more SPICLK pulses will not affect the measurement. The result is read in the clkBistResult register. For more information on calculating clock frequencies, see section 5.7.

Table 13: Commands

6.2 Address mapping

This section gives an overview of the corresponding address mapping for available commands and registers. See Table 14 for more information.

Command / Register	Type	Code / Address	
		Hex	Dec
-	-	14	20
Read interrupt with no clear	Command	18	24
Read interrupt with clear	Command	1C	28
Finger present query	Command	20	32
Wait for finger present	Command	24	36
Activate sleep mode	Command	28	40
Activate deep sleep mode	Command	2C	44
Activate idle mode	Command	34	52
fpcError	Register	38	56
ClkBIST	Command	3C	60
-	-	40	64
-	-	44	68
-	-	4C	76
-	-	50	80
imgCapSize	Register	54	84
-	-	5C	92
-	-	60	96
-	-	68	104
-	-	6C	108
tstColPattern	Register	78	120
clkBISTResult	Register	7C	124
-	-	84	132
-	-	88	136
FingerDriveConf	Register	8C	140
-	-	90	144
oscTrim	Register	94	148
-	-	98	152
-	-	9C	156
ADCShiftGain	Register	A0	160
-	-	A4	164

Command / Register Address	Type	Code / Address	
		Hex	Dec
-	-	A8	168
Capture image	Command	C0	192
Read image data	Command	C4	196
-	-	D0	208
fngrPresentStatus	Register	D4	212
fngrDetThresh	Register	D8	216
fngrDetCntr	Register	DC	220
Soft reset	Command	F8	248
hwID	Register	FC	252

Table 14: Command and register address mapping

7 Registers

This chapter gives an overview of the registers and their main properties.

7.1 Finger Detection

This section describes the register properties for finger detection threshold.

7.1.1 Finger Detection Threshold

The name of the finger detection threshold register is *fngrDetThresh*. The *fngrDetThresh* register has access to two bytes: one address byte and one read byte. Current register content is read when data is written to the register. Properties for this register are shown in Table 15.

fngrDetThresh		Register Address: 0xD8 (216d) Access: Read/Write rstN Value: 0x50
Data Bit(s)	Name	Function/Coding
7:0	fngrDetThrshld(7:0)	Threshold value for finger detects. The threshold value is compared to the pixel sum, calculated as: $Pixelsum = \frac{1}{2}\sum_x \sum_y \frac{Pixel(x,y)}{8}$

Table 15: Properties for the finger detection threshold register

7.1.2 Finger Detection Queries

The name of the finger detection query control register is *fngrDetCntr*. The *fngrDetCntr* register has access to three bytes: one address byte and two read bytes. Current register content is read when data is written to the register. Properties for this register are shown in Table 16.

fngrDetCntr		Register Address: 0xDC (220d) Access: Read/Write rstN Value: 0x00FF
Data Bit(s)	Name	Function/Coding
Byte 1:		
15:8	WaitFngrDetCntr(7:0)	The time between finger detect queries in wait for finger query mode. The wait time is calculated as: $time = \frac{255 \cdot WaitFngrDetCntr}{f_{clkSys}}$ Where f_{clkSys} is 10 MHz.
Byte 0:		
7:0	SleepFngrDetCntr(7:0)	The time between finger detect queries in sleep mode. The sleep time is calculated as: $time = \frac{64 \cdot SleepFngrDetCntr}{f_{OscLo}}$ Where f_{OscLo} is specified by the oscTrim register.

Table 16: Properties for the finger detection query register

7.2 Setup and status registers

This section describes the properties for registers used for setup and status.

7.2.1 Interrupts

The name of the interrupt register is *fpcInterrupts*. The *fpcInterrupts* register has access to two bytes: one address byte and one read byte. Properties for this register are shown in Table 17.

fpcInterrupts		Register Address: 0x18 (24d) or 0x1C (28d) Access: Read/Read with clear rstN Value: 0xFF
Data Bit(s)	Name	Function/Coding
7		Command done.
6		-
5		New image data available in FIFO.
4		-
3		-
2		Error. See fpcError register in section 7.2.2.
1		-
0		Finger down.

Table 17: Properties for the interrupt register

Read with Clear

Reading *fpcInterrupts* with the address 0x1C will clear the interrupt register in mainCtrl. A read with the address 0x18 will not clear the interrupt register.

Reset Value

A reset value (rstN) of *FFh* in the interrupt register indicates that a reset has occurred.

7.2.2 Errors

The name of the error register is *fpcError*. The *fpcError* register has access to two bytes: one address byte and one read byte. Properties for this register are shown in Table 18.

fpcError		Register Address: 0x38 (56d) Access: Read with clear rstN Value: 0x00
Data Bit(s)	Name	Function/Coding
7:1	Not used	Reset value.
0		Fifo underflow. Attempted to read data when image FIFO was empty.

Table 18: Properties for the error register

Read with Clear

Reading the *fpcError* register clears it to the reset value.

7.2.3 Finger Present Status

The name of the register for finger present status is *fngrPresentStatus*. The *fngrPresentStatus* register has access to three bytes: one address byte, and two data bytes. Current register content is read when data is written to the register. Properties for this register are shown in Table 19.

fngrPresentStatus		Register Address: 0xD4 (212d) Access: Read rstN Value: 0x0000
Data Bit(s)	Name	Function/Coding
Byte 1:0:		
15:12	Not used	Reset value
11:0	fngrPresentStatus	Each bit indicates finger presence on one sub-area, where bit 0 is sub area 0. See Figure 3 for details.

Table 19: Properties for the finger present status register

The register value is valid after an interrupt is issued from either the *Wait for finger present* command, the *Finger present query* command, or on waking up from Sleep mode.

7.2.4 Oscillator Frequency Calculation

The name of the register used to calculate oscillator frequency is *clkBISTResult*. The *clkBISTResult* register has access to five bytes: one address byte, and four data bytes. Current register content is read when data is written to the register. Properties for this register are shown in Table 20.

clkBISTResult		Register Address: 0x7C (124d) Access: Read rstN Value: 0x00 00 00 00
Data Bit(s)	Name	Function/Coding
Byte 3:2:		
31	Not used	Reset value.
30	doneSPI	A zero indicates test failed.
29:16	resultSPI (13:0)	Test result of oscillator low. Note that all '1' or all '0' indicates overflow or fail.
Byte 1:0		
15	Not used	Reset value.
	doneOscHi/doneclkSys	A zero indicates test failed.
13:0	resultOscHi/resultclkSys (13:0)	Test result of clkSys. Note that all '1' or all '0' indicates overflow or fail.

Table 20: Properties for the oscillator frequency calculation register

Refer to the command *clkBist* for a description how to calculate the frequency of the oscillators from the *clkBISTResult* register.

7.2.5 Oscillator Calibration

The name of the register for oscillator calibration is *oscTrim*. The *oscTrim* register has access to three bytes: one address byte, and two data bytes. Current register content is read when data is written to the register. Properties for this register are shown in Table 21.

oscTrim		Register Address: 0x94 (148d) Access: Read/Write rstN Value: 0x0D07
Data Bit(s)	Name	Function/Coding
Byte 1:		
15:12	Not used	Reset or the last value written to these bits is read.
11:8	ClockSysTrim(3:0)	Oscillator high frequencies (clkSys and OscHi) trim value.
Byte 0:		
7:6	Not used	Reset or the last value written to these bits is read.
5:0	OscLoTrim(5:0)	Oscillator low frequencies trim value. Bit 5 = 0 -> nominal frequency 16 KHz. Bit 5 = 1 -> nominal frequency 8 kHz.

Table 21: Properties for the oscillator calibration register

7.2.6 Shift Gain

The name of the register for shift gain is *ADCShiftGain*. The *ADCShiftGain* register has access to three bytes: one address byte, and two data bytes. Current register content is read when data is written to the register. Properties for this register are shown in Table 22.

ADCShiftGain		Register Address: 0xA0 (160d) Access: Read/Write rstN Value: 0x0000
Data Bit(s)	Name	Function/Coding
Byte 1:		
15:13	Not used	Reset or the last value written to these bits is read.
12:8	ADCShift(4:0)/ ImageShift	ADC/*Image* shift value.
Byte 0:		
7:4	Not used	Reset or the last value written to these bits is read.
3:0	ADCGain(3:0)/ImageGain	ADC/*Image* Gain trim value.

Table 22: Properties for the shift gain register

7.2.7 Image Capture Size

The name of the register for image capture size is *imgCaptSize*. The *imgCaptSize* register has access to five bytes: one address byte, and four data bytes. The current register content is read when data is written to the register. Properties for this register are shown in Table 23.

imgCaptSize		Register Address: 0x54 (84d) Access: Read/Write rstN Value: 0x00C000C0
Data Bit(s)	Name	Function/Coding
Byte 3:		
31:24	StartRow(7:0)	Image start row position. Valid range 0 to 191.
Byte 2:		
23:16	RowLength(7:0)	Image row length. Valid range 1 to 192.
Byte 1:		
15:8	StartCol (7:0)	Image start group position. Valid value is multiple of 8 in the range 0 to 184.
Byte 0:		
7:0	ColLength(7:0)	Image group length. Valid value is a multiple of 8 in the range 8 to 192.

Table 23: Properties for the imgCaptSize register

If the total requested amount of data is less than 25 pixels, there will not be a data present interrupt when data is ready to be read. In the case of very small amount of data, it is recommended to wait for the sensor to scan the requested pixels.

7.2.8 Hardware ID

The name of the register for hardware ID is *hwID.* The *hwID* register has access to three bytes: one address byte, and two read bytes. Properties for this register are shown in Table 24.

hwID		Register Address: 0xFC (252d) Access: Read rstN Value: 0x020A
Data Bit(s)	Name	Function | Coding
15:4	hwIDChip(11:0)	Chip version | 020 = Chip 1020.
3:0	hwIDRev(3:0)	Revision number | A = Revision A

Table 24: Properties for the HardwareID register

7.3 Configuration

This section describes the properties for registers used to configure the sensor.

7.3.1 Finger Drive

The name of the register for configuring the finger drive is *fngrDriveConf*. The *fngrDriveConf* register has access to two bytes: one address byte and one data byte. Current register content is read when data is written to the register. Properties for this register are shown in Table 25.

fngrDriveConf		Register Address: 0x8C (140d) Access: Read/Write rstN Value: 0x02
Data Bit(s)	Name	Function/Coding
7:6	Not used	Reset or the last value written to these is read.
5	FngrDrvVdBstEn	Enable voltage boost for TXOUT supply. This signal needs to be configured together with *FngrDrvVdIntEn*. '0' – VDDA supply TXOUT. Also turns off voltage boost. '1' – Voltage boost enabled and supply TXOUT.
4	FngrDrvVdIntEn	Enable Internal voltage supply to TXOUT. '0' – VDDTX supply TXOUT. '1' – Internal resource controlled by the *FngrDrvVdBstEn* signal supply TXOUT.
3	FngrDrvExtInv	Inverting TX out
2	FngrDrvTst	Finger drive test control. '0' – Finger drive disconnected from pixel test capacitor. '1' – Finger drive connected to pixel test capacitor according to the *tstColPatternEn* register.
1	FngrDrvExt	Finger drive external control. '0' – Finger drive disconnected from TXout pad. '1' – Finger drive connected to TXout pad.
0	Not used	Reset or the last value written to these bits is read

Table 25: Properties for the finger drive configuration register

7.3.2 Test Pattern

The *tstColPatternEn* register is used to configure test patterns by enabling capacitors. The *tstColPatternEn* register has access to three bytes: one address byte and two data bytes. Current register content is read when data is written to the register. Properties for this register are shown in Table 26.

tstColPatternEn		Register Address: 0x8C (140d) Access: Read/Write rstN Value: 0x02
Data Bit(s)	Name	Function/Coding
Byte 1:		
15:8	TstColPaEn1(7:0)	Test pattern 1 enables the register. Each bit enables one test capacitor. The pattern controls pixels on row 0, column 8-15, 24-31 and so on.
Byte 0:		
7:0	TstColPaEn0 (7:0)	Test pattern 0 enables the register. Each bit enables one test capacitor. The pattern controls pixels on row 0, column 0-7, 16-23 and so on.

Table 26: Properties for the test pattern register

8 Timing

This chapter offers an overview of some aspects of timing for the FPC1020 sensor.

8.1 Power-up Timing

The power-up timing sequence for the sensor is shown in Figure 15.

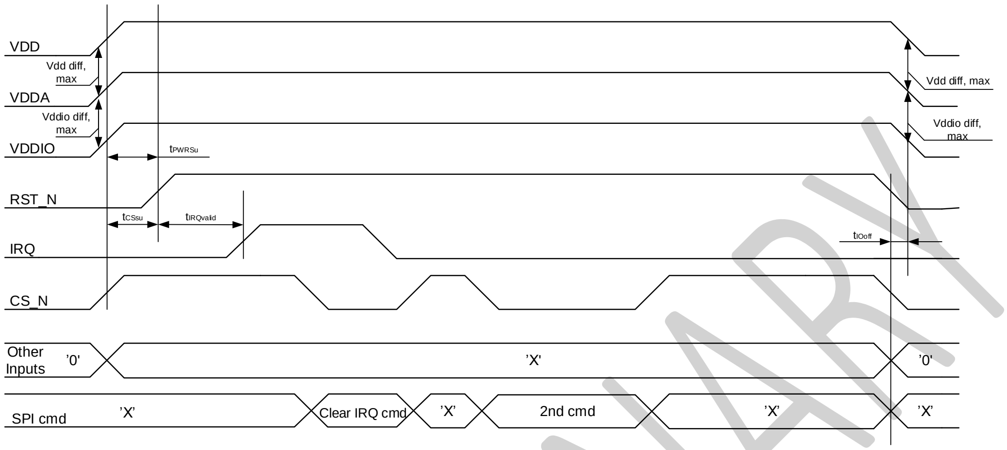

Figure 15: Power-up timing sequence

8.1.1 VDD diffmax

VDD diffmax is the maximum voltage difference between VDD and VDDA.

- VDD diffmax = 200 mV.

8.1.2 VDDIO

diffmax

VDDIO diffmax is greater than the maximum voltage difference between VDDIO and VDD or VDDA or larger. VDDIO diffmax is larger than the values for VDD and VDDA.

VDDIO > VDD and VDDA.

IOn

IOn is low until VDDIO is high, it follows VDDIO.

RST_N

The reset value RST_N is active 0.1ms after VDDD/VDDA/VDDIO goes high.

- tPWRsu = 0.1 ms

CS_N

CS_N should be set high before releasing RST_N.

- tCSsu > 0 ms.

8.1.3 IRQ

SPI communication can begin once IRQ is high. The maximum time for IRQ after reset deactivated is as follows:

- tIRQvalid = 1.3ms

8.2 SPI Timing

An overview of SPI timing for the sensor interface is shown in Figure 6.Figure 16: SPI timing

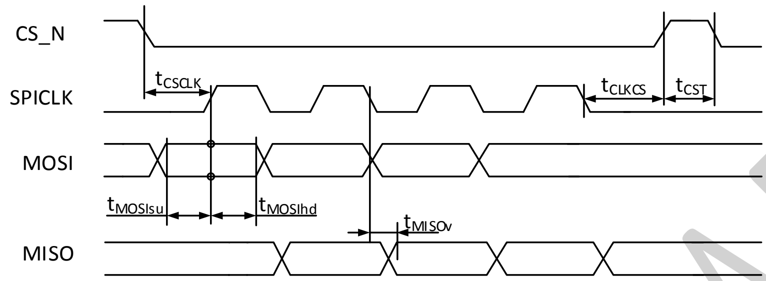

Figure 16: SPI timing

Typical values for the parameters in the SPI timing sequence are described in Table 27.

Symbol	Parameter	Minimum	Maximum	Units	Comments
t_{MISOv}	MISO valid time	TBD	TBD	ns	
t_{MOSIsu}	MOSI setup time	TBD		ns	
t_{MOSIhd}	MOSI hold time	TBD		ns	
	SPICLK Frequency	1	12	MHz	
t_{CSCLK}	Time for CS_N low to SPICLK high	41,67		ns	
t_{CLKSPI}	Time for SPICLK low to CS_N high	0		ns	
t_{CST}	Minimum CS_N high time before setting CS_N low.	31,25		ns	
	IRQ	1.3		ms	Asynchronous to SPICLK

Table 27: SPI timing for sensor interface

9 Reference Layout

A circuit board reference with an overview of the FPC1020 sensor interfaces is shown in Figure 17.

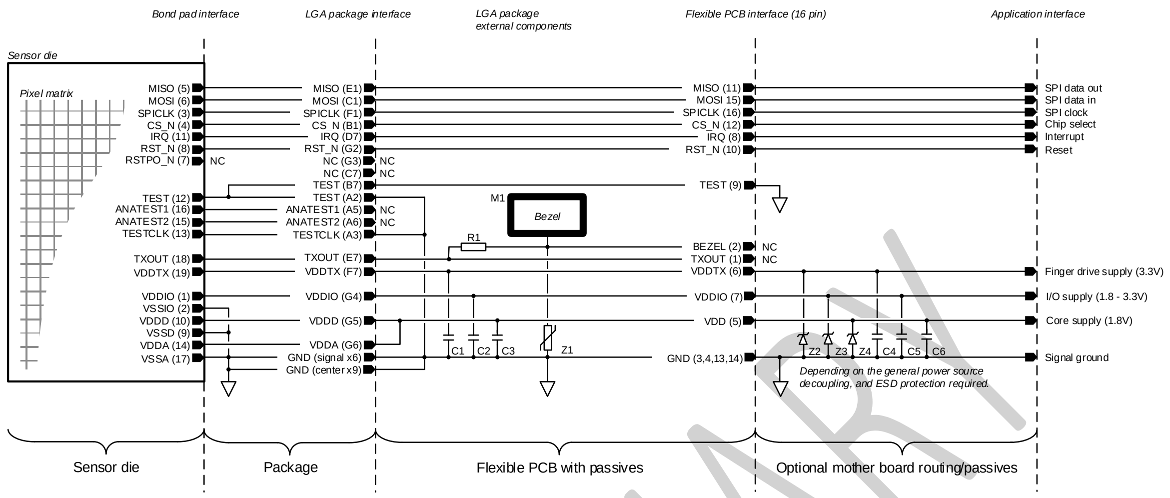

Figure 17: Reference Layout

10 ESD Protection

To generate an image, capacitive fingerprint sensors require a finger to be in contact with the sensor surface. This will expose all capacitive sensors to severe electro-static discharges (ESDs), as they usually are the "first point of contact". ESD discharge voltages are often under-estimated and the actual voltage levels may be surprisingly high. Discharges in the 1 to 2 kV range will typically not even be noticed – they wil not be felt in the finger of the user.

All sensors from Fingerprint Cards incorporate extensive internal ESD protection for all accessible front surfaces. The protection level is well in excess of 30kV using a standard Human Body Model discharge in a production environment.

10.1 Human Body Model

The Human Body Model, as shown in Figure 18, consists of a 100 pF capacitor, which simulates the capacitance between body and ground. This capacitor is charged to a test voltage. The resistance of the finger and skin is approximated by a 1500 ohm series resistor. The discharge will have a time constant of, 100pF x 1500 ohm = 150 nS. For a 15 kV discharge the peak current would be 15kV/1500 = 10A.

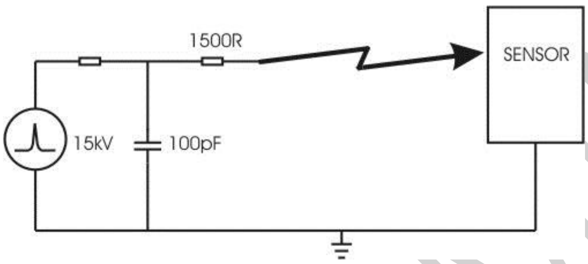

Figure 18: Human Body Model

Although the ESD-specification is given as a voltage level it is important to realize that an ESD test is effectively a current discharge test.

10.2 Internal Sensor Protection

Sensors from Fingerprint Cards have a robust sensor surface coating, which will deflect discharges to the surounding bezel. From the bezel, the discharge current will be conducted via the Transient Voltage Suppressor (TVS) to the local ESD drain node. The voltage at the bezel is thereby limited. The 100 ohm resistor will limit the current towards the sensor chip to very safe levels.

10.3 Voltages Induced by ESD current

In a simplified model, two currents occur during an ESD event - the main ESD current flowing through the TVS to the sensor ESD drain, and the much smaller current flowing through the 100 ohm resistor back into sensor chip input protection throught the TXOUT signal.

The current flow through the 100 ohm resistor will depend on the clamping voltage over the TVS. A 15kV discharge will generate a 200 mA current pulse into the chip protection diodes, well within the chip ESD rating. The duration of the pulse will be in the order of 600nS. After this time the current will decay exponentially. The charge through the protection diode can be estimated to 0.15 nC.

10.3.1 Sensor Cable Extensions

When the sensor is connnected using longer sensor cable lengths of over 0.2 meter, the electromagnetic coupling between the current in the ESD drain connection and other signal and supply connections need to be considered. This coupling is rather complicated and will depend on the cable geometry.

With a standard, short connection between the sensor and the receiving electronics, these effects are not significant and can be ignored.

Longer cable lengths between sensor and the receiving electronics can in some cases be acceptable. Exact guidelines are not possible since the ESD effects will depend on the actual installation but up to 0.2 meter would in general not cause any problems.

Extending the standard cable length will also affect signal integrity. The digital waveforms should be checked for adverse reflections. Problems with unwanted oscillation (ringing) become more evident as the length increases. At 1m the ringing will cause waveforms that are questionable.

10.3.2 Minimizing Effects on Downstream Electronics

The ESD pulse will continue past the sensor drain path and spread into the receiving electronics ground plane and most likely further on to a "protective earth" ground via a connecting cable. This connection will often have considerable length and may potential lead to ESD problems.

To help alleviate the risk of electromagnetic coupling a separate ESD return to divert the ESD current to a more suitable point is recommended.

A way to prevent problems with stray currents due to dual ground paths, is to front the separate ESD return with a TVS in order to break this current path at low voltages while allowing the ESD pulse to pass freely.

Even higher ESD diversion can be achieved by also increasing the inductance of the signal cable connection from the receiving electronics. The common mode of inductance can to help steer the ESD current over to the separate ESD return. One of the easiest means is to mount an EMI ferrite core on the cable near the electronics.

10.4 ESD Discharge Path

It is recommended that the separate ESD discharge path is connected directly to the signal ground plane, as illustrated in Figure 19.

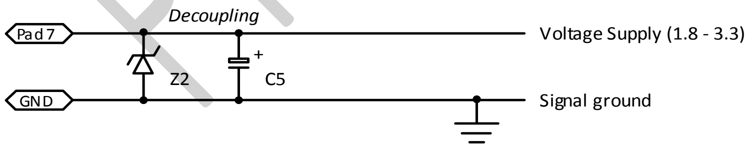

Figure 19: ESD discharge - signal ground

This solution requires the ground plane and the receiving electronics to consume the entire discharge induced by the end user. The ground plane connection should preferably be done close to a large decoupling capacitor.

11 Power Supply & Filtering

Depending on the overall quality of the connected power supply, i.e. noise, filter, or decoupling circuitries may be necessary. In normal cases a standard buffer capacitor in the range of 5-10µF is enough. In case of a noisy environment, other types of filtering may be required to obtain optimal performance.

Although the sensor is specified for a voltage supply range between 1.8 - 3.3 volts, different protection and decoupling circuitries may be necessary to reach full communication speed over the entire voltage range.

11.1 Ground Reference

A sensor in a fingerprint based authentication system will, by definition, always come in physical contact with the end user. In order to mitigate the common-mode disturbances, such as those induced by the end user, the sensor or the receiving electronics should be connected to a protective ground reference. For example, common mode disturbance may occur with isolated low cost switch-mode power supplies that do not have a direct connection or an EMI capacitor from the AC line input to the DC output.

12 Product Updates

An historical overview of the updates to the FPC1020 sensor can be found in this section.

12.1 Product History

An overview of the previous versions of the FPC1020 sensor product is shown in Table 28.

Revision	Date	Description	Details
1A	2014-04	First release of FPC1020 sensor	Article number: FPC1020W2-CW05

Table 28: Product History

12.2 Document History

The updates and changes between the previous versions of this specification are outlined in Table 29.

Revision	Date	Changes	Approver
A	2014-04	New document	Christian Skeppstedt

Table 29: Document History