

2013

**Product Catalog** 







### **SEIKO EPSON CORPORATION**

### **Business Concept**

The market for semiconductors is rapidly expanding with the fast emergence of a ubiquitous network society. A variety of mobile devices - mobile phones, information terminals, car electronics and intelligent home appliances - all require semiconductors. There seems to be no limit to the demand for more functions and better performance. Thin, lightweight, low-power devices that operate for extended periods on a single charge are in demand. In addition, devices with these features are expected to have shorter time to market. Never before has the development of new products been so challenging.

We have been focusing on the creation of compact, low-power semiconductors since we started the development of a CMOS LSI for watches in 1969. Since then, we have steadily built up our expertise in power-saving, space-saving and time-saving designs. This has enabled us to quickly obtain the semiconductor development technology needed to meet the demands of the new era of ubiquitous networks. Epson has the unique technologies and a passion for excellence that enable it to deliver the high added-value solutions that you need. Our goal is to be a true partner for you, by providing you with strategic advantages for your product development with technology to save power, time, and space.

### **Environmental Responsibility**

Epson semiconductor technology provides environmental value to customers by creating and manufacturing eco-friendly products.

1) We Epson's products are surely complying with the Eu-RoHS (2011/65/EU) Directive.

2) We are releasing information about the containing chemical substances of products at web-site. Product of QFP & BGA are described in the following URL.

http://www.epson.jp/device/semicon\_e/tech/package/lineup01.htm \*Some products are excluded.



Environmental management system third party certification status ISO14001 : 2004

Epson has acquired ISO14001 certification with Semiconductor business. Original approval date: 4th April 1999 (Bureau Veritas Japan CO.,Ltd.) Site: Fujimi Plant, Tohoku Epson Corporation Original approval date: 12th January 1999 (SGS) Site: Singapore Epson Industrial Pte. Ltd.

### **Epson's Quality Policy**

Keeping the customer in mind at all times, we make the quality of our products and services our highest priority. From the quality-assurance efforts of each employee to the quality of our company as a whole, we devote ourselves to creating products and services that please our customers and earn their trust.

Epson has acquired ISO9001 and ISO/TS16949 certification with its IC, module and their application products.



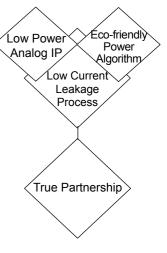
### Quality Management system third party certification status ISO9001:

Original approval date 10th October 1993 (Bureau Veritas Japan CO.,Ltd.) Site: Fujimi Plant, Hino Office, Suwa minami Plant, Tohoku Epson Corporation Original approval date 4th February 2003 (SGS) Site: Singapore Epson Industrial Pte. Ltd. **ISO/TS16949:** Original approval date 9th May 2006 (Bureau Veritas Japan CO.,Ltd.) Site: Fujimi Plant, Hino Office, Tohoku Epson Corporation Original approval date 7th June 2007 (SGS) Site: Singapore Epson Industrial Pte. Ltd.

### Epson's LSI

With our three core technologies - low current leakage process technology that dramatically reduces standby current, system algorithms for highly efficient power utilization, and analog IPs optimally designed for low power consumption - Epson presents solutions for you to develop applications that exceed your expectations.

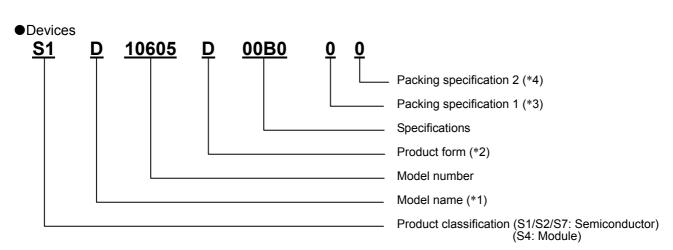
We offer optimally-designed products, information and services in a most timely manner from the very beginning of your product development to volume production. We believe our support throughout all stages of your product cycle will lead to the adoption of Epson devices for your next products.



### CMOS LSIs Contents 2013

Config	uration of product number		2
1. ASI	Cs Application Specific IC		
	Gate Arrays	S1L60000 series, S1L50000 series, S1L5V000 series,	
			4
1-2		S1X60000 series, S1X50000 series	
1-3	Standard Cells	S1K60000 series, S1K50000 series	7
	■Macro-cell lineup		
1-4	Development of ASICs		8
	JS Micro Controller Unit		
2-1	4-bit Microcontrollers	. S1C60Family, S1C63Family	10
2-2	16-bit Microcontrollers	. S1C17Family	13
2-3	32-bit Microcontrollers	. S1C33Family	16
2-4	Program development		18
	Program development process		
	Development tools		
3. ASS	<b>Ps</b> Application Specific Standard Products		
3-1		S1D13*** series, S2D13*** series	22
	■LCD controller		
	■LCD controller with Camera I/F		
	■Video Encoders		
	■Image Enhancement IC		
	■LCD controller for automotive		
	■EPD controller (supporting the E Ink's EPD)		
	■In-vehicle multi-camera interface IC		
3-2	Network & Image Controllers	. SxS6X000 series	25
		. S1V3*** series, S1V50300 series	
3-4			27
	Drivers for small and medium-sized panel		
	■STN LCD Drivers for large panel	. S1D17000 series	~~
		. S1D50000 series	
		. S1D14F50 series	
		. S1F77000 series	29
	kage Information		~~
		ity Assembly	
Informatio	on on CIMUS LSI's		44

#### Configuration of product number



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#### \*1: Model name

С	Microcontroller
D	Driver IC, Display Controller
F	Analog Switch
К	Standard Cell
L	Gate Array

\*2: Product form

В	BGA,WCSP
D	Bare Chip
F	Plastic QFP
Н	Ceramic DIP

\*3: Packing specification 1

0	Tape & reel	(non-heatproof)	)
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#### \*4: Packing specification 2

15th	Packing specifications
0	Besides tape & reel (tray)
А	TCP BL 2 directions
В	Tape & reel BACK
С	TCP BR 2 directions
D	TCP BT 2 directions
Е	TCP BD 2 directions
F	Tape & reel FRONT
G	TCP BT 4 directions
Н	TCP BD 4 directions

L	Ceramic QFP
М	Plastic SOP
Т	Tape Carrier (TAB)
Y	SOT89 (3 terminals)

Network & Image Controller

1 Tape & reel (heatproof)

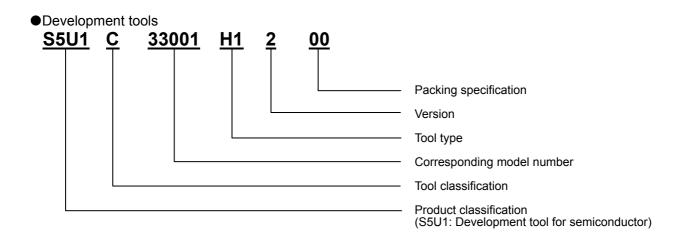
Interface IC

Speech & Audio IC

Embedded Array

Clock IC

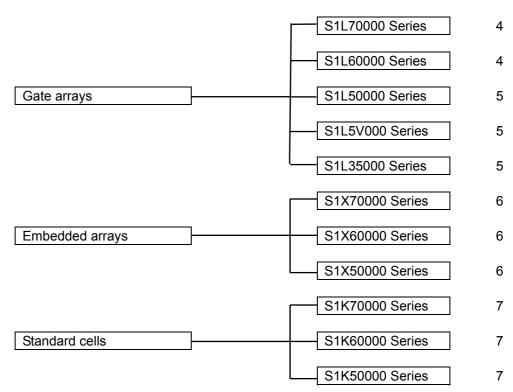
15th	Packing specifications
J	TCP SL 2 directions
К	TCP SR 2 directions
L	Tape & reel LEFT
М	TCP ST 2 directions
N	TCP SD 2 directions
Р	TCP ST 4 directions
Q	TCP SD 4 directions
R	Tape & reel RIGHT



When place an order please ask the detail product number to Epson sales representative.







## 1-1 Gate Arrays

#### ■ High-speed, high-density lineup

5		inght defieldy integrap					
				Core I/O			
S1L70000	series			1.8V <u>1.8V</u> 3.3V			
Ser	ies	S1L70000 Series		1.5V 1.5V 3.3V			
Feat	ures	Ultra large scale integration (0.18µm CMOS, using 4-, 5-, 6-layer interconnect process)     High-speed operation (43.6 ps internal gate delay at 1.8V, 2-input NAND Typ.)     Low power consumption (Internal cell: 0.18V 0.077µW/IMHz/BC)     Drive capacity (IoL=2, 4, 8, 12mA at 3.3V, IoL=1, 2, 4, 6mA at 1.8V, IoL=0.75, 1.5, 3, 4.5mA at 1.5V)     RAM (synchronous type) and various types of macro cells can be implemented.					
	4-layer Metallization	S1L70084	S1L70174	S1L70314			
Model Name	5-layer Metallization	S1L70085	S1L70175	S1L70315			
6-layer Metallizatio		S1L70086	S1L70086 S1L70176 S1L7				
Total BC (F	Raw Gates)	86,534	172,972	316,440			
	4-layer Metallization	64,901	112,432	205,686			
Usable Gates	5-layer Metallization	69,227	121,080	221,508			
	6-layer Metallization	73,554	129,729	237,330			
Total Lead Count Micro	80µm	60	-	-			
Lead Pitch	70µm	-	112	144			
Internal Gate		tpd=43.6ps (1.8V operation, F/O=1, typical wiring load)					
Delay Time	Input Buffer	tp	d=181ps (3.3V operation, F/O=2, typical wiring load)				
Output Buffer		tpd=1,510ps (3.3V/1.8V operation, CL=15pF)					
I/O Levels		LVCMOS, LVTTL, PCI-3.3V					
Input N	Nodes	LVCMOS, LVTTL, Schmitt, Pull-up/Pull-down, Fail-safe, Gated					
Output	Modes	Norr	nal, Open-drain, 3-state, Bidirectional, Fail-safe, Gated				

										Core	I/O	
										1.0\/	1.8V	
S1L60000	series									1.8V	3.3V	
	Series S1L60000 Series										2.0V	
Ser	ies									2.0V	3.3V	
			cale integration (							2.5V	2.5V 3.3V	
			operation (107 ps onsumption (Inte								3.3V	
Feat			ty (lo∟=0.1, 1, 3,				2.5V.					
			, 1, 2, 3, 6mA at									
		<ul> <li>RAM (synchi</li> </ul>	onous type, asy	nchronous type)	, PLL, and vario	us types of mac	ro cells can be ir	nplemented.		1	r	
Model	3-layer Metallization	S1L60093	S1L60173	S1L60283	S1L60403	S1L60593	S1L60833	S1L61233	S1L61583	S1L61903	S1L62513	
Name	4-layer Metallization	S1L60094	S1L60174	S1L60284	S1L60404	S1L60594	S1L60834	S1L61234	S1L61584	S1L61904	S1L62514	
Total BC (Raw Gates)		99,220	171,720	284,394	400,290	595,362	831,572	1,234,820	1,587,754	1,902,960	2,519,604	
Usable Gates	3-layer Metallization	59,520	103,032	142,197	200,145	297,681	332,628	493,928	635,101	761,184	1,007,841	
Usable Gales	4-layer Metallization	69,440	120,204	184,856	260,188	386,985	415,786	617,410	793,877	951,480	1,259,802	
Total Lead Count Micro	80µm	—	—	_	—	_	284	344	388	424	488	
Lead Pitch	70µm	112	148	188	224	272	—		-	-	—	
	Internal Gates		tpd=107ps (2.5V operation, F/O=1, typical wiring load)									
Delay Time	Input Buffer				tpd=270ps	(2.5V operation	, F/O=2, typical	wiring load)				
	Output Buffer				<b>t</b> pd	=1600ps (2.5V c	peration, C∟=15	pF)				
I/O Levels			CMOS, LVTTL, PCI-3.3V									
Input N	Nodes				LVTTL, CMOS	6, Pull-up/Pull-de	own, Schmitt, Fa	il safe, Gated				
Output	Modes				Normal, Oper	n-drain, 3-state,	Bidirectional, Fa	il safe, Gated				

Note: Figures shown for usable gates are approximations. The actual number of usable gates varies according to the implemented circuitry.

### ASICs

Core

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I/O

													Core		I/O
S1L50000	corioc												2.0V		2.0V 3.3V
Ser		S1L500	00 Serie	s									2.5V		2.5V 3.3V
				egration (0.3 on (0.14 ns						)			3.3V	:	3.3V 5.0V
Feat	ures	<ul> <li>Drive ca</li> </ul>	pacity (loL=	ption (Intern 0.1, 1, 3, 8, s type), PLL	12, 24mA a	it 5.0V, IoL=	0.1, 1, 2, 6,			0.5, 1, 3, 6	mA at 2.5V,	Iol=0.05, 0	.3, 0.6, 2, 4	mA at 2.0V)	)
	2-layer Metallization	S1L50062	S1L50122	S1L50282	S1L50552	S1L50752	S1L50992	S1L51252	S1L51772	S1L52502	S1L53352	S1L54422	S1L55062	S1L56682	S1L58152
Model Name	3-layer Metallization	S1L50063	S1L50123	S1L50283	S1L50553	S1L50753	S1L50993	S1L51253	S1L51773	S1L52503	S1L53353	S1L54423	S1L55063	S1L56683	S1L58153
	4-layer Metallization	S1L50064	S1L50124	S1L50284	S1L50554	S1L50754	S1L50994	S1L51254	S1L51774	S1L52504	S1L53354	S1L54424	S1L55064	S1L56684	S1L58154
Total BC (Raw Gates)		5,760	11,948	28,710	55,500	75,774	99,198	125,772	177,062	250,160	335,858	442,112	506,688	668,552	815,468
	2-layer Metallization	2,880	5,974	14,355	26,085	35,613	46,623	56,597	79,677	112,572	144,418	176,844	202,675	267,420	326,187
Usable Gates	3-layer Metallization	5,068	10,514	25,264	47,175	64,407	84,318	100,617	132,796	187,620	251,893	309,478	354,681	467,986	570,827
	4-layer Metallization	5,472	11,350	27,274	52,725	71,985	94,238	119,483	168,208	237,652	319,065	397,900	456,019	601,696	733,921
Total Lead Count Micro	80µm	-	56	88	124	144	168	188	224	264	308	352	376	432	480
Lead Pitch	70µm	48	64	104	144	168	192	216	-	-	-	-	-	-	-
	Internal Gates			tpd=0.1	4ns (3.3V d	peration, F	/O=2, typica	al wiring loa	d), 0.21ns (	2.0V operat	ion, F/O=2,	typical wiri	ng load)		
Delay Time	Input Buffer	tpd=0.	38ns (5.0V o	operation, F	/O=2, typica	I wiring load	l), 0.4ns (3.3	3V operation	, F/O=2, typ	oical wiring lo	oad), 1.3ns	2.0V operat	tion, F/O=2,	typical wirin	ig load)
	Output Buffer			tpd=2	.12ns (5.0V	operation, C	C∟=15pF), 2.	.02ns (3.3V	operation, C	L=15pF), 3.9	9ns (2.0V op	eration, C∟	=15pF)		
I/O Levels							CMC	S, LVTTL, I	PCI-5V, PC	-3.3V					
Input I	Nodes					LVTTL	, CMOS, Pu	ull-up/Pull-d	own, Schmi	itt, Fail safe	Gated				
Output	Modes					Norma	al, Open-dra	ain, 3-state,	Bidirectiona	al, Fail safe,	Gated				

#### S1L5V000 Series

				5.0V	5.0V				
Ser	ies	S1L5V000 Series		3.3V	3.3V				
Feat	ures	<ul> <li>High speed operation (internal gate d</li> <li>Low power consumption (Internal cell</li> </ul>	IS, using 2-,3-,4-layer interconnect process) elay: 0.19 ns at 5 V, 0.29 ns/ at 3.3V, 2-input power NAND T : 5V 1.3µW/MHz/BC, 3.3V 0.54µW/MHz/BC) mA at 5.0V, lo⊾=0.1, 1, 2, 6, 12mA at 3.3V) olemented	yp.)					
	2-layer Metallization	S1L5V042	S1L5V112	S1L5V252					
Model Name	3-layer Metallization	S1L5V043	S1L5V113	S1L5V253					
4-layer Metallization		S1L5V044	S1L5V114	S1L5V254					
Total BC (F	Raw Gates)	42,008	109,250	254,330					
2-layer Metallization		12,602	32,775	63,583					
Usable Gates	3-layer Metallization	25,205	65,550	127,165					
	4-layer Metallization	29,406	76,475	165,315					
Total Lead Count		104	168	256					
	Internal Gates	tpd=0.19ns (5.0V operation, F/O=2, typical wiring load), 0.29ns(3.3V operation, F/O=2, typical wiring load)							
Delay Time Input Buffer		tpd=0.45ns (5.0V operation, F/O=2, typical wiring load), 0.55ns(3.3V operation, F/O=2, typical wiring load)							
	Output Buffer	tpd=2.07ns (5.0V operation, CL=15pF), 2.95ns (3.3V operation, CL=15pF)							
I/O L	evels	CMOS, TTL, LVTTL							
	Modes		TTL, LVTTL, CMOS, Pull-up/Pull-down, Schmitt, Fail	-					
Output	Modes		Normal, Open-drain, 3-state, Bidirectional, Fail-sa	fe, Gated					

S1L35000 Series	s
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S1L35000	Series						Core	I/O
Se	ries	S1L35000 Series					3.3V	3.3V
Fea	ures	<ul> <li>Large scale integration (0.</li> <li>High speed operation (int</li> <li>Low power consumption (</li> <li>Driving capacity (lot=, 1, </li> <li>RAM (asynchronous type)</li> </ul>	ernal gate delay: 0.3ns at internal cell: 3.3V, 0.91 $\mu$ 4, 8, 12,mA at 5.0V, lo <sub>L</sub> =0	5V, 0.4ns/3.3V 2-input po W/MHz/BC)	ower NAND Typ.)		5.0V	5.0V
Model I	Name	S1X35063	S1X35073	S1L35043	S1L35063	S1L35093		S1L35163
Total BC (R	aw Gates)	13,632	28,170	41,417	64,320	95,760		161,841
Usable Gates		8,179	18,310	26,921	38,592	52,668		80,920
TOTAL Le	ead Count	58	90	110	130	162		210
	Internal Gates		tpd=0.3ns (5.0V operation	n, F/O=2, typical wiring load	), 0.4ns (3.3V operation, F/	O=2, typical wiring lo	ad)	
Delay Time	Input Buffer	tı	od=0.48ns (5.0V operation	n, F/O=2, typical wiring load	I), 0.63ns (3.3V operation, F	/O=2, typical wiring	oad)	
	Output Buffer		tpd=2.08n	is (5.0V operation, CL=15pF	), 2.86ns (3.3V operation, 0	C∟=15pF)		
1/01	evels			TTL, C	MOS			
Input	Modes			TTL, CMOS, Pull-up	/Pull-down, Schmitt			
Output	Modes			Normal, Open-drain,	3-state, Bidirectional			

Note: Figures shown for usable gates are approximations. The actual number of usable gates varies according to the implemented circuitry.

## 1-2 Embedded Arrays

An embedded array is an ASIC under a new method featuring consolidation of "Sea of gates" of a gate array and hard- macros installed in standard cells for specific applications. With this product, the concept of system-on-chip has been realized by consolidation of hard-macro cells for specific applications and a shorter gate array development period has become available, thanks to adoption of the "Sea of Gates" for the logic portion.

#### Designing the embedded arrays

When designing embedded arrays, execute system design first and determine the number of gates for the logic section and select the macro-cell to be used before starting manufacture of base bulks. The base bulks, placing necessary hard-macro cells and the Sea of Gates for the logic portion, are manufactured up to just before the routing process. In parallel with this manufacturing processes, processes from the circuit designing of the logic portion through post-simulation fix should be executed, similar to the cases of ordinary gate arrays, to go into sample production process after sign-off.

After the sign-off, samples can be shipped with the same delivery leadtime as that of the gate arrays. Also, when making logic circuit modifications or ROM data changes, developing cost and leadtime can be reduced to a level similar to that of the gate arrays.

#### Embedded arrays lineup

		Core	I/O
S1X70000	series	1.8V	1.8V 2.5V 3.3V
Series	S1X70000 Series		1.5V
	<ul> <li>High-density integration (based on 0.18µm CMOS process technology using 3/4/5/6-layer interconnect process, number of raw gates: 5,300,000 Max.)</li> </ul>	1.5V	2.5V 3.3V
Features	<ul> <li>High-speed operation (Internal gate delay: 43.6ps/1.8V, 2-input NAND Typ.)</li> <li>Lower power consumption (Internal cell: 0.077µW/MHz/gate, 1.8V, Typ.)</li> <li>Drive performance (IoL=2, 4, 8, 12mA at 3.3V, IoL=1.5, 3, 6, 9mA at 2.5V, IoL=1, 2, 4, 6mA at 1.8V, IoL=0.75, 1.5, 3, 4.5mA at 1.5V)</li> </ul>		
Macro Cells	RAM, ROM, various types of macro cells		
Package	48 to 256 pin QFP, PBGA, PFBGA, QFN		

		Core	I/O
1X60000	series	2.0V	2.0V
			3.3V
Series	S1X60000 Series	2.5V	2.5V 3.3V
Features	<ul> <li>High-density integration (based on 0.25µm CMOS process technology and 3/4/5-layer wiring technology, number of raw gates: 2,500,000 Max.)</li> <li>High-speed operation (Internal gate delay: 107ps/2.5V, 2-input NAND Typ.)</li> <li>Low power consumption (Internal cell: 0.18µW/MHz/gate, 2.5V, Typ.)</li> <li>Drive performance (IoL=0.1, 1, 3, 6, 12, 24mA at 3.3V, IoL=0.1, 1, 3, 6, 12, 24mA at 2.5V, IoL=0.05, 0.3, 1, 2, 4, 8mA at 2.0V)</li> </ul>		
Macro Cells	RAM, ROM, Flash, various types of macro cells		
Package	48 to 256 pin QFP, PBGA, PFBGA, QFN		

		Core	I/O
		2.0V	2.0V
S1X50000	series	2.00	3.3V
		2.5V	2.5V
Series	S1X50000 Series	2.5 V	3.3V
	<ul> <li>High-density integration (based on 0.35µm CMOS process technology and 3/4-layer wiring technology)</li> </ul>	3.3V	3.3V
Features	High-speed operation (Internal gate delay: 140ps/3.3V, 2-input power NAND Typ.)	0.01	5.0V
realures	● Low power consumption (Internal cell: 0.39µW/MHz/gate, 3.3V, Typ.)		
	● Drive performance (IoL=0.1, 1, 3, 8, 12, 24mA at 5.0V, IoL=0.1, 1, 2, 6, 12mA at 3.3V, IoL=0.1, 0.5, 1, 3, 6mA at 2.5V, IoL=0.05, 0.3, 0.6	6, 2, 4mA at 2.0V)	
Macro Cells	RAM, ROM, Flash, various types of macro cells		
Package	48 to 256 pin QFP, PBGA, PFBGA, QFN		

Core

I/O

#### 1-3 Standard Cells

#### Standard Cells

The standard cells are semi-custom ICs that incorporates a well-designed internal logic cell and ROM/RAM, CPU peripheral circuits or analog circuits into a single chip. Compared to the gate arrays, they boast higher design flexibility, functionality and integration capabilities, providing system LSI chips optimized to the customer needs. These features greatly help electronic device manufacturers design products with a compact body, lower power consumption, and a lower cost.

		Core	I/O
S1K70000	series	1.8V	1.8V 2.5V 3.3V
Series	S1K70000 Series		1.5V
Features	<ul> <li>Large scale integration (0.18µm CMOS, using 3-/, 4-/, 5-, or 6-layer interconnect process, number of raw gates: 7,300,000 Max.)</li> <li>High-speed operation (Internal gate delay: 38.9ps/1.8V, 2-input NAND Typ.)</li> <li>Low power consumption (Internal cell: 0.054µW/MHz/gate, 1.8V, Typ.)</li> <li>Drive capacity (IoL=2, 4, 8, 12mA at 3.3V, IoL=1.5, 3, 6, 9mA at 2.5V, IoL=1, 2, 4, 6mA at 1.8V, IoL=0.75, 1.5, 3, 4.5mA at 1.5V)</li> </ul>	1.5V	2.5V 3.3V
Macro Cells	RAM, ROM, various types of macro cells		
Packages	48 pin to 256 pin QFP, PBGA, PFBGA, QFN		

S1K60000	series
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Ultra larg number o     Features     Features     Low powe	00 Series ge scale integration (0.25µm CMOS, using 3-, 4- or 5-layer interconnect process, of raw gates: 3,900,000 Max.) ed operation (Internal gate delay:106ps/2.5V, 2-input NAND Typ.)	2.5V	3.3V 2.5V 3.3V
Features Features	of raw gates: 3,900,000 Max.)	2.07	3.3V
<ul> <li>Drive cap</li> </ul>	eu operation (internar gate delay, roopsi2.39, 2-input twartor 192.) er consumption (internar cell: 0.09,i/W/MHz/gate, 2.5V, Typ.) pacity (lo∟=0.1, 1, 3, 6, 12mA at 3.3V, Io⊥=0.1, 1, 3, 6, 9, 18mA at 2.5V, Io⊥=0.05, 0.3, 1, 2, 3, 6mA at 2.0V)		
Macro Cells RAM, ROM	I, Flash, various types of macro cells		
Packages 48 pin to 25	56 pin QFP, PBGA, PFBGA, QFN		

		Core	I/O
S1K5000		2.0V	2.0V 3.3V
Series	S1K50000 Series	2.5V	2.5V 3.3V
	<ul> <li>Large scale integration (0.35µm CMOS, using 3-, 4-layer interconnect process, number of raw gates: 1,450,000 Max.)</li> </ul>	3.3V	3.3V 5.0V
Features	<ul> <li>High-speed operation (Internal gate delay:136ps/3.3V, 2-input power-NAND Typ.)</li> <li>Low power consumption (Internal cell: 0.22µW/MHz/gate, 3.3V, Typ.)</li> <li>Drive capacity (IoL=0.1, 1, 3, 8, 12, 24mA at 5.0V, IoL=0.1, 1, 2, 6, 12mA at 3.3V, IoL=0.1, 0.5, 1, 3, 6mA at 2.5V, IoL=0.05, 0.3, 0.6, 2,</li> </ul>	4mA at 2.0V)	
Macro cell	RAM, ROM, Flash, various types of macro cells.		
Package	48 pin to 256 pin QFP, PBGA, PFBGA, QFN		

#### Macro-cell lineup

		0.35µm	n (50000	Series)	0.25µm	n (60000	Series)	0.18µm (70000 Series)					
	G/A	E/A	S/C	G/A	E/A	S/C	G/A	E/A	S/C				
CPU(C17)		-	Α	Α	—	Α	Α	—	Α	А			
Flash		—	А	А	_	А	А	_	_	_			
PLL		Α	Α	Α	Α	Α	Α	—	Α	А			
Analog	ADC	—	—	—	—	—	—	—	А	А			
Analog	DAC	_	Α	Α	— A		Α	—	Α	А			
SRAM		Α	Α	Α	Α	Α	Α	Α	Α	А			

A : Available

Flash uses the SuperFlash<sup>R</sup> technologies under license from Silicon Storage Technology, Inc. Please ask our sales department about macrocell lineup other than the above-mentioned

## 1-4 Development of ASICs

ASICs are developed you to coraborate with Seiko Epson. We are preparing design libraries for various ASIC development tools

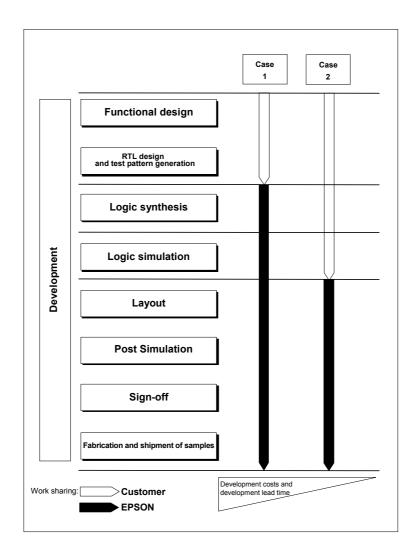
#### Case1. RTL Interface

After taking development as far as the function simulation stage, customers can send their Verilog-HDL or VHDL source files and test patterns to Seiko Epson via an HDL interface, so that Seiko Epson can perform logic synthesis.

#### Case2. Simulation Interface

Customers can use this interface to send Seiko Epson gate-level netlists and test patterns for Verilog-HDL or VHDL code that has completed the logic simulation stage.

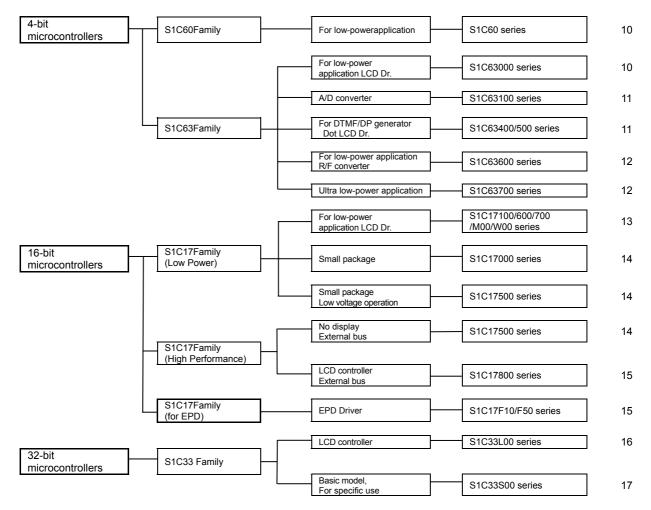
Seiko Epson will then perform the subsequent tasks beginning with interconnect layout.



2

# MCUs

Page



#### 4-bit Microcontrollers 2-1

4-bit single-chip applicationoriented microcontrollers S1C60Family: Application-oriented microcontroller

The S1C60 family microcontroller has a powerful CMOS 4-bit core CPU together with various peripheral circuits including ROM, RAM, I/O ports, and LCD drivers, all of which are condensed into a single chip. Also fused with this CMOS 4-bit single chip microcontroller is the unique low voltage/power consumption technology proprietary to Seiko Epson. The powerful functions and expansive architecture of the S1C60 family is suitable for specific purposes in diversified application fields, enabling the family to be the infinite application-oriented microcontroller.

#### S1C60 series

The microcontroller of this series integrates ROM, RAM, LCD driver, and various timer functions. It is suitable for applications to small sized equipment such as clocks, timers and thermometers.

	Display				Mer	nory		I/O			Time	r		SI	0			Inter	rupts	
Products	LCD Driver seg×com	Clock frequency Low/high Hz (Typ.)	Supply current halt/operating (frequency) µA (Typ.)	Supply voltage range (V)	ROM×12-bit	RAM×4-bit	Input port	Output port	I/O port	Event	Stopwatch	WDT	Clock	Asynchronous	Clock synchronous	R/F converter	SVD %1	External	Internal	Package (Form of delivery)
S1C60N05	20 × 1/2/3/4	32.768k	0.8/1.5	1.8 to 3.5	1,536	80	4	4	4	_	_	_	~	_	_	2		1	2	Chip
S1C60L05	2011 112/0/4	02.7000	0.0/1.0	1.2 to 2.0	1,000	00	-	-					•			-			-	QFP13-64
S1C60N08		32.768k	1.0/2.2	1.8 to 3.5																
S1C60L08	48 × 1/2/3/4	32.700K	1.0/2.2	0.9 to 1.7	4,096	832	9	8	8	2	~	~	~	_	1		~	3	3	Chip
S1C60A08	40 ~ 1/2/3/4	32.768k/ 500k	1.1/3.0(32k) 50(500k)	2.2 to 3.5	4,090	032	9	0	0	2	·		v	_		_	v	5	3	QFP15-100
S1C60N16		32.768k	0.7/1.4	2.2 to 3.6																
S1C60L16	38 × 1/2/3/4	32.100K	0.7/1.4	1.2 to 1.8	4,096	256	5	8	8	2	~	~	~	_	1	_	~	2	3	Chip
S1C60A16	30 × 1/2/3/4	32.768k/ 1M	1.5/2.4(32k) 50(1M)	2.2 to 3.6	7,090	230	5	5	5	2		•	•		1		•	2	5	QFP14-80

\*1: SVD is an abbreviation for Supply Voltage Detector.

#### 4-bit single-chip applicationoriented microcontrollers

The S1C63 Family provides abundant instructions as well as a high-speed instruction cycle (2-6 CPI) to the products to enable high-speed operation. The CMOS 4-bit microcontroller in this family also features low voltage operation and low current consumption.

S1C63Family: Application-oriented microcontroller

#### S1C63000 series

The microcontroller in this Family integrates ROM, RAM, LCD driver, and various timer functions. It is characterized by a wide range of operating voltages and low power consumption levels, and is suitable for watches and clocks for which you want to extend battery life, as well as portable devices with temperature measurement functions.

	Display	-		-	Men	nory		I/O			Tim	er	0	S	0				Inter	rupts	
Products	LCD Driver seg×com	Clock frequency Low/high Hz (Typ.)	Supply current sleep/halt/operating (frequency) µA (Typ.)	Supply voltage range (V)	ROM×13bit	RAM×4bit	Input port	Output port	I/O port	Programmable 8-bit	Stopwatch	WDT	Clock	Asynchronous	Clock synchronous	R/F converter	Buzzer	SVD %1	External	Internal	Package (Form of delivery)
S1C63003	22(Max) × 3/4/5 ※2	32.768k/ 550K	0.1 / 0.5/2.3(32k) 40(550k)	1.1 to 1.7 1.8 to 5.5	4,096	256	_	_	16 ※3	1	~	~	~	_	_	2	۲	_	4	11	Chip QFP12-48
S1C63004	36(Max) × 3/4/5/6/7/8 ※4	32.768k/ 4M,1M	0.1 / 0.5/2.3(32k) 220(4M),60(1M)	1.1 to 1.7 1.8 to 5.5	4,096	512	_	_	20 ※5	3 ※6	~	~	~	_	1 ※7	2	~	>	8	23	Chip QFP14-80 TQFP14-100
S1C63008	50(Max) × 3/4/5/6/7/8 ※8	32.768k/ 4M,1M	0.1 / 0.5/2.3(32k) 220(4M),60(1M)	1.1 to 1.7 1.8 to 5.5	8,192	1,024	_	_	24 ※9	3 ※6	~	~	~	_	1 ※7	2	~	>	8	23	Chip QFP15-100 TQFP14-100
S1C63016	56(Max) × 3/4/5/6/7/8 ※8	32.768k/ 4M,1M	0.1 / 0.5/2.3(32k) 220(4M),60(1M)	1.1 to 1.7 1.8 to 5.5	16,384	2,048	_	_	24 ※9	4 ※6	~	5	>	_	1 ※7	2	~	>	8	25	Chip QFP15-100 TQFP14-100
S1C6F016	56(Max) × 3/4/5/6/7/8 ※8	32.768k/ 4M	0.7 / 2.0/9.0(32k) 950(4M)	1.8 to 3.6 ※10	16,384 (Flash) ※11	2,048	_	_	24 ※9	4 ※6	~	~	~	_	1 ※7	2	~	~	8	25	Chip QFP15-100

\*1: SVD is an abbreviation for Supply Voltage Detector. \*2: Total 12 segment terminals share the function with I/O ports and R/F converter terminals (to be selected by mask option). \*3: Total 4 I/O ports share the function with sgment terminals (to be selected by mask option), and 4 share with R/F converter terminals (to be selected by software).

\*4: Total 16 segment terminals share the function with I/O ports and R/F converter terminals (to be selected by mask option).
 \*5: Total 8 I/O ports share the function with segment terminals (to be selected by mask option), and 4 share with R/F converter terminals (to be selected by software).

\*6: Two 8 bits serve as a 16-bit timer. \*7: Connectable to SPI
\*8: A total of 20 segment terminals share the function with I/O ports and R/F converter terminals (to be selected by mask option). \*9: Total 12 I/O ports share the function with segment terminals (to be selected by mask option), and 4 share with R/F converter terminals (to be selected by software). \*10: During programming in flash memory : 2.7V to 3.6V.

\*11: This product use SuperFlash® technology licensed from Silicon Storage Technology, Inc

#### S1C63100 series

A microcontroller being equipped with ROM, RAM, serial I/F, A/D converter, various timer functions, etc. It features built-in A/D converter, wide operating voltage range and low power consumption and is suitable for portable equipment.

	Display				Men	nory		I/O			Tim	er		SI	0						_	Inter	rupts	
Products	LCD Driver seg×com	Clock frequency Low/high Hz (Typ.)	Supply current halt/operating (frequency) µA (Typ.)	Supply voltage range (V)	ROM×13bit	RAM×4bit	Input port	Output port	I/O port	Programmable 8-bit	Stopwatch	WDT	Clock	Asynchronous	Clock synchronous	A/D converter	Buzzer	SVD %1	DTMF output	DP output	FSK demodulation circuit	External	Internal	Package (Form of delivery)
S1C63158	—	32.768k/4M	1.0/3.0(32k) 900(4M)	0.9 to 3.6 2.2 to 3.6	8,192	512	9	12	20	2 ※2	_	~	>	_	1	4 ※3	~	~	_			3	8	Chip QFP12-48 QFP13-64 PFBGA5U-60

\*1: SVD is an abbreviation for Supply Voltage Detector.\*2: Two 8 bits serve as a 16-bit timer.

\*3: 8 bits successive-approximation type and serves as general-purpose I/O.

#### S1C63400/500 series

A microcontroller being equipped with ROM, RAM, dot-matrix LCD driver, various timer functions, etc. It features wide operating voltage range and low power consumption and is suitable for portable equipment such as data banks which require dot-matrix indications.

	Display				Merr	nory		I/O			Tim	er		SI	0						-	Inter	rupts	
Products	LCD Driver seg×com	Clock frequency Low/high Hz (Typ.)	Supply current halt/operating (frequency) µA (Typ.)	Supply voltage range (V)	ROM×13bit	RAM×4bit	Input port	Output port	I/O port	Programmable 8-bit	Stopwatch	WDT	Clock	Asynchronous	Clock synchronous	R/F converter	Buzzer	SVD %1	DTMF output	DP output	FSK demodulation circuit	External	Internal	Package (Form of delivery)
S1C63408	60×8/9/16/17	32.768k/ 4M	1.3/3.0(32k) 550(4M)	1.3 to 3.6 1.8 to 3.6	8,192	1,024	4	4	4	2 ※2	~	~	~	1 *	3	_	_	~	_	_	_	4	11	Chip QFP15-128
S1C63567	60×8/16/17	32.768k/ 3.58M	1.5/10(32k) 600(3.58M)	2.2 to 5.5	16,384	5,120	8	12	16	2 ※2	>	~	>	1 ※	3	_	>	~	>	2	_	2	12	Chip QFP20-144

\*1: SVD is an abbreviation for Supply Voltage Detector.

\*2: Two 8 bits serve as a 16-bit timer.

st3: Either start/stop system or clock synchronous system can be selected, depending on software

#### S1C63600 series

The microcontroller of this series integrates ROM, RAM, multiplication and division circuits, LCD driver, R/F converter, and a variety of timer functions. Since this series features a wide range of operating voltage and low power consumption, it is best fit for portable equipment with temperature measuring facility that requires battery-powered operation.

	Display				Mer	nory		I/O			Tin	ner		SI	0						_	Inter	rupts	
Products	LCD Driver seg×com	Clock frequency Low/high Hz (Typ.)	Supply current sleep/halt/ operating (frequency) µA (Typ.)	Supply voltage range (V)	ROM×13bit	RAM×4bit	Input port	Output port	I/O port	Programmable 8-bit	Stopwatch	WDT	Clock	Asynchronous	Clock synchronous	R/F converter	Buzzer	SVD %1	DTMF output	DP output	FSK demodulation circuit	External	Internal	Package (Form of delivery)
S1C63654	32× 3/4/5/6	32.768k 32.768k/4M	/ 0.65/2.5(32k) 800(4M)	1.8 to 3.6 2.4 to 3.6	4,096	512	8	4	8	2 ※2	~	~	~	—	1	2	r	~	-	-	_	2	15	Chip QFP15-100
S1C63656	38 × 3/4	32.768k 32.768k/4M	/ 0.6/2.5(32k) 800(4M)	1.1 to 3.6 <u>*4</u> 2.4 to 3.6	6,144	1,024	8	4	8	2 ※2	~	~	~	_	1	2	~	~	-	_	_	2	18	Chip QFP20-144
S1C63658	56 × 4/5/8	32.768k 32.768k/4M	/ 0.65/2.5(32k) 800(4M)	1.8 to 3.6 2.4 to 3.6	8,192	1,024	8	8	8	3 ※2	~	~	~	_	1	2	~	~	-	_	_	2	16	Chip QFP20-144
S1C63666	64 × 4/5/8	32.768k 32.768k/4M	/ 0.65/2.5(32k) 800(4M)	1.5 to 3.6 2.4 to 3.6	16,384	5,120	8	8	8	3 ※2	~	~	2	_	1	2	~	۲	-	_	_	2	14	Chip QFP20-144
S1C63616	56 × 16 48 × 24 40 × 32	32.768k/4M	0.08/ 0.6/2.5(32k) 320(4M)	1.6 to 5.5	16,384	2,048	_	_	16	8 ※2	~	~	2	_	1 ※3	2	~	~	_	_	_	8	32	Chip TQFP15-128
S1C63632	64 × 16/ 56 × 24/ 48 × 32	32.768k/4M	0.08/ 0.6/2.5(32k) 320(4M)	1.6 to 5.5	31,744	8,192	-	_	24	8 ※2	~	~	~	_	1 ※3	2	~	۲	-	_	_	8	32	Chip QFP20-144 VFBGA10H-144
S1C6F632	64 × 16/ 56 × 24/ 48 × 32	32.768k/4M	0.7/ 2.0/9.0(32k) 960(4M)	1.8 to 3.6 ※5	31,744 (Flash) ※6	8,192	_		24	8 ※2	~	~	>	_	1 ※3	2	~	۲		_	_	8	32	Chip QFP20-144 VFBGA7H-144

\*2: Two 8 bits serve as a 16-bit timer.

\*3: Connectable to SPI

\*4: When using OSC1 single clock without LCD contrast adjustment (1.8V to 3.6V for other specifications).

\*5: During writing in flash memory: 7.0V (Typ)
 \*6: This product uses SuperFlash<sup>®</sup> technology licensed from Silicon Storage Technology, Inc.

#### S1C63700 series

The microcontroller of this series integrates ROM, RAM, LCD driver and a variety of timer functions. Since this series features ultra low nower consumption, it is best fit for nortable equipment such as watch which desires long life of battery

Since this	series tea	itures ultra i	low power co	nsumptio	on, it is	Dest fit	TOF L	ona	eidi	equi	pme	ent s	ucn	as v	vatc	n w	nicn	ae	sires	s ior	ig lite	3 01	Datt	ery.
	Display				Mer	nory		I/O			Tim	ner		SI	0	L			t			Inter	rupts	
Products	LCD Driver seg×com	Clock frequency Low/high Hz (Typ.)	Supply current halt/operating (frequency) µA (Typ.)	Supply voltage range (V)	ROM ×13bit (Byte)	RAM ×4bit (Byte)	Input port	Output port	I/O port	Programmable 8-bit	Stopwatch	WDT	Clock	Asynchronous	Clock synchronous	R/F converte	Buzzer	SVD %1	DTMF output	DP output	FSK demodulation circuit	External	Internal	Package (Form of delivery)
S1C63709	64×4/5/8	32.768k	0.15/3.5(32k)	1.0 to 3.6	12.288	2,048	13		18	3	~	~	٢		1							2	18	Chip
31003709	04~4/3/6	32.768k/4M	1000(4M)	2.1 to 3.6	12,200	2,040	13	_	10	Ж1	*	~	•	_	'	_	•	•	_	_	_	4	10	QFP20-144

\*1: Two 8 bits serve as a 16-bit timer.

#### 2-2 16-bit Microcontrollers

16-bit RISC Microcontrollers S1C17 Family Application-oriented microcontroller

The S1C17 Family, 16-bit RISC microcontrollers integrate a wide variety of peripheral circuits such as various interfaces that meet various types of sensors and the EPD Driver/controller, LCD driver/controller that covers the wide display area into a single chip design. They can realize both high-speed operation and low power consumption, and provide the products suitable to portable gears. Also, various flash ROM built-in products are lined up. The flexible development environment and on-chip ICE functions can shorten the product development period.

#### S1C17100/600/700/M00/W00 series (Stand-alone Low Power)

This 16-bit MCU has improved the throughput and the development environment while maintaining low power consumption just like 4/8-bit EPSON MCU. This 16-bit MCU incorporates an LCD driver, power circuit, clock function and various types of I/F and enables to realize applications with 1 chip. This MCU is most suitable for portable terminals such as clock (watch, clock) and remote controller.

With FOII	p. m.		5 most a	1	portable	lem	iiiiais	5 500	JII a		JUK	( •• •	aici	1, U	100	к) е	inu	Ten	nou		Unu	UIIC				
Display	С	lock freque	ncy	current sleep/		N	lemor	ý	I/O			Т	ïmei	r ı								P	10-bit	sor		
LCD Driver seg×com	High speed [Hz] (Max.)	Low speed [Hz] (Typ.)	built-in oscillator (Hz) (Typ.)	halt/ operating (32K)/ operating (1M) µA(Typ.)	Supply voltage (V)	Flash (Byte)	ROM (Byte)	RAM (Byte)	I/O port	8-bit PWM	16-bit	16-bit PWM	Stopwatch	WDT	Clock	Real Time Clock	IdS	I <sup>2</sup> C master	I <sup>2</sup> C slave	UART(IrDA1.0)	Remote control circuit	R/F converte	A/D converter, 1	Multiplier/Divi	SVD %1	Package (Form of delivery)
40x4/3/21 36x8	4.2M	32.768k	2.7M	0.15/ 0.9/ 7.0/250	1.8 to 3.6	-	32K	2K	36	3	3	1	1	~	1	_	1	~	~	2	٢	2	8	٢	~	Chip TQFP14-100 VFBGA7H-144
12x4/3/2/1 8x8	8.2M	32.768k	2.7M	0.6/2.0/ 12/400	1.8 to 3.6 ※2	32K ※3	I	2K	19	2	3	2	1	~	1	—	1	~	~	1	-	1	4	~	~	Chip QFP12-48
20x4/3/2/1 16x8	8.2M	32.768k	2.7M	0.6/2.0/ 12/340	1.8 to 3.6 ※2	32K ※3	-	2K	24	2	3	2	1	~	1	_	1	~	~	1	_	1	4	~	~	Chip TQFP13-64 VFBGA8H-81
40x4/3/2/1 36x8	8.2M	32.768k	2.7M	0.75/2.5/ 15/410	1.8 to 3.6 ※2	32K ※3	_	2K	36	3	3	1	1	~	1	_	1	~	~	2	~	2	8	~	~	Chip TQFP14-100 VFBGA7H-144
40x4/3/2/1 36x8	8.2M	32.768k	2.7M	0.75/2.5/ 15/410p	1.8 to 3.6 ※2	64K ※3	_	4K	36	3	3	1	1	~	1	_	1	~	~	2	~	2	8	~	~	Chip TQFP14-100 VFBGA7H-144
56x4/3/2/1 52x8	8.2M	32.768k	2.7M	0.75/2.3/ 14/400	1.8 to 3.6 ※2	₩3	_	4K	47	3	3	1	1	~	1	—	1	~	~	2	~	2	8	~	~	Chip TQFP15-128
40x4/3/2/1 36x8	8.2M	32.768k	2.7M	0.75/2.3/ 14/400	1.8 to 3.6 ※2	128K ※3	_	8K	36	3	3	3	1	~	1	~	1	~	~	2	~	2	8	~	~	Chip TQFP14-100
56x4/3/2/1 52x8	8.2M	32.768k	2.7M	0.75/2.3/ 14/400	1.8 to 3.6 ※2	128K ※3		8K	47	3	З	3	1	~	1	~	1	۷	٢	2	٢	2	8	٢	~	Chip TQFP15-128
20 x 4	4.2M	32.768k	2M/1M /500k		2.0 to 3.6	_	16K	2K	12	1	_	1	_	~	1	~	1	_		1	_	_	-	~	~	Chip
20 x 4	4.2M	32.768k	2M/1M /500k/ 32k	0.09/0.42/ 10/350	2.0 to 3.6	16K ※8	Ι	2K	12	1		1	_	~	1	~	1	~	_	1	Ι	_	$\left -\right $	٢	~	Chip TQFP13-64
32 x 4	4.2M	32.768k	2M/1M /500k/ 32k	0.09/0.42/ 10/350	2.0 to 3.6	16K ※8		2K	12	1	_	1	_	~	1	~	1	_	_	1	-	_	-	٢	~	Chip※7 TQFP14-80
32 x 4 28 x 8	16.3M	32.768k	7.37M	0.35/0.8/12.5/ 210	1.8 to 5.5 ※9	32K ※8	Ι	4K	19	Ι	5	—	—	~	—	~	2	~	~	1	Ι	1	-	Ι	~	Chip TQFP13-64
64x16/8 56x24	8.2M	32.768k	2.7M	1.0/2.0/ 12/400	1.8 to 3.6 ※2	64K ※3		4K	29	_	4	4	1	~	1	—	1	—	~	1	~	2	8	~	~	Chip TQFP15-128 VFBGA10H-144
72x16 56x32	8.2M	32.768k	_	1.0/2.6/ 17/550	1.8 to 3.6 ※2	64K ※3	_	4K	28	2	3	1	1	~	1	_	1	✔ ※6	✔ ※6	1	۲	_	-	_	~	Chip TQFP24-144 VFBGA10H-144 VFBGA7H-161 PFBGA6U-96
88x16 72x32	8.2M	32.768k	2.7M	1.0/2.5/ 16/450	1.8 to 3.6 ※2	128K ※3	1	12K	28	3	3	2	1	~	1	_	1	✔ ※6	✔ ※6	2	۲	_	-	~	~	Chip QFP21-176 VFBGA8H-181 VFBGA10H-180
120x16/24/ 32 60x64	8.2M	32.768k	2.7M	1.0/2.5/ 15/450	1.8 to 3.6 ※4	256K ※3		12K	34	_	5	4	1	~	1	_	3	~	~	2	۲	2	8	۲	~	Chip QFP21-216 VFBGA10H-24
128x16/24/ 32 64x64	8.2M	32.768k	2.7M	1.2/2.7/ 18/550	1.8 to 3.6 ※2	512K ※3	_	12K	35	_	5	4	1	~	1	_	3	~	~	2	۲	2	8	~	~	Chip VFBGA10H-240
160x16/24/ 32 64x64	8.2M	32.768k	2.7M	1.2/2.7 18/550	1.8 to 3.6 ※4	1M ※3		12K	35	_	5	4	1	~	1	_	3	~	~	2	~	2	8	~	~	Chip QFP22-256
34 x 4 30 x 8	4.2M	32.768k	4M/2M/ 1M/ 500k/	0.15/ 0.3/ 4/ 250		64K ※10	_	4K	39	_	2	2	_	~	_	1	~	~	_	2	_	4 ※12	_	~	~	Chip QFP14-80 QFP15-100 SQFN9-64
24 x 4 20 x 8			700k	0.15/ 0.5/ 8/ 250					31														Ш			QFN9-64 QFN-13-64
72 x 8 64 x 16 56 x 24	4.2M	32.768k	4M/2M/ 1M/ 500k/ 700k	0.15/ 0.3/ 4/ 250		64K ※10	_	4K	41	_	2	2	—	~	—	~	1	~	~	1	_	<b>2</b> ※12	-	~	~	Chip TQFP15-128
72 x 8 64 x 16 56 x 24	4.2M	32.768k	4M/2M/ 1M/ 500k/ 700k	0.15/ 0.3/ 4/ 250	1.2 to 3.6 ※10	96K ※10		8K	41	_	4	3	_	~	_	~	2	~	~	2	۲	<b>2</b> ※12	6 ※11	~	~	Chip TQFP15-128
	Display LCD Driver seg×com 40x4/3/21 36x8 12x4/3/2/1 36x8 20x4/3/2/1 16x8 20x4/3/2/1 36x8 40x4/3/2/1 36x8 56x4/3/2/1 52x8 40x4/3/2/1 52x8 20 x 4 20 x 8 20 x 4 20 x 4 20 x 8 20	Display         C           LCD Driver seg×com         High priver (Max.)           40x4/3/21 36x8         4.2M           12x4/3/2/1 36x8         8.2M           20x4/3/2/1 16x8         8.2M           40x4/3/2/1 36x8         8.2M           40x4/3/2/1 36x8         8.2M           40x4/3/2/1 36x8         8.2M           40x4/3/2/1 36x8         8.2M           20x4/3/2/1 36x8         8.2M           20x4/3/2/1 36x8         8.2M           20x4         4.2M           20x4         4.2M           20x4         4.2M           20x4         4.2M           20x4         4.2M           32x4         4.2M           32x4         8.2M           64x16/8         8.2M           72x16         8.2M           72x16         8.2M           72x32         8.2M           120x16/24/ 32         8.2M           3	Display         Clock freque           LCD Driver seg×com         High speed (Max.)         Low speed (Hz) (Typ.) $40x4/3/21$ 36x8         4.2M         32.768k $12x4/3/2/18x8$ 8.2M         32.768k $20x4/3/2/116x8$ 8.2M         32.768k $40x4/3/2/136x8$ 8.2M         32.768k $20x4$ 4.2M         32.768k $20x4$ 4.2M         32.768k $20x4$ 4.2M         32.768k $32x4$ 8.2M         32.768k $32x4$ 4.2M         32.768k $32x4$ 8.2M         32.768k $56x32$ 8.2M         32.768k $72x16$ 8.2M         32.768k $72x16$ 8.2M         32.768k $120x16/24/32/32$ 8.2M         32.768k $120x16/24/32$ 8.2M         32.768k <t< td=""><td>Display         Clock frequency           LCD Driver seg.xcom         High  H2  (Max.)         Low speed  H2  (Typ.)         built-in oscillator (H2)           40x4/3/21 36x8         4.2M         32.768k         2.7M           20x4/3/2/1 16x8         8.2M         32.768k         2.7M           40x4/3/2/1 36x8         8.2M         32.768k         2.7M           40x4/3/2/1 36x8         8.2M         32.768k         2.7M           40x4/3/2/1 36x8         8.2M         32.768k         2.7M           56x4/3/2/1 36x8         8.2M         32.768k         2.7M           56x4/3/2/1 36x8         8.2M         32.768k         2.7M           20 x 4         4.2M         32.768k         2.7M           20 x 4         4.2M         32.768k         2.7M           20 x 4         4.2M         32.768k         2.M1M           20 x 4         4.2M         32.768k         2.MV1M           20 x 4         4.2M         32.768k         2.M1M           32 x 4         16.3M         32.768k         7.37M           64x16/8         8.2M         32.768k         2.7M           72x16         8.2M         32.768k         2.7M           72x16         <td< td=""><td><math display="block">\begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block">\begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{                                    </math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td>Display         Clock trequery         Supply trepulsion operation operatioperation operation operation operation operation o</td><td>Index of all all of all all all of all all all all all all all all all al</td><td>Display         Circle frequency         Under stress         Display         Circle frequency         Under stress         Display         Display</td><td>Display         Display         Uniformation of participant of partinantex participant of partinante</td></td<></td></t<>	Display         Clock frequency           LCD Driver seg.xcom         High  H2  (Max.)         Low speed  H2  (Typ.)         built-in oscillator (H2)           40x4/3/21 36x8         4.2M         32.768k         2.7M           20x4/3/2/1 16x8         8.2M         32.768k         2.7M           40x4/3/2/1 36x8         8.2M         32.768k         2.7M           40x4/3/2/1 36x8         8.2M         32.768k         2.7M           40x4/3/2/1 36x8         8.2M         32.768k         2.7M           56x4/3/2/1 36x8         8.2M         32.768k         2.7M           56x4/3/2/1 36x8         8.2M         32.768k         2.7M           20 x 4         4.2M         32.768k         2.7M           20 x 4         4.2M         32.768k         2.7M           20 x 4         4.2M         32.768k         2.M1M           20 x 4         4.2M         32.768k         2.MV1M           20 x 4         4.2M         32.768k         2.M1M           32 x 4         16.3M         32.768k         7.37M           64x16/8         8.2M         32.768k         2.7M           72x16         8.2M         32.768k         2.7M           72x16 <td< td=""><td><math display="block">\begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block">\begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td><math display="block"> \begin{array}{                                    </math></td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td>Display         Clock trequery         Supply trepulsion operation operatioperation operation operation operation operation o</td><td>Index of all all of all all all of all all all all all all all all all al</td><td>Display         Circle frequency         Under stress         Display         Circle frequency         Under stress         Display         Display</td><td>Display         Display         Uniformation of participant of partinantex participant of partinante</td></td<>	$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{                                    $	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Display         Clock trequery         Supply trepulsion operation operatioperation operation operation operation operation o	Index of all all of all all all of all all all all all all all all all al	Display         Circle frequency         Under stress         Display         Circle frequency         Under stress         Display         Display	Display         Display         Uniformation of participant of partinantex participant of partinante

 \*1: SVD is an abbreviation for Supply Voltage Detector. \*2: During programming in flash memory: 2.7V to 3.6V
 \*3: This product uses SuperFlash<sup>®</sup> technology licensed from Silicon Storage Technology, Inc. \*4: During programming in flash memory: 2.5V to 3.6V
 \*5: Single instruction is executed in 1.5 clocks; the consumption current is 14µA at 32 kHz execution and 420µA at 1 MHz execution. \*6: Master fur \*6: Master function only

Actioning matching and a second matching of the second

\*12: Independent operation for each channel. \_\_\_\_: Under Development

#### S1C17000 series (small package), S1C17500 series (small package with low-voltage operation)

The series products specialized for applications.

The lineup includes the WCSP 48-pin package (approximately 3 mm ), which is optimum for portable devices requiring a limited mounting area. With its extensive serial I/F and A/D converter, this series is also available to sensor applications.

	Display		Clock frequer	псу			M	lemory	,	I/O			Tin	ner				SI	0						
Products	LCD Driver seg×com	High speed [Hz] (Max.)	Low speed [Hz] (Typ.)	built-in oscillator (Hz) (Typ.)	Supply current sleep/ halt/ operating (32K)/ operating (1M) µA(Typ.)	Supply voltage (V)	Flash (Byte)	ROM (Byte)	RAM (Byte)	I/O port	8-bit PWM	16-bit	16-bit PWM	Stopwatch	WDT	Clock	SPI	l²C	UART(IrDA1.0)	Remote control circuit	R/F converter	A/D converter, 10-bit	Multiplier/Divisor	SVD	Package (Form of delivery)
S1C17001	_	8.2M	32.768k	_	0.5/2.5/ 10/256	1.65 to 2.7 (Core) 1.65 to 3.6/ (I/O)	_	32K	2K	28	2	3	1	1	~	1	1	1 ※1	1	~	_		-	_	Chip QFP12-48 QFN7-48 WCSP-48
S1C17003	_	20M	32.768k	_	1.0/3.3/ 8.0/350	1.65 to 1.95 (Core) 1.65 to 3.6 (I/O)	_	64K	4K	34	3	3	1	1	~	1	1	1	2	~	_	4	~	_	Chip TQFP12-64 WCSP-48
S1C17554	Ι	24M	32.768k	_	0.8/2.7/ 16/450	1.65 to 1.95 (Core) 1.65 to 5.5 (I/O)	128K ※2	_	16K	34 / 40 ※3	_	5	4	1	~	1	3	1	2	~	_	4	2	I	Chip TQFP13-64 WCSP-48
S1C17564	_	24M	32.768k	2 to 12M	0.8/2.7 16/ 450	2.0 to 5.5	128K ※2	_	16K	40	_	5	4	1	~	1	3	1	2	~	_	4	2	_	Chip TQFP13-64
S1C17555	-	12M	32.768k	2M/4M/ 8M/12M	1.0/2.9/ 140/ 3500	1.65~1.95 (Core) 1.65~3.6 (I/O)	128K ※4	_	16K	20	_	5	4	1	~	1	3	1	1	_	_		>		WCSP-48
S1C17565	_	24M	32.768k	2M/4M/ 8M/12M	1.0/ 2.9/ 140/ 3500	1.65~1.95 (Core) 1.65~3.6 (I/O)	128K ※4	_	16K	24	—	5	4	1	~	1	3	1	2	~	—	6 ※5	~	—	Chip TQFP13-64

\*1: Master function only

2: During programming in flash memory : 7.0V(Typ) /Erasing:7.5V(Typ)
 3: TQFP12-64 :I/O=40, WCSP-48:I/O=34

\*4: During programming in flash memory : 7.5V(Typ) \*5: Resolutioh 12-bit

: Under Development

#### S1C17500 Series (High-performance models)

The 16-bit RISC MCUs allowing the 32-bit level sophisticated processing to perform. The device has a wide variety of interfaces such as USB, UART, SPI, I<sup>2</sup>C, I<sup>2</sup>S, A/D converter, and remote control interfaces, and it can improve the user interface of various home appliances (for example, the washing machines, rice cookers, and coffee makers) that use music, voice, touch switch and other interfaces.

	Display	Cloc	ck freque	ency			I	Men	nory		Bu	s	I/	0		Т	ïme	r			S	10								
Products	VRAM with built-in LCD controller/ Max.	High speed [Hz] (Max.)	Low speed [Hz] (Typ.)	built-in oscillator (Hz) (Typ.)	Supply current sleep/ halt/ operating (frequency) µA(Typ.)	Supply voltage (V)	Flash (Byte)	ROM (Byte)	RAM (Byte)	Battery backup (bytes)	Data bus	Address bus	I/O port	Support of multiple voltages *6	8-bit PWM	110-01 MMMJ HH-91	Stopwatch	WDT	Clock	SPI		UART(IrDA1.0)	Remote control circuit	A/D converter. 10-bit	Card I/F	Multiplier/MAC	Divisor	USB	Package (Form of delivery)	Others
S1C17501	_	48M	32.768 k		1.4%3/ 16m(48M) / 37m(48M)	3.0 to 3.6	96K ※1 128 K ※1		4K		8/16 ※4	23	91 ※5	_	6	2 1			1 ※2	2	1	1	2	8	~	2	—	FS. 2.0	TQFP14-100 TQFP15-128 ※7	
*1: This pr	roduct uses S	uperFlash	<sup>®</sup> techno	logy licens	ed from Silico	on Storage	e Tec	hno	logy,	Inc.																				

\*2: Real-time clock (The battery backed up operation is supported.)

×3: Unmounted OSC1.

\*4: The TQFP14-100 has the 8-bit fixed data bus.

\*5: Universal serial interface (Any of UART, SPI and I<sup>2</sup>C functions can be selected.)

\*6: Coexistence of 5V and 3V (and other) different interface voltages is supported.

\*7: TQFP14-100 (96KB flash memory), TQFP15-128 (128KB flash memory)

#### S1C17800 series (High-performance models)

The 16-bit RISC MCUs allowing the 32-bit level sophisticated processing to perform. The device having the LCDC can display the 1-bpp maximum VGA monochrome images. Also, the device integrates a wide variety of interfaces such as USB, UART, SPI, I<sup>2</sup>C, I<sup>2</sup>S, ADC, and remote control interfaces, and it can improve the user interface of various home appliances (for example, the washing machines, rice cookers, and coffee makers) that use the display, music, voice, touch panel and other interfaces.

	Display	Cloc	k freque	ncy			Ν	/lem	iory		Bus	5	I/O			Tim	ner			ę	SIO				Ĩ	[			
Products	VRAM with built-in LCD controller/Max.	High speed [Hz] (Max.)	Low speed [Hz] (Typ.)	built-in oscillator (Hz) (Typ.)	Supply current sleep/ halt/ operating (frequency) µA(Typ.)	Supply voltage (V)	Flash (Byte)	ROM (Byte)	RAM (Byte)	Battery backup (bytes)	Data bus	Address bus	I/U port Support of multiple voltages	8-bit PWM	16-bit	16-bit PWM	Stopwatch	Clock	SPI	1 <sup>2</sup> C	UART(IrDA1.0)	l <sup>2</sup> S	A ID control circuit	Card I/F	Multiplier/MAC	Divisor	ASU	Package (Form of delivery)	Others
S1C17801	STN 120×120 1bpp/ QVGA 4bpp, VGA 1bpp	48M	32.768k	Ι	1.4%6 / 16m(48M) / 37m(48M)	3.0 to 3.6	128K ※7		4K	2K8 ※1	8/16 ※3	23 🖇	91 «4	- 6	2	1	— v	• 1 ※	2 2	1	1	2	•	3	1		FS 2.0	TQFP15-128 PFBGA7U-144	l/F of LCD-DR only
S1C17803	STN QVGA 1bpp/ QVGA 4bpp, VGA 1bpp	33M	32.768k	_	1.3%6 / 15m(33M) / 19m(33M)	2.7 to 5.5	128K ※7		16K	168	8/162	23 9	17 🗸	4	1	2	— v	• 1 **	2 2 ※4	2 +2 ※4	1 +2 ※4	1.	/ /	4 <b>~</b>	~	~	_	TQFP14-100 TQFP15-128	l/F of LCD-DR only

\*1: Also used as the VRAM

\*2: Real-time clock (The battery backed up operation is supported.)

\*3: The TQFP14-100 has the 8-bit fixed data bus.

\*4: Universal serial interface (Any of UART, SPI and I<sup>2</sup>C functions can be selected.)
 \*5: Coexistence of 5V and 3V (and other) different interface voltages is supported.

\*5: Coexistence of 5V and 3V (and other) different interface

\*6: Unmounted OSC1.

\*7: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

#### S1C17F10/F50 series (EPD application)

#### Specific to electronic paper (EPD) applications

The product also includes embedded features such as a real-time clock, theoretical regulation, a driver capable of wringing the maximum performance from segmented EPDs, and a temperature sensor. As a result, the device does not simply drive the display, but also corrects temperature effects that could harm display quality making it possible to maximize the characteristics of an e-paper display with a single chip. The S1C17F10 series is an ultra-low power consumption microcontroller which consists of display memory for active EPD panels, an EPD timing controller for transmitting display data and an EPD panel control library (EPD Tcon Library). As a communication interface with EPD panels and other devices, this series has built-in synchronous serial interface, parallel interface, UART and I<sup>2</sup>C. Environment conditions can also be detected by temperature and humidity measurement with an R/F converter, and supply voltage measurement with a supply voltage detection circuit and brown-out reset.

	Display	С	lock frequ	ency			M	emor	у	I/O			Tir	ner				SIO			tion	_		
Products	EPD Driver segment (TP/BP)	High speed [Hz] (Max.)	Low speed [Hz] (Typ.)	Build-in oscilator [Hz] (Typ.)	Supply current Sleep/ Halt/ operating(32K)/ operating(4M) µA(Typ.)	Supply	Flash (Byte)	ROM (Byte)	RAM (Byte)	I/O port	8-bit PWM	16-bit	16-bit PWM	Stopwatch WDT	Clock	Real Time Clock	SPI	I <sup>2</sup> C	UART(IrDA1.0)	R/F converter	Temperature detecttion	Multiplier/Divider	SVD %1	Package (Form of delivery)
S1C17F57	64 (2TP/2BP)	4.2M	32.768k	2M/1M /500k	0.12/ 0.55/ 20/ 1400	2.0 to 3.6	32K ※2	_	2K	29	2 -	_	2	1 🗸	1	~	1	1	1	1	~	~	٢	Chip TQFP15-128
S1C17F13	—	20M	32.768k	20M/16M /12M/8M /32k	0.35/0.77/ 11.93/1450	2.0 to 3.6	128K ※2	_	20K	37	_	4	2 -	- ~	1	~	3	1	1	2	~	~	~	Chip TQFP13-64

%1: SVD is an abbreviation for Supply Voltage Detector%2: During programming in flash memory 7.0V(Typ)

					comm interfa						Form of de	livery
Products	EPD Driver segment (TP/BP)	Supply voltage (V)	EPD Drive voltage (V)	Flash ROM (Byte)	I <sup>2</sup> C Slave	SPI slave	Internal oscillator Frequency [Hz]	Tempera ture sensor	Power on reset	Boosting circuit	Package	Chip
S1D14F57	256 (2TP/2BP)	1.75 to 5.5	9.15 /12.30 /15.45	16K ※1	~	~	1M	~	~	~	_	~

## 2-3 32-bit Microcontrollers

 32-bit RISC Microcontrollers S1C33 Family Application-oriented microcontroller

The S1C33 Family are 32-bit RISC microcontrollers having the DMA, serial interface, various timers, PLL, prescaler and other basic functions, plus high-performance A/D converter, USB controller, the LCD controller allowing the color display, and other powerful peripheral functions. The devices featuring the high-speed operation and low power consumption are suitable to a wide variety of home appliances such as printer and other office automation (OA) equipment, IC dictionary, multifunctional remote controllers, and toys.

#### S1C33L00 series

The 32-bit RISC microcontroller has the built-in LCD controller and can greatly contribute to the compact instrumentation design and reduced power consumption in the IC dictionary, PDA and other portable display applications.

	CF	PU C	ore	Dis	play		Supply		1	Memo	ory	1/0	0		Tir	ner				SIO			bit	DM	A			Ô	Ô		
Products	STD	ЪЕ	ADV		CD roller LLL (ddq)	Clock frequency Low/high Hz (Max.)	current Sleep/ Halt/ operating (frequency) (Typ.) ※ 1	Supply voltage range (V)	ROM (Byte)	RAM (Byte)	VRAM (Byte)	Input port	Output port	8-bit PWM	16-bit	16-bit PWM	WDT	Clock	UART(IrDA1.0)	SPI	L'C	ŕs	A/D converter, 10-bit	HSDMA	IDMA	USB	SDRAMC	NAND flash C(SLC)	NAND flash C(MLC)	Package (Form of delivery)	Remarks
S1C33L17	_	~	Ι	16	16	66M / 32.768K	1μΑ / 3.2mA(48M) / 22mA (48M)	Core 1.65 to 1.95 I/O 2.7 to 3.6 USB 3.0 to 3.6	_	8K	12K	_	82 ※ 2/3	1		4	1	3		1	_	2	5	4	128	FS 2.0	٢	۲	۲	Chip TQFP24-144 PFBGA12U-180	
S1C33L26	_	r	_	16	24	60M / 32.768K	1.6µA / 4.1mA(48M) / 22mA (48M)	Core 1.65 to 1.95 I/O 2.7 to 3.6 USB 3.0 to 3.6	_	12K	20K	6	71 ※ 2/3	8	1	1	1	2		2 ※4		1	6	_	8	FS 2.0	۲	2	r	Chip TQFP15-128 TQFP24-144 PFBGA10U-180	Graphic feature integrated Separated RTC power supply
S1C33L27		~		16	24	60M / 32.768K	1μΑ / 4.3mA(48M) / 18mA (48M)	Core 1.65 to 1.95 I/O 2.7 to 3.6 USB 3.0 to 3.6	_	22.5 K	32K	8	95 ※ 2/3	6	4	2	1	1		4 ※4		2	8	_	8	FS 2.0	2	2	~	Chip TQFP15-128 TQFP24-144 QFP20-144 PFBGA12U-1 80	Separated RTC power supply

\*1: All peripheral clock = OFF

\*2: In common with the bus line
\*3: This is specification varies depending on the type of package

\*4: Universal serial interface (Any of UART, SPI and I<sup>2</sup>C functions can be selected)

#### S1C33S00 series

S1C33S00 series: The model for multi-channel serial interfaces.

	CF	PU C	ore				N	lemor	y	١/	0		Tim	ner			S	SIO			nit.	it	DI	MA					-	
Products	STD	PE	ADV	Clock frequency Low/high Hz (Max.)	Supply current Sleep/ Halt/ operating (frequency) (Typ.) ※ 1	Supply voltage range (V)	ROM(Byte)	RAM(Byte)	Battery backup RAM(Bvte)	Input por	Output port	8-bit PWM	16-bit	16-bit PWM	WDT	Clock	UART(IrDA1.0)	SPI	I <sup>2</sup> C	I <sup>2</sup> S	Remote control circuit	A/D converter, 10-bit	HSDMA	IDMA	USB	SDRAM	NAND flash C	JPEG	Package (Form of delivery)	Remarks
S1C33S03		~	I	90M / 32.768K	16µA / 3.5mA (48M) / 103.5mA (90M)	Core 1.65 to 1.95 I/O 2.7 to 3.6	I	100 K	~	1	96 ※ 2/3	4	4	Ļ	1	6	i	4	4 % 4	I	_		2	14	_	~	~		TQFP24-144 PFBGA12U-180	Graphic LSI Dedicated buses Separated RTC power supply
S1C33S07	_	v		60M / 32.768K	1µA / 3mA (48M)/ 19mA (48M)	Core 1.65 to 1.95 I/O 2.7 to 3.6		22K	_	5	86 ※ 2		6	6	1	3		1	1 ※ 4	1	_	5	4	128	_	~	~	_	TQFP24-144	

\*1: All peripheral clock = OFF
\*2: In common with the bus line
\*3: This is specification varies depending on the type of package
\*4: Each channel consists of two single line bidirectional serial buses

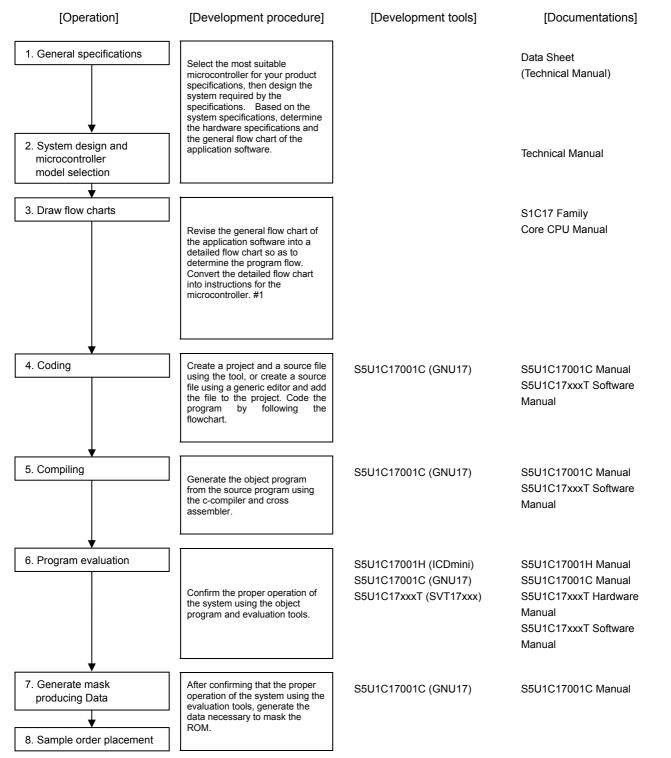
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## 2-4 Program development

#### Program development process

The relationship between the S1C17 Family program development procedure and its development tool is provided as an example. The basic procedure is the same as that for the other MCU families, whose details and development tools are explained in each

I he basic procedure is the same as that for the other MCU families, whose details and development tools are explained in each manual.



#### Development tools

#### S1C60 Family development tools

#### Hardware

S5U1C62000H2	S1C60 Family Common
(ICE62R)	In-circuit emulator
S5U1C62***E (EVA62**)	Evaluation board
S5U1C60***K (KIT60**)	S1C60** Individual ROM

#### Software package

S5U1C62000A	S1C60 Family Common Tool
(ASM62)	(including model-by-model software tool)

#### S1C63 Family development tools

#### Hardware

S5U1C63000H2/6	S1C63 Family Common
(ICE63)	In-circuit emulator
S5U1C63***P	Peripheral circuit board
(PRC63***)	
S5U1C6F666T1	Demonstration board
S5U1C6F632T1/2 (SVT6F632)	Software evaluation board

#### Software package

S5U1C63000A	S1C63 Family Common tool
(ASM63)	(including model-by-model software tool)

#### S1C33 Family development tools

#### Hardware

S5U1C33001H	S1C33 Family Common
(ICD33)	Omitted pin type On-chip ICE

#### Software package

S5U1C33001C	S1C33 Family Common
(GNU33)	C Compiler package

#### S1C63/S1C88 Option Soft tool

S5U1C88000Q1 S1C63/S1C88 Family embedded sy simulator	/stem
--	-------

#### S1C17 Family development tools

Hardware

	S1C17 Family Common Omitted pin type On-chip ICE
S5U1C17xxxT (SVTxxx)	Software Evalution Board

#### Software package

	S1C17 Family Common C compiler assembler package

# **ASSPs**

3

Page

	LCD controller	S1D13*** series	22
	LCD controller with Camera I/F	S1D13*** series	23
	Video Encoders	S1C13*** series	23
Display controllers	Image Enhancement IC	S2D13*** series	23
	LCD controller for automotive	S2D13*** series	24
	EPD controller (supporting the E ink's EPD)	S1D13*** series	24
	In-vehicle multi-Camera interface IC	S2D13*** series	24
Network & image controller	]	SxS6X000 series	25
Speech & Audio	]	S1V3*** series	26
	Drivers for small and Medium-sized panel	S1D15000 series	27
LCD drivers	STN LCD Drivers for large panel	S1D17000 series	28
Thermal-head drivers	]	S1D50000 series	28
EPD drivers	]	S1D14F50 series	29
USB bus switch ICs	]	S1F77000 series	29

### 3-1 Display controllers

Our LCD controllers feature high performance, low power consumption which was achieved by applying an original architecture based on our own "saving technology". These LCD controllers can be used on a variety of CPUs. Since the product line-up listed below allows to support a wide range of LCD panels, including those from small to large scale and those from monochrome to color, these controllers are best suited to mobile devices, OA devices, FA devices and vehicle-mounted devices.

			LCD Interfa	ice Support		Color	Internal	External	Supply	Voltage		
Products	CPU Interface Support	Mono- chrome STN	Color STN	TFT	Typical resolution	Depth (Max.)	Memory Capacity	Memory Capacity	Core	ю	Additional features	Package
S1D13505F00A	8bit /16bit I/F Direct addressing	4-bit / 8-bit	4-bit / 8-bit / 16-bit	9-bit / 12-bit / 18-bit	VGA	MSTN: 16 grayscale CSTN: 4K colors TFT: 64K colors MSTN:	0	Up to 2MB EDO-RAM	2.7V to 5.5V	2.7V to 5.5V	CRT support	QFP15-128
S1D13506F00A	8bit /16bit I/F Direct addressing	4-bit / 8-bit	4-bit / 8-bit / 16-bit	9-bit / 12-bit / 18-bit	VGA	MSTN: 64 grayscale CSTN: 64K colors TFT: 64K colors	0	Up to 2MB EDO-RAM	2.7V to 5.5V	2.7V to 5.5V	CRT or NTSC, PAL support, 2D BitBLT	QFP15-128
S1D13700F02A	8bit I/F, Direct addressing Indirect addressing	4-bit	n/a	n/a	QVGA	16 grayscale	32KB, SRAM	n/a	3.0V to 3.6V	3.0V to 5.5V	3 overlay screens	TQFP13-64
S1D13705F00A	8bit I/F (with external logic) 16bit I/F, Direct addressing	4-bit / 8-bit	4-bit / 8-bit	9-bit / 12-bit	QVGA	MSTN: 16 grayscale CSTN: 256 colors TFT: 256 colors	80KB, SRAM	n/a	2.7V to 3.6V	2.7V to 5.5V	SwivelView	QFP14-80
S1D13706F00A	8bit I/F (with external logic), 16bit I/F, Direct addressing	4-bit / 8-bit	4-bit / 8-bit / 16-bit	9-bit / 12-bit / 18-bit	QVGA	MSTN: 64 grayscale CSTN: 64K colors TFT: 64K colors	80KB, SRAM	n/a	1.8V to 3.6V	1.8V to 3.6V	SwivelView, Picture in picture	TQFP15-100
S1D13742F01A	8bit /16bit I/F Indirect addressing	n/a	n/a	18-bit	VGA	256K colors	768KB, SRAM	n/a	1.4V to 1.6V	1.65V to 3.60V	SwivelView	QFP20-144
S1D13743F00A	8bit /16bit I/F Indirect addressing	n/a	n/a	18-bit / 24-bit	WQVGA	16M colors	768KB, SRAM 464KB, SRAM	n/a	1.4V to 1.6V	1.65V to 3.60V	SwivelView	QFP20-144
S1D13748F00A	16bit I/F, Indirect addressing	n/a	n/a	18-bit / 24-bit	WVGA	64K colors	1024KB, SRAM	n/a	1.35V to 1.65V	1.62V to 3.60V	Picture in picture	QFP20-144
S1D13748B00B	16bit I/F, Indirect addressing	n/a	n/a	18-bit / 24-bit	WVGA	64K colors	1024KB, SRAM	n/a	1.35V to 1.65V	1.62V to 3.60V	Picture in picture	PFBGA10U-121
S1D13781F00A	8bit / 16bit I/F, Direct addressing Indirect addressing, SPI	4-bit / 8-bit	8-bit / 16-bit	16-bit / 18-bit / 24-bit	WQVGA	MSTN: 64 CSTN: 64K colors TFT: 16M colors MSTN:	384KB, SRAM	n/a	1.35V to 1.65V	1.62V to 3.60V	PinP, α-Blend, 2D BitBLT	QFP15-100
S1D13A04F00A	8bit I/F (with external logic) 16bit I/F, Direct addressing	4-bit / 8-bit	4-bit / 8-bit / 16-bit	9-bit / 12-bit / 18-bit	QVGA	64 grayscale CSTN: 64K colors TFT: 64K colors	160KB, SRAM	n/a	1.8V to 2.75V	3.0V to 3.6V	2D BitBLT, SwivelView, USB client 1.1	TQFP15-128
S1D13A04B00B	8bit I/F (with external logic) 16bit I/F, Direct addressing	4-bit / 8-bit	4-bit / 8-bit / 16-bit	9-bit / 12-bit / 18-bit	QVGA	MSTN: 64 grayscale CSTN: 64K colors TFT: 64K colors	160KB, SRAM	n/a	1.8V to 2.75V	3.0V to 3.6V	2D BitBLT, SwivelView, USB client 1.1	PFBGA10U-121
S1D13A05B00B	8bit I/F (with external logic) 16bit I/F, Direct addressing	4-bit / 8-bit	4-bit / 8-bit / 16-bit	9-bit / 12-bit / 18-bit	QVGA	MSTN: 64 grayscale CSTN: 64K colors TFT: 64K colors	256KB, SRAM	n/a	1.8V to 2.75V	3.0V to 3.6V	2D BitBLT, SwivelView, USB client 1.1	PFBGA10U-121
S1D13517F00A	8bit /16bit I/F, Indirect addressing	n/a	n/a	18-bit / 24-bit	SVGA	16M colors	0	Up to 16MB SDRAM	2.3V to 2.7V	3.0V to 3.6V	Picture in picture α-Blend	QFP15-128
S1D13U11F00A	USB2.0 HS	n/a	n/a	18-bit / 24-bit	SVGA	16M colors	0	Up to 16MB SDRAM	1.65V to 1.95V	3.0V to 3.6V	PinP $\alpha$ -Blend	QFP20-144

#### LCD controller

### ■LCD controller with Camera I/F

		LCD Interface Support				Internal	External			Supply Voltage				
Products	CPU Interface Support	Mono- chrome STN	Color STN	TFT	Typical resolution	Color Depth (Max.)	Memory Capacity	Memory Capacity	Camera (pixel)	JPEG Codec			Additional features	Package
S1D13513F01A	16bit I/F, Direct addressing, Indirect addressing, Serial I/F	8-bit	8-bit	18-bit	VGA	MSTN: 64 grayscale CSTN: 256K colors TFT: 256K colors	0	Up to 16MB SDRAM	0.3MP	n/a	1.65V to 1.95V	3.0V to 3.6V	2D Sprite, 2D BitBLT	QFP22-208
S1D13513B01B	16bit I/F, Direct addressing, Indirect addressing, Serial I/F	8-bit	8-bit	18-bit / 24-bit	VGA	MSTN: 64 grayscale CSTN: 256K colors TFT: 16M colors	0	Up to 64MB SDRAM	0.3MP	n/a	1.65V to 1.95V	3.0V to 3.6V	2D Sprite, 2D BitBLT	PBGA1UC256
S1D13515F00A	16bit I/F, Direct addressing, Indirect addressing, Serial I/F	n/a	n/a	18-bit / 24-bit	XGA	16M colors	0	Up to 64MB SDRAM	0.3MP	n/a	1.65V to 1.95V	3.0V to 3.6V	Prewarping Embedded RISC CPU	QFP22-256
S1D13515B00B	16bit I/F, Direct addressing, Indirect addressing, Serial I/F	n/a	n/a	18-bit / 24-bit	XGA	16M colors	0	Up to 64MB SDRAM	0.3MP	n/a	1.65V to 1.95V	3.0V to 3.6V	Prewarping Embedded RISC CPU	PBGA1UC256
S1D13717F00B	16bit I/F, Direct addressing, Indirect addressing, Serial port I/F for LCD	n/a	n/a	18-bit	176x220	64K colors	224KB, SRAM	n/a	0.3MP	Encode/ Decode	1.65V to 1.95V	2.75V to 3.25V	SD memory card I/F	QFP21-176
S1D13717B00B	16bit I/F, Direct addressing, Indirect addressing, Serial port I/F for LCD	n/a	n/a	18-bit	176x220	64K colors	224KB, SRAM	n/a	0.3MP	Encode/ Decode	1.65V to 1.95V	2.75V to 3.25V	SD memory card I/F	PFBGA12U-180
S1D13715F01A	16bit I/F, Direct addressing, Indirect addressing, Serial port I/F for LCD	n/a	n/a	18-bit / 24-bit	QVGA	16M colors	320KB, SRAM	n/a	1.3MP	Encode/ Decode	1.65V to 1.95V	2.75V to 3.25V	2D BitBLT, SwivelView	QFP21-176
S1D13715B00B	16bit I/F, Direct addressing, Indirect addressing, Serial port I/F for LCD	n/a	n/a	18-bit / 24-bit	QVGA	16M colors	320KB, SRAM	n/a	1.3MP	Encode/ Decode	1.65V to 1.95V	2.75V to 3.25V	2D BitBLT, SwivelView	PFBGA10U-160
S1D13719B00B	16bit I/F, Direct addressing, Indirect addressing	n/a	n/a	18-bit / 24-bit	QVGA	16M colors	512KB, SRAM	n/a	2.0MP	Encode/ Decode	1.65V to 1.95V	2.30V to 3.25V	2D BitBLT, SwivelView, SD memory card I/F	PFBGA10U-180

#### ■Video Encoders

	CPU Interface			Input Data Format		Internal	External	Su	pply Voltag	Additional		
	Support TV Outp		TV Standard	RGB	YUV	Memory Capacity	Memory Capacity	Core	ю	DAC	features	Package
S1D13506F00A	8bit /16bit I/F Direct addressing	Composite / S-video	PAL NTSC	5:6:5 8bpp 4bpp	n/a	0	Up to 2MB EDO-RAM	2.7V to 5.5V	2.7V to 5.5V	2.7V to 5.5V	LCD support 2D BitBLT	QFP15-128
S1D13746F01A	8bit /16bit I/F Direct addressing, Serial I/F (only for register access)	Composite / S-video	PAL: B, D, G, H, I, M, N, Nc NTSC: M, J	8:8:8 6:6:6 5:6:5 3:3:2	4:2:2 4:2:0	312KB, SRAM	n/a	1.35V to 1.65V	1.62V to 3.6V	2.7V to 3.3V	SwivelView, Image Enhanceme nt Engine	QFP15-128
S1D13746B01B	8bit /16bit I/F Direct addressing, Serial I/F (only for register access)	Composite / S-video	PAL: B, D, G, H, I, M, N, Nc NTSC: M, J	8:8:8 6:6:6 5:6:5 3:3:2	4:2:2 4:2:0	312KB, SRAM	n/a	1.35V to 1.65V	1.62V to 3.6V	2.7V to 3.3V	SwivelView, Image Enhanceme nt Engine	PFBGA7U-100

#### ■Image Enhancement IC

Products	Supported CPU interface	Input/Output data format	Operating temperature range	Supply Core	voltage IO	Package
S2D13782F00A	I <sup>2</sup> C SPI	RGB-16/18/24bit, YUV-16bit, YUV-8bit (ITU-R BT.656)	-40°C to 105°C	1.65V to 1.95V	1.65V to 1.95V 3.0V to 3.6V	QFP15-100

#### ■LCD controller for automotive

		LC	CD Inter	face Supp	ort	Color	Internal	External			Supply '	Voltage			
Products	CPU Interface Support	Mono- chrome STN	Color STN	TFT	Typical resolution	Depth (Max.)	Memory Capacity	Memory Capacity	Camera (pixel)	JPEG Codec	Core	Ю	Temp. Range	Additional features	Package
S2D13513F01A	16bit I/F, Direct addressing, Indirect addressing, Serial I/F	8-bit	8-bit	18-bit	VGA	64 grayscale 256K colors	0	Up to 16MB SDRAM	0.3MP	n/a	1.65V to 1.95V	3.0V to 3.6V	-40 to 105°C	2D Sprite, 2D BitBLT	QFP22-208
S2D13513B01B	16bit I/F, Direct addressing, Indirect addressing, Serial I/F	8-bit	8-bit	18-bit / 24-bit	VGA	64 grayscale 16M colors	0	Up to 64MB SDRAM	0.3MP	n/a	1.65V to 1.95V	3.0V to 3.6V	-40 to 105°C	2D Sprite, 2D BitBLT	PBGA1UC256
S2D13515F00A	16bit I/F, Direct addressing, Indirect addressing, Serial I/F	n/a	n/a	18-bit / 24-bit	XGA	16M colors	0	Up to 64MB SDRAM	0.3MP	n/a	1.65V to 1.95V	3.0V to 3.6V	-40 to 105°C	Prewarping Embedded RISC CPU	QFP22-256
S2D13515B00B	16bit I/F, Direct addressing, Indirect addressing, Serial I/F	n/a	n/a	18-bit / 24-bit	XGA	16M colors	0	Up to 64MB SDRAM	0.3MP	n/a	1.65V to 1.95V	3.0V to 3.6V	-40 to 105°C	Prewarping Embedded RISC CPU	PBGA1UC256
S2D13719F00A	16bit I/F, Direct addressing, Indirect addressing	n/a	n/a	18-bit / 24-bit	QVGA	16M colors	512KB, SRAM	n/a	2.0MP	Encod e/ Decod e	1.65V to 1.95V	2.3V to 3.6V	-40 to 105°C	2D BitBLT, SwivelView, SD memory card I/F	QFP22-208

#### ■EPD controller (supporting the E Ink's EPD)

Products	Supported CPU interface	Built-in memory	External memory	Maximum resolution	Gray scale	Supply Core	voltage IO	Other functions	Package
S1D13521B01B	16bit I/F Indirect addressing	_	SDRAM I/F (for frame buffer)	4096 x 4096	GrayScale:5bpp 2/3/4/5bpp	1.65V to 1.95V	1.65V to 1.95V 2.70V to 3.60V	16 area partial update	PFBGA8U-181 PFBGA12U-180
S1D13522A00B	16bit I/F Indirect addressing, Serial I/F	2MB	_	1024 x 768	2/3/4bpp	1.65V to 1.95V	1.65V to 3.60V	15 area partial update, Picture in Picture with Transparency	PFBGA10U-144 PFBGA7SX-144
S1D13524B01B	16bit I/F Indirect addressing, Serial I/F		Mobile DDR I/F (for frame buffer)	2560 x 2048	Color: RGB565 GrayScale:4bpp	1.40V to 1.60V	1.65V to 3.60V	Color Processor, 15 area partial update,	PFBGA11UK-241

#### ■In-vehicle multi-camera interface IC

Products	Supported CPU interface	Function	Operating		Supply voltage		Package
TTOQUELS	Supported Of O Internace	T difetion	temperature range	Core	10	Analog signals	T ackage
S2D13P04F00A	I <sup>2</sup> C SPI	Including four channels of NTSC/PAL decoders 8-bit digital output (supporting ITU-R BT656) Equipped with multi-image synthesis mode Distortion correction function	-40°C to +85°C	1.65V to 1.95V	3.0V to 3.6V	3.0V to 3.6V	QFP15-100
S2D13P04B00B	I <sup>2</sup> C SPI	Including four channels of NTSC/PAL decoders 8-bit digital output (supporting ITU-R BT656) Equipped with multi-image synthesis mode Distortion correction function	-40°C to +85°C	1.65V to 1.95V	3.0V to 3.6V	3.0V to 3.6V	PFBGA10U-121

### 3-2 Network & Image Controllers

The controller LSI which carried the protocol processing function to make network connection easily was developed originally. Furthermore, also preparing the product which contained a camera function and JPEG encoder ability.

#### ■ Network & Image Controllers

Products	Supply voltage (V)	Additional features	Package
S1S60000F00A ×1	3.3	<ul> <li>Built-in the protocol stack necessary for TCP/IP connection.</li> <li>Requires no license expense by using the independently developed protocol stack.</li> <li>Enables network connection by simple command operation.</li> <li>Controls hardware via network without a host CPU by using a general-purpose I/O pin and I<sup>2</sup>C bus.</li> </ul>	QFP15-100
S2S65P10F00A	2.4 to 3.6(I/O) 1.8(Core power) 1.8(PLL)	<ul> <li>Intelligent interlace/progressive converter</li> <li>4 channel inputs, 2 channel outputs</li> <li>Supports ITU-R BT.601(4:2:2)/ITU-R BT.656</li> <li>4 to 1 intelligent image switcher</li> <li>4 images synthetic output(QVGAx4)</li> <li>Area motion detect</li> <li>Aspect ratio converter</li> <li>No need external memory</li> </ul>	QFP15-100

×1 : This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

### 3-3 Speech & Audio

### Speech & Audio

Products	Supply voltage (V)	Additional features	Package
S1V30340F00A7 / S1V30341F00** / S1V30343F00** / S1V30345F00** S1V30340F05A7 / S1V30341F05** / S1V30343F05** / S1V30345F05**	2.2 to 5.5V	•EPSON high quality codec format (Built in ROM for Voice data) •Sampling Frequency 16KHz •Bit rate 40k, 32k, 24k, 16kbps •High Quality 16bit mono DAC •SPI Slave / <sup>12</sup> C / UART	QFP13-52
S1V30340F01A7 / S1V30341F01** / S1V30343F01** / S1V30345F01** S1V30345F01** S1V30340F06A7 / S1V30341F06** / S1V30343F06** / S1V30345F06**	2.2 10 3.30	•Clock Frequency 32.768KHz, 12.288MHz *F00 F01 32.768KHz *F05 F06 12.288MHz	QFP12-48
S1V30080M0*A		EPSON high quality codec format(Built in ROM for Voice data)     *5ch, 5octave Melody Synthesizer integrated     Mixing function support     *Sampling frequency 16K, 8KHz     *10bit mono DAC integrated	SSOP2-16
S1V30080F0*A	2.2 to 5.5V	•Standalone interface / SPI Slave / I <sup>2</sup> C •Clock Frequency 8.192MHz(fs:8KHz), 16.384MHz(fs:16KHz)	QFP12-48
S1V30080F1*A		× M00 F00 for external clock × M01 F11 for Oscillator	QFP13-52
S1V3G340F00A	2.2 to 5.5V		QFP13-52
S1V3S344A00A	3.3V or 5V	EPSON high quality codec format (Built in Flash-Memory for Voice data)     Sampling Frequency 16KHz     Bit rate 40k, 32k, 24k, 16kbps     High Quality 16bit mono DAC     SPI Slave 1 <sup>2</sup> C / UART     Clock Frequency 32.768KHz(Oscillator, external clock), 12.288MHz(external clock)     integrate Flash	QFP13-52

## 3-4 LCD Drivers

#### Drivers for small and medium-sized panel

Stores a bit-image display data from the MPU in the built-in display RAM (by bit-by-bit assignment), and drives the LCD panel. The built-in RAM storage allows the LCD display to operate with very low power consumption.

#### S1D15000 series

Products	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (bits)	Micro processor interface	Frequency (kHz)	Package	Remarks
S1D15E00D01B	1.8 to 3.6	3.2 to 10	1/100	132	100	132×100 bits	8-bit parallel / Serial	40	Au bump chip	4-line MLS driving
S1D15710D10B	1.8 to 5.5	4.5 to 18	1/65	224	65	224×65 bits	8-bit parallel / Serial	22	Au bump chip	Built-in power circuit for LCD, High power voltage follower version
S1D15711D00B	1.8 to 5.5	4.5 to 9	1/9	200	9	200×9 bits	8-bit parallel / Serial	46	Au bump chip	Built-in power circuit for LCD
S1D15712D01B	2.7 to 5.5	5.6 to 16.2	1/81	256	81	256×81×2 bits	8-bit parallel / Serial	400	Au bump chip	Built-in power circuit for LCD 4-line MLS driving 4-gray scale
S1D15714D01E	2.7 to 5.5	VDD to 16	1/65	168	65	168×65 bits	8-bit parallel / Serial	100	Au bump chip	Built-in power circuit for LCD 4-line MLS driving
S1D15715D00B	1 0 to 5 5	4.5.45.0.0	1/17	400	17	102×33	8-bit	21.76	A., human ahia	Built-in power circuit for
S1D15716D00B	1.8 to 5.5	4.5 to 9.0	1/9	102	9	bits	parallel / Serial	23.04	Au bump chip	LCD
S1D15719D22B	2.7 to 5.5	5.6 to 25	1/132	180	132	180×132 bits	8-bit parallel / Serial	4896	Au bump chip	Built-in power circuit for LCD 4-line MLS driving 4-gray scale
S1D15721D01B	2.7 to 5.5	5.6 to 16.2	1/81	256	81	256×81 bits	8-bit parallel / Serial	420	Au bump chip	Built-in power circuit for LCD 4-line MLS driving LCD drive voltage 4-gray scale
S1D15722D01B	2.7 to 5.5	15 to 25	1/184	224	184	224×184×2 bits	8-bit parallel / Serial	640	Au bump chip	External bias input required 4-line MLS driving LCD drive voltage 4-gray scale
S2D15730D00B	2.7 to 5.5	11 to 27	1/132	180	132	180×144×2 bits	8-bit parallel / Serial	2000	Au bump chip	Built-in power circuit for LCD 4-line MLS driving 4-gray scale
S2D15731D00B	2.7 to 5.5	11 to 27	1/132	256	132	256×160×2 bits	8-bit parallel / Serial	2000	Au bump chip	Built-in power circuit for LCD 4-line MLS driving 4-gray scale
S2D15102D00B	2.7 to 5.5	3.6 to 7.0	1/1 to 1/4	80	4	80×4 bits	Serial	Variable	Au bump chip	Built-in bias circuit for LCD panel

#### S2D19600 Series (1-chip monochrome TFT driver)

Products	Supply voltage (V)	LCD drive voltage (V)	Gate drive voltage (V)	Source output	Gate output	Data RAM capacity	MPU interface	Oscillation frequency (MHz)	Package	Remarks
S2D19600D00B	2.7 to 5.5	to 5.5	to 32	320	320	320×320 ×4 bits	8-bit Parallel/ serial	1	Au bump chip	Built-in power circuit for LCD panel



#### ■ STN LCD Drivers for large panel

#### S1D17000 series

#### • Selectable Segment or Common driver

Products	Supply voltage Range (V)	LCD voltage range (V)	Duty	Outputs	Data bus	Package	Remarks
S1D17A03D00B	2.4 to 5.5	8 to 40	to 1/480	160	4-/8-bit parallel	Au bump chip	Pin input enables to select the common or segment driver.
S1D17A04D00B	2.4 to 5.5	8 to 40	to 1/480	240	4-/8-bit parallel	Au bump chip	Pin input enables to select the common or segment driver.

#### Segment driver (S1D17A08) and common driver (S1D17E02) for COG

Products	Supply voltage Range (V)	LCD voltage range (V)	Duty	Outputs	Data bus	Package	Remarks
S1D17E02D00B	2.5 to 5.5	15 to 45	~1/240	240	_		For COG. APT driving method common driver
S1D17A08D00B	2.5 to 5.5	2.6 to 5.5	~1/240	320	4-/8-bit parallel		For COG. APT driving method segment driver

### 3-5 Thermal-head Drivers

#### ■ Thermal-head drivers

Products	Logic supply voltage range V	Output withstand voltage V (Max.)	Output current mA (Max.)	Clock frequency MHz (Max.) [#]	Number of driver outputs	Description	Package
S1D53150D0A0	3.3 / 5 ±10%	40	12 / 22	20[12] / 25[16]	128	One side output 400dpi	Bare Chip
S1D53230D0A0	3.3 / 5 ±10%	50	10 / 13	35[12 / 16]	128	One side output 400dpi	-
S1D56110D0A0			30				-
S1D56120D0A0	5±10%	32	45	7 [5]	64	One side output 200dpi	
S1D56200D0A0		32	70	7 [6]	64	One side output 200dpi	-
S1D56220D0A0	3 / 3.3 / 5 ±10%	9	60	7[5] / 7[5] / 10[8]	64	One side output 200dpi, Battery Use	
S1D56240D0A0	3.3 / 5 ±10%	10	60	4[3] / 10[8]	64	One side output 200dpi, Battery Use	-
S1D56520D0A0	3.3 / 5 ±10%	32	10 / 13.5	30	128	One eide eutrut 200dri	-
S1D56540D0A0	3.375±10%	32	50	16[12 / 16]	120	One side output 300dpi	
S1D56700D0A0			50	40 [9]	64	300dpi 3-step latch Heat history control	-
S1D56710D0A0	5±10%	32	50	10 [8]	04	300dpi 5-step latch Heat history control	
S1D56730D0A0			15	16 [16]	128	600dpi 5-step latch Heat history control	
S1D56840D0A0	5±10%	32	50	10 [8]	96	One side output 300dpi	
S1D56850D0A0	JI 1070	52	20	10 [0]	90	6 One side output 300dpi	

#: In case of cascade connection

## 3-6 EPD drivers

#### Segment type EPD drivers

The S1D14F50 series is EPD driver ICs that is good for a segment type E-paper with small display capacity. These driver ICs can expand the segment display domain when coupled with the S1C17F57 that is 16-bit MCU embedded EPD drivers. This combination has high efficiency of battery power to meet E-paper characteristics.

#### S1D14F50 series

Products	Supply voltage range (V)	EPD voltage range (V)	Driver output Segment (TP/BP)	Flash (bit)	Command Interface	Built-in oscillator [MHz]	Package	Remarks
S1D14F57	1.75 to 5.5	9.15/12. 30/15.45	256 (2TP/2BP)	16k (Note1)	I <sup>2</sup> C Slave SPI Slave	2	Bare Chip	Built-in power circuit for EPD Temperature Sensor Power on Reset

Note1: During programming in flash memory 7.0V(Typ)

### 3-7 USB bus switch ICs

#### ■ USB bus switch ICs

		Operational			Bus switch			
Products	Input voltage range	power consumption	ON Resistance Pin canacity		PK	(G		
S1F77310M0A	3.0V to 3.6V	14µA (Max.)	1μA (Max.)	5.3Ω (Typ.)	1.7 pF (Typ.)		PLP0616	16B-8PIN
S1F77330B0A	3.0V to 3.6V	14μA (Max.)	1μA (Max.)	6.0Ω (Тур.)	D-system: 2.7 pF (Typ.)	D*-system: 1.45 pF (Typ.)	WCSP	(10balls)
S1F77330M0A	3.0V to 3.6V	14μA (Max.)	1μA (Max.)	6.0Ω (Тур.)	D-system: 2.7 pF (Typ.)	D*-system: 1.45 pF (Typ.)	PLP06272	25A-10PIN

Note: D-system having DX and DY pins, and D\*-system having D1X, D1Y, D2X and D2Y pins

# Package Information

4

PFBGA

WCSP

COF, TCM

Resin-core bump packaging technology

Package Lineup

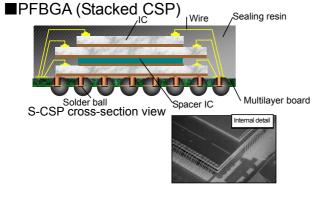
Package Externals

#### Introduction of Typical Package with 4-1 High-Density Assembly

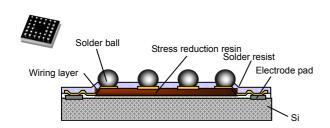
This package allows you to develop lightweight and compact products friendly to the environment by integrating the super-low power CMOS LSI, that is a key device, with the high density assembly, that is a key technology.

Seiko Epson has pursued the particular assembly technology by integrating super-miniaturization technology (cultivated by watch manufacturing) with low power technology, including CMOS LSI technology.

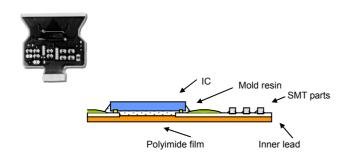
Seiko Epson intends to proceed reinforcing the global and speedy technical development power and exposing information for IT and digital network society that will continue to evolve further today. Seiko Epson will timely propose the super-thin, light-weight, and high-density assembly technology as the total solution, which enhances the commercial value when you en-visage the development of products.



WCSP



#### ■COF, TCM (Tape Carrier Module)



PFBGA allows you to greatly reduce the mounting area by mix and layer-stacking IC chips in one package, and to mix-load memory, microcomputer, sound source ICs and so on according to your system requirements.

Outline specifications

Connection method: Wire bonding connection Package height : 1.4mm Max. (3chips Max. + Spacer) 1.2mm Max. (Max. 2chips) : Min. 0.5mm Ball pitch

The Wafer Level Chip Size Package (WCSP) is optimum as a light weight, compact and thin package of portable devices that require high-density packaging. The WCSP is available in RTC, PLL and other medium and small pin device applications.

- Space saving package with full real chip size
- Ball pitch: 0.65/0.5/0.4mm pitch
- Under-filling is not required because this package provides a stress reduction structure at secondary mounting.
- package facilitates changing from a conventional This interposer-type package; so, it enables you to replace bare-chip mounting (wire bonding or face-down bonding) with SMT mounting.

IC chips and SMT parts are mounted on a film substrate to realize not only a thin packaging but also a lightweight, compact and high-density package of high degree of freedom.

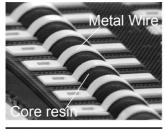
Also, gold or tin-plated lead can be bonded to gold bumps, and this inner lead bonding method has a characteristic of low impedance. This package is applicable mainly to LCD drivers and composite modules loaded with a driver and peripheral devices and customizable with them.

- Gold or tin -plated outer lead
- Package thickness : Less than 1mm
- Ease of multi-pin use

#### Resin-Core Bump COG Mouting technology

The resin core bump technology allows bonding to an elastic resin as the core (having almost the same height as the conventional bump) and metal wirings on the core. This technology replaces the conventional gold bump, forms the bump on IC pins and allows direct bonding of bump wiring and the wiring on the substrate (ITO coating and others) without using ACF particles while maintaining the resin's elastic characteristics.

#### Resin -core bump



Metal

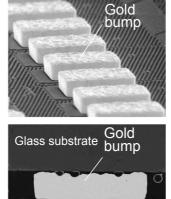
Wire

Core resin

Glass substrate

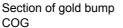
IC

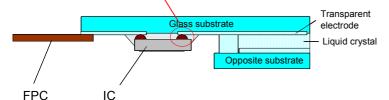
#### Conventional gold bump



Section of resin-core bump

COG





IC

Because the resin is much more elastic than ACF particles (several  $\mu m \phi),$  the traceability (or connection stability) to the variation of substrate or IC thickness and others can be significantly improved.

This technology can to a long way to solving the problems of conventional COG technology, such as the poor connection stability (point connection) due to the use of low-elastic ACF particle collection, and poor insulation between bumps.

Although the current application of this technology is COG-packaging LCD drivers and other devices, it is anticipated that it will be applicable to other packaging designs in the future.

- Significantly improves connection reliability.
- Allows fine bump pitch through photolithography technology.
- Allows highly flexible bump layout through relocation wiring technology.
- Minimizes environmental load because the soldering process is not used.

Unit: mm

Unit: mm

Unit: mm

Unit: mm

Unit: mm

### 4-2 Package Lineup

#### ■PFBGA (Plastic Fine-pitch Ball Grid Array)

Number of pins	Epson package name	JEITA package name	Body size (Nom.)	Mounting height (Max.)	Ball pitch	Storage rank
48	PFBGA7U-48	P-TFBGA-048-0707-0.80	7 X 7	1.2	0.8	SE2
60	PFBGA5U-60	P-TFBGA-060-0505-0.50	5 X 5	1.2	0.5	SE2
81	PFBGA8U-81	P-TFBGA-081-0808-0.80	8 X 8	1.2	0.8	SE2
96	PFBGA6U-96	P-TFBGA-096-0606-0.50	6 X 6	1.2	0.5	SE2
100	PFBGA7U-100	P-TFBGA-100-0707-0.65	7 X 7	1.2	0.65	SE2
112	PFBGA8U-112	P-TFBGA-112-0808-0.65	8 X 8	1.2	0.65	SE2
121	PFBGA8U-121	P-TFBGA-121-0808-0.65	8 X 8	1.2	0.65	SE2
121	PFBGA10U-121	P-TFBGA-121-1010-0.80	10 X 10	1.2	0.8	SE2
144	PFBGA7U-144	P-TFBGA-144-0707-0.50	7 X 7	1.2	0.5	SE2
144	PFBGA10U-144	P-TFBGA-144-1010-0.80	10 X 10	1.2	0.8	SE2
160	PFBGA10U-160	P-TFBGA-160-1010-0.65	10 X 10	1.2	0.65	SE2
161	PFBGA8U-161	P-TFBGA-161-0808-0.50	8 X 8	1.2	0.5	SE2
177	PFBGA13U-177	P-TFBGA-177-1313-0.80	13 X 13	1.2	0.8	SE2
180	PFBGA10U-180	P-TFBGA-180-1010-0.65	10 X 10	1.2	0.65	SE2
180	PFBGA12U-180	P-TFBGA-180-1212-0.80	12 X 12	1.2	0.8	SE2
181	PFBGA8U-181	P-TFBGA-181-0808-0.50	8 X 8	1.2	0.50	SE2
208	PFBGA12U-208	P-TFBGA-208-1212-0.65	12 X 12	1.2	0.65	SE2
220	PFBGA14U-220	P-TFBGA-220-1414-0.80	14 X 14	1.2	0.8	SE2
256	PFBGA14U-256	P-TFBGA-256-1414-0.80	14 X 14	1.2	0.8	SE2
280	PFBGA16U-280	P-TFBGA-280-1616-0.80	16 X 16	1.2	0.8	SE2

#### ■VFBGA (Very Thin Fine-pitch Ball Grid Array)

		<b>J</b> /				
Number of pins	Epson package name	JEITA package name	Body size (Nom.)	Mounting height (Max.)	Ball pitch	Storage rank
49	VFBGA4H-49	P-VFBGA-049-0404-0.50	4 X 4	1.0	0.5	SE2
81	VFBGA5H-81	P-VFBGA-081-0505-0.50	5 X 5	1.0	0.5	SE2
81	VFBGA8H-81	P-VFBGA-081-0808-0.80	8 X 8	1.0	0.8	SE2
96	VFBGA6H-96	P-VFBGA-096-0606-0.50	6 X 6	1.0	0.5	SE2
121	VFBGA6H-121	P-VFBGA-121-0606-0.50	6 X 6	1.0	0.5	SE2
121	VFBGA10H-121	P-VFBGA-121-1010-0.80	10 X 10	1.0	0.8	SE2
144	VFBGA7H-144	P-VFBGA-144-0707-0.50	7 X 7	1.0	0.5	SE2
144	VFBGA10H-144	P-VFBGA-144-1010-0.80	10 X 10	1.0	0.8	SE2
161	VFBGA7H-161	P-VFBGA-161-0707-0.50	7 X 7	1.0	0.5	SE2
180	VFBGA10H-180	P-VFBGA-180-1010-0.65	10 X 10	1.0	0.65	SE2
181	VFBGA8H-181	P-VFBGA-181-0808-0.50	8 X 8	1.0	0.5	SE2
240	VFBGA10H-240	P-VFBGA-240-1010-0.50	10 X 10	1.0	0.5	SE2

#### ■PBGA (Plastic Ball Grid Array)

Number of pins	Epson package name	JEITA package name	Body size (Nom.)	Mounting height (Max.)	Ball pitch	Storage rank
256	PBGA1UC256	P-LBGA-0256-1717-1.00	17 X 17	1.3	1.0	SE3
256	PBGA1UE256	P-LBGA-0256-1717-1.00	17 X 17	1.7	1.0	SE3

#### ■LQFP (Low profile Quad Flat Package)

Number of pins	Epson package name	JEITA package name	Body size (Nom.)	Mounting height (Max.)	Lead pitch	Lead shape	Storage rank
48	QFP12-48PIN	P-LQFP048-0707-0.50	7 X 7	1.7	0.5	STD	SE2
64	QFP13-64PIN	P-LQFP064-1010-0.50	10 X 10	1.7	0.5	STD	SE3
80	QFP14-80PIN	P-LQFP080-1212-0.50	12 X 12	1.7	0.5	STD	SE3
100	QFP15-100PIN	P-LQFP100-1414-0.50	14 X 14	1.7	0.5	STD	SE3
128	QFP15-128PIN	P-LQFP128-1414-0.40	14 X 14	1.7	0.4	STD	SE3
144	QFP20-144PIN	P-LQFP144-2020-0.50	20 X 20	1.7	0.5	STD	SE3 *
176	QFP21-176PIN	P-LQFP176-2424-0.50	24 X 24	1.7	0.5	STD	SE3 *
184	QFP20-184PIN	P-LQFP184-2020-0.40	20 X 20	1.7	0.4	STD	SE3 *
208	QFP22-208PIN	P-LQFP208-2828-0.50	28 X 28	1.7	0.5	STD	SE3 *
216	QFP21-216PIN	P-LQFP216-2424-0.40	24 X 24	1.7	0.4	STD	SE3 *
256	QFP22-256PIN	P-LQFP256-2828-0.40	28 X 28	1.7	0.4	STD	SE3 *

\* Some products must be stored under different conditions. Contact Epson for details.

#### ■TQFP (Tin Quad Flat Package)

Number of pins	Epson package name	JEITA package name	Body size (Nom.)	Mounting height (Max.)	Lead pitch	Lead shape	Storage rank
48	TQFP12-48PIN	P-TQFP048-0707-0.50	7 X 7	1.2	0.5	STD	SE2
64	TQFP12-64PIN	P-TQFP064-0707-0.40	7 X 7	1.2	0.4	STD	SE2
64	TQFP13-64PIN	P-TQFP064-1010-0.50	10 X 10	1.2	0.5	STD	SE2 *
80	TQFP14-80PIN	P-TQFP080-1212-0.50	12 X 12	1.2	0.5	STD	SE3
100	TQFP14-100PIN	P-TQFP100-1212-0.40	12 X 12	1.2	0.4	STD	SE3
100	TQFP15-100PIN	P-TQFP100-1414-0.50	14 X 14	1.2	0.5	STD	SE3 *
128	TQFP15-128PIN	P-TQFP128-1414-0.40	14 X 14	1.2	0.4	STD	SE3 *
144	TQFP24-144PIN	P-TQFP144-1616-0.40	16 X 16	1.2	0.4	STD	SE3

\* Some products must be stored under different conditions. Contact Epson for details.

#### ■QFN (Quad Flat Non-leaded Package)

Number of pins	Epson package name	JEITA package name	Body size (Nom.)	Mounting height (Max.)	Lead pitch	Lead shape	Storage rank
24	QFN4-24PIN	P-VQFN024-0404-0.50	4 X 4	1.0	0.5	STD	SE2
32	QFN5-32PIN	P-VQFN032-0505-0.50	5 X 5	1.0	0.5	STD	SE2
48	QFN7-48PIN	P-VQFN048-0707-0.50	7 X 7	1.0	0.5	STD	SE2
52	QFN8-52PIN	P-VQFN052-0808-0.50	8 X 8	1.0	0.5	STD	SE2
64	QFN9-64PIN	P-VQFN064-0909-0.50	9 X 9	1.0	0.5	STD	SE2

#### SON (Small Outline Non-leaded Package)

Number of pins	Epson package name	JEITA package name	Body size (Nom.)	Mounting height (Max.)	Lead pitch	Lead shape	Storage rank
6	SON-6PIN	P-WSON06-02.60x01.60-0.50	1.6 X 2.6	0.8	0.5	STD	SE2
8	SON1-8PIN	P-VSON08-03.08x03.00-0.65	3 X 3.8	1.0	0.65	STD	SE2
16	SON2-16PIN	P-VSON16-04.40x05.30-0.65	5.3 X 4.4	1.0	0.65	STD	SE2
6	VSON-6PIN	P-USON06-01.20x01.60-0.50	1.6 X 1.2	0.6	0.5	STD	SE1

#### ■SOP (Small Outline Package)

Number of pins	Epson package name	JEITA package name	Body size (Nom.)	Mounting height (Max.)	Lead pitch	Lead shape	Storage rank
8	SOP3B-8PIN	P-SOP08-03.90x04.90-1.27	4.9 X 3.9	1.75	1.27	STD	SE2
8	SOP3C-8PIN	P-LSOP08-04.40x05.00-1.27	5.0 X 4.4	1.7	1.27	STD	SE1
16	SOP3A-16PIN	P-LSOP16-04.40x10.00-1.27	10.0 X 4.4	1.7	1.27	STD	SE2

#### ■SSOP (Shrink Small Outline Package)

							•
Number of pins	Epson package name	JEITA package name	Body size (Nom.)	Mounting height (Max.)	Lead pitch	Lead shape	Storage rank
16	SSOP2-16PIN	P-LSSOP16-04.40x06.60-0.80	6.6 X 4.4	1.7	0.8	STD	SE4

#### ■SOT (Small Outline Transistor Package)

SOT	(Small Outline Tra	ansistor Package)					Unit: mm
Number of pins	Epson package name	Package name	Body size (Nom.)	Mounting height (Max.)	Lead pitch	Lead shape	Storage rank
3	SOT89-3PIN	(P-SOT89-3)	4.5 X 2.5	1.6	1.5	STD	SE2

#### ■PLP (Plating Lead Package)

Number of pins	Epson package name	Package name	Body size (Nom.)	Mounting height (Max.)	Lead pitch	Lead shape	Storage rank
8	PLP061616B-8PIN	(P-UPLP008-01.60x01.60-0.50)	1.6 X 1.6	0.60	0.5	STD	SE2
10	PLP062725A-10PIN	(P-UPLP010-02.50x02.70-0.50)	2.7 X 2.5	0.60	0.5	STD	SE2
10	PLP063031A-10PIN	(P-UPLP010-03.10x03.00-0.50)	3.0 X 3.1	0.65	0.5	STD	SE2
28	PLP064040A-28PIN	(P-UPLP028-04.00x04.00-0.50)	4.0 X 4.0	0.65	0.5	STD	SE2

### Package diagrams, storage rank documents, and various environment-related information

Available on the following Web page. http://www.epson.jp/device/semicon/index.htm

Product information: Technology information: Package lineup

Unit: mm

Unit: mm

Unit: mm

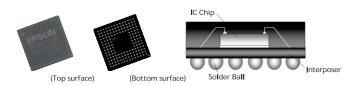
Unit: mm

Unit: mm

### 4-3 Package Externals

VFBGA (Very Thin Fine-pitch Ball Grid Array) & PFBGA (Plastic Fine-pitch Ball Grid Array)

4

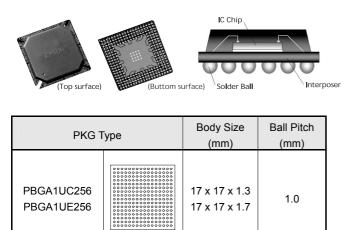


РКС Туре		Body Size (mm)	Ball Pitch (mm)
VFBGA4H-49		4 x 4 x 1.0	0.5
PFBGA5U-60		5 x 5 x 1.2	0.5
VFBGA5H-81		5 x 5 x 1.0	0.5
VFBGA6H-96 PFBGA6U-96		6 x 6 x 1.0 6 x 6 x 1.2	0.5
VFBGA6H-121		6 x 6 x 1.0	0.5
VFBGA7H-144 PFBGA7U-144		7 x 7 x 1.0 7 x 7 x 1.2	0.5
VFBGA7H-161		7 x 7 x 1.0	0.5
PFBGA8U-161		8 x 8 x 1.2	0.5
VFBGA8H-181 PFBGA8U-181		8 x 8 x 1.0 8 x 8 x 1.2	0.5
VFBGA10H-240		10 x 10 x 1.0	0.5
PFBGA7U-100		7 x 7 x 1.2	0.65
PFBGA8U-112		8 x 8 x 1.2	0.65
PFBGA8U-121		8 x 8 x 1.2	0.65

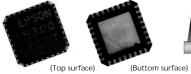
РКС Туре		Body Size (mm)	Ball Pitch (mm)
PFBGA10U-160		10 x 10 x 1.2	0.65
PFBGA10U-180		10 x 10 x 1.2	0.65
PFBGA12U-208		12 x 12 x 1.2	0.65
PFBGA7U-48		7 x 7 x 1.2	0.8
VFBGA8H-81 PFBGA8U-81		8 x 8 x 1.0 8 x 8 x 1.2	0.8
VFBGA10H-121 PFBGA10U-121		10 x 10 x 1.0 10 x 10 x 1.2	0.8
VFBGA10H-144 PFBGA10U-144	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 &$	10 x 10 x 1.0 10 x 10 x 1.2	0.8
PFBGA12U-180		12 x 12 x 1.2	0.8
PFBGA14U-220		14 x 14 x 1.2	0.8
PFBGA16U-280		16 x 16 x 1.2	0.8

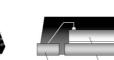
## **Package Information**

## PBGA (Plastic Ball Grid Array)



## QFN (Quad Flat Non-leaded Package)





(Top surface)

IC Chip Lead

PKG Type		Body Size (mm)	Lead Pitch (mm)
QFN4-24PIN		4 x 4 x 1.0	0.5
QFN5-32PIN		5 x 5 x 1.0	0.5
QFN7-48PIN		7 x 7 x 1.0	0.5
QFN8-52PIN		8 x 8 x 1.0	0.5
QFN9-64PIN		9 x 9 x 1.0	0.5

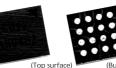
## LQFP (Low profile Quad Flat Package) & TQFP (Thin

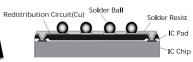
## Quad Flat Package)

PKG Type		Body Size (mm)	Lead Pitch (mm)
QFP12-48PIN		7 x 7 x 1.7	0.5
QFP13-64PIN		10 x 10 x 1.7	0.5
QFP14-80PIN		12 x 12 x 1.7	0.5
QFP15-100PIN		14 x 14 x 1.7	0.5
QFP15-128PIN		14 x 14 x 1.7	0.4
QFP20-144PIN		20 x 20 x 1.7	0.5
QFP21-176PIN		24 x 24 x 1.7	0.5
QFP22-208PIN		28 x 28 x 1.7	0.5
QFP21-216PIN		24 x 24 x 1.7	0.4

F	КС Туре	Body Size (mm)	Lead Pitch (mm)
QFP22-256PIN		28 x 28 x 1.7	0.4

WCSP (Wafer level Chip Scale Package)





(Buttom surface) (Top surfa

Products		Ball Count	Body Size (mm)	Ball Pitch (mm)
S1L5012		16	2.4 x 2.4 x 0.7	0.5
S1L5028		25	3.0 x 3.0 x 0.7	0.5
S1L5075		49	4.2 x 4.2 x 0.7	0.5
S1L5125		81	5.0 x 5.0 x 0.7	0.5
S1C17003		48	3.1 x 3.1 x 0.8	0.4

PI	КС Туре	Body Size (mm)	Lead Pitch (mm)
TQFP12-48PIN		7 x 7 x 1.2	0.5
TQFP12-64PIN		7 x 7 x 1.2	0.4
TQFP13-64PIN		10 x 10 x 1.2	0.5
TQFP14-80PIN		12 x 12 x 1.2	0.5
TQFP14-100PIN		12 x 12 x 1.2	0.4
TQFP15-100PIN		14 x 14 x 1.2	0.5
TQFP15-128PIN		14 x 14 x 1.2	0.4
TQFP24-144PIN		16 x 16 x 1.2	0.4

#### **LSI Device Precautions**

## 1. General precautions for use of CMOS LSI devices

Seiko Epson's CMOS LSI devices are designed and manufactured to assure trouble-free operation when used under normal operating conditions. All products are subjected to stringent electrical and mechanical testing to ensure reliability, but users are strongly recommended to observe the following precautions when designing systems, handling or storing devices to minimize the chance of failure.

#### Cautions to be observed when designing

#### Use within the rated ranges

Use ICs not to exceed the rated ranges of operating voltage, temperature, input/output voltage and current. Devices may sometimes work properly for a short period of time even when used outside the rated ranges, but their failure ratio may increase. Even within the rated conditions, failure ratio will change depending on the operating temperature and voltage of embedded systems. This must be fully considered when designing systems.

#### Handling of input/output control pins

When a noise such as spark and electrostatic is given from an input or output terminals, IC may malfunction. Pay sufficient attention in product designing. Electromagnetic interference can cause ICs to operate erratically. Shield all interference sources in equipment that uses ICs.

#### Latch up phenomenon

Excessive electrical noise occurred to a power or input/output pin can cause ICs to latch up, resulting in device malfunction or damage. If this occurs, turn off the power, isolate the problem, then supply power again.

#### Protection against electrostatic discharge (ESD)

Although all pins are equipped with an anti-electro static circuit, electro static beyond the capacity may lead to breakage. Take appropriate countermeasures when handling ICs.

- Avoid using packing and transporting containers made of plastic. Use electrically conductive containers. Also, special care must be taken when handling ICs, by wearing a antistatic wrist strap or taking other possible measures.
- · Use a soldering iron and test circuits without high voltage leakage with grounding.

#### Notes on storage

#### Storage condition

- Take care so that packages are not subjected to impact, vibration or water leakage.
- Do not store and use the product under conditions where moisture condensation may be formed due to rapid changes in temperature. Also, do not put load on products.
- · When storing, avoid dusty locations or locations with corrosive gases.
- After a long period of storage, check to see that the pins are not discolored, solderability is not degraded, etc., before use.
- Check moisture-proof bags for tear or wear before use. Also check the silica gel in the bag has not absorbed moisture when the bag is opened.
- Storage conditions after opening a moisture proof-bag, soldering method and soldering temperature must meet the requirements specified by Epson for respective products.

#### Conditions of use environment

#### Precautions for use environment

Use the IC in the proper temperature and humidity. The humidity must be 85% or lower (to prevent dew condensation). In the environment where the IC is directly exposed to dust, salt, or acid gas such as SO2, it may cause electrical leakage between leads or corrosion. In order to prevent such problems, apply corrosion-proof coatings to printed circuit boards and ICs.

#### Protection against excessive physical stresses and rapid temperature change

Do not expose ICs to excessive mechanical vibration, repetitive shock stress, or rapid temperature changes. These can cause the plastic package resin to crack and/or the bonding wires to break.

#### Light shading precaution

Exposing semiconductor devices to the light may have a chance to lead to miss function, since the light affects the device characteristics.

To prevent IC from miss function, please take into account the following points about substrates and products, packaged with IC.

- At product design and assembly, please consider the product structure so that IC is shaded in actual use.
- At testing process, please provide shaded environment for the device under test.
- ·Please consider surface, back and side of IC chip, since IC should be shaded entirely.

## 2. Package products

## 2.1 Cautions on surface mount

#### **Mechanical stress**

Minimize mechanical stress to a printed circuit board during or after soldering. The load applied from the surface when soldering a package onto the printed circuit board must be within 10N (1Kgf).

#### Package leads

As for a surface mount device, the pattern on a board and the lead of a package are soldered surface to surface. Although we are shipping products securing sufficient lead flatness for soldering, when handling, take care not to apply force otherwise it may result in deformation of the lead.

#### Signal leads on the package surface

Some packages are structured to expose a portion of the signal leads on the surface. When using these products, pay sufficient attention not to let the package be soiled. Also, handling with bare hands must be avoided.

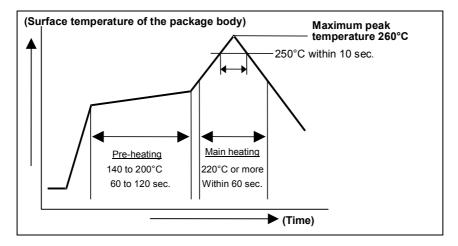
### Soldering precautions

Use infrared or air reflow or the combination of these methods for soldering.

#### i. Infrared reflow and air reflow methods

The temperature profile (on resin surface) of the reflow furnace should be within the allowable package heat-resistant temperature profile shown below.

#### Allowable package heat-resistant temperature profile



#### Thermal stress to packages

Soldering process is recommended to be carried out in the shortest time at the lowest temperature to minimize thermal stress to packages. Settings of the soldering profile should be performed upon through confirmation that the state of soldering and reliability after soldering are optimized.

#### Solder reflow processing multiple times

If solder reflow is to be carried out multiple times, it should be performed within the allowable storage period specified as storage rank for each product. (Reflow is allowed twice.)

#### ii. Hand soldering

Hand soldering using a soldering iron should be performed under the following conditions:

Maximum temperature of the soldering iron	Time	Times	
350 °C	Within 5 sec per pin	Twice or less	

Pay sufficient attention not to let a soldering iron contact any parts other than leads, such as a package body.

#### iii. Flow soldering

. Flow soldering is not recommended.

#### **LSI Device Precautions**

## 2.2 Notes on storage

#### Moisture absorption and reliability

The resin used in surface-mount packages absorbs moisture over time even stored in room conditions. When IC packages are put into reflow ovens with much moisture absorption, the resin may have a crack or a delamination between the resin and lead frame may occur. Therefore, surface mount ICs must be kept under typical storage conditions shown below before reflow soldering.

#### ■ Typical storage conditions and storage periods for (Surface-Mount) IC packages

Storage condition	Storage environments before opening the bag	
Before opening sealed moisture proof bag	30°C, 85% RH or less	Within 12 months (1 year)

#### • Storage ranks and storage conditions

Storage rank	Storage environments after opening the bag	
SE1 (JEDEC MSL2)	30°C, 85% RH or less Within 12 months (1 year)	
SE2 (JEDEC MSL2a)	30°C, 70% RH or less	Within a month
SE3 (JEDEC MSL3)	30°C, 70% RH or less	Within 168 hours(1 Week)
SE4 (JEDEC MSL4)	30°C, 70% RH or less	Within 72 hours(3 days)

•Regarding the storage ranks of respective products (IC packages) after opening the moisture-proof bags, refer to the tables of storage ranks shown in 4-2 Package Lineup.

#### Surface-mount package baking conditions

When surface-mount IC packages exceed the recommended storage periods, or their storage periods or storage conditions are unknown and therefore moisture absorption is a concern, it is recommended to dry-bake them before reflow soldering. This baking process will prevent the resin from cracking during soldering. When dry-baking, see below.

Standard baking conditions for IC packages

Baking temperature	Baking hours	Max. Baking times
125±5°C	From 20 to 36 hours	Twice

•When the storage duration after opening the bag exceeds the specified period or unknown, re-bake packages before mounting.

•Storage conditions from the baking to the reflow soldering are the same as the above-mentioned storage conditions.

Note: If products are shipped in Tape & Reel, transfer the products into heatproof trays before baking.

## 3. Bare chips

#### General precautions

- •The passivation film applied on bare chip surface is not to protect the chip from external shock but to protect the internal metallization.
- Moisture and dust in the air and careless handling of products during assembly will lead to defective products. Adequate caution must be exercised for storage environment and chip handling.

### Packing

•When bare chips are shipped, they are put in dedicated trays, and the trays are clipped so that chips are properly held in the trays during transportation. Then the trays are packed in antistatic bags. Do not open the bags more than necessary to prevent foreign substances from coming into the bags and falling on the chips inside. Do not leave trays open, either.

#### Bare chip storage precautions

- •Allowable storage periods before and after opening the pack are maximum 12 months under the conditions mentioned below.
- If the bags are opened, assemble the products without much delay in order to prevent the bonding degradation caused by the quality change in the bonding pad surfaces.

#### Bare chip storage conditions and storage periods

State	Storage conditions	Allowable storage period
Before opening	Lower than 35°C, 80% RH point	6 months
After opening	Lower than 30°C, 80% RH point	30 days
	In dry N2 gas with dew point lower than -30°C	6 months

#### Bare chip mounting

## Mounting environment

- Perform bare chip mounting in the clean environment where chip surface is not exposed to contaminated air or substances.
- Die pick up method

It is recommended to use a die collet for picking up a die. Choose die collets that can minimize the contact area on the chip.

• Mount boards (PCBs, etc.)

Use boards where no residues such as chemicals are left, or conductive failure (such as bonding failure) or Al pad corrosion may occur.

Pick up tool control

Clean the pick up tool periodically. Any foreign substance attached to the collet will lead high rate of continuous failures.

Bare chip cleaning

Do not clean bare chips. If bare chips are cleaned, extreme caution must be exercised about residues on chips.
Protection from static electricity

Use products in the environment where they are not exposed to ESD. When mounting a bare chip, mount it after assembling all other peripheral parts.

#### Material

• For mold resins, use "semiconductor grade" products. This is recommended to prevent corrosion in bonding pads due to moisture absorption, or the mold resign internal stress due to temperature changes. Similar precautions must be taken for other materials to be used.

## Information

## ■Non-Promotional Product Information

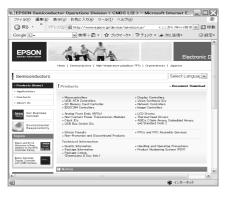
Epson is considering the discontinuation of the following products, though they will be continuously supplied to the customers currently using them. For your new projects, however, please consider alternative products. For the latest non-promotional product information, please visit the Epson website.

Products	Model name
Clock IC	S1T54100B, S1T54110F
LCD driver	S1D15B10
32-bit microcontrollers	S1C33L01,S1C33L03,S1C33L11,S1C33401,S1C33209,S1C33205,S1C33222,S1C33221 S1C33240,S1C33210,S1C33701,S1C33S01, S1C33E08, S1C33001
Display controllers	S1D13771, S1D13774, S1D13745
Organic EL controllers	S1D13701,S1D13702
VFD controllers	S1D13703
Audio IC	S1V30300,S1V30331,S1V30332,S1V30333
Network & Image controller	S1S60020,S1S65010,S2S65A00,S2S65A30

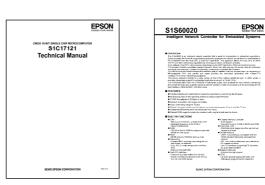
## ■Information on CMOS LSI's

Epson provides a number of sources of information regarding its products, including catalogs, brochures, technical manuals, and software on the website.

http://www.epson.jp/device/semicon\_e/







Manuals





Brochures

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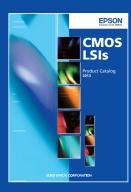
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