



NEC Electronics Inc.

**μPD23C4000
4,194,304-Bit
Mask-Programmable CMOS ROM**

Description

The μPD23C4000 is a 4,194,304-bit ROM fabricated with CMOS silicon-gate technology. The device is static in operation and has three-state outputs, fully TTL-compatible inputs and outputs, and an output enable pin which is mask-programmable and can be specified as active low, active high, or don't care.

The μPD23C4000 can be hardware-configured as either 256K x 16 bits or as 512K x 8 bits by tying the WORD/BYTE pin high or low, respectively. In the word configuration, pins O₀-O₁₅ are active. In the byte configuration, pin O_{15/A-1} becomes the additional bit required to address 512K bytes.

The μPD23C4000 is available in a 40-pin plastic DIP and a 64-pin plastic QFP.

Features

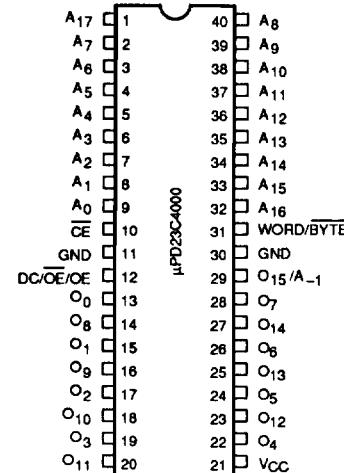
- Programmable organization
 - 262,144 words by 16 bits (word)
 - 524,288 words by 8 bits (byte)
- Fast access time of 250 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS technology
- Fully static operation
- Low power dissipation
- 40-pin plastic DIP or 64-pin plastic QFP packaging

Ordering Information

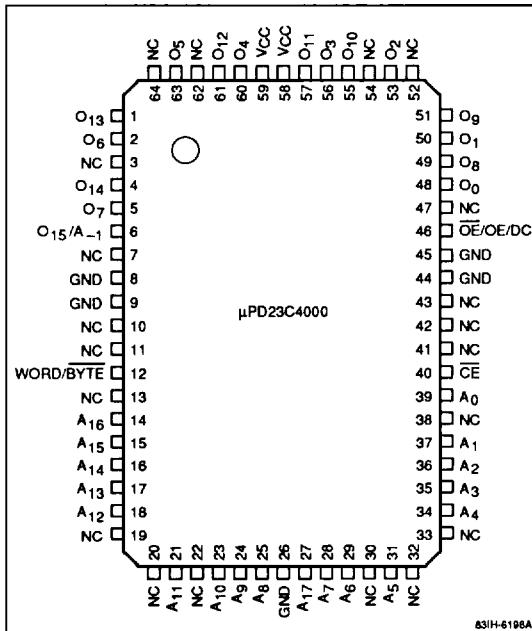
Part Number	Access Time (max)	Package
μPD23C4000C	250 ns	40-pin plastic DIP
μPD23C4000GF	250 ns	64-pin plastic QFP

Pin Configurations

40-Pin Plastic DIP



64-Pin Plastic QFP



Pin Identification

Symbol	Function
A ₀ - A ₁₇	Address inputs
O ₀ - O ₁₄	Outputs
O _{15/A-1}	Output 15 (word)/LSB address (byte)
CE	Chip enable
OE/OE/DC	Output enable (Note 1)
WORD/BYTE	Word/byte select input
GND	Ground
V _{CC}	+5-volt power supply
NC	No connection

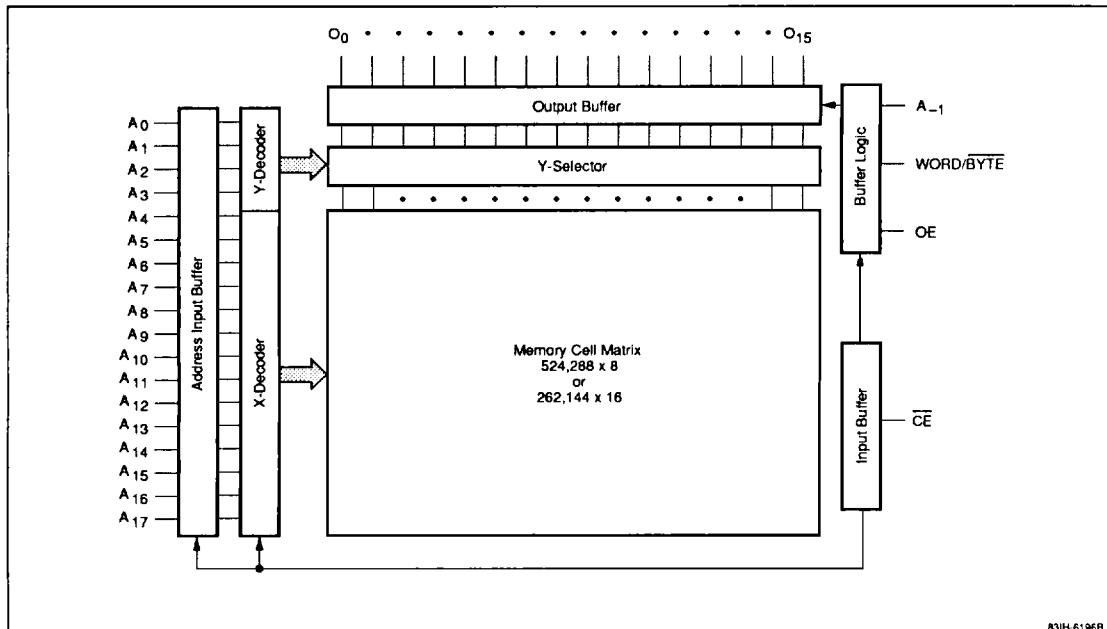
Notes:

- (1) This pin is user definable as active low, active high, or "don't care."

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C _I		15	pF	
Output capacitance	C _O		15	pF	

Block Diagram

DC Characteristics $T_A = -10 \text{ to } +70^\circ\text{C}; V_{CC} = +5.0 \text{ V } \pm 10\%$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -400 \mu\text{A}$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = +2.5 \text{ mA}$
Input leakage current	I_{IL}	-10		10	μA	$V_I = 0 \text{ V to } V_{CC}$
Output leakage current	I_{LOH}	-10		10	μA	$V_O = 0 \text{ V to } V_{CC}; \text{ chip deselected}$
Power supply current	I_{CC1}			50	mA	$CE = V_{IL}$
	I_{CC2}			1.5	mA	$CE = V_{IH}; \text{ chip deselected}$
	I_{CC3}			100	μA	$CE \geq V_{CC} - 0.2 \text{ V; chip deselected}$

AC Characteristics $T_A = -10 \text{ to } +70^\circ\text{C}; V_{CC} = +5.0 \text{ V } \pm 10\%$

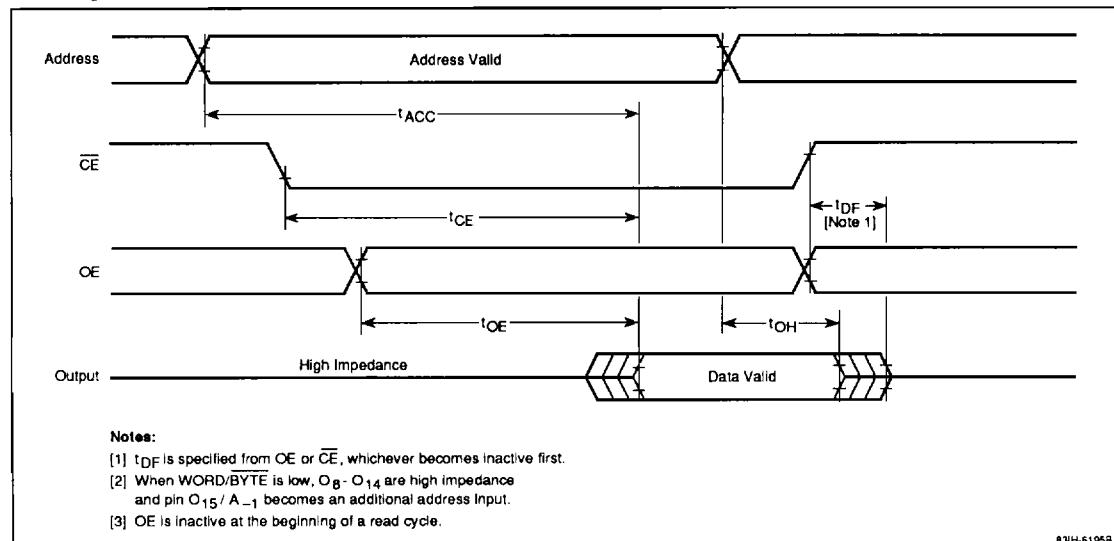
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			250	ns	
Chip enable access time	t_{CE}			250	ns	
Output enable access time	t_{OE}			110	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		70	ns	
Output disable time for O_8-O_{15} referenced to WORD/BYTE	t_{HDF}			100	ns	
Output enable access time referenced to WORD/BYTE	t_{WB}			250	ns	

Notes:

- (1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL + 100 pF.

Timing Waveform

Read Cycle



WORD/BYTE Selection Timing

