October 1990
Edition 6.0

FUJITSU

DATA SHEET

MB81464-12/-15

MOS 262,144 BIT DYNAMIC RANDOM ACCESS MEMORY

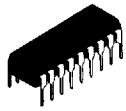
65,536 x 4 Bits Dynamic Random Access Memory

The Fujitsu MB81464 is a fully decoded, dynamic random access memory organized as 65,536 words by 4 bits. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage, and system memory for microprocessor units where low power dissipation and a compact layout is required.

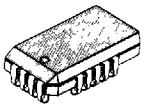
The multiplexed row and column address inputs permit the MB81464 to be housed in standard 18-pin DIP and PLCC, or 20-pin ZIP packages. Additionally, the MB81464 offers new functional enhancements that make it more versatile than previous dynamic RAMs. The $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle provides an on-chip refresh capability. The MB81464 also features page mode which allows high speed random access of up to 256 bits within the same row.

The MB81464 uses silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process technology. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including the sense amplifiers. Clock timing requirements are non critical, and power supply tolerance is very wide. All inputs are TTL compatible.

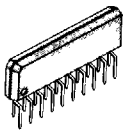
- 65,536 x 4 DRAM organization
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row Access Time (t_{RAC})
  120 ns max. (MB 81464-12)
  150 ns max. (MB 81464-15)
- Cycle Time (t_{RC})
  220 ns min. (MB 81464-12)
  260 ns min. (MB 81464-15)
- Page Cycle Time (t_{PC})
  120 ns max. (MB 81464-12)
  145 ns max. (MB 81464-15)
- Single +5 V Supply, ±10% tolerance
- Low Power
  358 mW max. (MB 81464-12)
  314 mW max. (MB 81464-15)
  27.5 mW max. (standby)
- On-chip substrate bias generator for high performance
- All inputs/outputs are TTL compatible
- 4 ms/256 refresh cycles
- Early write or $\overline{OE}$ controlled write capacity
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh capability
- Read write capability
- On-chip latches for addresses and DQs
- Compatible with µPD41254, HM50464, and TM4464
- Standard 18-Pin Plastic Packages:
  DIP (MB81464-XXP)
  PLCC (MB81464-XXPV)
  Standard 20-Pin Plastic Package:
  ZIP (MB81464-XXPSZ)
  Standard 18-Pin Ceramic Package:
  DIP (MB81464-XXC) Metal Seal



PLASTIC PACKAGE
DIP-18P-M03



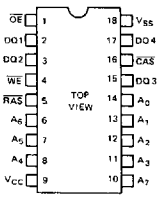
PLASTIC PACKAGE
LCC-18P-M04

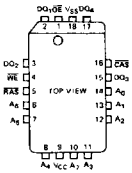


PLASTIC PACKAGE
ZIP-20P-M01

DIP-18C-A01: See Page 22

PIN ASSIGNMENT





Pin assignment for ZIP: See page 21

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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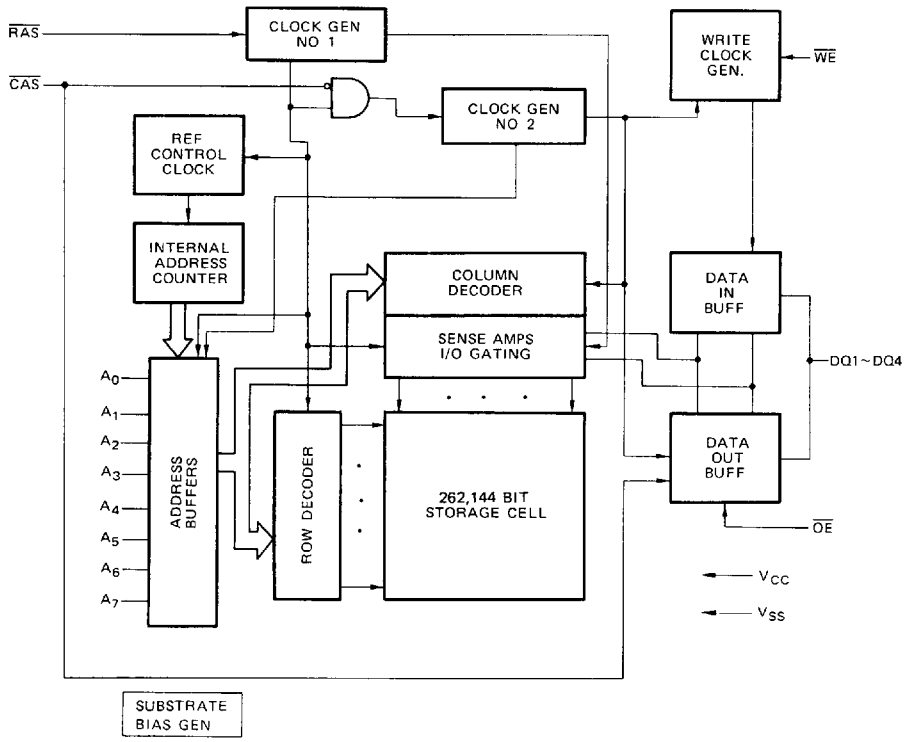
Fig. 1 – MB 81464 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value		Unit
		Typ	Max	
Input Capacitance A_0 to A_7	C_{IN1}	–	7	pF
Input Capacitanct $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	–	10	pF
Data I/O Capacitance (DQ1 to DQ4)	C_{DQ}	–	7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to 70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	–	6.5	V	
Input Low Voltage, all inputs except DQ	V_{IL}	-2.0	–	0.8	V	
Input Low Voltage, DQ	V_{ILD}*	-1.0	–	0.8	V	

* The device will withstand undershoots to the -2.0 V level with a maximum pulse width of 20 ns at the -1.5 V level.

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81464-12	I_{CC1}			65	mA
	MB 81464-15				57	
STANDBY CURRENT Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}			5.0	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81464-12	I_{CC3}			55	mA
	MB 81464-15				50	
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling; t_{PC} = min)	MB 81464-12	I_{CC4}			35	mA
	MB 81464-15				30	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81464-12	I_{CC5}			60	mA
	MB 81464-15				55	
INPUT LEAKAGE CURRENT any input (0V ≦ V_{IN} ≦ 5.5V, 4.5V ≦ V_{CC} ≦ 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	-10		10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0 V ≦ V_{OUT} ≦ 5.5 V)		$I_{DQ(L)}$	-10		10	μA
OUTPUT LEVEL Output High Voltage (I_{OH} = -5 mA)		V_{OH}	2.4			V
OUTPUT LEVEL Output Low Voltage (L_{OL} = 4.2 mA)		V_{OL}			0.4	V

* : I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
I_{CC} is dependent on input low voltage level V_{ILD}, V_{ILD} > -0.5 V.

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AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter NOTES	Symbol	MB 81464-12		MB 81464-15		Unit
		Min	Max	Min	Max	
Time between Refresh	t_{REF}		4		4	ms
Random Read/Write Cycle Time	t_{RC}	220		260		ns
Read-Modify-Write Cycle Time	t_{RWC}	305		345		ns
Page Mode Cycle Time	t_{PC}	120		145		ns
Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	195		225		ns
Access Time from $\overline{RAS}$ 4 6	t_{RAC}		120		150	ns
Access Time from $\overline{CAS}$ 5 6	t_{CAC}		60		75	ns
Output Buffer Turn Off Delay	t_{OFF}	0	25	0	30	ns
Transition Time	t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time	t_{RP}	90		100		ns
$\overline{RAS}$ Pulse Width	t_{RAS}	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	60		75		ns
$\overline{CAS}$ Precharge Time (Page mode only)	t_{CP}	50		60		ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)	t_{CPN}	32		35		ns
$\overline{CAS}$ Pulse Width	t_{CAS}	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time	t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time 7 8	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time	t_{CRS}	10		10		ns
Row Address Set Up Time	t_{ASR}	0		0		ns
Row Address Hold Time	t_{RAH}	12		15		ns
Column Address Set Up Time	t_{ASC}	0		0		ns
Column Address Hold Time	t_{CAH}	20		25		ns
Read Command Set Up Time	t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$ 9	t_{RRH}	15		20		ns
Read Command Hold Time Referenced to $\overline{CAS}$ 9	t_{RCH}	0		0		ns
Write Command Set Up Time 10	t_{WCS}	−5		−5		ns
Write Command Hold Time	t_{WCH}	30		35		ns
Write Command Pulse Width	t_{WP}	30		35		ns
Write Command to $\overline{RAS}$ Lead Time 10	t_{RWL}	40		45		ns

AC CHARACTERISTICS (cont'd)

(At recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB 81464-12		MB 81464-15		Unit
			Min	Max	Min	Max	
Write Command to $\overline{CAS}$ Lead Time	10	t_{CWL}	40		45		ns
Data In Set Up Time		t_{DS}	0		0		ns
Data In Hold Time		t_{DH}	30		35		ns
Access Time from $\overline{OE}$		t_{OEA}		30		40	ns
$\overline{OE}$ to Data In Delay Time		t_{OED}	25		30		ns
Output Buffer Turn Off Delay from $\overline{OE}$		t_{OEZ}	0	25	0	30	ns
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$		t_{OEH}	0		0		ns
$\overline{CAS}$ Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ refresh)		t_{FCS}	20		20		ns
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ refresh)		t_{FCH}	25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time (Refresh cycles)		t_{RPC}	10		10		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycles)		t_{CPR}	30		30		ns
$\overline{OE}$ to $\overline{RAS}$ in active Set Up Time		t_{OES}	0		0		ns
D_{IN} to $\overline{CAS}$ Delay Time	11	t_{DZC}	0		0		ns
D_{IN} to $\overline{OE}$ Delay Time	11	t_{DZO}	0		0		ns
Refresh Counter Test Cycle Time	12	t_{RTC}	430		505		ns
Refresh Counter Test Cycle $\overline{RAS}$ Pulse Width	12	t_{TRAS}	330	10000	395	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	12	t_{CPT}	60		70		ns

Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5 ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS} is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only. Even if $t_{WCS} \leq t_{WCS}$(min), the write cycle can be excuted by satisfying t_{RWL} or t_{CWL} specification.
11. Either t_{DZC} or t_{DRO} must be satisfied for all cycles.
12. Refresh Counter Test Cycle only.

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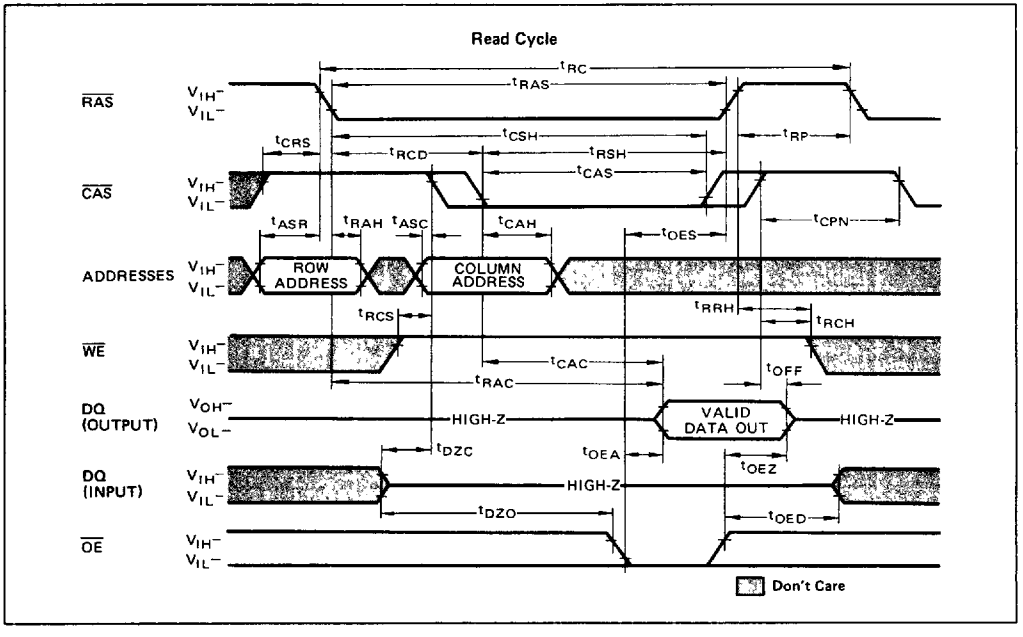
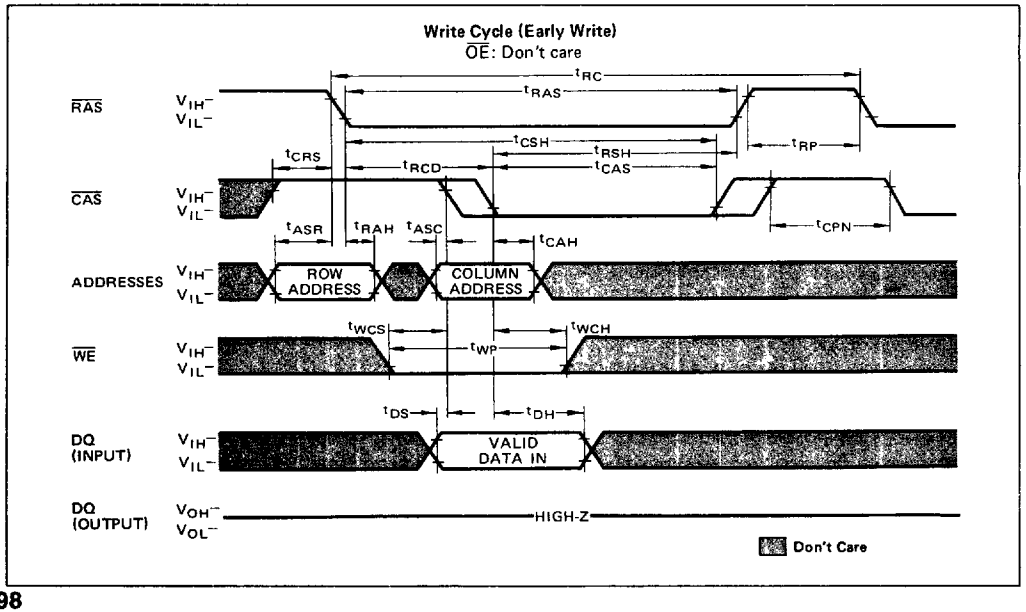
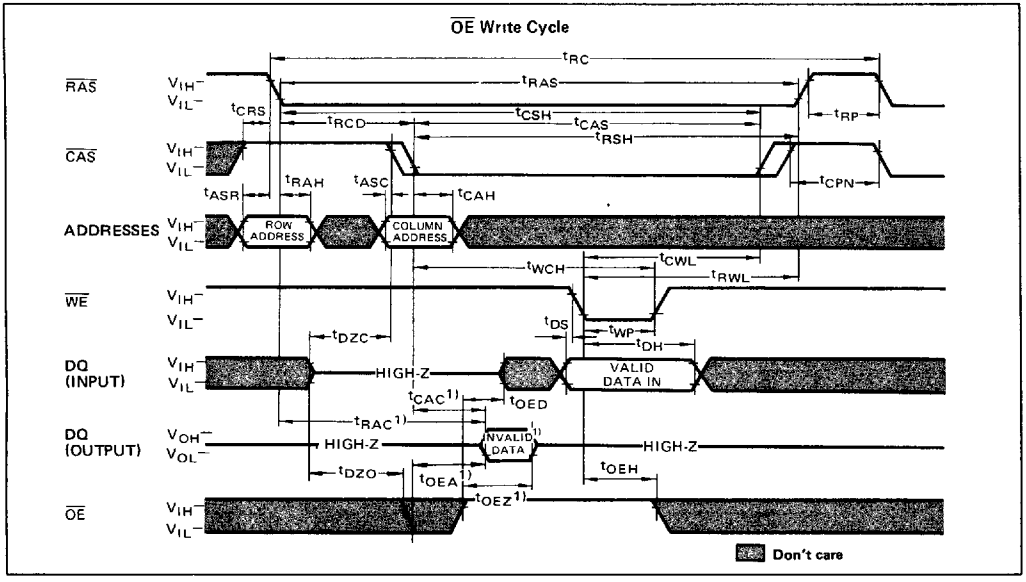
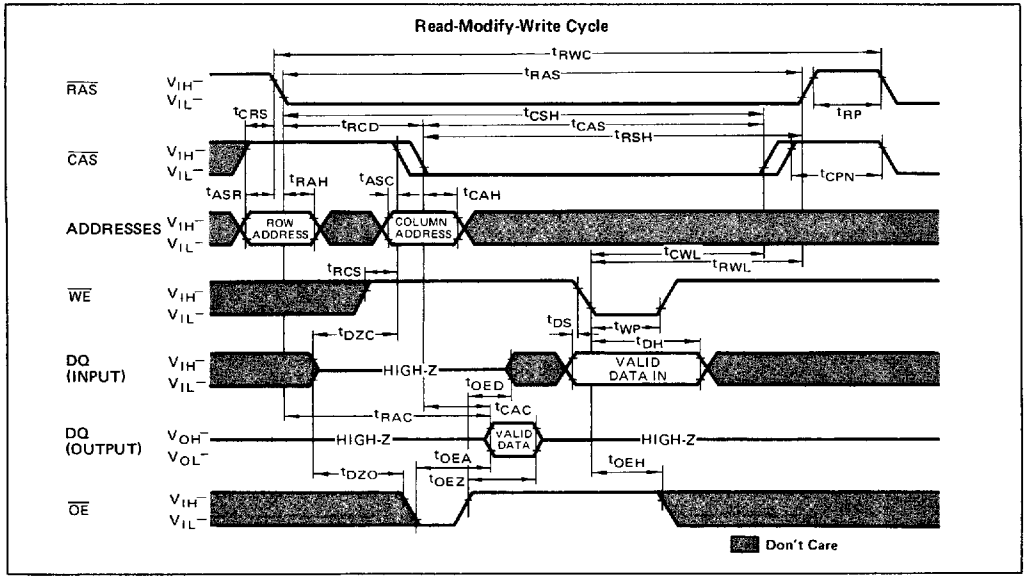

Read Cycle
RAS
CAS
ADDRESSES
WE
DQ (OUTPUT)
DQ (INPUT)
OE
ROW ADDRESS
COLUMN ADDRESS
VALID DATA OUT
HIGH-Z
Don't Care


Write Cycle (Early Write)
OE: Don't care
RAS
CAS
ADDRESSES
WE
DQ (INPUT)
DQ (OUTPUT)
ROW ADDRESS
COLUMN ADDRESS
VALID DATA IN
HIGH-Z
Don't Care





Note: 1) When $\overline{OE}$ is kept high through a cycle, the DQ pins are kept high-Z state.

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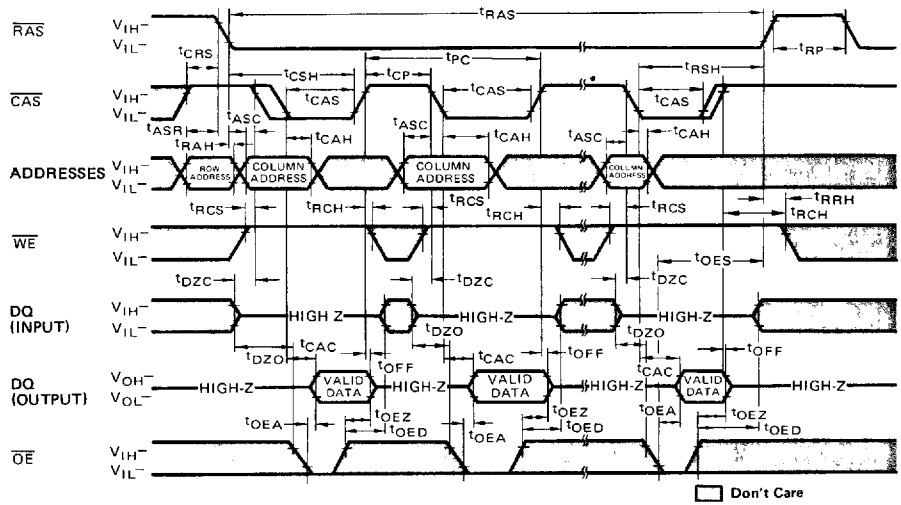
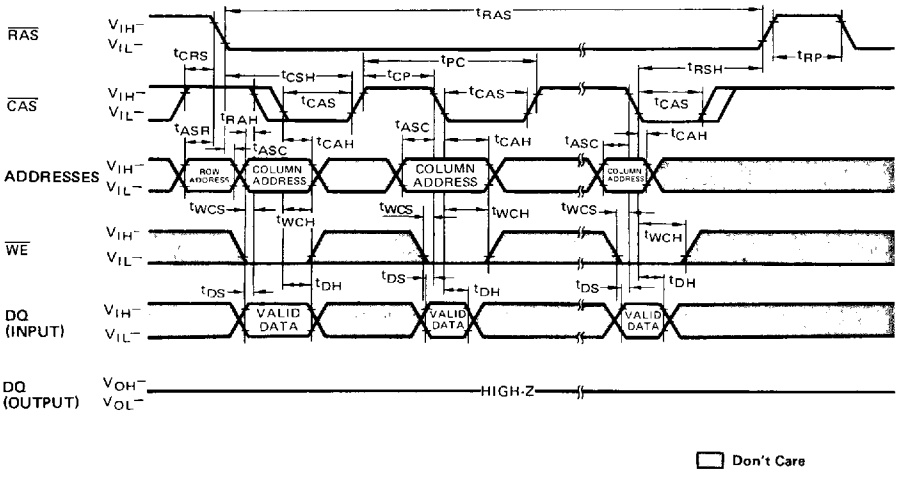
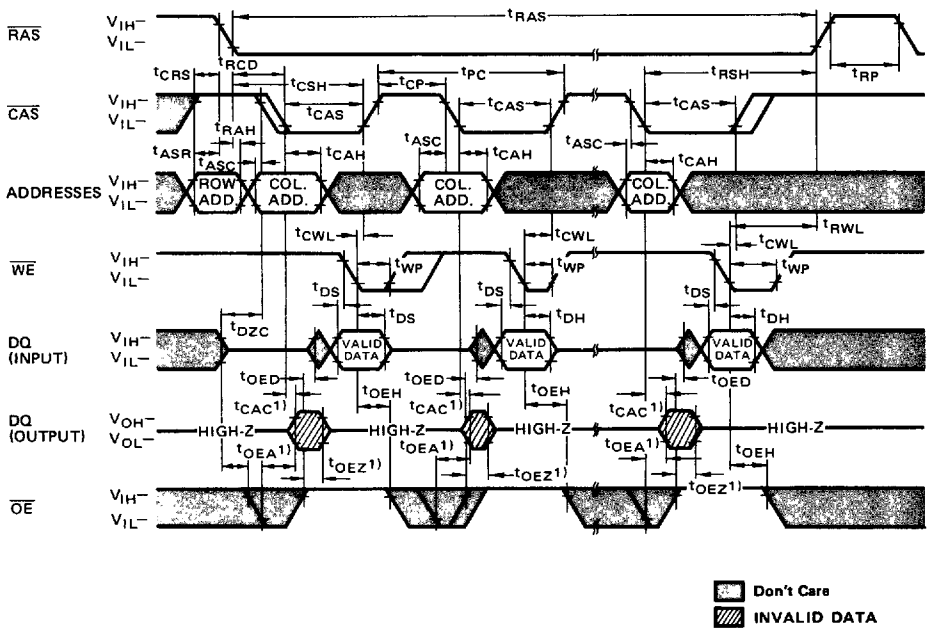
Page Mode Read Cycle



Page Mode Write Cycle
($\overline{OE}$=Don't Care)



Page Mode $\overline{OE}$ Write Cycle



Note: 1) When $\overline{OE}$ is kept high through a cycle, the DQ pins are kept high-Z state.

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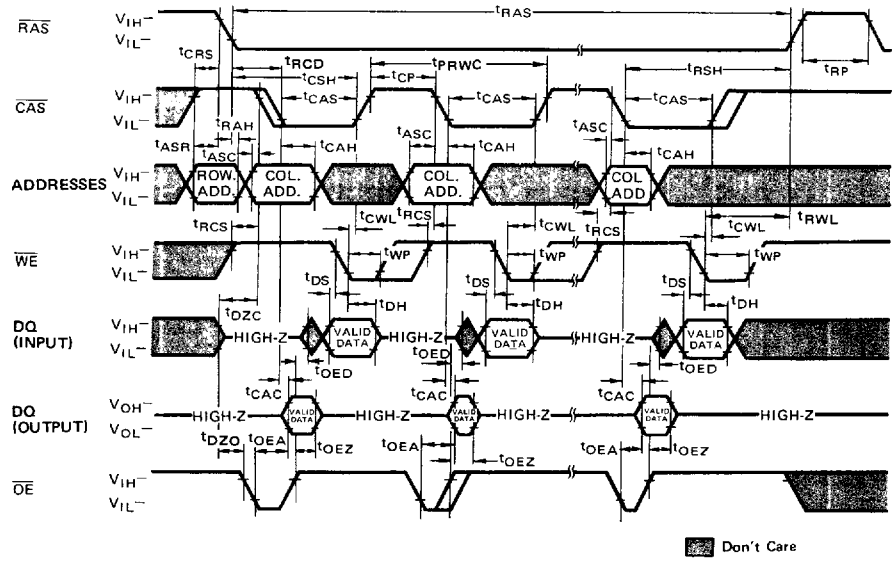
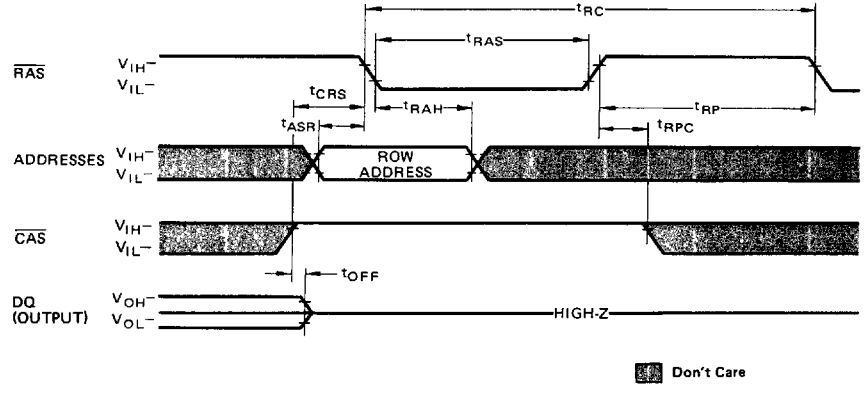
Page Mode Read Modify-Write Cycle



RAS-Only Refresh Cycle
(WE, OE=Don't Care)



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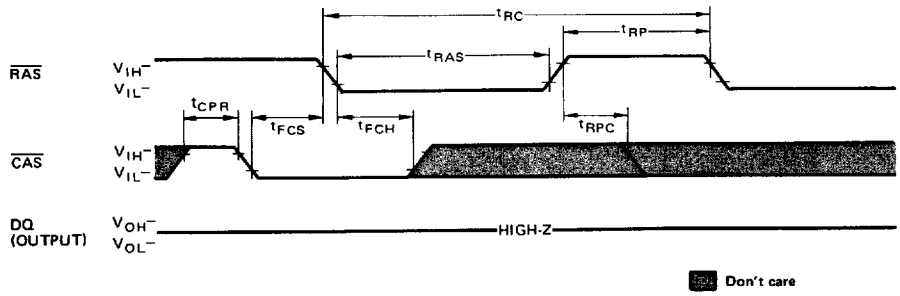
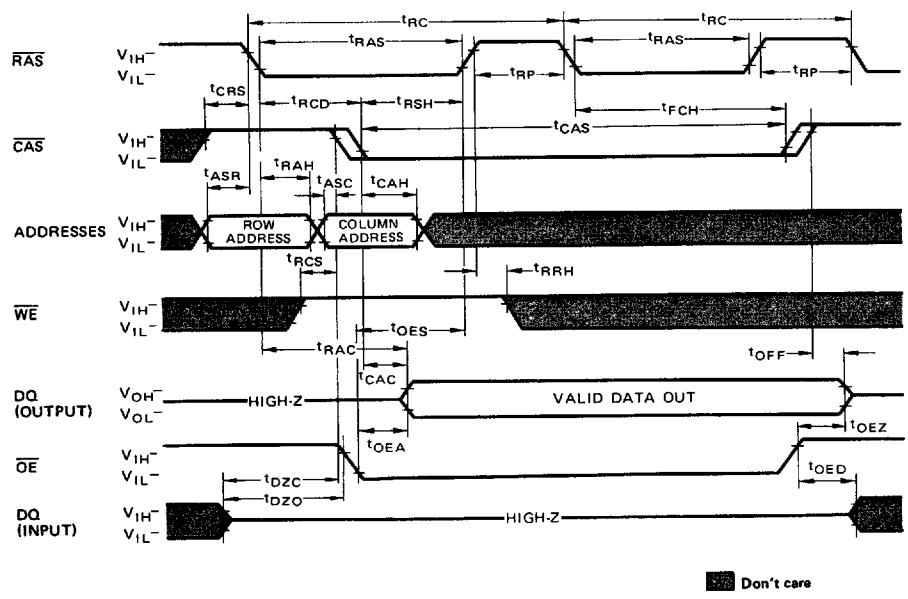
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

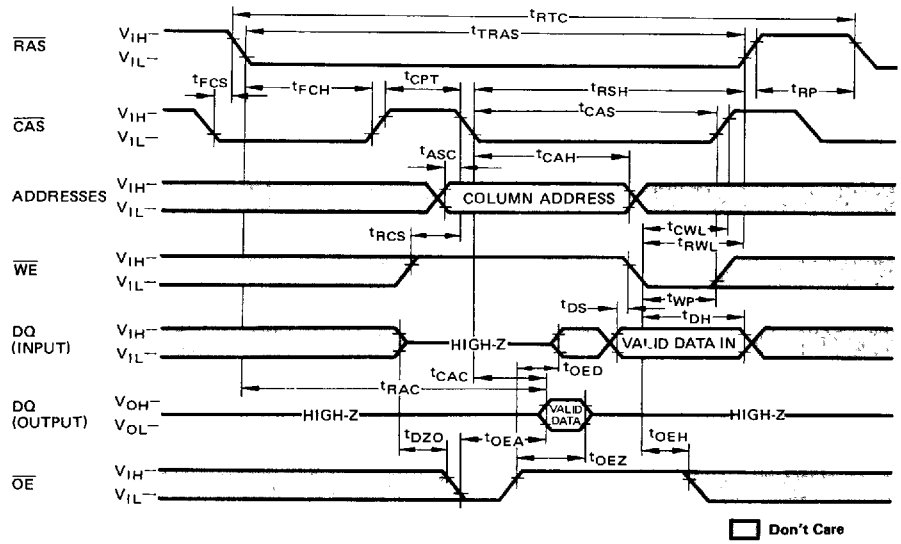
NOTE: Addresses, $\overline{WE}$, $\overline{OE}$ = Don't care



Hidden Refresh Cycle



Refresh Counter Test Cycle



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode parallel 4 bits of 262,144 storage cell locations within the MB 81464.

Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins (A_0 through A_7) and latched with the Column Address Strobe ($\overline{CAS}$).

The row and column address inputs must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable.

The read mode or write mode is selected with the Write Enable ($\overline{WE}$) input. A high on $\overline{WE}$ selects read mode and low selects write mode. The data inputs are disabled when the read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data-outs will remain in the high-impedance state allowing a write cycle.

Data Pins:

Data Inputs;

Data are written during a write or read-modify-write cycle. The later falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed by $\overline{CAS}$ with setup and hold times referenced to $\overline{CAS}$. In a read-modify-write cycle, thus the data will be strobed by $\overline{WE}$ with set-up and hold times referenced to $\overline{WE}$.

In a read-modify-write cycle, $\overline{OE}$ must be low after t_{DZO} to change the data pins from input mode to output mode and then $\overline{OE}$ must be changed to low before t_{OED} to return the data pins to input mode. In an early write cycle, data pins are in input mode regardless of the status of $\overline{OE}$.

Data Outputs;

The three-state output buffers provide direct TTL compatibility with a fan out of two standard TTL loads. Data-out are the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle, the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied. The outputs become valid after the access time has elapsed and remain valid while $\overline{CAS}$ and $\overline{OE}$ are low. In a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high brings the outputs into the high impedance state.

Output Enable:
The $\overline{OE}$ controls the impedance of the output buffers. In the high state on $\overline{OE}$, the output buffers are high impedance state. In the low state on $\overline{OE}$, the output buffers are low impedance state. But in early write cycle, the output buffers are in high impedance state even if $\overline{OE}$ is low. In the page mode read cycle, $\overline{OE}$ can be allowed low through the cycle. In the page mode early write cycle, $\overline{OE}$ can be allowed high throughout the cycle. In the page mode read-modify-write or delayed write cycle, $\overline{OE}$ must be changed from low to high with t_{OED}.

Page Mode:
Page Mode operation permits strobing the row-address into the MB 81464 while maintaining $\overline{RAS}$ at a low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh;
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 through A_7) at least every four milliseconds.
The MB 81464 offeres the following three types of refresh.

$\overline{RAS}$-Only Refresh:
$\overline{RAS}$-only refresh avoids any output during refresh because the output buffuers are in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed.
Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh;
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 81464 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and a internal refresh operation takes place.
After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh:
Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time.
In MB 81464, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses i.e., it doesn't need to apply refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in the cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle:
A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be accessed can be defined as follows:

*A ROW ADDRESS – All bits are defined by the refresh counter.
*A COLUMN ADDRESS – All the bits A_0 to A_7 are defined by latching levels on A_0 to A_7 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure
The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for the following operations:

1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Throughout the test, use the same column address.
3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
6) Complement the test pattern and repeat step 3), 4) and 5).

1

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1

Fig. 2 – CURRENT WAVEFORM (V_{CC} = 5.5 V, T_A = 25°C)

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

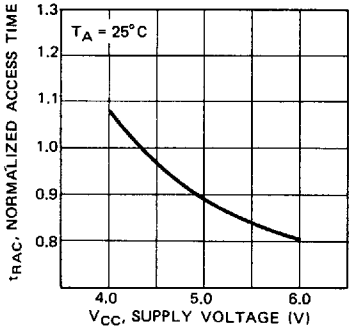


Fig. 4 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

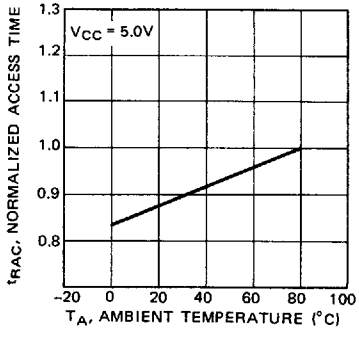


Fig. 5 – OPERATING CURRENT vs. CYCLE RATE

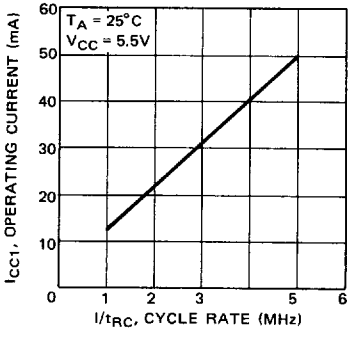


Fig. 6 – OPERATING CURRENT vs. SUPPLY VOLTAGE

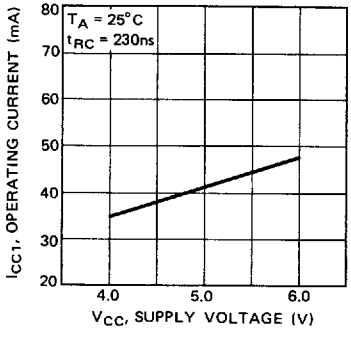


Fig. 7 – OPERATING CURRENT vs. AMBIENT TEMPERATURE

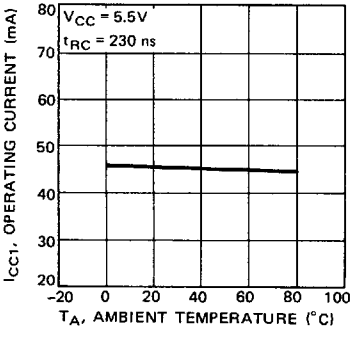
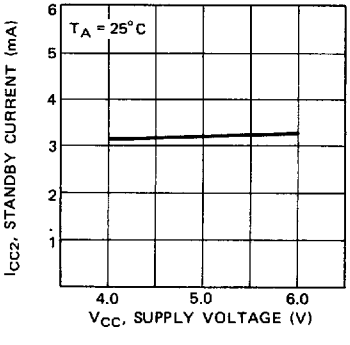


Fig. 8 – STANDBY CURRENT vs. SUPPLY VOLTAGE



1

Fig. 9 – STANDBY CURRENT vs. AMBIENT TEMPERATURE

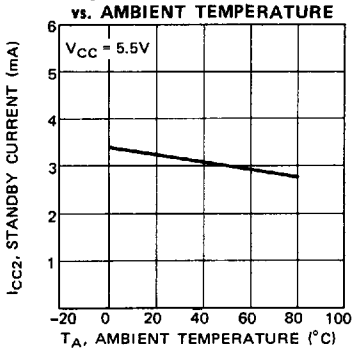


Fig. 10 – REFRESH CURRENT 1 vs. CYCLE RATE

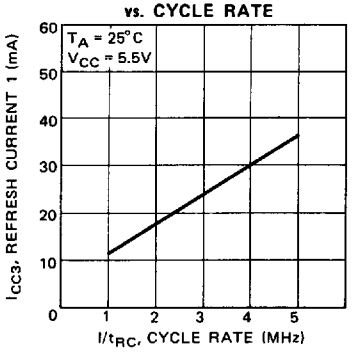


Fig. 11 – REFRESH CURRENT 1 vs. SUPPLY VOLTAGE

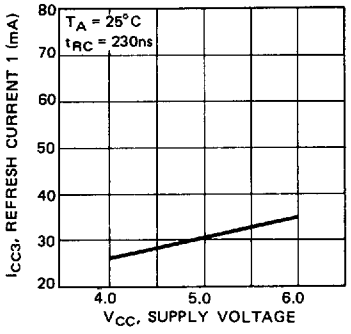


Fig. 12 – PAGE MODE CURRENT vs. CYCLE RATE

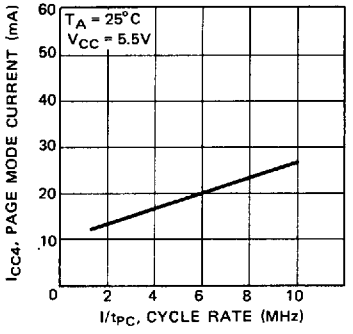


Fig. 13 – PAGE MODE CURRENT vs. CYCLE RATE

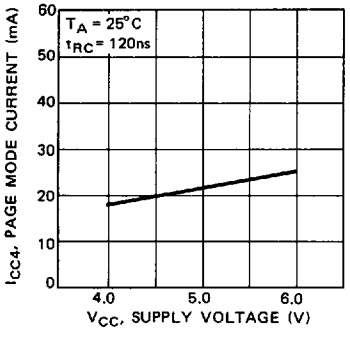


Fig. 14 – REFRESH CURRENT 2 vs. CYCLE RATE

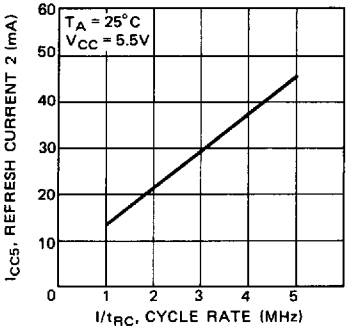


Fig. 15 – REFRESH CURRENT 2 vs. SUPPLY VOLTAGE

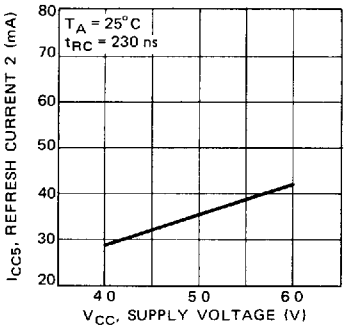


Fig. 16 – ADDRESS AND DATA INPUT VOLTAGE vs. SUPPLY VOLTAGE

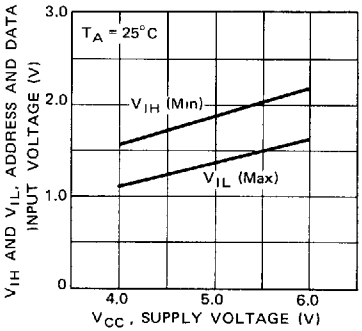


Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs. AMBIENT TEMPERATURE

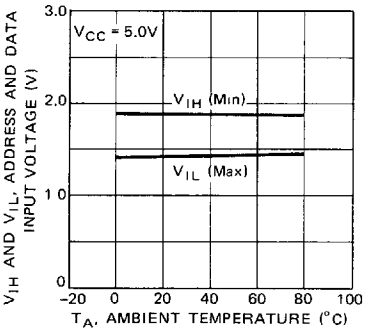


Fig. 18 – $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ AND $\overline{OE}$ INPUT VOLTAGE vs. SUPPLY VOLTAGE

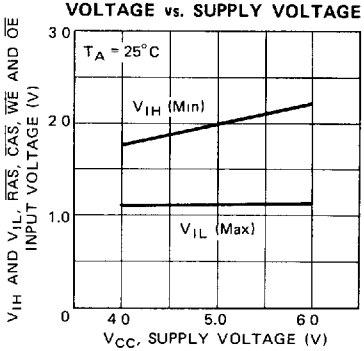


Fig. 19 – $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ AND $\overline{OE}$ INPUT VOLTAGE vs. AMBIENT TEMPERATURE

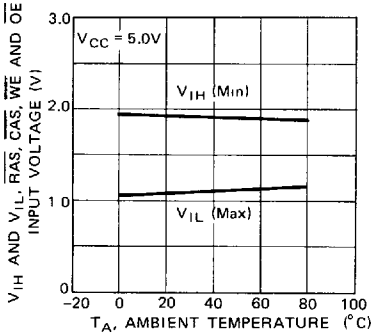


Fig. 20 – ACCESS TIME vs. LOAD CAPACITANCE

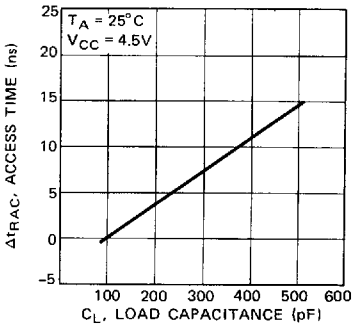


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Fig. 21 – OUTPUT CURRENT vs. OUTPUT VOLTAGE

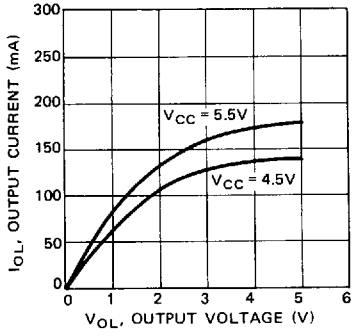


Fig. 22 – OUTPUT CURRENT vs. OUTPUT VOLTAGE

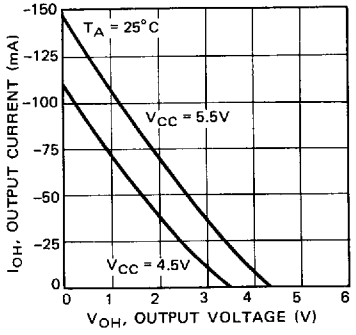


Fig. 23 – SUBSTRATE VOLTAGE DURING POWER UP

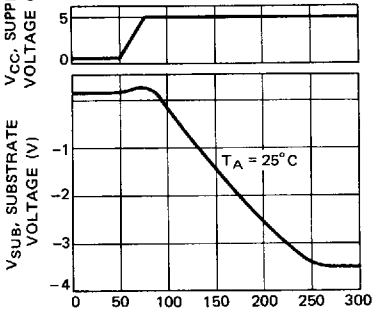
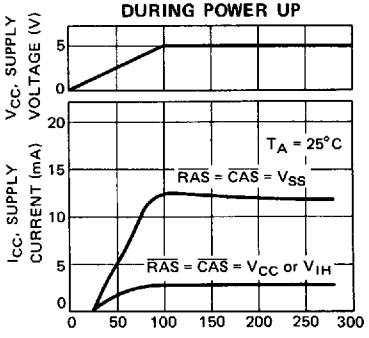


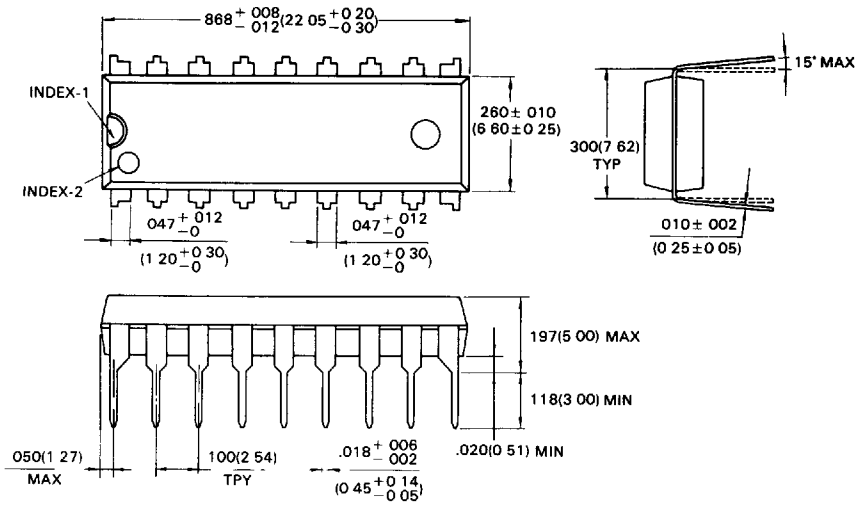
Fig. 24 – CURRENT WAVEFORM DURING POWER UP



PACKAGE DIMENSIONS

(Suffix: -P)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-18P-M03)



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Dimensions in inches (millimeters)

T-46-23-17

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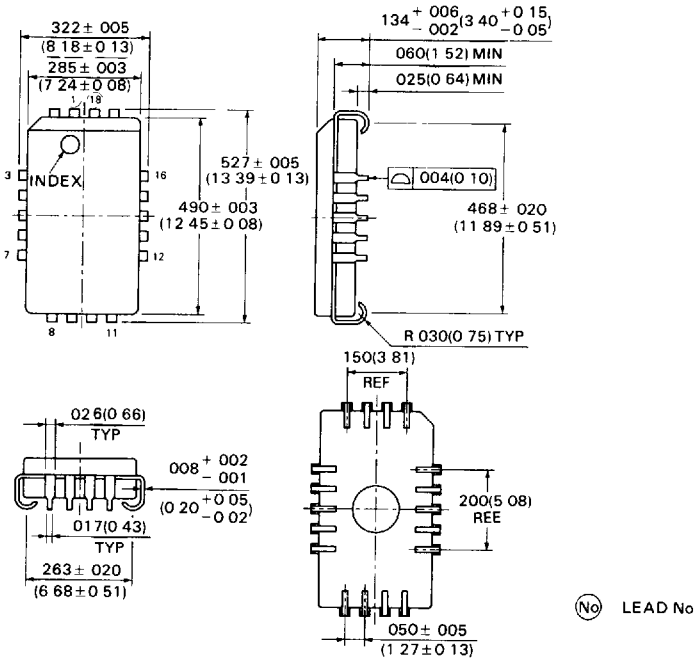
PACKAGE DIMENSIONS
(Suffix: -PD)

18-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-18P-M04)



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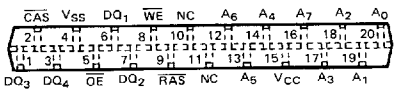
Dimensions in inches (millimeters)

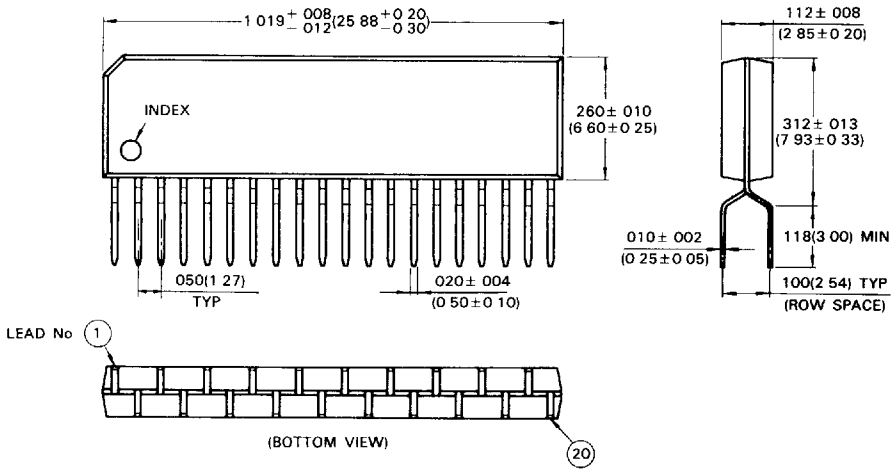
T-46-23-17

PACKAGE DIMENSIONS

(Suffix: -PSZ)



20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-20P-M01)



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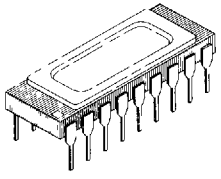
Dimensions in inches (millimeters)

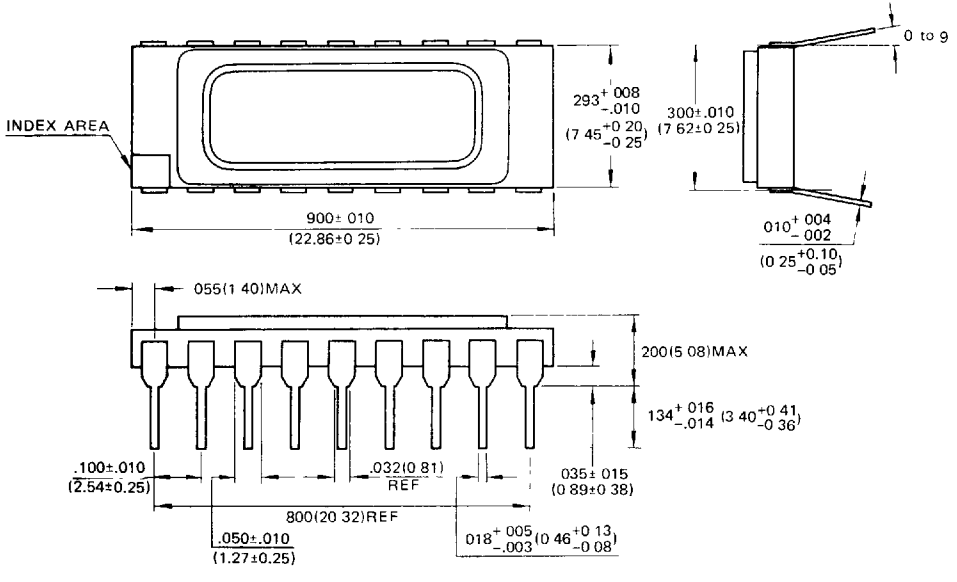
PACKAGE DIMENSIONS

(Suffix: -C)



DIP-18C-A01

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)



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Dimensions in inches (millimeters)