

PIC18(L)F26/46K22 Rev. A2 Silicon Errata and Data Sheet Clarification

The PIC18(L)F26/46K22 family devices that you have received conform functionally to the current Device Data Sheet (DS41412C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC18(L)F26/46K22 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select Configure>Select Device, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (Debugger>Select Tool).
4. Perform a "Connect" operation to the device (Debugger>Connect). Depending on the development tool used, the part number and Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18(L)F26/46K22 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾
		A2
PIC18F46K22	0101 0100 000x xxxx	0 0010
PIC18LF46K22	0101 0100 001x xxxx	0 0010
PIC18F26K22	0101 0100 010x xxxx	0 0010
PIC18LF26K22	0101 0100 011x xxxx	0 0010

Note 1: The Device ID is located in the last configuration memory space.

2: Refer to the "PIC18(L)F2XK22/4XK22 Flash Memory Programming Specification" (DS41398) for detailed information on Device and Revision IDs for your specific device.

PIC18(L)F26/46K22

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾
				A2
Comparators	CxSYNC Control	1.	The comparator output to the device pin (Cx) always bypasses the Timer1 synchronization latch.	X
Clock Switching	Fail-Safe Clock Monitor	2.	When the FCMEN Configuration bit is set and the IESO Configuration bit is not set, then a clock failure during Sleep will not be detected.	X
Power-on Reset (POR)	Power-on Reset	3.1	Transient current spikes on some parts during power-up may cause the part to become stuck in Reset.	X
Power-on Reset (POR)	Power-on Reset	3.2	Min VDD for PIC18F2X/4XK22 parts is limited to 2.3V. Min VDD for PIC18LF2X/4XK22 parts is 1.8V.	X
Timer1/3/5 Gate	Timer1/3/5 Gate	4.	The Timer1/3/5 gate times cannot be resolved to the two Least Significant bits, when using Fosc as the Timer1/3/5 source.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: Comparators

The CxSYNC controls are inoperative. The comparator output (Cx) always bypasses the Timer1 synchronization latch.

Work around

None.

Affected Silicon Revisions

A2							
X							

2. Module: Clock Switching

When the FCMEN Configuration bit is set and the IESO Configuration bit is not set, then a clock failure during Sleep will not be detected.

Work around

The IESO Configuration bit must also be set when the FCMEN Configuration bit is set.

Affected Silicon Revisions

A2							
X							

3. Module: Power-on Reset (POR)

- 3.1 There may be transient current spikes on some parts during power-up. If the application cannot supply enough current to get past these transients, then the part may become stuck in Reset.

Work around

Ensure that the application is capable of supplying at least 30 mA of transient current during power-up.

Affected Silicon Revisions

A2							
X							

- 3.2 Min VDD for PIC18F2X/4XK22 parts is limited to 2.3V. Min VDD for PIC18LF2X/4XK22 parts is 1.8V.

Work around

None.

Affected Silicon Revisions

A2							
X							

4. Module: Timer1/3/5 Gate

The Timer gate times cannot be resolved to the two Least Significant timer bits when the source frequency is FOSC (TMR_xCS [1:0]=01). This is because the gate edges are synchronized with the Fosc/4 clock.

Work around

None.

Affected Silicon Revisions

A2							
X							

PIC18(L)F26/46K22

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41412C):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: I/O Ports

In Table 10-5, the Buffer Type column listed ST (Schmitt Trigger) for functions RB1-RB7, when the Pin Type was I (Input), should be TTL. The Table below reflects the correction.

TABLE 10-5: PORTB I/O SUMMARY

Pin	Function	TRIS Setting	ANSEL Setting	Pin Type	Buffer Type	Description
RB0/INT0/CCP4/ FLT0/SRI/SS2/ AN12	RB0	0	1	O	DIG	LATB<0> data output; not affected by analog input.
		1	0	I	TTL	PORTB<0> data input; disabled when analog input enabled.
	INT0	1	0	I	ST	External interrupt 0.
	CCP4 ⁽³⁾	0	1	O	DIG	Compare 4 output/PWM 4 output.
		1	0	I	ST	Capture 4 input.
	FLT0	1	0	I	ST	PWM Fault input for ECCP auto-shutdown.
	SRI	1	0	I	ST	SR Latch input.
	SS2 ⁽³⁾	1	0	I	TTL	SPI slave select input (MSSP2).
RB1/INT1/P1C/ SCK2/SCL2/ C12IN3-/AN10	RB1	0	1	O	DIG	LATB<1> data output; not affected by analog input.
		1	0	I	TTL	PORTB<1> data input; disabled when analog input enabled.
	INT1	1	0	I	ST	External Interrupt 1.
	P1C ⁽³⁾	0	1	O	DIG	Enhanced CCP1 PWM output 3.
	SCK2 ⁽³⁾	0	1	O	DIG	MSSP2 SPI Clock output.
		1	0	I	ST	MSSP2 SPI Clock input.
	SCL2 ⁽³⁾	0	1	O	DIG	MSSP2 I ² C TM Clock output.
		1	0	I	I ² C	MSSP2 I ² C TM Clock input.
	C12IN3-	1	1	I	AN	Comparators C1 and C2 inverting input.
	AN10	1	1	I	AN	Analog input 10.

Legend: AN = Analog input or output; TTL = TTL compatible input; HV = High Voltage; OD = Open Drain; XTAL = Crystal; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I²CTM = Schmitt Trigger input with I²C.

Note 1: Default pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

2: Alternate pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

3: Function on PORTD and PORTE for PIC18(L)F4XK22 devices.

TABLE 10-5: PORTB I/O SUMMARY

Pin	Function	TRIS Setting	ANSEL Setting	Pin Type	Buffer Type	Description
RB2/INT2/CTED1/ P1B/SDI2/SDA2/ AN8	RB2	0	1	O	DIG	LATB<2> data output; not affected by analog input.
		1	0	I	TTL	PORTB<2> data input; disabled when analog input enabled.
	INT2	1	0	I	ST	External interrupt 2.
	CTED1	1	0	I	ST	CTMU Edge 1 input.
	P1B ⁽³⁾	0	1	O	DIG	Enhanced CCP1 PWM output 2.
	SDI2 ⁽³⁾	1	0	I	ST	MSSP2 SPI data input.
	SDA2 ⁽³⁾	0	0	O	DIG	MSSP2 I ² C TM data output.
		1	0	I	I ² C	MSSP2 I ² C TM data input.
	AN8	1	1	I	AN	Analog input 8.
RB3/CTED2/P2A/ CCP2/SDO2/ C12IN2-/AN9	RB3	0	1	O	DIG	LATB<3> data output; not affected by analog input.
		1	0	I	TTL	PORTB<3> data input; disabled when analog input enabled.
	CTED2	1	0	I	ST	CTMU Edge 2 input.
	P2A	0	1	O	DIG	Enhanced CCP1 PWM output 1.
	CCP2 ⁽²⁾	0	1	O	DIG	Compare 2 output/PWM 2 output.
		1	0	I	ST	Capture 2 input.
	SDO2 ⁽²⁾	0	1	O	DIG	MSSP2 SPI data output.
	C12IN2-	1	1	I	AN	Comparators C1 and C2 inverting input.
	AN9	1	1	I	AN	Analog input 9.
RB4/IOC0/P1D/ T5G/AN11	RB4	0	1	O	DIG	LATB<4> data output; not affected by analog input.
		1	0	I	TTL	PORTB<4> data input; disabled when analog input enabled.
	IOC0	1	0	I	TTL	Interrupt-on-change pin.
	P1D	0	1	O	DIG	Enhanced CCP1 PWM output 4.
	T5G	1	0	I	ST	Timer5 external clock gate input.
	AN11	1	1	I	AN	Analog input 11.
RB5/IOC1/P2B/ P3A/CCP3/T3CKI/ T1G/AN13	RB5	0	1	O	DIG	LATB<5> data output; not affected by analog input.
		1	0	I	TTL	PORTB<5> data input; disabled when analog input enabled.
	IOC1	1	0	I	TTL	Interrupt-on-change pin 1.
	P2B ⁽¹⁾⁽³⁾	0	1	O	DIG	Enhanced CCP2 PWM output 2.
	P3A ⁽¹⁾	0	1	O	DIG	Enhanced CCP3 PWM output 1.
	CCP3 ⁽¹⁾	0	1	O	DIG	Compare 3 output/PWM 3 output.
		1	0	I	ST	Capture 3 input.
	T3CKI ⁽²⁾	1	0	I	ST	Timer3 clock input.
	T1G	1	0	I	ST	Timer1 external clock gate input.
	AN13	1	1	I	AN	Analog input 13.

Legend: AN = Analog input or output; TTL = TTL compatible input; HV = High Voltage; OD = Open Drain; XTAL = Crystal; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I²CTM = Schmitt Trigger input with I²C.

Note 1: Default pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

2: Alternate pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

3: Function on PORTD and PORTE for PIC18(L)F4XK22 devices.

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TABLE 10-5: PORTB I/O SUMMARY

Pin	Function	TRIS Setting	ANSEL Setting	Pin Type	Buffer Type	Description
RB6/KBI2/PGC	RB6	0	1	O	DIG	LATB<6> data output; not affected by analog input.
		1	0	I	TTL	PORTB<6> data input; disabled when analog input enabled.
	IOC2	1	0	I	TTL	Interrupt-on-change pin.
	TX2 ⁽³⁾	0	1	O	DIG	EUSART 2 asynchronous transmit data output.
	CK2 ⁽³⁾	0	1	O	DIG	EUSART 2 synchronous serial clock output.
		1	0	I	ST	EUSART 2 synchronous serial clock input.
	PGC	x	x	I	ST	In-Circuit Debugger and ICSP™ programming clock input.
RB7/KBI3/PGD	RB7	0	1	O	DIG	LATB<7> data output; not affected by analog input.
		1	0	I	TTL	PORTB<7> data input; disabled when analog input enabled.
	IOC3	1	0	I	TTL	Interrupt-on-change pin.
	RX2 ^{(2), (3)}	1	0	I	ST	EUSART 2 asynchronous receive data input.
	DT2 ^{(2), (3)}	0	1	O	DIG	EUSART 2 synchronous serial data output.
		1	0	I	ST	EUSART 2 synchronous serial data input.
	PGD	x	x	O	DIG	In-Circuit Debugger and ICSP™ programming data output.
		x	x	I	ST	In-Circuit Debugger and ICSP™ programming data input.

Legend: AN = Analog input or output; TTL = TTL compatible input; HV = High Voltage; OD = Open Drain; XTAL = Crystal; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I²C™ = Schmitt Trigger input with I²C.

Note 1: Default pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

2: Alternate pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

3: Function on PORTD and PORTE for PIC18(L)F4XK22 devices.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (8/2010)

Initial release of this document.

PIC18(L)F26/46K22

NOTES:

Note the following details of the code protection feature on Microchip devices:

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