

# SN54ALS373, SN54AS373, SN74ALS373A, SN74AS373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS083B – APRIL 1982 – REVISED DECEMBER 1994

- Eight Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- pnp Inputs Reduce dc Loading on Data Lines
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

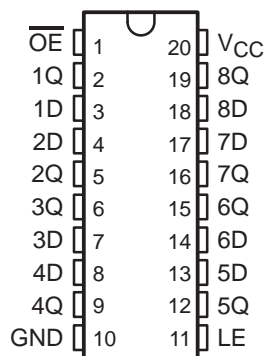
While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

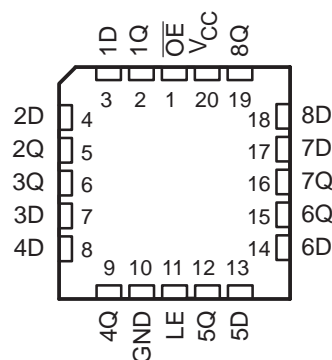
$\overline{OE}$  does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS373 and SN54AS373 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS373A and SN74AS373 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS373, SN54AS373 . . . J PACKAGE  
SN74ALS373A, SN74AS373 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54ALS373, SN54AS373 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

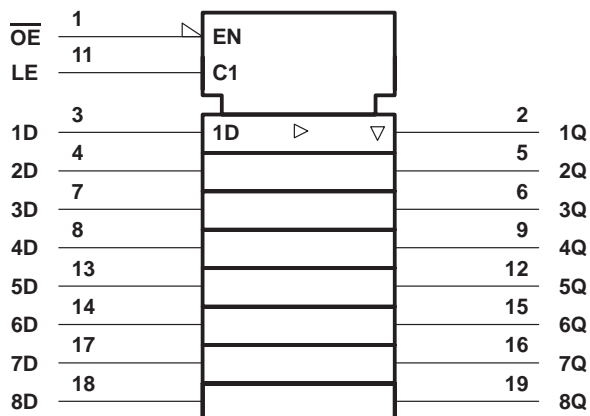
# SN54ALS373, SN54AS373, SN74ALS373A, SN74AS373

## OCTAL TRANSPARENT D-TYPE LATCHES

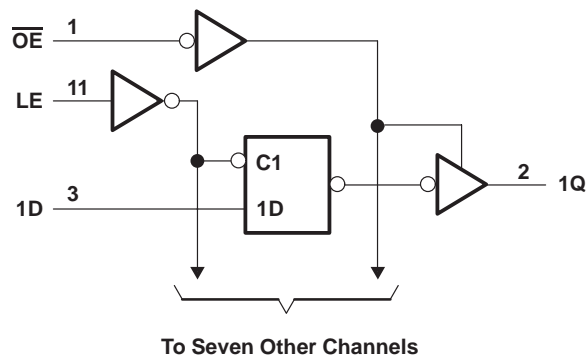
### WITH 3-STATE OUTPUTS

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#### logic symbol†



#### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to any output in the high state or power-off state	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS373	-55°C to 125°C
SN74ALS373A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

	SN54ALS373			SN74ALS373A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.7			0.8	V
$I_{OH}$ High-level output current			-1			-2.6	mA
$I_{OL}$ Low-level output current			12			24	mA
$t_w$ Pulse duration, LE high	12			10			ns
$t_{su}$ Setup time, data before LE↓	10			10			ns
$t_h$ Hold time, data after LE↓	7			7			ns
$T_A$ Operating free-air temperature	-55		125	0		70	°C

# SN54ALS373, SN54AS373, SN74ALS373A, SN74AS373

## OCTAL TRANSPARENT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		SN54ALS373			SN74ALS373A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$	-1.5			-1.5			V
$V_{OH}$	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ ,	$I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.4	3.3					
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4	0.25	0.4	V		
		$I_{OL} = 24\text{ mA}$			0.35	0.5			
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$	20			20			$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.4\text{ V}$	-20			-20			$\mu\text{A}$
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$	0.1			0.1			mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$	20			20			$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$	-0.1			-0.1			mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$	-20	-112	-30	-112	mA		
$I_{CC}$	$V_{CC} = 5.5\text{ V}$	Outputs high	9	16	9	16	mA		
		Outputs low	16	25	16	25			
		Outputs disabled	17	27	17	27			

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = 500\ \Omega$ , $R_2 = 500\ \Omega$ , $T_A = \text{MIN to MAX}\S$				UNIT
			SN54ALS373		SN74ALS373A		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	D	Q	2	17	2	12	ns
$t_{PHL}$			1	19	4	16	
$t_{PLH}$	LE	Any Q	6	29	6	22	ns
$t_{PHL}$			1	27	7	23	
$t_{PZH}$	$\overline{OE}$	Any Q	6	22	1	18	ns
$t_{PZL}$			5	24	5	20	
$t_{PHZ}$	$\overline{OE}$	Any Q	2	16	1	10	ns
$t_{PLZ}$			2	24	2	12	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54ALS373, SN54AS373, SN74ALS373A, SN74AS373

## OCTAL TRANSPARENT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to any output in the high state or power-off state	5.5 V
Operating free-air temperature range, $T_A$ : SN54AS373	–55°C to 125°C
SN74AS373	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

	SN54AS373			SN74AS373			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$I_{OH}$ High-level output current			–12			–15	mA
$I_{OL}$ Low-level output current			32			48	mA
$t_w^*$ Pulse duration, LE high	5.5			4.5			ns
$t_{su}^*$ Setup time, data before LE↓	2			2			ns
$t_h^*$ Hold time, data after LE↓	3			3			ns
$T_A$ Operating free-air temperature	–55		125	0		70	°C

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS373			SN74AS373			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2			–1.2	V	
$V_{OH}$	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -2$ mA	$V_{CC} - 2$		$V_{CC} - 2$				V	
	$V_{CC} = 4.5$ V	$I_{OH} = -12$ mA	2.4	3.2					
		$I_{OH} = -15$ mA			2.4	3.3			
$V_{OL}$	$V_{CC} = 4.5$ V	$I_{OL} = 32$ mA	0.27	0.5				V	
		$I_{OL} = 48$ mA			0.32	0.5			
$I_{OZH}$	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			50			50	μA	
$I_{OZL}$	$V_{CC} = 5.5$ V, $V_O = 0.4$ V			–50			–50	μA	
$I_I$	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1			0.1	mA	
$I_{IH}$	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20			20	μA	
$I_{IL}$	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			–0.02	–0.5		–0.02	–0.5	mA
$I_{O§}$	$V_{CC} = 5.5$ V, $V_O = 2.25$ V			–30	–112		–30	–112	mA
$I_{CC}$	$V_{CC} = 5.5$ V	Outputs high	55	90	55	90		mA	
		Outputs low	55	85	55	85			
		Outputs disabled	65	100	65	100			

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



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**switching characteristics (see Figure 1)**

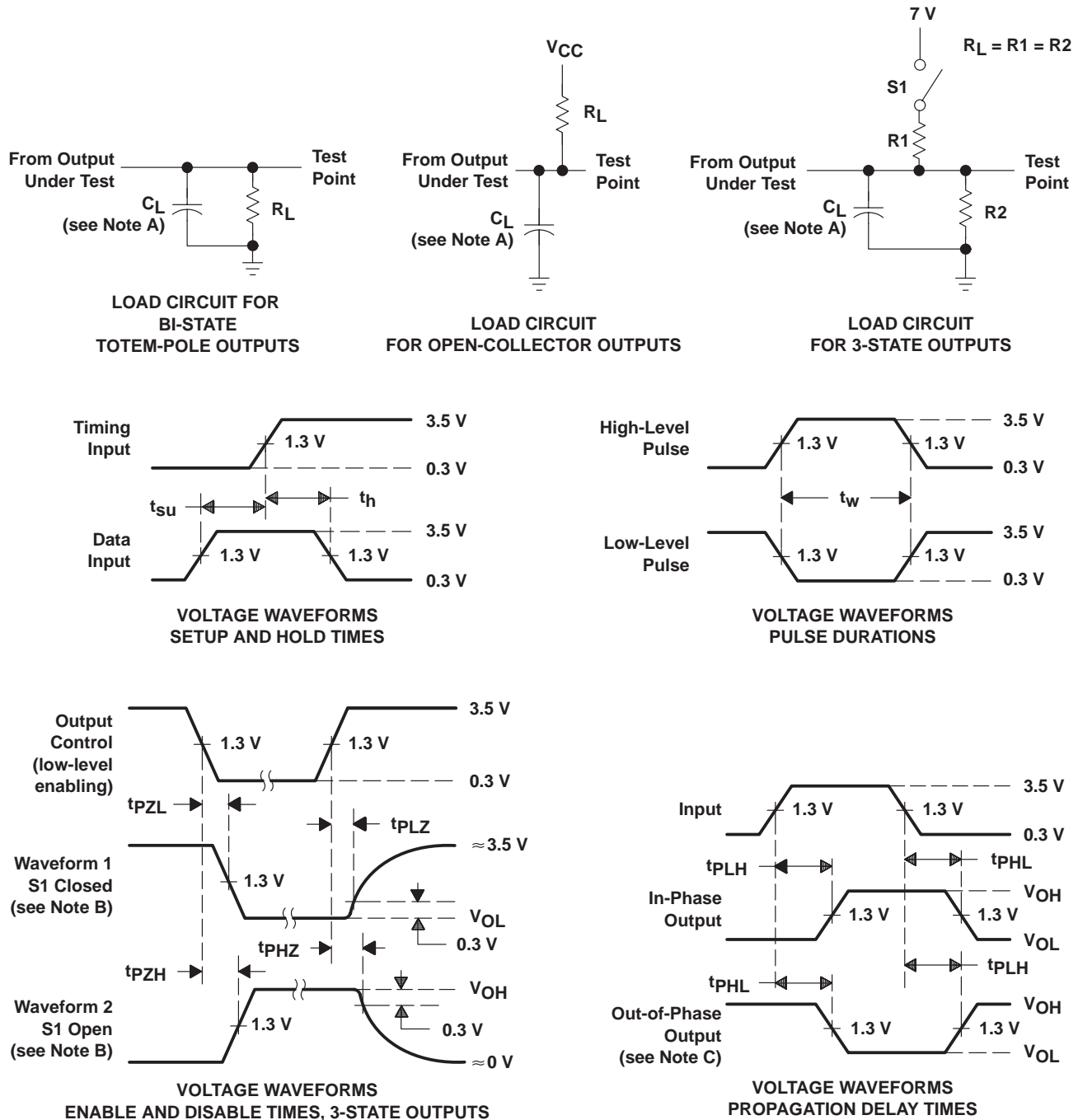
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54AS373		SN74AS373		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Q	3	9	3.5	6	ns
t <sub>PHL</sub>			3	8	3.5	6	
t <sub>PLH</sub>	LE	Any Q	6.5	14.5	6.5	11.5	ns
t <sub>PHL</sub>			5	9	5	7.5	
t <sub>PZH</sub>	$\overline{OE}$	Any Q	2	7.5	2	6.5	ns
t <sub>PZL</sub>			4.5	10.5	4.5	9.5	
t <sub>PHZ</sub>	$\overline{OE}$	Any Q	3	10	3	6.5	ns
t <sub>PLZ</sub>			3	8	3	7	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



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