

FIELD PROGRAMMABLE LOGIC ARRAY (18 × 42 × 10)

82S152 (O.C.)/82S153 (T.S.)
82S152A (O.C.)/82S153A (T.S.)

INTEGRATED FUSE LOGIC
SERIES 20

DESCRIPTION

The 82S152 and 82S153 are two-level logic elements, consisting of 32 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

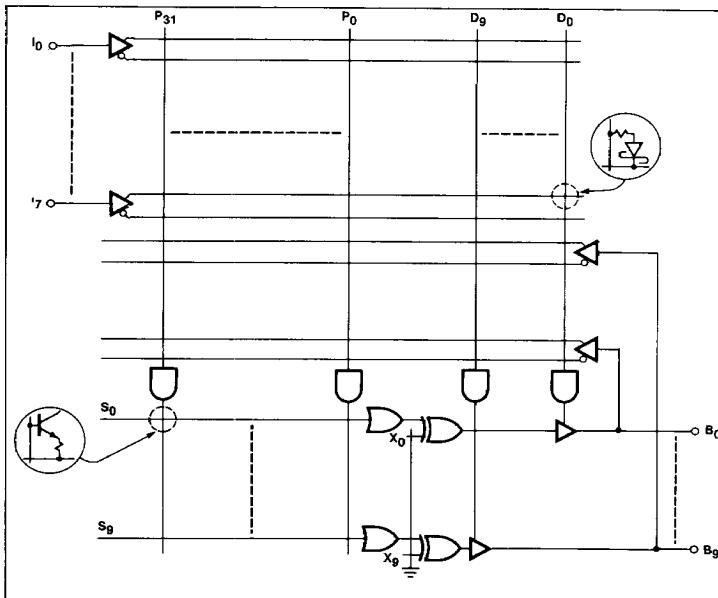
All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement (I, B) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND-OR or AND-NOR logic functions.

The 82S152 and the 82S153 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Both devices are available in a 20 pin slim line package. For the commercial temperature range (0°C to $+75^{\circ}\text{C}$) specify N82S152/153 N or F and N82S152A/153A N or F. For the military temperature range (-55°C to $+125^{\circ}\text{C}$) specify S82S152/153 F only and S82S152A/153A F only.

FUNCTIONAL DIAGRAM



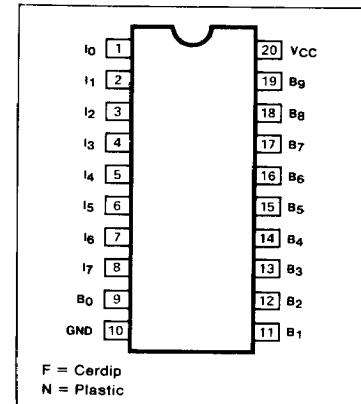
FEATURES

- Field programmable (Ni-Cr links)
- 8 Inputs
- 32 AND gates
- 10 OR gates
- 10 bidirectional I/O lines
- Active high or low outputs
- 42 Product Terms:
 - 32 Logic terms
 - 10 Control terms
- I/O propagation delay:
 - N82S152/153: 40ns (max)
 - N82S152A/153A: 30ns (max)
 - S82S152/153: 60ns (max)
 - S82S152A/153A: 45ns (max)
- Input loading
 - N82S152/153: $-100\mu\text{A}$ (max)
 - S82S152/153: $-150\mu\text{A}$ (max)
- Power dissipation:
 - 650mW (typ)
- Output options:
 - 82S152: open collector
 - 82S153: tri-state
- TTL compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

PIN CONFIGURATION



F = Cerdip

N = Plastic

LOGIC FUNCTION

Typical product term:

$$P_n = A \cdot B \cdot C \cdot D \cdot \dots$$

Typical logic function:

At Output Polarity = H

$$Z = P_0 + P_1 + P_2 + \dots$$

At Output Polarity = L

$$Z = P_0 + P_1 + P_2 + \dots$$

NOTES:

1. For each of the 10 outputs, either function Z (active-high) or Z (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

Signetics

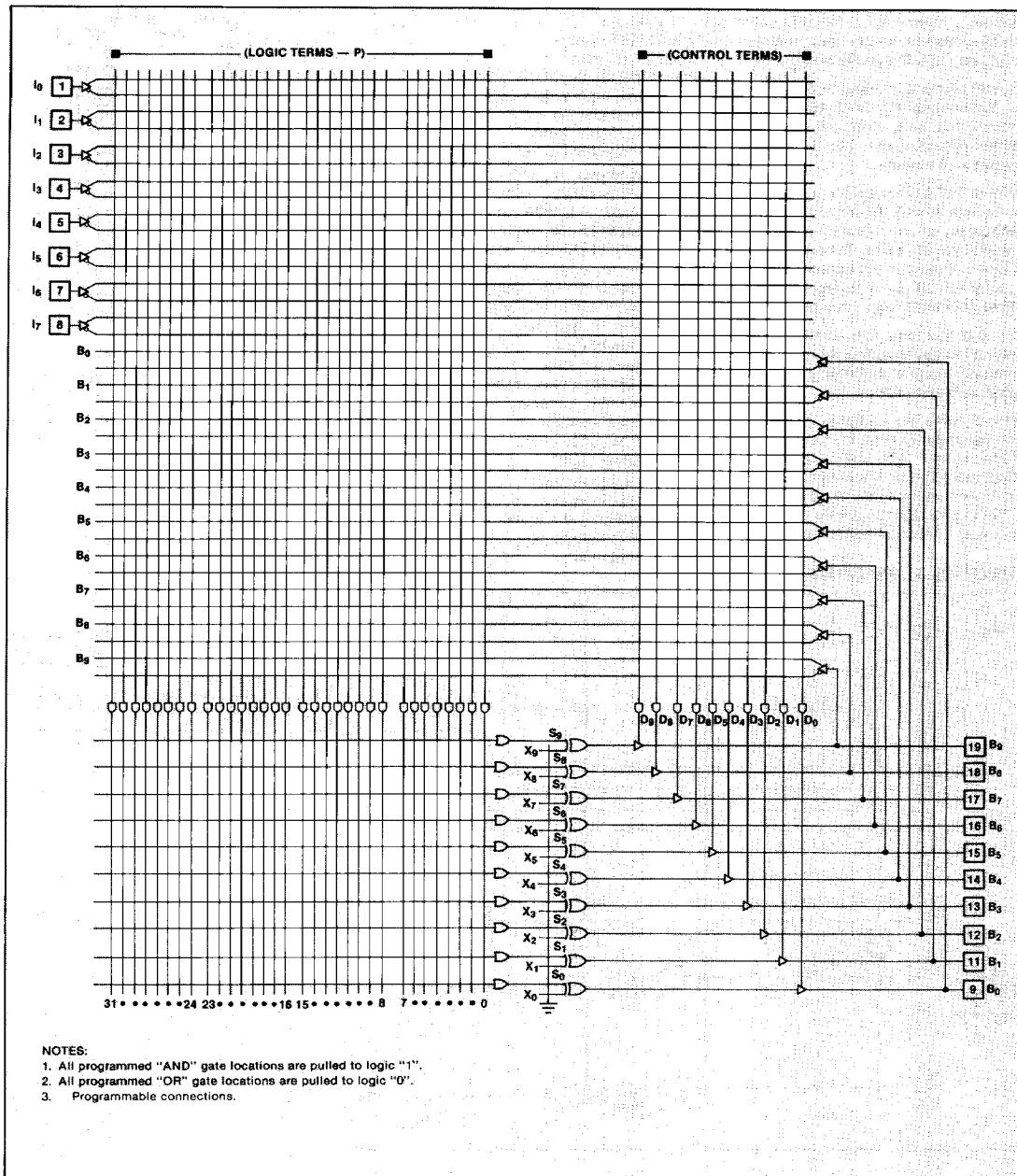
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FPLA LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING		UNIT
	Min	Max	
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
V _{OUT}	Output voltage	+5.5	Vdc
I _{IN}	Input currents	+30	mA
I _{OUT}	Output currents	+100	mA
T _A	Temperature range Operating	+75	C°
N82S152/153/152A/153A	0		
S82S152/153/152A/153A	-55	+125	
T _{STG}	Storage	-65	+150

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

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DC ELECTRICAL CHARACTERISTICS N82S152/153, N82S152A/153A: 0°C ≤ T_A ≤ +75°C, 4.75 ≤ V_{CC} ≤ 5.25V
S82S152/153, S82S152A/153A: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITION	N82S152/153			S82S152/153			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{IL}	Input voltage ³ Low				85			V
V _{IH}	High	V _{CC} = min			2.0			
V _{IC}	Clamp ^{3,4}	V _{CC} = max			- .8	- 1.2		
V _{OOL}	Output voltage Low ^{3,5}	V _{CC} = min			.5			V
V _{OOL}	Low ^{3,5}	I _{OL} = 15mA			2.4			
V _{OOL}	High ^{3,6}	I _{OL} = 12mA			- 2mA			
I _{IL}	Input current Low	V _{IN} = 0.45V			- 100			μA
I _{IL}	High	V _{IN} = 5.5V			40			
I _{OOLK}	Output current Leakage (82S152)	V _{CC} = max			40			μA
I _{O(OFF)}	Hi-Z state (82S153)	V _{OUT} = 5.5V			40			μA
I _{OS}	Short circuit (82S153) ^{4,6,7}	V _{OUT} = 5.5V			- 40			
I _{OS}		V _{OUT} = .45V			- 70			
I _{OS}		V _{OUT} = 0V			- 15			
I _{CC}	V _{CC} supply current ⁸	V _{CC} = max			130	155		mA
C _{IN}	Capacitance Input	V _{CC} = 5V			8			pF
C _B	I/O	V _{IN} = 2.0V			15			
		V _B = 2.0V						

AC ELECTRICAL CHARACTERISTICS

R_A = 470Ω, R₂ = 1kΩ

N82S152/153, N82S152A/153A: 0°C ≤ T_A ≤ +75°C, 4.75 ≤ V_{CC} ≤ 5.25V

S82S152/153, S82S152A/153A: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	TEST CONDITIONS	N82S152/153			S82S152/153			UNIT
				Min	Typ	Max	Min	Typ	Max	
T _{PD}	Propagation delay Output enable	Output ±	Input ±	C _L = 30pF	30	40	30	55	ns	
T _{OE}		Output ±	Input ±		25	35	25	45		
T _{OD}	Output disable ⁹	Output+	Input ±	C _L = 5pF	25	35	25	45	ns	
PARAMETER	TO	FROM	TEST CONDITIONS	N82S152A/153A			S82S152A/153A			UNIT
				Min	Typ	Max	Min	Typ	Max	
T _{PD}	Propagation delay Output enable	Output ±	Input ±	C _L = 30pF	20	30	20	45	ns	
T _{OE}		Output ±	Input ±		20	30	20	40		
T _{OD}	Output disable ⁹	Output+	Input ±	C _L = 5pF	20	30	20	40	ns	

Notes on following page.

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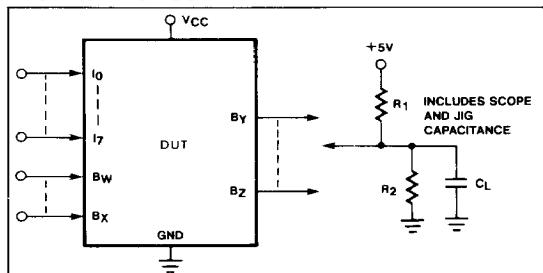
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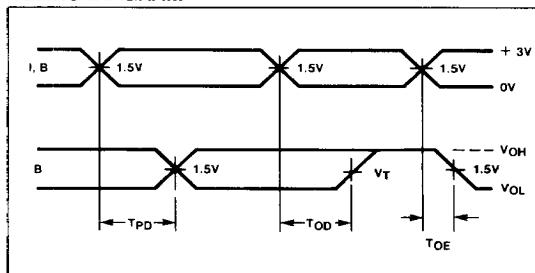
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device or these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with +10V applied to $I_{O,7}$.
6. Measured with +10V applied to $I_{O,7}$. Output sink current is supplied thru a resistor to V_{CC} .
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with $I_{O,7}$ and $B_{O,9}$ at 4.5V.
9. Measured at $V_T = V_{OL} + 0.5V$.

TEST LOAD CIRCUIT



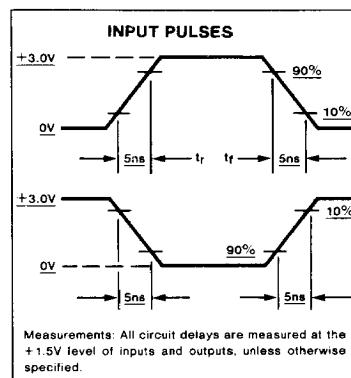
TIMING DIAGRAM



TIMING DEFINITIONS

- T_{PD} Propagation delay between input and output.
- T_{OD} Delay between input change and when output is off (Hi-Z or High).
- T_{OE} Delay between input change and when output reflects specified output level.

VOLTAGE WAVEFORM



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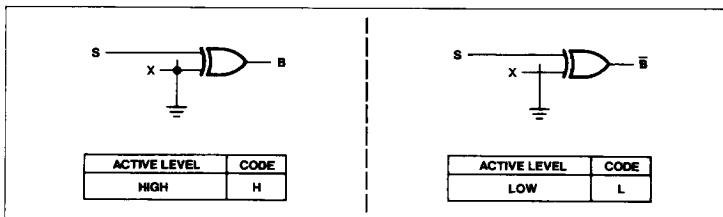
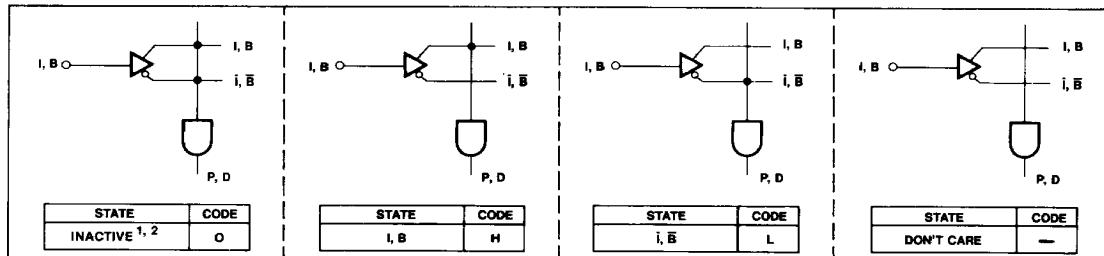
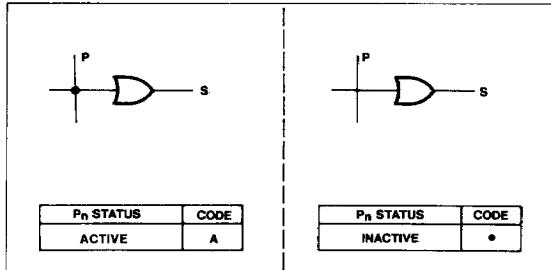
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LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this Table the logic state of variables I, P, and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY — (B)**"AND" ARRAY — (I, B)****"OR" ARRAY — (B)****NOTES**

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n, D_n .
2. Any gate P_n, D_n will be unconditionally inhibited if any one of its (I, B) link pairs is left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

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FPLA PROGRAM TABLE

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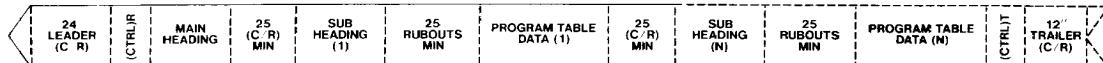
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TWX TAPE CODING (LOGIC FORMAT)

The FPLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar,

fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however, limit tape length to a roll of 1.75 inch inside diameter and 4.25 inch outside diameter.



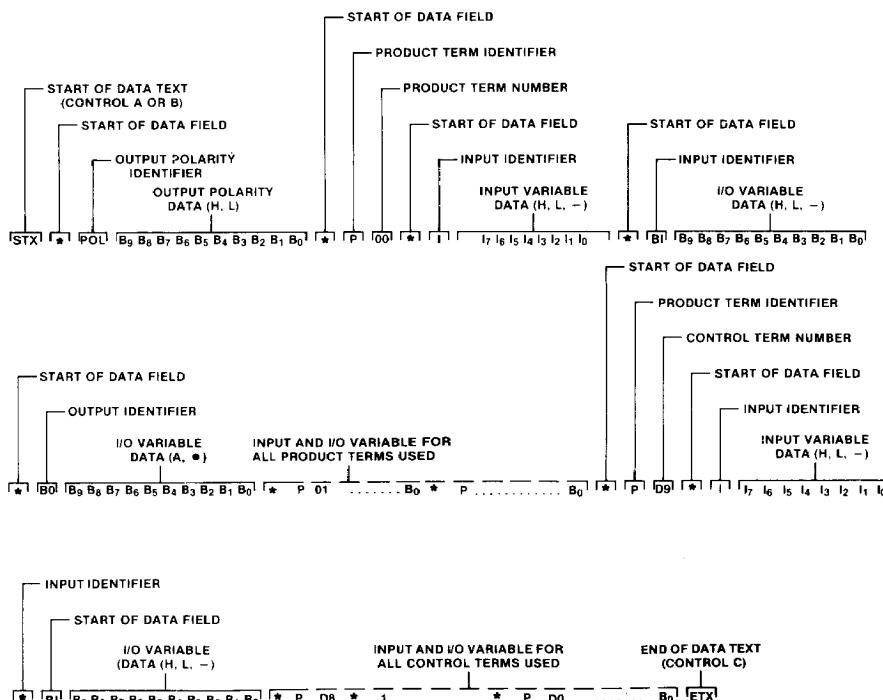
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a (\$) character, whether used or not:

1. Customer Name _____
4. Purchase Order No. _____
2. Customer TWX No. _____
5. Number of Program Tables _____
3. Date _____
6. Total Number of Parts _____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a (\$) character, whether used or not:

1. Signetics Device No. _____
4. Date _____
2. Program Table No. _____
5. Customer Symbolized Part No. _____
3. Revision _____
6. Number of Parts _____

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of output polarity, product term, and output information separated by appropriate identifiers in accordance with the following format. Entries for the data fields correspond to those defined in the Logic PROGRAM TABLE:



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