RC4200
Analog Multiplier

Features
- High accuracy
- Nonlinearity – 0.1%
  Temperature coefficient – 0.005%/°C
- Multiple functions
- Multiply, divide, square, square root, RMS-to-DC conversion, AGC and modulate/demodulate
- Wide bandwidth – 4 MHz
- Signal-to-noise ratio – 94 dB

Applications
- Low distortion audio modulation circuits
- Voltage-controlled active filters
- Precision oscillators

Description
The RC4200 analog multiplier has complete compensation for nonlinearity, the primary source of error and distortion. This multiplier also has three onboard operational amplifiers designed specifically for use in multiplier logging circuits. These amplifiers are frequency compensated for optimum AC response in a logging circuit, the heart of a multiplier, and can therefore provide superior AC response.

The RC4200 can be used in a wide variety of applications without sacrificing accuracy. Four-quadrant multiplication, two-quadrant division, square rooting, squaring and RMS conversion can all be easily implemented with predictable accuracy. The nonlinearity compensation is not just trimmed at a single temperature, it is designed to provide compensation over the full temperature range. This nonlinearity compensation combined with the low gain and offset drift inherent in a well-designed monolithic chip provides a very high accuracy and a low temperature coefficient.

Block Diagram
**Functional Description**

The RC4200 multiplier is designed to multiply two input currents ($I_1$ and $I_2$) and to divide by a third input current ($I_4$). The output is also in the form of a current ($I_3$). A simplified circuit diagram is shown in the Block Diagram. The nominal relationship between the three inputs and the output is:

$$I_3 = \frac{I_1 I_2}{I_4} \quad (1)$$

The three input currents must be positive and restricted to a range of 1 μA to 1 mA. These currents go into the multiplier chip at op amp summing junctions which are nominally at zero volts. Therefore, an input voltage can be easily converted to an input current by a series resistor. Any number of currents may be summed at the inputs. Depending on the application, the output current can be converted to a voltage by an external op amp or used directly. This capability of combining input currents and voltages in various combinations provides great versatility in application.

Inside the multiplier chip, the three op amps make the collector currents of transistors Q1, Q2 and Q4 equal to their respective input currents ($I_1$, $I_2$, and $I_4$). These op amps are designed with current source outputs and are phase-compensated for optimum frequency response as a multiplier. Power drain of the op amps was minimized to prevent the introduction of undesired thermal gradients on the chip. The three op amps operate on a single supply voltage (nominally -15V) and total quiescent current drain is less than 4 mA. These special op amps provide significantly improved performance in comparison to 741-type op amps.

The actual multiplication is done within the log-antilog configuration of the Q1-Q4 transistor array. These four transistors, with associated proprietary circuitry, were specially designed to precisely implement the relationship.

$$V_{BEN} = \frac{kT}{Q} \ln \frac{I_{C_N}}{I_{S_N}} \quad (2)$$

Previous multiplier designs have suffered from an additional undesired linear term in the above equation; the collector current times the emitter resistance. The $I_C r_E$ term introduces a parabolic nonlinearity even with matched transistors. Fairchild Semiconductor has developed a unique and proprietary means of inherently compensating for this undesired $I_C r_E$ term. Furthermore, this Fairchild Semiconductor developed circuit technique compensates linearity error over temperature changes. The nonlinearity versus temperature is significantly improved over earlier designs.

From equation (2) and by assuming equal transistor junction temperatures, summing base-to-emitter voltage drops around the transistor array yields:

$$\frac{K T}{q} \left[ \ln \frac{I_1}{I_{S_1}} - \ln \frac{I_2}{I_{S_2}} - \ln \frac{I_3}{I_{S_3}} + \ln \frac{I_4}{I_{S_4}} \right] = 0 \quad (3)$$

This equation reduces to:

$$\frac{I_1 I_2}{I_3 I_4} = \frac{I_{S_1} I_{S_2}}{I_{S_3} I_{S_4}} \quad (4)$$

The rate of reverse saturation current $I_{S_1} I_{S_2}/I_{S_3} I_{S_4}$, depends on the transistor matching. In a monolithic multiplier this matching is easily achieved and the rate is very close to unity, typically $1.0\pm1\%$. The final result is the desired relationship:

$$I_3 = \frac{I_1 I_2}{I_4} \quad (5)$$

The inherent linearity and gain stability combined with low cost and versatility makes this new circuit ideal for a wide range of nonlinear functions.

**Pin Assignments**

![Pin Assignments Diagram]

- $I_2$ (2)
- $V_{OS2}$
- $-V_S$ (3)
- $I_3$ (Output) (4)
- $I_1$ (8)
- $V_{OS1}$ (7)
- GND (6)
- $I_4$ (5)
Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage(^1)</td>
<td>-22</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Current</td>
<td>-5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>RM4200/4200A, 65°C, +150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RC4200/4200A, 65°C, 125°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>RM4200/4200A, 0°C, 70°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RC4200/4200A, 0°C, 117°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. For a supply voltage greater than -22V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics
(Still air, soldered into PC board)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>8-Lead Plastic DIP</th>
<th>8-Lead SOIC</th>
<th>8-Lead Ceramic DIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Junction Temperature</td>
<td>+125°C</td>
<td>+125°C</td>
<td>+175°C</td>
</tr>
<tr>
<td>Maximum PD TA &lt; 50°C</td>
<td>468mW</td>
<td>300mW</td>
<td>833mW</td>
</tr>
<tr>
<td>Thermal Resistance (\theta_{JC})</td>
<td>—</td>
<td>—</td>
<td>45°C/W</td>
</tr>
<tr>
<td>Thermal Resistance (\theta_{JA})</td>
<td>160°C/W</td>
<td>240°C/W</td>
<td>150°C/W</td>
</tr>
<tr>
<td>For TA &gt; 50°C Derate at</td>
<td>6.25mW/°C</td>
<td>4.17mW/°C</td>
<td>8.33mW/°C</td>
</tr>
</tbody>
</table>

Electrical Characteristics
(Over operating temperature range, \(V_S = -15V\) unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Test Conditions</th>
<th>4200A</th>
<th>4200</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Error as Multiplier</td>
<td>TA = +25°C</td>
<td>±2.0</td>
<td>±3.0</td>
</tr>
<tr>
<td></td>
<td>With External Trim</td>
<td>±0.2</td>
<td>±0.2</td>
</tr>
<tr>
<td></td>
<td>Versus Temperature</td>
<td>±0.005</td>
<td>±0.005</td>
</tr>
<tr>
<td></td>
<td>Versus Supply (-9 to -18V)</td>
<td>±0.1</td>
<td>±0.1</td>
</tr>
<tr>
<td>Nonlinearity(^2)</td>
<td>50μA ≤ I₁, I₂, I₄ ≤ 250 μA, TA = +25°C</td>
<td>±0.1</td>
<td>±0.3</td>
</tr>
<tr>
<td>Input Current Range (I₁, I₂ and I₄)</td>
<td></td>
<td>1.0</td>
<td>1000</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>I₁ = I₂ = I₄ = 150 μA, TA = +25°C</td>
<td>±5.0</td>
<td>±10</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>I₁ = I₂ = I₄ = 150 μA, TA = +25°C</td>
<td>300</td>
<td>500</td>
</tr>
<tr>
<td>Average Input Offset Voltage Drift</td>
<td>I₁ = I₂ = I₄ = 150 μA</td>
<td>±50</td>
<td>±100</td>
</tr>
<tr>
<td>Output Current Range (I₃)(^3)</td>
<td></td>
<td>1.0</td>
<td>1000</td>
</tr>
</tbody>
</table>
Electrical Characteristics (continued)
(Over operating temperature range, $V_S = -15V$ unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Test Conditions</th>
<th>4200A</th>
<th>4200</th>
</tr>
</thead>
</table>
| Frequency Response,         | -3dB point                        | -18  | 4.0  | -9.0 | -18  | 4.0  | -9.0 | MHz   
| Supply Voltage              |                                  |      |      |      |      |      |      | V     |
| Supply Current              | $I_1 = I_2 = I_4 = 150 \mu A$    | 4.0  |      |      | 4.0  |      |      | mA    |
| $TA = +25^\circ C$          |                                  |      |      |      |      |      |      |       |

Notes:
1. Refer to Figure 6 for example.
2. The input circuits tend to become unstable at $I_1, I_2, I_4 < 50 \mu A$ and linearity decreases when $I_1, I_2, I_4 > 250 \mu A$ (eq. @ $I_1 = I_2 = 500 \mu A$, nonlinearity error = 0.5%).
3. These specifications apply with output ($I_3$) connected to an op amp summing junction. If desired, the output ($I_3$) at pin (4) can be used to drive a resistive load directly. The resistive load should be less than 700$\Omega$ and must be pulled up to a positive supply such that the voltage on pin (4) stays within a range of 0 to +5V.

Applications Discussion

Current Multiplier/Divider
The basic design criteria for all circuit configurations using the RC4200 multiplier is contained in equation (1), that is,

$$I_3 = \frac{I_1 I_2}{I_4}$$

The current-product-balance equation restates this as:

$$I_1 I_2 = I_3 I_4 \quad (6)$$

![Figure 1. Current Multiplier/Divider](image1)

Dynamic Range and Stability

The precision dynamic range for the RC4200 is from +50 $\mu A$ to +250 $\mu A$ inputs for $I_1, I_2$ and $I_4$. Stability and accuracy degrade if this range is exceeded.

To improve the stability for input currents less than 50 $\mu A$, filter circuits ($R_S C_S$) are added to each input (see Figure 2).

![Figure 2. Current Multiplier/Divider with Filters](image2)

Amplifier A1 is used to convert the $I_3$ current to an output voltage.

Multiplier: $V_z =$ constant $\neq 0$
Divider: $V_y =$ constant $\neq 0$
**Voltage Multiplier/Divider**

\[
\begin{align*}
\text{Resistors } R_a \text{ and } R_b & \text{ extend the range of the } V_X \text{ and } V_Y \\
\text{inputs by picking values such that: } & \\
I_1(\text{min.}) = \frac{V_X(\text{min.})}{R_1} + \frac{V_{\text{REF}}}{R_a} = 50 \mu A, \\
I_1(\text{max.}) = \frac{V_X(\text{max.})}{R_1} + \frac{V_{\text{REF}}}{R_a} = 250 \mu A, \\
I_2(\text{min.}) = \frac{V_Y(\text{min.})}{R_2} + \frac{V_{\text{REF}}}{R_b} = 50 \mu A, \\
I_2(\text{max.}) = \frac{V_Y(\text{max.})}{R_2} + \frac{V_{\text{REF}}}{R_b} = 250 \mu A.
\end{align*}
\]

Resistor \( R_C \) supplies bias current for \( I_3 \) which allows the output to go negative.

Resistors \( R_{CX} \) and \( R_{CY} \) permit equation (6) to balance, ie.:

\[
\begin{align*}
\frac{V_X}{V_{\text{REF}}} + \frac{V_Y}{V_{\text{REF}}} &= \left( \frac{V_0}{V_{\text{REF}}} \right) + \frac{V_X}{R_{CX}} + \frac{V_Y}{R_{CY}}
\end{align*}
\]

**Extended Range Multiplier**

The input and output voltage ranges can be extended to include 0 and negative voltage signals by adding bias currents. The \( R_{SCS} \) filter circuits are eliminated when the input and biasing resistors are selected to limit the respective currents to 50 \( \mu A \) min. and 250 \( \mu A \) max.

**Extended Range**

The input and output voltage ranges can be extended to include 0 and negative voltage signals by adding bias currents. The \( R_{SCS} \) filter circuits are eliminated when the input and biasing resistors are selected to limit the respective currents to 50 \( \mu A \) min. and 250 \( \mu A \) max.

\[
\begin{align*}
\frac{V_X V_Y}{R_1 R_2} &= \frac{V_0 V_{\text{REF}}}{R_0 R_4} \\
V_0 &= \frac{V_X V_Y}{V_Z} \text{ where } K = \frac{R_0 R_4}{R_1 R_2}
\end{align*}
\]

**Cross-Product Cancellation**

Cross-products are a result of the \( V_X V_R \) and \( V_Y V_R \) terms. To the extend that \( R_1 R_2 = R_{CX} R_D \), and \( R_2 R_1 = R_{CY} R_D \) cross-product cancellation will occur.

**Arithmetic Offset Cancellation**

The offset caused by the \( V_{\text{REF}}^2 \) term will cancel to the extent that \( R_0 R_b = R_0 R_d \), and the result is:

\[
\begin{align*}
\frac{V_Y V_X}{R_1 R_2} &= \frac{V_0 V_{\text{REF}}}{R_0 R_d} \text{ or } V_0 = \frac{V_X V_Y}{K}
\end{align*}
\]

where \( K = \frac{R_0 R_d}{V_{\text{REF}}^2 R_1 R_2} \)

**Resistor Values**

Inputs:

\[
\begin{align*}
V_X(\text{min.}) & \leq V_X(\text{max.}) \\
A V_X &= V_X(\text{max.}) - V_X(\text{min.}) \\
V_Y(\text{min.}) & \leq V_Y(\text{max.}) \\
A V_Y &= V_Y(\text{max.}) - V_Y(\text{min.}) \\
V_{\text{REF}} &= \text{Constant (+7V to +18V)} \\
K &= \frac{V_0}{V_X V_Y}(\text{Design Requirements})
\end{align*}
\]
Procedure

1. Set all trimmer pots to 0V on the wiper.
2. Connect Vx input to ground. Put in a full scale square wave on Vy input. Adjust X OS (R5) for no square wave on V0 output (adjust for 0 feedthrough).
3. Connect Vy input to ground. Put in a full scale square wave on Vx input. Adjust Y OS (R9) for no square wave on V0 output (adjust for 0 feedthrough).
4. Connect VX and VY to ground. Adjust V OS (R16) for 0V on V0 output.

Multiplying Circuit Offset Adjust

\[ R_1 = \frac{\Delta V_X}{200 \mu A}, \quad R_2 = \frac{\Delta V_Y}{200 \mu A}, \quad R_d = \frac{V_{REF}}{250 \mu A} \]

\[ R_a = \frac{\Delta V_X V_{REF}}{250 \mu A \Delta V_X - 200 \mu A V_x^{(max.)}} \]

\[ R_b = \frac{\Delta V_Y V_{REF}}{250 \mu A \Delta V_Y - 200 \mu A V_y^{(max.)}} \]

\[ R_c = \frac{R_a R_b}{R_d}, \quad R_{cx} = \frac{R_1 R_b}{R_d}, \quad R_{cy} = \frac{R_2 R_a}{R_d} \]

\[ R_0 = \frac{\Delta V_X \Delta V_Y K}{160 \mu A} \]
Extended Range Divider

As with the extended range multiplier, resistors $R_{az}$ and $R_{ao}$ are added to cancel the cross-product error caused by the biasing resistors, i.e.,

\[
\frac{V_X}{R_1} \frac{V_0}{R_{ao}} + \frac{V_Z}{R_{az}} = \frac{V_{REF}}{R_a} + \frac{V_{REF}}{R_b} = \frac{V_{REF}}{R_c} + \frac{V_{REF}}{R_d}
\]

\[
\frac{V_{XREF}}{R_1 R_b} + \frac{V_{ZREF}}{R_{az} R_b} + \frac{V_{ZREF}}{R_{ao} R_b} = \frac{V_{XREF}}{R_c R_d} + \frac{V_{ZREF}}{R_{az} R_d} + \frac{V_{ZREF}}{R_{ao} R_d}
\]

To cancel cross-product and arithmetic offset:

$R_{ao}R_b = R_0R_d, R_{az}R_b = R_dR_c \text{ and } R_aR_b = R_cR_d$

and the result is:

\[
\frac{V_X V_{REF}}{R_1 R_b} = \frac{V_0 V_{REF}}{R_0 R_4} \text{ or } V_0 = \frac{V_X}{V_Z K}
\]

where $K = \frac{V_{REF} R_0 R_4}{R_1 R_b}$

Notice that it is necessary to match the above resistor cross-products to within the amount of error tolerable in the output offset, i.e., with a 10V F.S. output, 0.1% resistor cross-product match will give 0.1% x 10V untrimmable output voltage.

**Resistor Values**

**Inputs:**

$V_X(\text{min.}) \leq V_X \leq V_X(\text{max.})$

$\Delta V_X = V_X(\text{max.}) - V_X(\text{min.})$

$V_Z(\text{min.}) \leq V_Z \leq V_Z(\text{max.})$

$\Delta V_Z = V_Z(\text{max.}) - V_Z(\text{min.})$

$V_{REF} = \text{Constant (+7V to +18V)}$

**Outputs:**

$V_0(\text{min.}) \leq V_0 \leq V_0(\text{max.})$

$\Delta V_0 = V_0(\text{max.}) - V_0(\text{min.})$

$K = \frac{V_0 V_Z}{V_X} (\text{Design Requirement})$

\[
R_0 = \frac{\Delta V_0}{750 \mu A}, \ R_b = \frac{\Delta V_{REF}}{250 \mu A}, \ R_4 = \frac{\Delta V_Z}{200 \mu A}
\]

\[
R_c = \frac{\Delta V_X V_{REF}}{750 \mu A \Delta V_0 - 700 \mu A V_0(\text{max.})}
\]

\[
R_d = \frac{\Delta V_Z V_{REF}}{250 \mu A \Delta V_Z - 200 \mu A V_Z(\text{max.})}
\]

\[
R_a = \frac{R_c R_d}{R_b}, \ R_{az} = \frac{R_c R_4}{R_b}, \ R_{ao} = \frac{R_0 R_d}{R_b}
\]

\[
R_1 = \frac{\Delta V_0 \Delta V_Z}{600 \mu A K}
\]
Divider Circuit with Offset Adjustment

**General**
- $10K \leq R_5 = R_{13} = R_{17} \leq 50K$
- $R_7 + R_8 = R_1 || R_a || R_z || R_{ao}$
- $R_6 = R_7 (V_S/0.05)$
- $R_9 = R_b$
- $R_{10} = 100 \times R_4$
- $R_{11} = 20K$
- $R_{12} = 100K$
- $R_{14} + R_{15} = R_9 || R_c$
- $R_{16} = R_{15} (V_S/0.10)$

**Example: Two-Quad Divider**
- $V_0 = K(V_x/V_Z), K = k, V_{REF} = +V_S = +15V$
- $-10 \leq V_x \leq +10$, therefore $\Delta V_x = 20$
- $0 \leq V_z \leq +10$, therefore $\Delta V_Z = 20$
- $-10 \leq V_0 \leq +10$, therefore $\Delta V_0 = 20$
- $R_0 = 26.7K$
- $R_6 = 60K$
- $R_4 = 50K$
- $R_c = 37.5K$
- $R_d = 300K$
- $R_a = 187.5K$
- $R_{az} = 31.25$
- $R_{ao} = 133K$

**Figure 7. Divider Circuit with Offset Adjustment**
Divider Circuit Offset Adjustment Procedure

1. Set each trimmer pot to 0V on the wiper.

2. Connect VX (input) to ground. Put a DC voltage of approximately 1/2 VZ (max.) DC on the VZ (input) with an AC (squarewave is easiest) voltage of 1/2 VZ (max.) peak-to-peak superimposed on it. Adjust XOS (R5) for zero feedthrough. (No AC at V0)

\[
V_Z \text{(Max.)} \quad - \quad - \quad - \quad - \quad - \\
\frac{1}{2} V_Z \text{(Max.)} \quad - \quad - \quad - \quad - \quad - \\
0V \quad - \quad - \quad - \quad - \quad -
\]

3. Connect VX (input) to VZ (input) and put in the 1/2 VZ(max.) DC with an AC of approximately 20 mV less than VZ(max.).

Adjust ZOS (R13) for zero feedthrough.

\[
V_Z \text{(Max.)} \quad - \quad - \quad - \quad - \quad - \\
\frac{1}{2} V_Z \text{(Max.)} \quad - \quad - \quad - \quad - \quad - \\
0V \quad - \quad - \quad - \quad - \quad -
\]

\[
\approx 10 \text{ mV}
\]

4. Return VX (Input) to ground and connect VZ(max.) DC on VZ(input). Adjust output VO(V17) for VO = 0V

5. Connect VX (input) to VZ (input) and and in VZ (max.) DC. (The output will equal K.) Decrease the input slowly until the output (V0 - K) deviates beyond the desired accuracy. Adjust ZOS to bring it back into tolerance and return to Step 4. Continue steps 4 and 5 until VZ reduces to the lowest value desired.

Notice that as the input to VX and VZ gets closer to zero (an illegal state) the system noise will predominate so much that an integrating voltmeter will be very helpful.

Square Root Circuit \( V_0 = N \sqrt{V_X} \)

\[
V_X V_{\text{REF}} R_{1} R_{b} + V_{\text{REF}} R_{a} R_{b} + V_{0} V_{\text{REF}} R_{b} R_{d} + V_{0} V_{\text{REF}} R_{a} R_{d} + V_{\text{REF}} R_{b} R_{c} = R_{c} R_{d} R_{0} R_{4}
\]

If \( R_{a} R_{b} R_{c} R_{d} \) and \( R_{a} R_{b} R_{d} R_{0} R_{4} = R_{c} R_{d} R_{0} R_{4} \)

Then

\[
\frac{V_0^2}{R_d R_4} = \frac{V_X V_{\text{REF}}}{R_1 R_b} \quad \text{or} \quad V_0^2 = V_X K \quad \text{where} \quad K = \frac{V_{\text{REF}} R_0 R_4}{R_1 R_b}
\]

and \( V_0 = N \sqrt{V_X} \) where \( N = \sqrt{K} \)

\( 0 \leq V_X \leq V_X \text{(max.)} \) and \( V_0 \text{(max.)} = N \sqrt{V_X \text{(max.)}} \)

\[
\begin{align*}
N &= \frac{V_0}{\sqrt{V_X}} \quad \text{(Design Requirements)} \\
R_1 &= \frac{V_0 \text{(max.)}^2}{74 \mu A N^2} \\
R_a &= R_d = \frac{V_{\text{REF}}}{50 \mu A} \\
R_b &= R_c = \frac{V_{\text{REF}}}{150 \mu A} \\
R_4 &= \frac{V_0 \text{(max.)}}{50 \mu A} \\
R_{ao} &= \frac{V_0 \text{(max.)}}{125 \mu A} \\
R_0 &= \frac{V_0 \text{(max.)}}{255 \mu A}
\end{align*}
\]

Figure 8.
Square Root Circuit Offset Adjust

R14-R17 can be used in place of R9 to help reduce linearity error due to resistor product mis-match (See Appendix 1).

10K ≤ \( R_5 \) = \( R_{13} \) ≤ 50K
\[ R_7 = 100\Omega \]
\[ R_6 = R_7 \frac{V_S}{0.05} \]
\[ R_S = R_1 || R_s || R_{ao} \]
\[ R_o = R_b \]
\[ R_{10} = R_0 || R_C \]
\[ R_{11} = 100\Omega \]
\[ R_{12} = R_{11} \frac{V_S}{0.1} \]

Procedure

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale (0 to \( V_X \)(max.) squarewave on \( V_X \) input. Adjust \( V_{OS}(R5) \) for proper peak-to-peak amplitude on \( V_0 \) output. (Scaling adjust)
3. Connect \( V_X \) input to ground. Adjust \( V_{OS}(R13) \) for 0V on \( V_0 \) output.
Squaring Circuits $V_0 = K V_X^2$

![Figure 10. Squaring Circuit](image-url)

\[
\frac{V_X^2}{R_1^2} + \frac{2V_XV_{\text{REF}}}{R_1R_a} + \frac{V_{\text{REF}}^2}{R_a^2} = \frac{V_0V_{\text{REF}}}{R_0R_d} + \frac{V_{\text{REF}}^2}{R_cR_d} + \frac{V_XV_{\text{REF}}}{R_cR_d}
\]

If $R_a^2 = R_cR_d$ and $R_1R_a = 2R_{CX}R_D$,

then \( \frac{V_0V_{\text{REF}}}{R_0R_d} = \frac{V_X^2}{R_1^2} \) or \( V_0 = KV_X^2 \) where \( K = \frac{R_0R_d}{V_{\text{REF}}R_1^2} \).

\( V_X(\text{min.}) \leq V_X \leq V_X(\text{max.}) \) \( \Delta V_X = V_X(\text{max.}) - V_X(\text{min.}) \)

\( K = \frac{V_0}{V_X^2} \) (Design Requirement)

\( R_1 = \frac{\Delta V_X}{200\mu A} \)

\( R_a = \frac{\Delta V_XV_{\text{REF}}}{250\mu A\Delta V_X - 200\mu A V_X(\text{max.})} \)

\( R_d = \frac{V_{\text{REF}}}{250\mu A} \)

\( R_c = \frac{R_a^2}{R_d} \)

\( R_{CX} = \frac{R_1R_a}{2R_d} \)

\( R_0 = \frac{\Delta V_X^2K}{160\mu A} \)
Squaring Circuits Offset Adjust

![Squaring Circuit Diagram](image)

**Figure 11. Squaring Circuit Offset Adjust**

\[10K \leq R_{10} = R_{11} \leq 50K\]

\[R_8, R_{15} = 100\Omega\]

\[R_9, R_{14} = 100\Omega \frac{V_S}{0.1}\]

\[R_5, R_6 = R_1 \parallel R_a\]

\[R_{16} = R_0 \parallel R_c \parallel R_a\]

**Procedure**

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale (±VX) squarewave on VX input. Adjust ZOS(R10) for uniform output.
3. Connect VX input to ground. Adjust VOS(R11) for 0V on V0 outputs.
Appendix 1—System Errors

There are four types of accuracy errors which affect overall system performance. They are:

- **Nonlinearity**—Incremental deviation from absolute accuracy. See Note 1.
- **Scaling Error**—Linear deviation from absolute accuracy.
- **Output Offset**—Constant deviation from absolute accuracy.
- **Feedthrough**—Cross-product errors caused by input offsets and external circuit limitations. See Note 2.

This nonlinearity error in the transfer function of the RC4200 is $\pm 0.1\%$ maximum ($\pm 0.03\%$ maximum for the RC4200A). That is,

$$I_3 = \frac{I_1 I_2}{I_4} \pm 0.1\% \text{ F.S.}^{(4)}$$

The other system errors are caused by voltage offsets on the inputs of the RC4200 and can be as high as $\pm 3.0\%$ ($\pm 2.0\%$ for RC4200A).

$$V_0 = \frac{V_X V_Y}{V_Z} \frac{R_0 R_4}{R_1 R_2} \pm 3.0\% \text{ F.S.}^{(3)(4)}$$

**Notes:**

1. The input circuits tend to become unstable at $I_1, I_2, I_4 < 50 \mu A$ and linearity decreases when $I_1, I_2, I_4 > 250 \mu A$ (e.g., $I_1 = I_2 = 500 \mu A$, nonlinearity error $= 0.5\%$).
2. This section will not deal with feedthrough which is proportional to frequency of operation and caused by stray capacitance and/or bandwidth limitations. (Refer to Figure 12.)
3. Not including resistor tolerance or output offset on the operational amplifier.
4. For $50 \mu A \leq I_1, I_2, I_4 \leq 250 \mu A$.

**Errors Caused by Input Offsets**

$$V_0 = \frac{V_X V_Y}{V_Z} \frac{R_0 R_4}{R_1 R_2} \pm 0.1\% \text{ F.S.}^{(4)}$$

System errors can be greatly reduced by externally trimming the input offset voltages of the RC4200. ($\pm 3.0\%$ F.S. for RC4200 and $\pm 0.1\%$ for RC4200A.)

**Extended Range Circuit Errors**

The extended range configurations have a disadvantage in that additional accuracy errors may be introduced by resistor product mismatching.

**Multiplier**

An error in resistor product matching will cause an equivalent feedthrough or output offset error. See Figure 6.

$$R_1 R_4 = R_{CX} R_{O} \pm \alpha, \ V_{XF} \text{ feedthrough (} V_Y = 0) = 1 \alpha V_X$$
$$R_2 R_4 = R_{CY} R_{O} \pm \beta, \ V_{YF} \text{ feedthrough (} V_X = 0) = \pm \beta V_Y$$
$$R_4 R_0 = R_{CD} \pm \gamma, \ V_0 \text{ offset (} V_X = V_Y = 0) = \pm \gamma V_{\text{REF}*}$$

**Note:**

* Output offset errors can always be trimmed out with the output op amp offset adjust, VOS (R16).
Reducing Mismatch Errors
You need not use 0.01% resistors to reduce resistor product mismatch errors. Here are a couple of ways to obtain maximum accuracy out of the extended range multiplier (see Figure 4) using 1% resistors.

Method 1
VX feedthrough, for example, occurs when VY = 0 and VOSY ≠ 0. This VX feedthrough will equal ±VXVOSY. Also, if VOSZ ≠ 0, there is a VX feedthrough equal to VXVOSZ. A resistor-product error of α will cause a VX feedthrough of ±αVX. Likewise, VY feedthrough errors are: ±VYVOSX, ±VYVOSZ and ±βVY.

Total feedthrough:
±VXVOSY ±VYVOSX ±αVX ±βVY ±(VX + VY)VOSZ

By carefully abusing XOS(R5), YOS(R9) and ZOS(R20) this equation can be made to very nearly equal zero and the feedthrough error will practically disappear.

A residual of set will probably remain which can be trimmed out with VOS(R16) at the output of amp.

Method 2
Notice that the ratios of R1Rb:RCXRd and R2Ra:RCYRd are both dependent of Rd also that R1, R2, Ra and Rb are all functions of the maximum input requirements. By designing a multiplier for the same input ranges on both VX and VY then R1 = R2, RCX = RCY and Ra = Rb. (Note: it is acceptable to design a four quadrant multiplier and use only two quadrants of it.)

Select Rd to be 1% or 2% below (or above) the calculated value. This will cause α and β to both be positive (or negative) by nearly the same amount. Now the effective value of Rd can be trimmed with an offset adjustment ZOS(R20) on pin 5.

This technique causes: a slight gain error which can be compensated with the R0 value, and an output of offset error that can be trimmed with VOS(R16) on the output op amp.

Extended Range Divider
The only cross-product error of interest is the VZ feedthrough (VX = 0 and VOSX ≠ 0) which is easily adjusted with XOS(R5). See Figure 6.

Resistor product mismatch will cause scaling errors (gain) that could be a problem for very low values of VZ. Adjustments to YOS(R18) can be made to improve the high gain accuracy.

Square Root and Squaring
These circuits are functions of single variables so feedthrough, as such, is not a consideration. Cross product errors will effect incremental accuracy that can be corrected YOS(R14) or ZOS(R10). See Figure 9 and Figure 11.
Appendix 2—Applications

Design Considerations for RMS-to-DC Circuits

Average Value

Consider \( V_{\text{IN}} = A \sin \omega t \). By definition,

\[
V_{AVG} = \frac{1}{T} \int_0^T V_{\text{IN}} \, dt
\]

Where \( T = \text{Period} \)

\[
\omega = 2\pi f = \frac{2\pi}{T}
\]

\[
V_{AVG} = \frac{2}{T} \int_0^T A \sin \omega t \, dt
\]

\[
= \frac{2A}{T} \left[ \frac{1}{\omega} \cos \omega t \right]_0^T
\]

\[
= \frac{2A}{2\pi} [ -\cos(\pi) + \cos(0) ]
\]

Average Value of \( A \sin \omega t \) is \( \frac{2A}{\pi} \)

RMS Value

Again, consider \( V_{\text{IN}} = A \sin \omega t \)

\[
V_{\text{rms}} = \sqrt{V_{AVG}} = \sqrt{\frac{1}{T} \int_0^T |V_{\text{IN}}|^2 \, dt}
\]

\[
V_{\text{rms}} \text{ for } A \sin \omega t \text{dt:}
\]

\[
V_{\text{rms}} = \sqrt{\frac{1}{T} \int_0^T A^2 \sin^2 \omega t \, dt}
\]

\[
= \sqrt{\frac{A^2}{T} \left[ \frac{T}{2} - \frac{1}{2} \cos 2\omega t \right]_0^T}
\]

\[
= \sqrt{\frac{A^2}{2} \left[ \frac{T}{2} - \frac{1}{4\omega} \sin 2\omega t \right]_0^T}
\]

\[
= \sqrt{\frac{A^2}{2}}
\]

Therefore, the rms value of \( A \sin \omega t \) becomes:

\[
V_{\text{rms}} = \frac{A}{\sqrt{2}}
\]

RMS Value for Rectified Sine Waves

Consider \( V_{\text{IN}} = |A \sin \omega t| \), a rectified wave. To solve, integrate of each half cycle.

i.e. \( \frac{1}{T} \int_0^T V_{\text{IN}}^2 \, dt = \)

\[
\frac{1}{T} \int_0^T A^2 \sin^2 \omega t \, dt + \frac{T}{2} (-A \sin \omega t)^2 \, dt
\]

This is the same as \( \frac{1}{T} \int_0^T A^2 \sin^2 \omega t \, dt \)

so, \( |A \sin \omega t|_{\text{rms}} = A \sin \omega t_{\text{rms}} \)

Practical Consideration: \( |A \sin \omega t| \) has high-order harmonics; \( A \sin \omega t \) does not. Therefore, non-ideal integrators may cause different errors for two approaches.

![Figure 14](image-url)
Amplitude Modulator with A.G.C.

In many AC modulator applications, unwanted output modulation is caused by variations in carrier input amplitude. The versatility of the RC4200 multiplier can be utilized to eliminate this undesired fluctuation. The extended range multiplier circuit (Figure 4) shows an output amplitude inversely proportional to the reference voltage VREF.

\[ V_0 = \frac{V_X V_Y}{V_{REF}} \frac{R_0 R_d}{R_1 R_2} \]

By making VREF proportional to VY (where VY is the carrier input) such that:

\[ V_{REF} = V_H = \int |V_Y| \]

Then the denominator becomes a variable value that automatically provides constant gain, such that the modulating input (VX) modulates the carrier (VY) with a fixed scale factor even though the carrier varies in amplitude.

If VH is made proportional to the average value of Asinot (i.e., 2A/π) and scaled by a value of π/2 then:

\[ V_H = A \]

and if: VX = Modulating input (VM)
and: VY Carrier input (Asinot)

Then: V0 = K VM sinot  where K = \[ R_0 R_d \frac{R_1}{R_2} \]

The resistor scaling is determined by the dynamic range of the carrier variation and modulating input.

The resistor values are solved, as with the other extended range circuits, in terms of the input voltages.

Input voltages:
- Modulation voltage (VM): 0 ≤ VM ≤ VX(max.)
- Carrier (VY): VY = Asinot
- Carrier amplitude fluctuation (ΔA):
  - A(min.) sint ≤ VY ≤ A(max.) sinωt
- Dynamic Range (N): A(max.)/A(min.), A(max.) = VH(max.) and A(min.) = VH(min.)
The maximum and minimum values for $I_1$ and $I_2$ lead to:

$I_1(\text{max.}) = \frac{V_X(\text{max.})}{R_1} + \frac{V_H(\text{max.})}{R_a} = 250\,\mu\text{A}$

$I_1(\text{min.}) = \frac{V_H(\text{min.})}{R_a} = 50\,\mu\text{A} \quad V_M(\text{min.}) = 0$

$I_2(\text{max.}) = \frac{A(\text{max.})}{R_2} + \frac{V_H(\text{max.})}{R_a} = 250\,\mu\text{A}$

$I_2(\text{min.}) = \frac{V_H(\text{min.})}{R_a} = 50\,\mu\text{A}$

For a dynamic range of $N$, where

$N = \frac{A(\text{max.})}{A(\text{min.})} < 5$,

These equations combine to yield:

$R_1 = \frac{V_X(\text{max.})}{(5-N)50\,\mu\text{A}}$, $R_2 = \frac{A(\text{max.})}{(5-N)50\,\mu\text{A}}$,

$R_a = \frac{A(\text{min.})}{50\,\mu\text{A}}$ and $R_O = K \frac{R_1 R_2}{R_a}$.

**Example 1**

$V_Y = Asin\omega t$, $2.5\,\text{V} \leq A \leq 10\,\text{V}$, therefore $N = 4$

$0\,\text{V} \leq V_M \leq 10\,\text{V}$, therefore $V_X(\text{max.}) = 10\,\text{V}$

$K = 1$, therefore $V_0 = V_M \sin\omega t$

$R_1 = \frac{V_X(\text{max.})}{50\,\mu\text{A}} = \frac{10\,\text{V}}{50\,\mu\text{A}} = 200\,\text{K}$

$R_1 = \frac{A(\text{max.})}{50\,\mu\text{A}} = \frac{10\,\text{V}}{50\,\mu\text{A}} = 200\,\text{K}$

$R_a = \frac{A(\text{min.})}{50\,\mu\text{A}} = \frac{2.5\,\text{V}}{50\,\mu\text{A}} = 50\,\text{K}$

$R_O = K \frac{R_1 R_2}{R_a} = 1 \frac{200\,\text{K} \times 200\,\text{K}}{50\,\text{K}} = 800\,\text{K}$

**Example 2**

$V_Y = Asin\omega t$, $3 \leq A \leq 6$, therefore $N = 2$

$0\,\text{V} \leq V_M \leq 8\,\text{V}$, therefore $V_X(\text{max.}) = 8\,\text{V}$

$K = 0.2$, therefore $V_0 = 0.2 \, V_M \sin\omega t$

so:

$R_1 = 53.3\,\text{K}$, $R_2 = 40\,\text{K}$

$R_a = 60\,\text{K}$ and $R_O = 7.11\,\text{K}$
Limited Range, First Quadrant Applications

The following circuit has the advantage that cross-product errors are due only to input offsets and nonlinearity error is sightly less for lower input currents.

The circuit also has no standby current to add to the noise content, although the signal-to-noise ratio worsens at very low input currents (1-5 \mu A) due to the noise current of the input stages.

The \( R_sC_s \) filter circuits are added to each input to improve the stability for input currents below 50 \mu A.

Caution!

The bandpass drops off significantly for lower currents (<50 \mu A) and non-symmetrical rise and fall times can cause second harmonic distortion.

Thermal Symmetry

The scale factor is sensitive to temperature gradients across the chip in the lateral direction. Where possible, the package should be oriented such that forces generating temperature gradients are located physically on the line of thermal symmetry. This will minimize scale-factor error due to thermal gradients.
Figure 18. Outputs
Figure 19a. Output Noise Current ($I_3$) vs. Input Currents ($I_1, I_2$) for $I_4 = 250 \mu A$

Figure 19b. Output Noise Current ($I_3$) vs. Input Currents ($I_4, I_1$) for $I_2 = 250 \mu A$

Figure 20. AC Feedthrough vs. Frequency
Mechanical Dimensions

8-Lead SOIC Package

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Inches</th>
<th>Millimeters</th>
<th>Notes</th>
</tr>
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Notes:
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.
## Mechanical Dimensions (continued)

### 8-Lead Plastic DIP Package

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**Notes:**

2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.
Mechanical Dimensions (continued)

8-Lead Ceramic DIP Package

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Notes:
1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
## Ordering Information

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<th>Part Number</th>
<th>Package</th>
<th>Operating Temperature Range</th>
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**Note:**

/883B suffix denotes MIL-STD-883, Level B processing

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.