SP8607

600MHz ÷ 2

The SP8607 is an emitter coupled logic divider which features ECL 10K compatible outputs when used with external pulldown resistors. The inputs are AC coupled.

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 80mW
- Temperature Range:
 - -55°C to +125°C (A Grade)
 - -30°C to +70°C (B Grade)

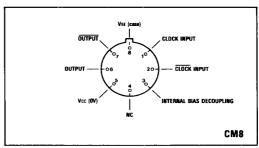


Fig.1 Pin connections - bottom view

ABSOLUTE MAXIMUM RATINGS

Supply voltage
Output current
10mA
Storage temperature range
Max. junction temperature
Max. clock I/P voltage
-8V
-55°C to +150°C
+175°C
4175°C
2.5V p-p

ORDERING INFORMATION

SP8607 A CM √ SP8607 B CM √ SP8607 AB CM √ SP8607 AC CM

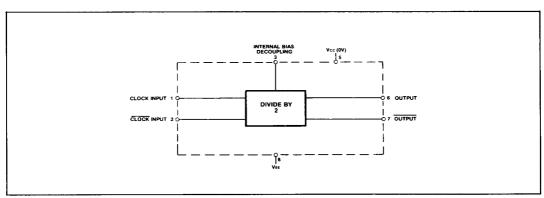


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 0.25V$ Temperature: Tamb A Grade = -55°C to +125°C B Grade = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.	Units	Conditions	Notes
Maximum frequency (sinewave input)	fmax	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	fmin		40	MHz	Input = 400-800mV p-p	
Power supply current	lee		18	mA	VEE = -5.2V	
					Outputs unloaded	
Output low voltage	Vol	-1.8	-1.4	V	VEE = -5.2V	Note 4
Output high voltage	Vон	-0.85	-0.7	V	VEE = -5.2V	Note 4
Minimum output swing	Vоит	400	1	m∨	VEE = -5.2V	

NOTES

- Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range. The temperature coefficients of $V_{OH} = +1.63 \text{mV/}^{\circ}\text{C}$ and $V_{OL} = +0.34 \text{mV/}^{\circ}\text{C}$ but these are not tested.
- The test configuration for dynamic testing is shown in Fig.5. 3.
- 4. Tested at 25°C only.

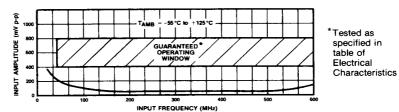


Fig.3 Typical characteristic of SP8607A

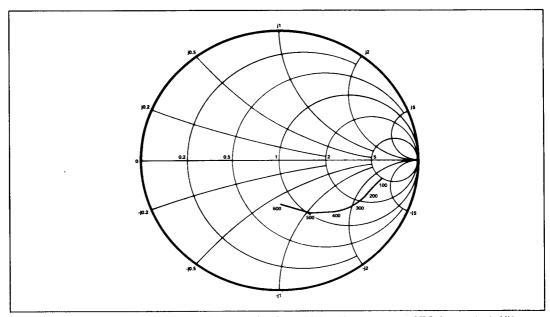


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

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OPERATING NOTES

- The clock inputs (pins 1 and 2) can be driven singleended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 3, to ground.
- 2. In the absence of a signal the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the unused input to VEE (ie pin 1 or 2 to pin 8). This causes a drop in sensitivity of about 100mV.
- 3. The circuit will operate down to DC but slew rate must be better than $100V/\mu s$.
- 4. The outputs are compatible with ECL II. There is an internal load of 4k on each output. The outputs can be interfaced to ECL 10K by addition of a pulldown resistor of 1.5k to the outputs to increase the output voltage swing.
- 5. Input impedance is a function of frequency. See Fig. 4.
- 6. All components should be suitable for the frequency in use.

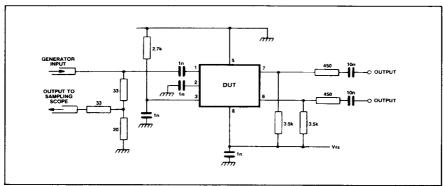


Fig.5 Test circuit

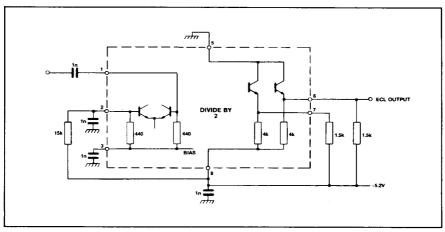


Fig.6 Typical application showing interfacing