TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC4015BP, TC4015BF

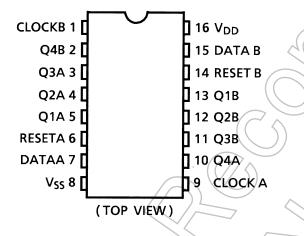
TC4015B Dual 4-Stage Static Shift Register (with serial input/parallel output)

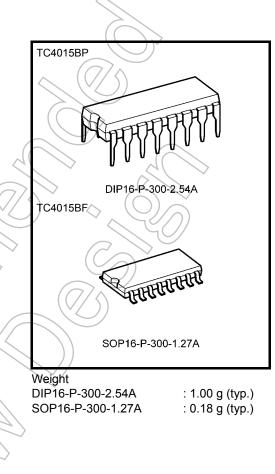
TC4015B contains two circuits of 4 stage shift registers and the independent output is drived from each stage. As all the D type flip-flops of every stage have common RESET input, asynchronous clear operation can be achieved by an external signal at arbitrary timing. The flip-flop of each stage is triggered by rising edge of CLOCK input.

RESET input of "H" level resets the contents of all the stages to "L" regardless of CLOCK and DATA inputs and all of data outputs Q1 through Q4 become "L".

This can be used for converting serial data to palallel one and for ring counters of any numbering systems.

Pin Assignment





Truth Table

		. / /						
	Inputs	X N	Outputs					
$CLOCK\Delta$	DATA	RESET	Q1	Q2	Q3	Q4		
	- F())	L	Q1	Q2	Q3		
	Ŧ	L	<u></u> Η	Q1	Q2	Q3		
	*	L	No Change					
*	*	Н	$\langle \rangle$	ľ	L	L		

 Δ : Level change

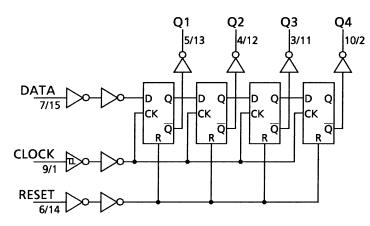
*: Don't care

Start of commercial production 1978-04

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Logic Diagram

1/2 TC4015B



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	V _{DD}	V_{SS} – 0.5 to V_{SS} + 20	V
Input voltage	V _{IN}	V _{SS} – 0.5 to V _{DD} + 0.5	_v)
Output voltage	Vout	V _{SS} - 0.5 to V _{DD} + 0.5	Ň
DC input current	I _{IN}	±10	mA
Power dissipation	PD	300 (DIP)/180 (SOP)	mW
Operating temperature range	T _{opr}	-40 to 85	°C
Storage temperature range	T _{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (V_{SS} = 0 V) (Note)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
DC supply voltage	VDD	_	3	_	18	V
Input voltage	VIN		0		V _{DD}	V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{DD} or V_{SS} .

Static Electrical Characteristics ($V_{SS} = 0 V$)

		Sym-	Test Condition		-40°C			25°C			85°C	
Charac	teristics	bol		V _{DD} (V)	Min	Max	Min	Тур.	Max	Min	Max	Unit
High-level output voltage			$ I_{OUT} < 1 \mu A$	5	4.95		4.95	5.00	_	4.95	_	
		VOH		10	9.95		9.95	10.00 <		9.95	—	V
0			$V_{IN} = V_{SS}, V_{DD}$	15	14.95	—	14.95	15.00	λ	14.95	_	
			I _{OUT} < 1 μΑ	5	—	0.05	—	0.00	0.05		0.05	
Low-level voltage	output	V _{OL}	$V_{IN} = V_{SS}, V_{DD}$	10	—	0.05	—	0.00	0.05	2_	0.05	V
			VIN - VSS, VDD	15	—	0.05		0.00	0.05		0.05	
			V _{OH} = 4.6 V	5	-0.61	—	-0.51	-1.0		-0.42	—	
			V _{OH} = 2.5 V	5	-2.50	—	-2.10	-4.0	> —	-1.70	—	
Output hig	h current	Iон	V _{OH} = 9.5 V	10	-1.50		-1.30	-2.2	—	-1.10	_	mA
			V _{OH} = 13.5 V	15	-4.00	- <	-3.40	9.0	—	-2.80	\searrow	
			$V_{IN} = V_{SS}, V_{DD}$			6				\geq		
		I _{OL}	$V_{OL} = 0.4 V$	5	0.61	$\left(\left(\right) \right)$	0.51	1.2		0.42	<	mA
Output low	/ current		$V_{OL} = 0.5 V$	10	1.50	\sim	1.30	3.2	$\langle \langle \rangle$	(1.10	/ —	
Culpution	ourient		V _{OL} = 1.5 V	15	4.00		3.40	12.0		2.80	—	
			$V_{IN} = V_{SS}, V_{DD}$		20				$\langle \rangle$			
		VIH	$V_{OUT} = 0.5 V, 4.5 V$	5	3.5	$\geq -$	3.5	2.75		3.5	—	V
Input high	voltage		V _{OUT} = 1.0 V, 9.0 V	10	7.0	—	7.0	5.50) —	7.0	—	
mparmgn	voltage		V _{OUT} = 1.5 V, 13.5 V	(15)	11,0	_//	11.0	8.25	_	11.0	—	v
			I _{OUT} < 1 μA		\geq							
			V _{OUT} = 0.5 V, 4.5 V	5	—	1.5	\searrow	2.25	1.5		1.5	
Input low voltage	VIL	V _{OUT} = 1.0 V, 9.0 V	_10	—	3.0		4.50	3.0		3.0	v	
input low voltage		V _{OUT} = 1.5 V, 13.5 V	15	_	4.0	—	6.75	4.0	—	4.0	v	
			I _{OUT} <1 µA		~	$\langle \zeta \rangle$	\geq					
Input	"H" level	Чн	VIH = 18 V	18	1	0.1		10 ⁻⁵	0.1		1.0	μA
current	"L" level	h		18	(\overline{q})	0.1		-10 ⁻⁵	-0.1		-1.0	μπ
		\leq	New York M	5		5		0.005	5	_	150	
Quiescent current	Quiescent supply current		V _{IN} = V _{SS} , V _{DD} (Note)	10	4	10		0.010	10		300	μA
ourient		~		15		20		0.015	20	—	600	

Note: All valid input combinations.



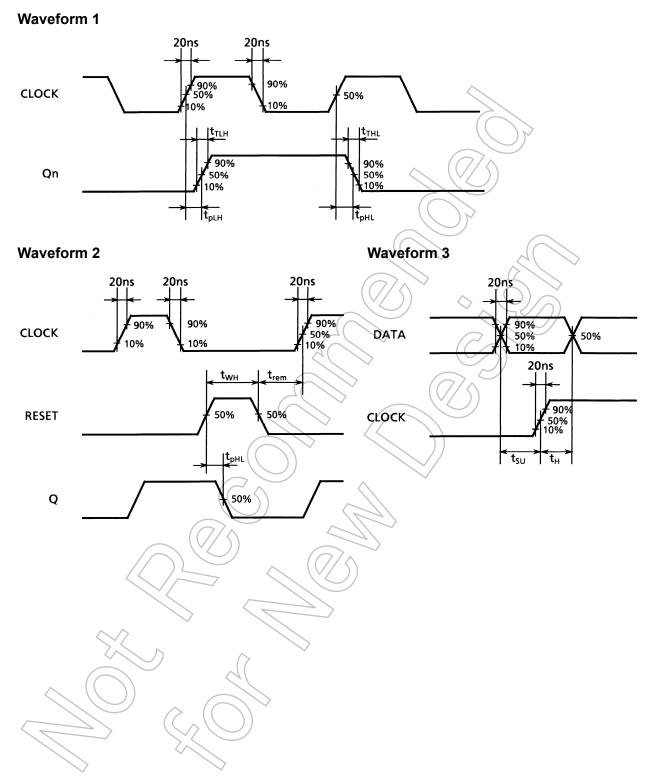
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Dynamic Electrical Characteristics (Ta = 25° C, V_{SS} = 0 V, C_L = 50 pF)

Characteristics	Symbol	Test Condition		Min		Max	Unit
Characteristics	Symbol		V _{DD} (V)	IVIIII	Тур.	Wax	Unit
Output transition time			5	_	70	200	
(low to high)	t _{TLH}	—	10	-	35	100	ns
			15	\nearrow	30	80	
Output transition time			5	(-)	70	200	
(high to low)	t _{THL}	—	10	X	35	100	ns
			15	'A	30	80	
Propagation delay time	t _{pLH}		5	Ì	130	320	
(CLOCK-Q)		—	(10)	> —	60	160	ns
	t _{pHL}		15	_	50	120	
Propagation delay time		20	5	_	90	400	
(RESET-Q)	t _{pHL}	-	10	—	45	200	ns
		$(7/\uparrow)$	15	(40	2 160	
			5 🗸	3.0	8) —	
Max clock frequency	f _{CL}		10	6.0	17	—	MHz
			15 ((8.5	[∨] 20		
		× ·	5	Ð	35	180	
Min clock pulse width	t _W		(10//) -	25	80	ns
			15	/	20	50	
Min pulse width			5	_	50	200	
(RESET)	twn))	10	—	25	80	ns
			15	—	20	60	
Min set-up time	$(\subset \land)$		5	_	8	70	
(DATA-CLOCK)	tsu		10		4	40	ns
	7/		15	_	0	30	
Min hold time	$\boldsymbol{\mathbb{Y}}$	$(\overline{\Omega})$	5		6	60	
(DATA-CLOCK)	th 🤇		10	_	5	30	ns
			15		4	20	
Min removal time			5	—	0	80	
(RESET-CLOCK)	t _{rem}	<u> </u>	10	—	0	30	ns
	\wedge	~	15	—	0	20	
Max clock input rise time	trCL		5				
Max clock input fall time	tfCL	—	10		No limit		μS
	())		15		1 1	r	
Input capacitance	CIN	—		—	5	7.5	pF

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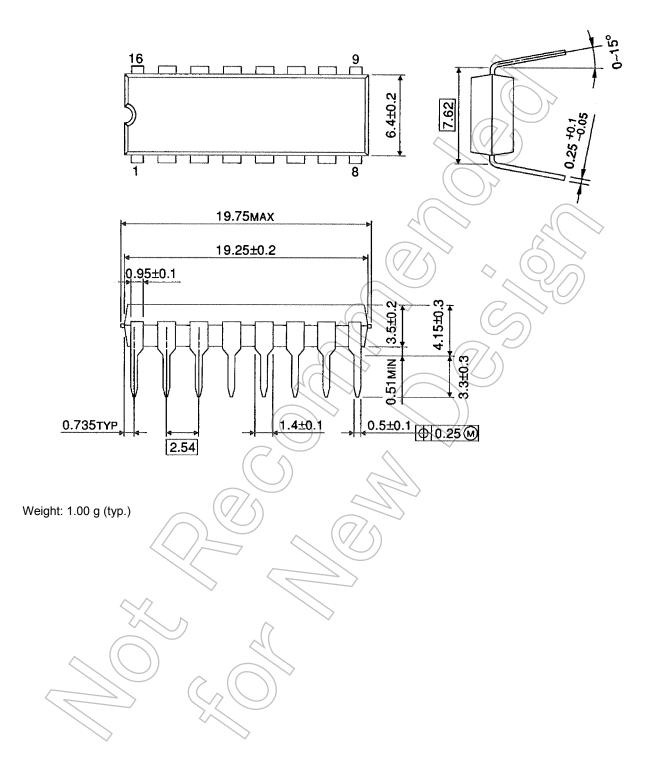
Waveforms for Measurement of Dynamic Characteristics



Package Dimensions

DIP16-P-300-2.54A

Unit : mm

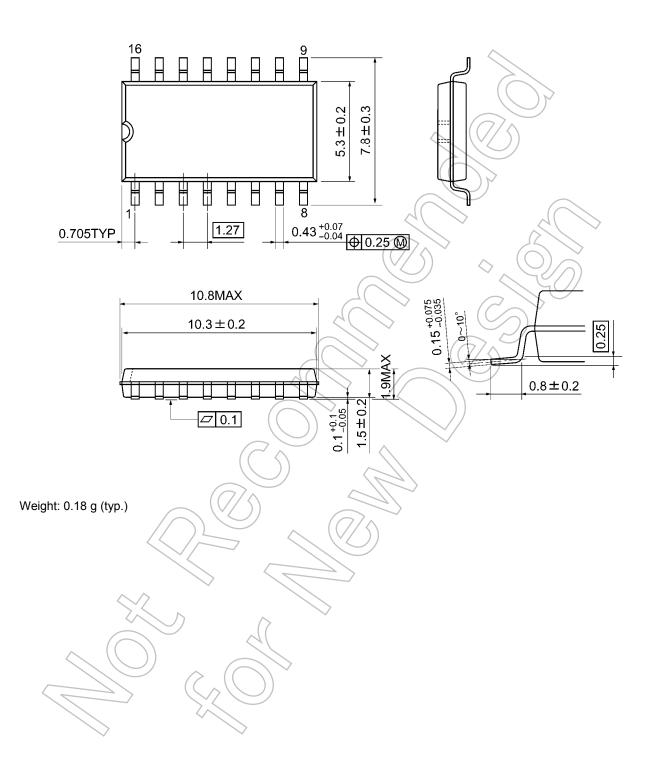




Package Dimensions

SOP16-P-300-1.27A

Unit: mm



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