

SN65LBC172, SN75LBC172 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

SLLS163D – JULY 1993 – REVISED APRIL 2003

- Meets or Exceeds EIA Standard RS-485
- Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments
- Support Data Rates up to and Exceeding Ten Million Transfers Per Second
- Common-Mode Output Voltage Range of -7 V to 12 V
- Positive- and Negative-Current Limiting
- Low Power Consumption . . . 1.5 mA Max (Output Disabled)
- Functionally Interchangeable With SN75172

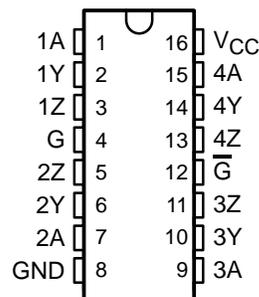
description

The SN65LBC172 and SN75LBC172 are monolithic quadruple differential line drivers with 3-state outputs. Both devices are designed to meet the requirements of EIA Standard RS-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown circuitry making it suitable for party-line applications in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultra-low power consumption and inherent robustness.

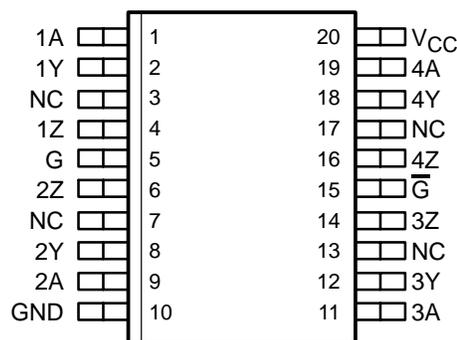
Both the SN65LBC172 and SN75LBC172 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used with the SN75LBC173 or SN75LBC175 quadruple line receivers. The SN65LBC172 and SN75LBC172 are available in the 16-pin DIP package (N) and the 20-pin wide-body small-outline inline-circuit (SOIC) package (DW).

The SN75LBC172 is characterized for operation over the commercial temperature range of 0°C to 70°C . The SN65LBC172 is characterized over the industrial temperature range of -40°C to 85°C .

**N PACKAGE
(TOP VIEW)**



**DW PACKAGE
(TOP VIEW)**



NC – No internal connection

**FUNCTION TABLE
(each driver)**

INPUT A	ENABLES		OUTPUTS	
	G	\bar{G}	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance (off)



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 **TEXAS
INSTRUMENTS**

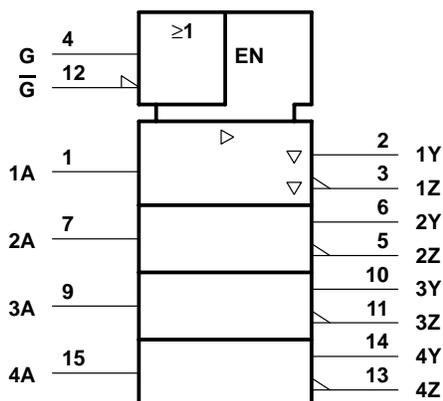
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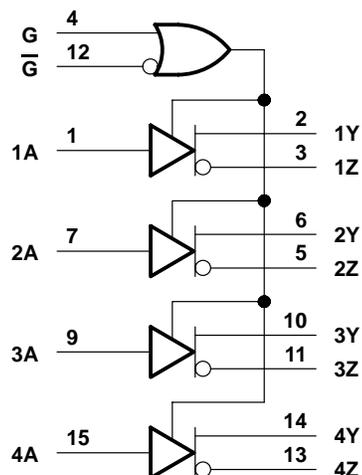
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logic symbol†

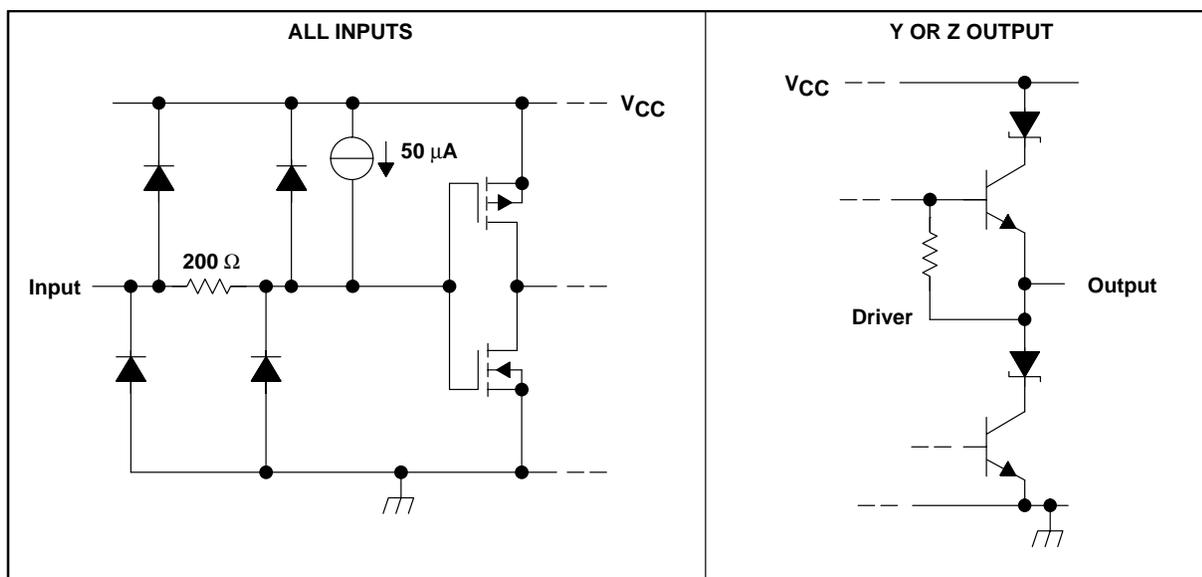


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the N package.

logic diagram (positive logic)



schematic diagrams of inputs and outputs



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 7 V
Output voltage range, V_O	–10 V to 15 V
Voltage range at A, \bar{G} , G	–0.3 V to $V_{CC} + 0.5$ V
Continuous power dissipation	Internally limited‡
Operating free-air temperature range, T_A : SN65LBC172	–40°C to 85°C
SN75LBC172	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}		0.8			V
Voltage at any bus terminal (separately or common mode), V_O	Y or Z	12			V
		–7			
High-level output current, I_{OH}	Y or Z	–60			mA
Low-level output current, I_{OL}	Y or Z	60			mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature, T_A	SN65LBC172	–40			85
	SN75LBC172	0			70

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = -18 mA				-1.5	V
V _{OD}	Differential output voltage‡	R _L = 54 Ω, See Figure 1	SN65LBC172	1.1	1.8	5	V
			SN75LBC172	1.5	1.8	5	
		R _L = 60 Ω, See Figure 2	SN65LBC172	1.1	1.7	5	
			SN75LBC172	1.5	1.7	5	
Δ V _{OD}	Change in magnitude of common-mode output voltage§					±0.2	V
V _{OC}	Common-mode output voltage	R _L = 54 Ω, See Figure 1				3 -1	V
Δ V _{OC}	Change in magnitude of common-mode output voltage§					±0.2	V
I _O	Output current with power off	V _{CC} = 0, V _O = -7 V to 12 V				±100	μA
I _{OZ}	High-impedance-state output current	V _O = -7 V to 12 V				±100	μA
I _{IH}	High-level input current	V _I = 2.4 V				-100	μA
I _{IL}	Low-level input current	V _I = 0.4 V				-100	μA
I _{OS}	Short-circuit output current	V _O = -7 V to 12 V				±250	mA
I _{CC}	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal-transmission distance.

§ Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
t _{d(OD)}	Differential output delay time	R _L = 54 Ω, See Figure 3			2	11	20	ns
t _{t(OD)}	Differential output transition time				10	15	25	
t _{pZH}	Output enable time to high level	R _L = 110 Ω, See Figure 4				20	30	ns
t _{pZL}	Output enable time to low level	R _L = 110 Ω, See Figure 5				21	30	ns
t _{PHZ}	Output disable time from high level	R _L = 110 Ω, See Figure 4				48	70	ns
t _{PLZ}	Output disable time from low level	R _L = 110 Ω, See Figure 5				21	30	ns



PARAMETER MEASUREMENT INFORMATION

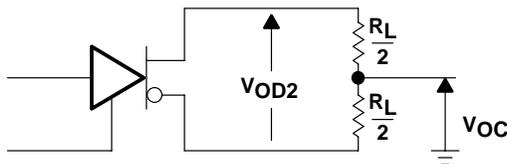
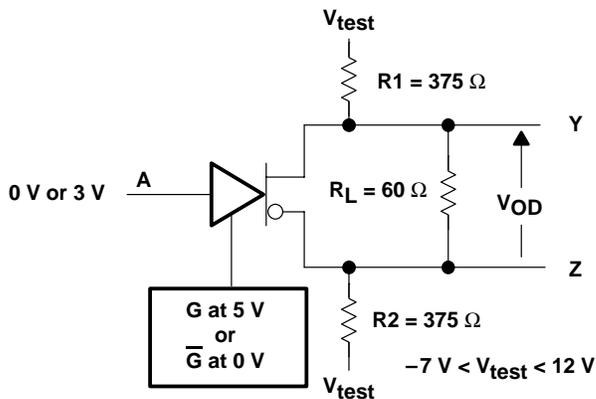
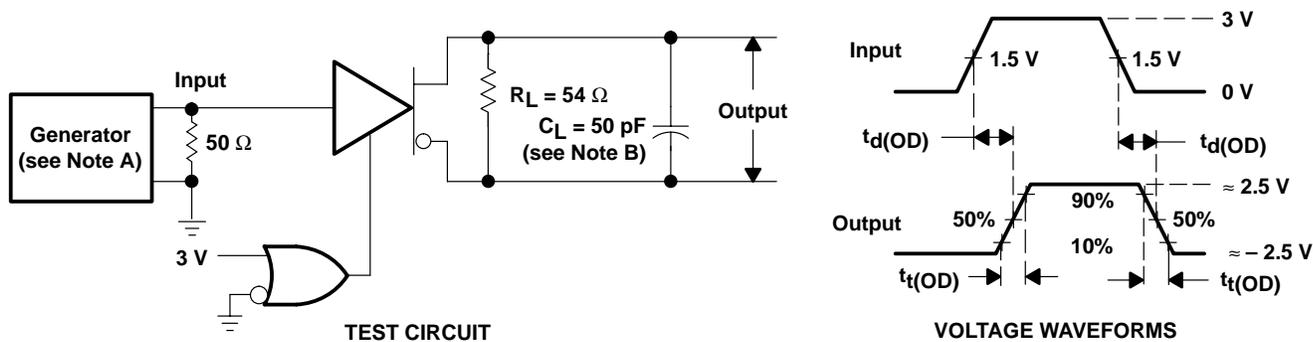


Figure 1. Differential and Common-Mode Output Voltages



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, duty cycle = 50%, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and stray capacitance.

Figure 2. Driver V_{OD} Test Circuit



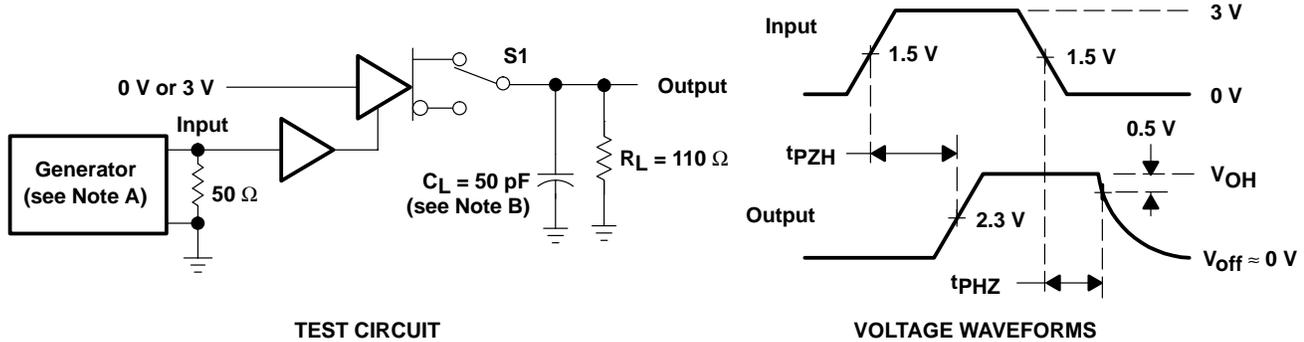
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, duty cycle = 50%, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and stray capacitance.

Figure 3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms

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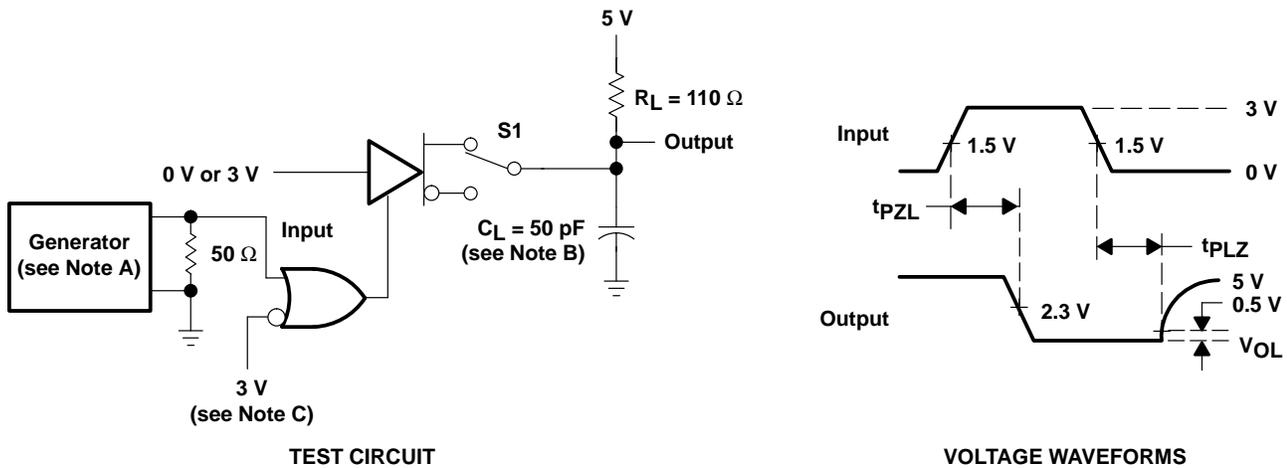
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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_r \leq$ 5 ns, $t_f \leq$ 5 ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and stray capacitance.

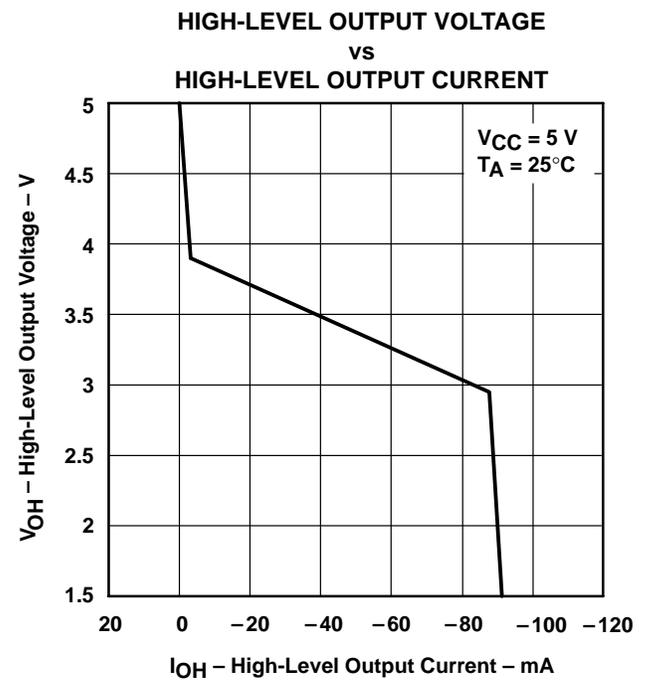
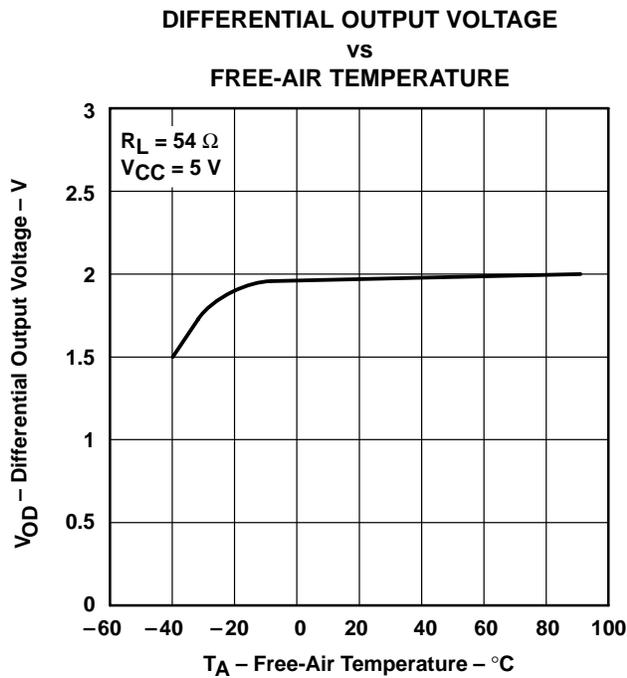
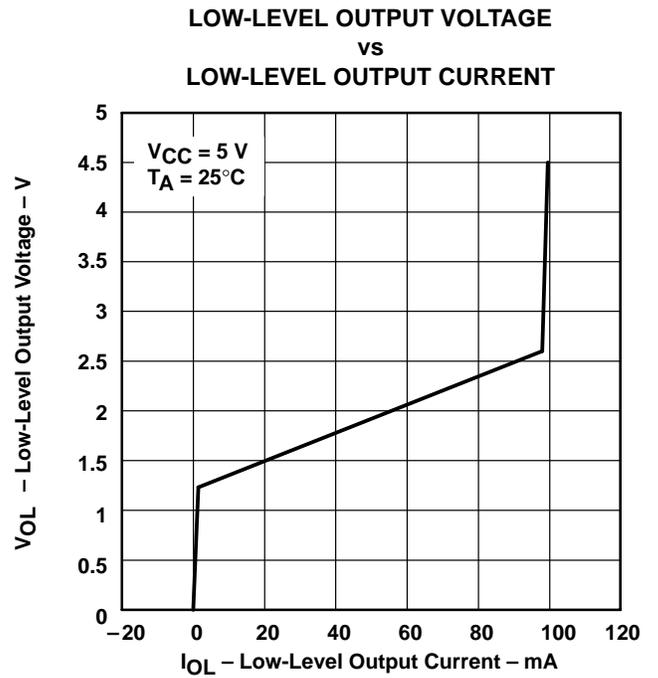
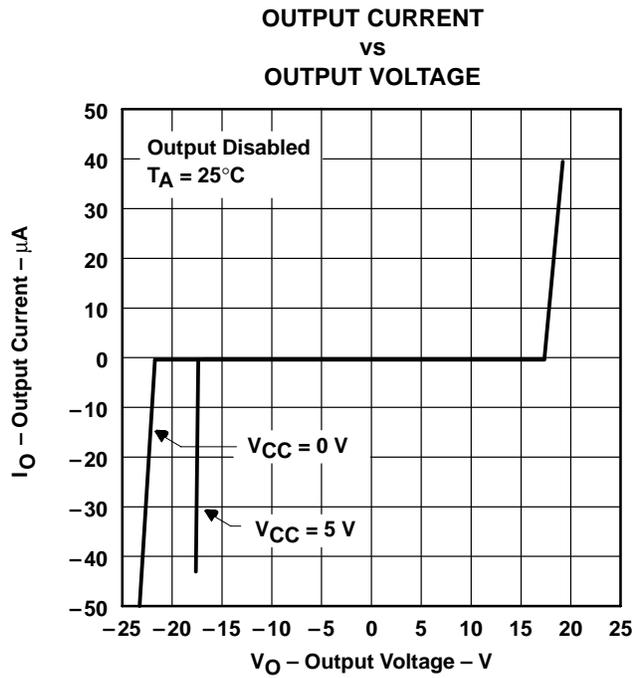
Figure 4. t_{pZH} and t_{pHZ} Test Circuit and Voltage Waveforms



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_r \leq$ 5 ns, $t_f \leq$ 5 ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and stray capacitance
 C. To test the active-low enable \overline{G} , ground G and apply an inverted waveform to \overline{G} .

Figure 5. t_{pZL} and t_{pLZ} Test Circuit and Waveforms

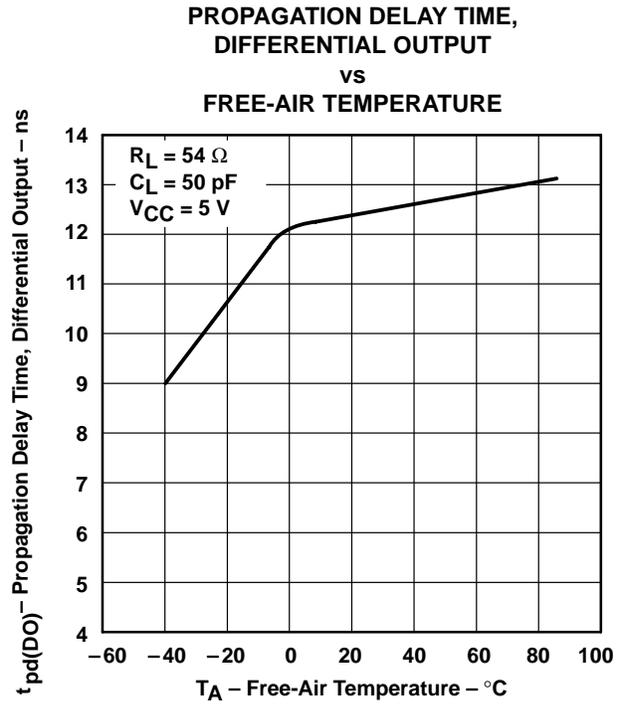
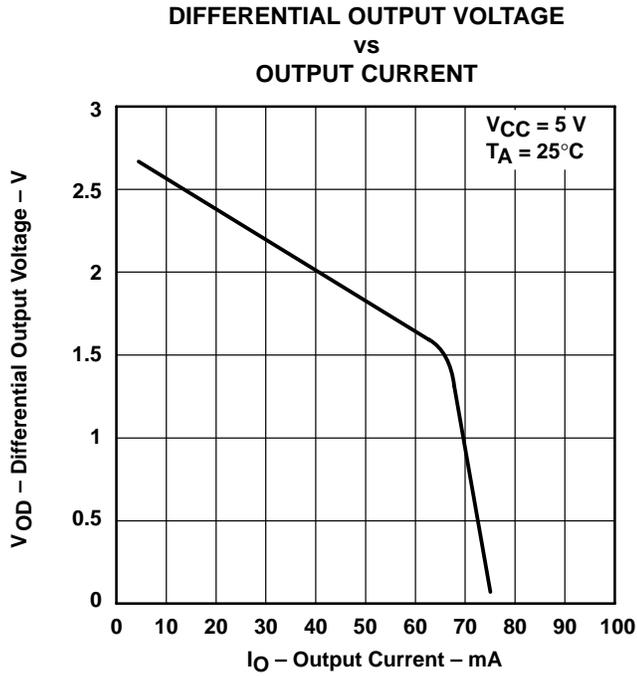
TYPICAL CHARACTERISTICS



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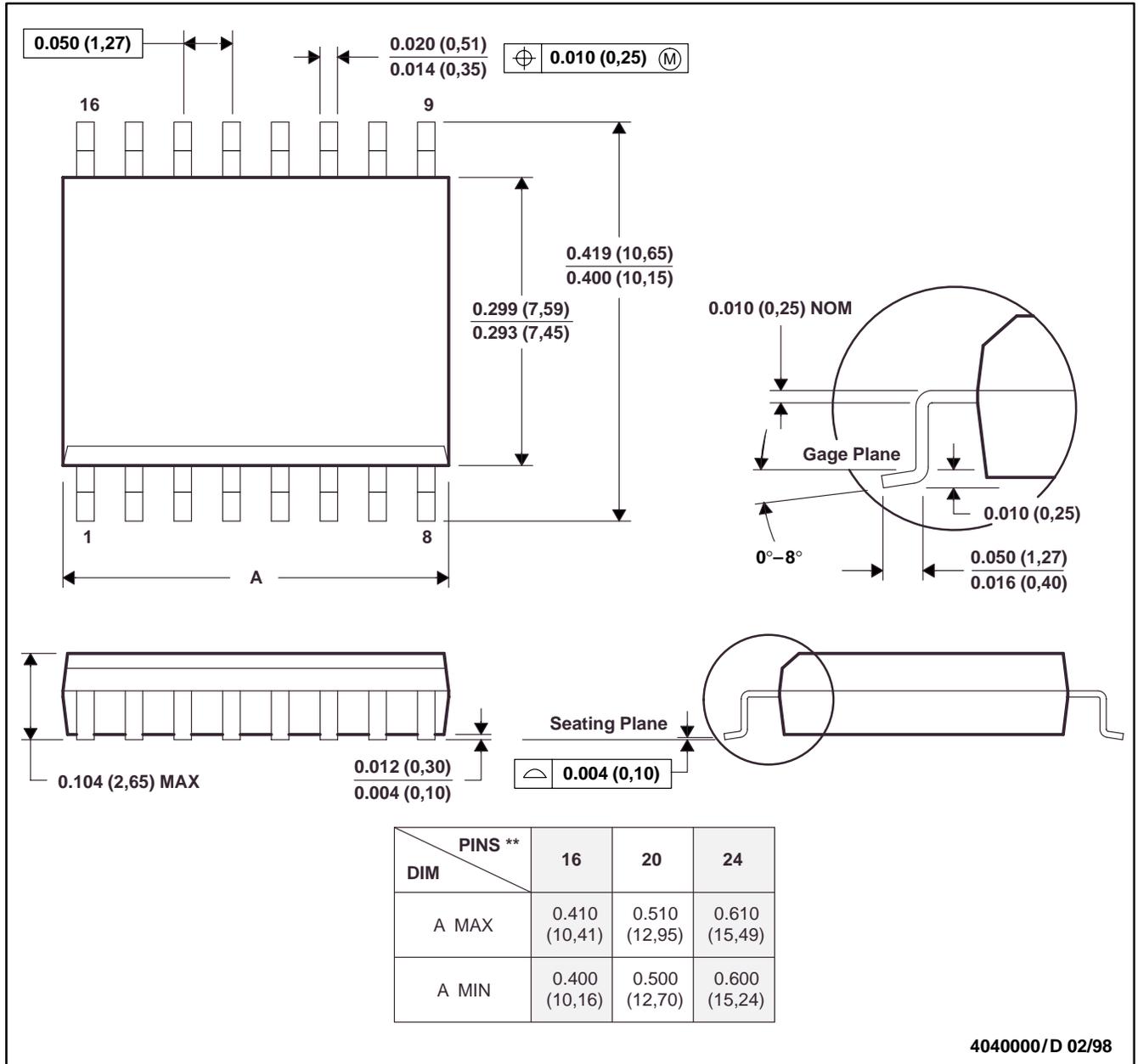
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MECHANICAL DATA

DW (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

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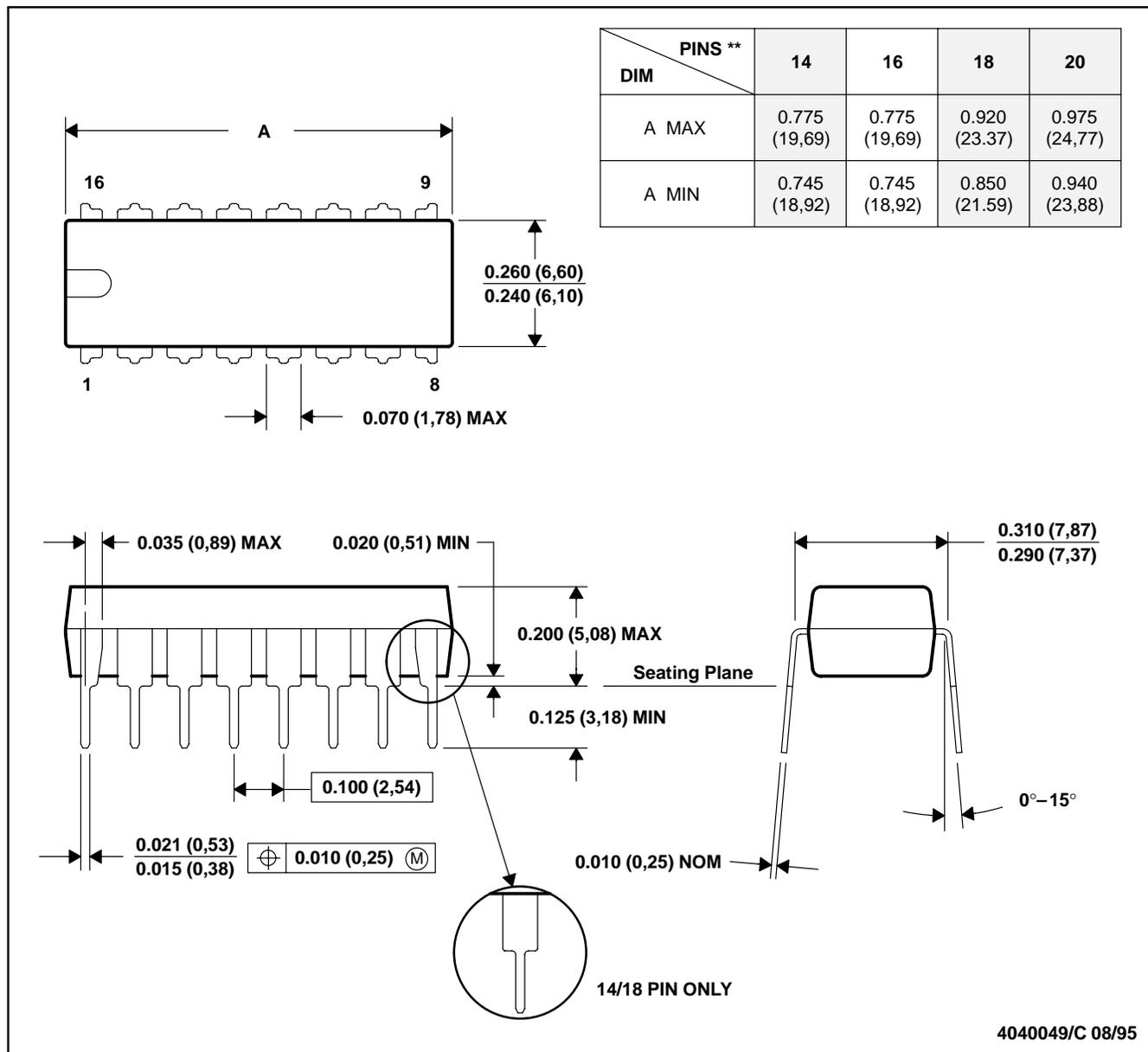
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MECHANICAL DATA

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65LBC172DW	ACTIVE	SOIC	DW	20	25	None	CU NIPDAU	Level-1-220C-UNLIM
SN65LBC172N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75LBC172DW	ACTIVE	SOIC	DW	20	25	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LBC172DWR	ACTIVE	SOIC	DW	20	2000	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LBC172N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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