

# SN74LVCC4245A

## OCTAL DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS584F – NOVEMBER 1996 – REVISED AUGUST 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

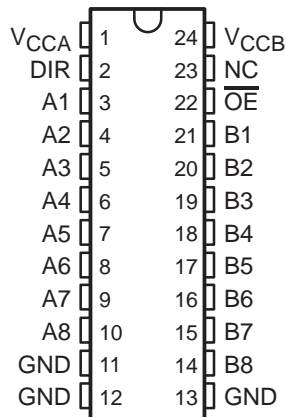
#### description

This 8-bit (octal) noninverting bus transceiver uses two separate power-supply rails. The A port,  $V_{CCA}$ , is dedicated to accept a 5-V supply level, and the configurable B port, which is designed to track  $V_{CCB}$ , accepts voltages from 3 V to 5 V. This allows for translation from a 3.3-V to a 5-V environment and vice versa.

The SN74LVCC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

The SN74LVCC4245A is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DB, DW, OR PW PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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**TEXAS  
INSTRUMENTS**

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The logic diagram shows the internal structure of the 74VHC147 decoder. It features two 3-input AND gates at the top, two 3-input OR gates at the bottom, and a central 3-to-8 decoder core. The inputs are DIR (pin 2), A1 (pin 3), and OE (pin 22). The output B1 (pin 21) is shown, along with connections to seven other channels, indicated by a bracket and the text "To Seven Other Channels".

Supply voltage range, $V_{CCA}$ and $V_{CCB}$	−0.5 V to 6 V
Input voltage range, $V_I$ (see Note 1): I/O ports (A port)	−0.5 V to $V_{CCA} + 0.5$ V
I/O ports (B port)	−0.5 V to $V_{CCB} + 0.5$ V
Except I/O ports	−0.5 V to $V_{CCA} + 0.5$ V
Output voltage range, $V_O$ (see Note 1): (A port)	−0.5 V to $V_{CCA} + 0.5$ V
(B port)	−0.5 V to $V_{CCB} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	−50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	−50 mA
Continuous output current, $I_O$	±50 mA
Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, $T_{stg}$	−65°C to 150°C

NOTES: 1. This value is limited to 6 V maximum.

2. The package thermal impedance is calculated in accordance with JESD 51.

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**recommended operating conditions (see Note 3)**

		V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	NOM	MAX	UNIT
V <sub>CCA</sub>	Supply voltage			4.5	5	5.5	V
V <sub>CCB</sub>	Supply voltage			2.7	3.3	5.5	V
V <sub>IHA</sub>	High-level input voltage	4.5 V	2.7 V	2			V
			3.6 V	2			
			5.5 V	2			
V <sub>IHB</sub>	High-level input voltage	4.5 V	2.7 V	2			V
			3.6 V	2			
			5.5 V	3.85			
V <sub>ILA</sub>	Low-level input voltage	4.5 V	2.7 V			0.8	V
			3.6 V			0.8	
			5.5 V			0.8	
V <sub>ILB</sub>	Low-level input voltage	4.5 V	2.7 V			0.8	V
			3.6 V			0.8	
			5.5 V			1.65	
V <sub>IA</sub>	Input voltage			0		V <sub>CCA</sub>	V
V <sub>IB</sub>	Input voltage			0		V <sub>CCB</sub>	V
V <sub>OA</sub>	Output voltage			0		V <sub>CCA</sub>	V
V <sub>OB</sub>	Output voltage			0		V <sub>CCB</sub>	V
I <sub>OHA</sub>	High-level output current	4.5 V	3 V			–24	mA
I <sub>OHB</sub>	High-level output current	4.5 V	2.7 V to 4.5 V			–24	mA
I <sub>OLA</sub>	Low-level output current	4.5 V	3 V			24	mA
I <sub>OLB</sub>	Low-level output current	4.5 V	2.7 V to 4.5 V			24	mA
T <sub>A</sub>	Operating free-air temperature			–40		85	°C

NOTE 3: All unused inputs of the device must be held at the associated V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	UNIT
V <sub>OHA</sub>		I <sub>OH</sub> = –100 µA	4.5 V	3 V	4.4	4.49		V
		I <sub>OH</sub> = –24 mA	4.5 V	3 V	3.76	4.25		
V <sub>OHB</sub>		I <sub>OH</sub> = –100 µA	4.5 V	3 V	2.9	2.99		V
		I <sub>OH</sub> = –12 mA	4.5 V	2.7 V	2.2	2.5		
				3 V	2.46	2.85		
		I <sub>OH</sub> = –24 mA	4.5 V	2.7 V	2.1	2.3		
				3 V	2.25	2.65		
				4.5 V	3.76	4.25		
V <sub>OLA</sub>		I <sub>OL</sub> = 100 µA	4.5 V	3 V			0.1	V
		I <sub>OL</sub> = 24 mA	4.5 V	3 V		0.21	0.44	
V <sub>OLB</sub>		I <sub>OL</sub> = 100 µA	4.5 V	3 V			0.1	V
		I <sub>OL</sub> = 12 mA	4.5 V	2.7 V		0.11	0.44	
		I <sub>OL</sub> = 24 mA	4.5 V	2.7 V		0.22	0.5	
				3 V		0.21	0.44	
				4.5 V		0.18	0.44	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	5.5 V	3.6 V		±0.1	±1	µA
				5.5 V		±0.1	±1	
I <sub>OZ</sub> <sup>†</sup>	A or B ports	V <sub>O</sub> = V <sub>CCA/B</sub> or GND, V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V	3.6 V		±0.5	±5	µA
I <sub>CCA</sub>	B to A	A <sub>n</sub> = V <sub>CC</sub> or GND	5.5 V	Open		8	80	µA
		I <sub>O</sub> (A port) = 0, B <sub>n</sub> = V <sub>CCB</sub> or GND	5.5 V	3.6 V		8	80	
				5.5 V		8	80	
I <sub>CCB</sub>	A to B	A <sub>n</sub> = V <sub>CCA</sub> or GND, I <sub>O</sub> (B port) = 0	5.5 V	3.6 V		5	50	µA
				5.5 V		8	80	
ΔI <sub>CCA</sub> <sup>‡</sup>	A port	V <sub>I</sub> = V <sub>CCA</sub> – 2.1 V, Other inputs at V <sub>CCA</sub> or GND, $\overline{\text{OE}}$ at GND and DIR at V <sub>CCA</sub>	5.5 V	5.5 V		1.35	1.5	mA
	$\overline{\text{OE}}$	V <sub>I</sub> = V <sub>CCA</sub> – 2.1 V, Other inputs at V <sub>CCA</sub> or GND, DIR at V <sub>CCA</sub> or GND	5.5 V	5.5 V		1	1.5	
	DIR	V <sub>I</sub> = V <sub>CCA</sub> – 2.1 V, Other inputs at V <sub>CCA</sub> or GND, $\overline{\text{OE}}$ at V <sub>CCA</sub> or GND	5.5 V	3.6 V		1	1.5	
ΔI <sub>CCB</sub> <sup>‡</sup>	B port	V <sub>I</sub> = V <sub>CCB</sub> – 0.6 V, Other inputs at V <sub>CCB</sub> or GND, $\overline{\text{OE}}$ at GND and DIR at GND	5.5 V	3.6 V		0.35	0.5	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	Open	Open		5		pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CCA/B</sub> or GND	5 V	3.3 V		11		pF

<sup>†</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

<sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or the associated V<sub>CC</sub>.

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$ , $V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		$V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$ , $V_{CCB} = 2.7\text{ V TO } 3.6\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{PHL}$	A	B	1	7.1	1	7	ns
$t_{PLH}$			1	6	1	7	
$t_{PHL}$	B	A	1	6.8	1	6.2	ns
$t_{PLH}$			1	6.1	1	5.3	
$t_{PZL}$	$\overline{OE}$	A	1	9	1	9	ns
$t_{PZH}$			1	8.3	1	8	
$t_{PZL}$	$\overline{OE}$	B	1	8.2	1	10	ns
$t_{PZH}$			1	8.1	1	10.2	
$t_{PLZ}$	$\overline{OE}$	A	1	4.7	1	5.2	ns
$t_{PHZ}$			1	4.9	1	5.2	
$t_{PLZ}$	$\overline{OE}$	B	1	5.4	1	5.4	ns
$t_{PHZ}$			1	6.3	1	7.4	

operating characteristics,  $V_{CCA} = 5\text{ V}$ ,  $V_{CCB} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 0$ , $f = 10\text{ MHz}$	20	pF
		Outputs disabled		6.5	

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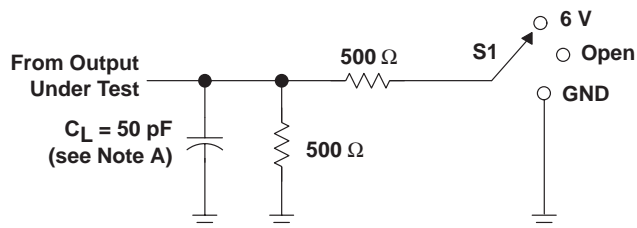
## OCTAL DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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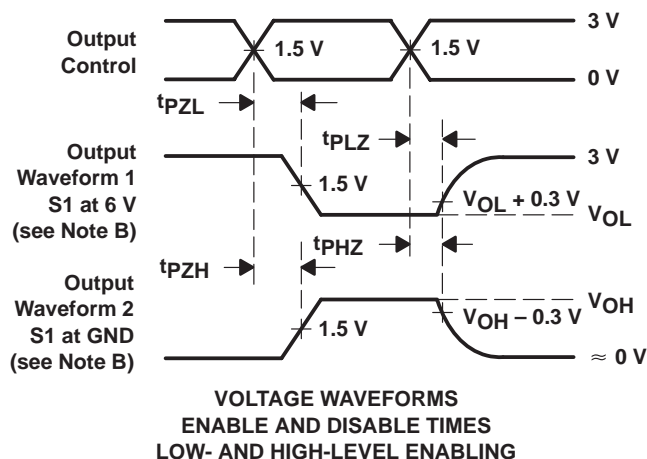
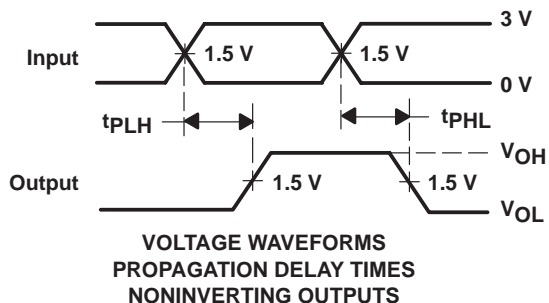
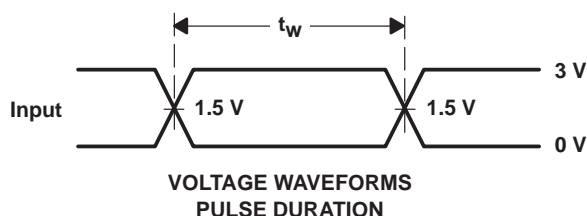
#### PARAMETER MEASUREMENT INFORMATION FOR A TO B

$V_{CCA} = 4.5\text{ V TO }5.5\text{ V}$  AND  $V_{CCB} = 2.7\text{ V TO }3.6\text{ V}$



LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND

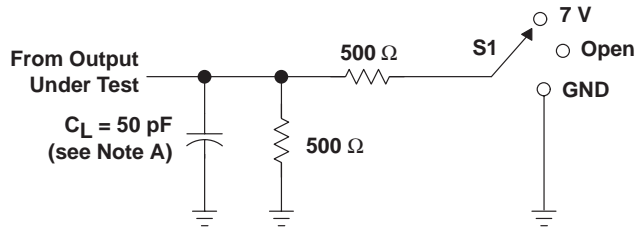


- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

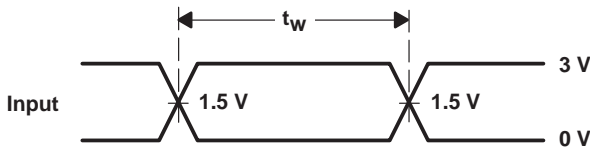
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**PARAMETER MEASUREMENT INFORMATION FOR A TO B**  
 **$V_{CCA} = 4.5\text{ V TO }5.5\text{ V}$  AND  $V_{CCB} = 3.6\text{ V TO }5.5\text{ V}$**

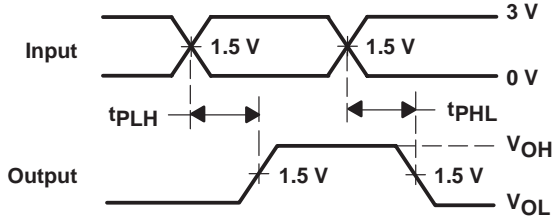


**LOAD CIRCUIT**

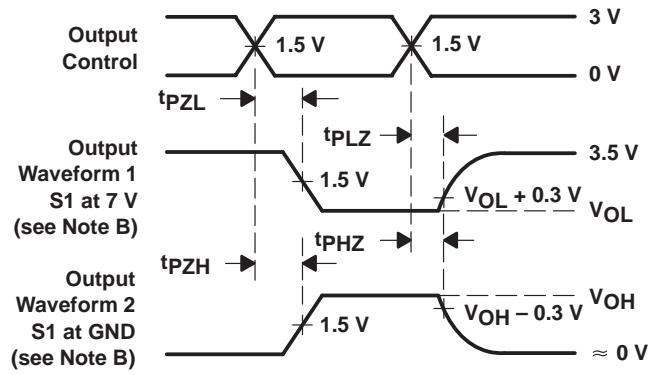
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	GND



**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
NONINVERTING OUTPUTS**



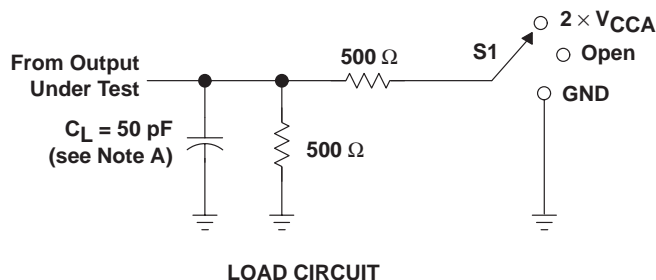
**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

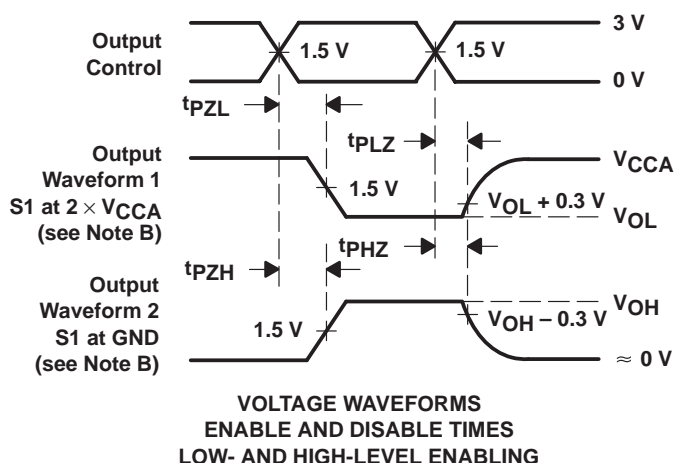
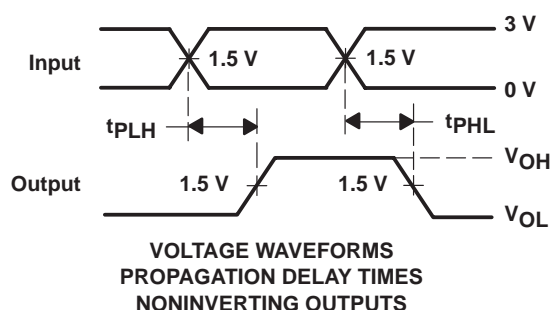
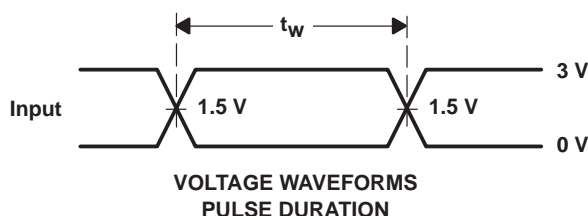
**Figure 2. Load Circuit and Voltage Waveforms**

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**PARAMETER MEASUREMENT INFORMATION FOR B TO A**  
 $V_{CCA} = 4.5\text{ V TO }5.5\text{ V AND }V_{CCB} = 2.7\text{ V TO }3.6\text{ V}$



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCA}$
$t_{PHZ}/t_{PZH}$	GND

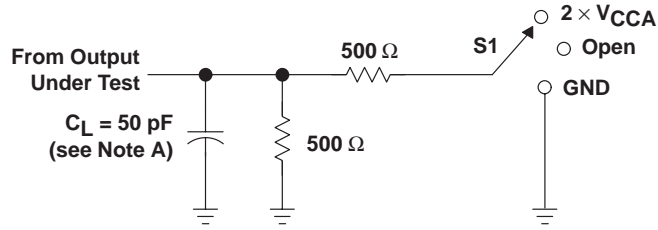


- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 3. Load Circuit and Voltage Waveforms**

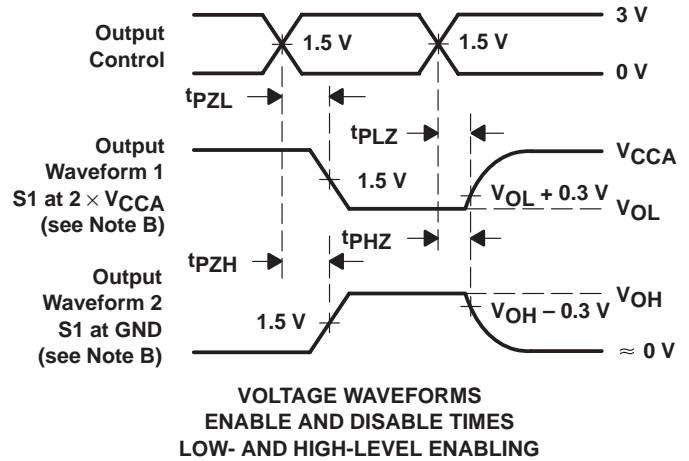
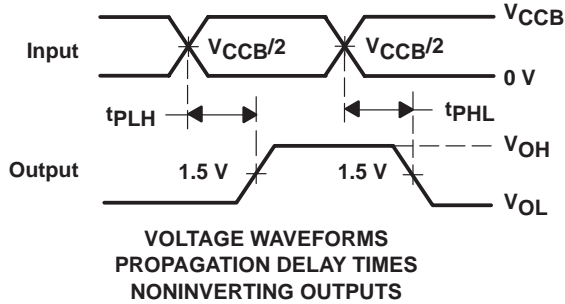
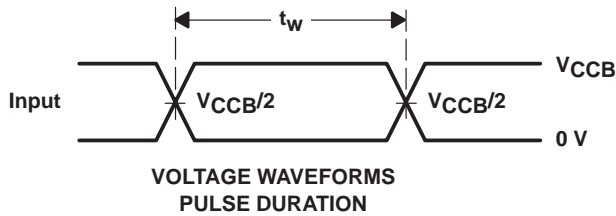


**PARAMETER MEASUREMENT INFORMATION FOR B TO A**  
 **$V_{CCA} = 4.5\text{ V TO }5.5\text{ V}$  AND  $V_{CCB} = 3.6\text{ V TO }5.5\text{ V}$**



**LOAD CIRCUIT**

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCA}$
$t_{PHZ}/t_{PZH}$	GND



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

**Figure 4. Load Circuit and Voltage Waveforms**

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