LMX2594 15 GHz Wideband PLLatinum™ RF Synthesizer With Phase Synchronization and JESD204B Support

1 Features

- 10-MHz to 15-GHz Output Frequency
- –110 dBc/Hz Phase Noise at 100 kHz Offset With 15 GHz Carrier
- 45-fs rms Jitter at 7.5 GHz (100 Hz to 100 MHz)
- Programmable Output Power Up to 7 dBm at 15 GHz
- PLL Key Specifications
  - Figure of Merit: –236 dBc/Hz
  - Normalized 1/f Noise: –129 dBc/Hz
  - High Phase Detector Frequency
    - 400-MHz Integer Mode
    - 300-MHz Fractional Mode
  - 32-bit Fractional-N Divider
- Remove Integer Boundary Spurs With Programmable Input Multiplier
- Synchronize Output Phase Across Multiple Devices
- Support for SYSREF With 9-ps Resolution Programmable Delay
- Frequency Ramp and Chirp Generation Ability for FMCW Applications
- < 20-µs VCO Calibration Speed
- 3.3-V Single Power Supply Operation

2 Applications

- 5G and mm-wave Wireless Infrastructure
- Test and Measurement Equipment
- Radar
- MIMO
- Phased Array Antennas and Beam Forming
- High Speed Data Converter Clocking (Supports JESD204B)

3 Description

The LMX2594 is a high-performance, wideband PLL with integrated VCOs that can generate any frequency from 10 MHz to 15 GHz without using an internal doubler, thus eliminating the need for sub-harmonic filters. The high performance PLL with figure of merit of –236 dBc/Hz and high phase detector frequency can attain very low in-band noise and integrated jitter. The high speed N-divider has no pre-divider, thus significantly reducing the amplitude and number of spurs. There is also a programmable input multiplier to mitigate integer boundary spurs.

The LMX2594 allows users to synchronize the output of multiple devices and also enables applications that need deterministic delay between input and output. A frequency ramp generator can synthesize up to 2 segments of ramp in an automatic ramp generation option or a manual option for maximum flexibility. The fast calibration algorithm allows changing frequencies faster than 20 µs. The LMX2594 adds support for generating or repeating SYSREF (compliant to JESD204B standard) making it an ideal low-noise clock source for high-speed data converters. Fine delay adjustment (9 ps resolution) is provided in this configuration to account for delay differences of board traces.

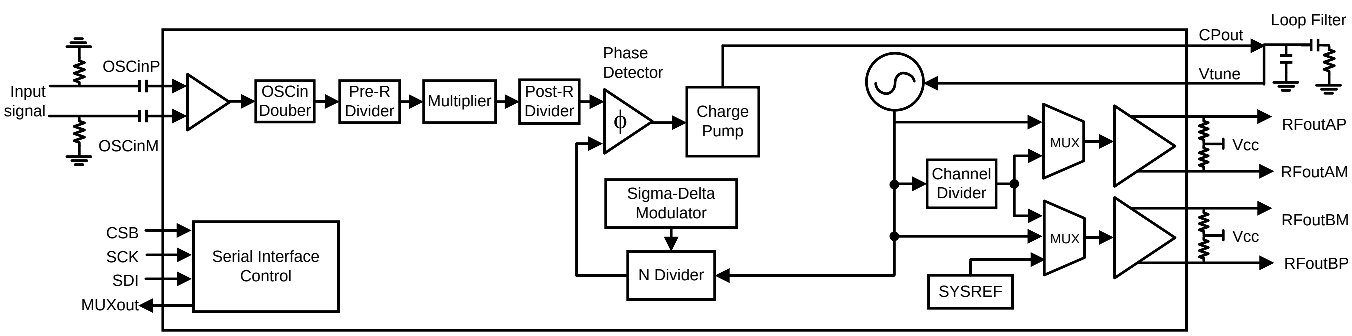
The output drivers within LMX2594 delivers output power as high as 7 dBm at 15 GHz carrier frequency. The device runs from a single 3.3 V supply and has integrated LDOs that eliminate the need for on-board low noise LDOs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMX2594	VQFN (40)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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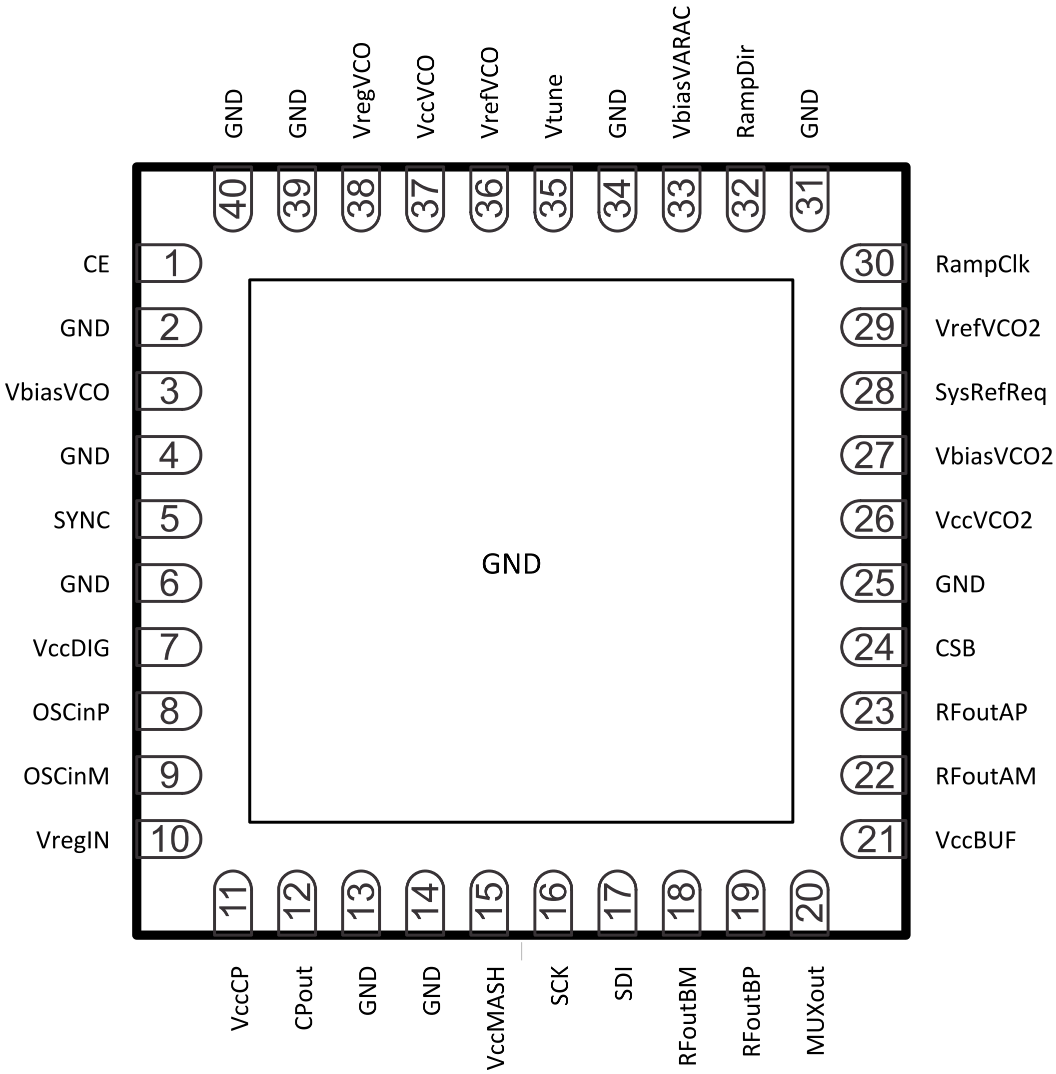
4 Revision History

DATE	REVISION	NOTES
March 2017	*	Initial release

5 Pin Configuration and Functions

RHA Package
40-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CE	Input	Chip enable input. Active HIGH powers on the device.
2, 4, 25, 31, 34, 39, 40	GND	Ground	VCO ground
3	VbiasVCO	Bypass	VCO bias. Requires connecting 10 µF capacitor to VCO ground. Place close to pin.
5	SYNC	Input	Phase synchronization pin. Has programmable threshold.
6, 14	GND	Ground	Digital ground
7	VccDIG	Supply	Digital supply. TI recommends bypassing with a 0.1 µF capacitor to digital ground.
8	OSCinP	Input	Reference input clock (+). High-impedance self-biasing pin. Requires AC coupling capacitor. (0.1 µF recommended)
9	OSCinM	Input	Reference input clock (–). High impedance self-biasing pin. Requires AC coupling capacitor. (0.1 µF recommended)
10	VregIN	Bypass	Input reference path regulator output. Requires connecting 1 µF capacitor to ground. Place close to pin.
11	VccCP	Supply	Charge pump supply.TI recommends bypassing with a 0.1 µF capacitor to charge pump ground.
12	CPout	Output	Charge pump output. TI recommends connecting C1 of loop filter close to pin.
13	GND	Ground	Charge pump ground
15	VccMASH	Supply	Digital supply. TI recommends bypassing with a 0.1 µF and 10 µF capacitor to digital ground.
16	SCK	Input	SPI clock. High impedance CMOS input. 1.8 to 3.3 V logic.
17	SDI	Input	SPI data. High impedance CMOS input. 1.8 to 3.3 V logic.
18	RFoutBM	Output	Differential output B (–). Requires pullup (typically 50-Ω resistor) to V_{CC} as close as possible to pin. Can be used as an output signal or SYSREF output.
19	RFoutBP	Output	Differential output B (+). Requires pullup (typically 50-Ω resistor) to V_{CC} as close as possible to pin. Can be used as an output signal or SYSREF output.
20	MUXout	Output	Multiplexed output pin — lock detect, readback, diagnostics, ramp status
21	VccBUF	Supply	Output buffer supply. TI recommends bypassing with a 0.1 µF capacitor to RFout ground.
22	RFoutAM	Output	Differential output A (–). Requires connecting 50-Ω resistor pullup to Vcc as close as possible to pin.
23	RFoutAP	Output	Differential output A (+). Requires connecting 50-Ω resistor pullup to Vcc as close as possible to pin.
24	CSB	Input	SPI latch. *Chip Select Bar* . High-impedance CMOS input. 1.8 to 3.3 V logic.
26	VccVCO2	Supply	VCO supply. TI recommends bypassing with a 0.1 µF and 10 µF capacitor to VCO ground.
27	VbiasVCO2	Bypass	VCO bias. Requires connecting 1 µF capacitor to VCO ground.
28	SysRefReq	Input	SYSREF request input for JESD204B support
29	VrefVCO2	Bypass	VCO supply reference. Requires connecting 10 µF capacitor to VCO ground.
30	RampClk	Input	Input pin for ramping mode that can be used to clock the ramp in manual ramping mode or as a trigger input.
32	RampDir	Input	Input pin for ramping mode that can be used to change ramp direction in manual ramping mode or as a trigger input.
33	VbiasVARAC	Bypass	VCO Varactor bias. Requires connecting 10 µF capacitor to VCO ground.
35	Vtune	Input	VCO tuning voltage input.
36	VrefVCO	Bypass	VCO supply reference. Requires connecting 10 µF capacitor to ground.
37	VccVCO	Supply	VCO supply. Recommend bypassing with 0.1 µF and 10 µF capacitor to ground.
38	VregVCO	Bypass	VCO regulator node. Requires connecting 1 µF capacitor to ground.
DAP	GND	Ground	RFout ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Power supply voltage	–0.3	3.6	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500 V HBM is possible with the necessary precautions. Pins listed as ±XXX V may actually have higher performance.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250 V CDM is possible with the necessary precautions. Pins listed as ±YYY V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power supply voltage	3.15	3.3	3.45	V
T_A	Ambient temperature	–40	25	85	°C
T_J	Junction Temperature			125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LMX2594 RHA (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance [2]	15.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) DAP

6.5 Electrical Characteristics

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ +85°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{CC}	Supply voltage			3.15	3.3	3.45	V
I_{CC}	Supply current	OUTA_PD = 0, OUTB_PD = 1 OUTA_MUX = OUTB_MUX = 1 OUTA_PWR = 31, CPG=7 f_{OSC}= f_{PD} = 100 MHz, f_{VCO} = f_{OUT} = 14 GHz p_{OUT} = 3 dBm with 50-Ω resistor pullup			340		mA
	Power on reset current	RESET=1			170		
	Power down current	POWERDOWN=1			5		
OUTPUT CHARACTERISTICS							
p_{OUT}	Single-ended output power(1)	50-Ω resistor pullup OUTx_PWR = 50	f_{OUT} = 8 GHz		5		dBm
			f_{OUT} = 15 GHz		2		
		1-nH inductor pullup OUTx_PWR = 50	f_{OUT} = 8 GHz		10		
			f_{OUT} = 15 GHz		7		
Xtalk	Isolation between outputs A and B. Measured on output A	OUTA_MUX = VCO OUTB_MUX = channel divider			–50		dBc
H2	Second Harmonic(1)	OUTA_MUX = VCO f_{VCO} = 8 GHz			-20		dBc
H3	Third Harmonic(1)	OUTA_MUX = VCO f_{VCO} = 8 GHz			-50		dBc
INPUT SIGNAL PATH							
f_{OSCin}	Reference input frequency	OSC_2X = 0		5		1400	MHz
		OSC_2X = 1		5		200	
v_{OSCin}	Reference input voltage	AC-coupled required (2)		0.2		2	Vpp
f_{MULT}	Multiplier frequency (only applies when multiplier is enabled)	Input range		30		70	MHz
		Output range		180		250	
PHASE DETECTOR AND CHARGE PUMP							
f_{PD}	Phase detector frequency (2)	Integer mode	FRAC_ORDER = 0	0.125		400	MHz
		Fractional mode	FRAC_ORDER = 1,2,3	5		300	
			FRAC_ORDER = 4	5		240	
I_{CPout}	Charge-pump leakage current	CPG = 0			15		nA
	Effective charge pump current. This is the sum of the up and down currents	CPG = 4			3		mA
		CPG = 1			6		
		CPG = 5			9		
		CPG = 3			12		
		CPG = 7			15		
$PN_{PLL\_1/f}$	Normalized PLL 1/f noise	f_{PD} = 100 MHz, f_{VCO} = 12 GHz(3)			–129		dBc/Hz
PN_{PLL_flat}	Normalized PLL noise floor				–236		dBc/Hz

(1) Output power, spurs, and harmonics can vary based on board layout and components.
(2) For lower VCO frequencies, the N divider minimum value can limit the phase-detector frequency.
(3) The PLL noise contribution is measured using a clean reference and a wide loop bandwidth and is composed into flicker and flat components. PLL_flat = PLL_FOM + 20 × log(Fvco/Fpd) + 10 × log(Fpd / 1Hz). PLL_flicker (offset) = PLL_flicker_Norm + 20*log(Fvco / 1GHz) – 10*log(offset / 10kHz). Once these two components are found, the total PLL noise can be calculated as PLL_Noise = 10 × log($10^{PLL\_Flat / 10}$ + $10^{PLL\_flicker / 10}$)

Electrical Characteristics (continued)

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ +85°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VCO CHARACTERISTICS							
PN_{VCO}	VCO phase noise	VCO1 f_{VCO} = 8.0 GHz	10 kHz		– 80		dBc/Hz
			100 kHz		– 107		
			1 MHz		– 128		
			10 MHz		– 148		
			90 MHz		– 157		
		VCO2 f_{VCO} = 9.2 GHz	10 kHz		– 79		
			100 kHz		– 105		
			1 MHz		– 127		
			10 MHz		– 147		
			90 MHz		– 157		
		VCO3 f_{VCO} = 10.3 GHz	10 kHz		– 77		
			100 kHz		– 104		
			1 MHz		– 126		
			10 MHz		– 147		
			90 MHz		– 157		
		VCO4 f_{VCO} = 11.3 GHz	10 kHz		– 76		
			100 kHz		– 103		
			1 MHz		– 125		
			10 MHz		– 145		
			90 MHz		– 158		
		VCO5 f_{VCO} = 12.5 GHz	10 kHz		– 74		
			100 kHz		– 100		
			1 MHz		– 123		
			10 MHz		– 144		
			90 MHz		– 157		
		VCO6 f_{VCO} = 13.3 GHz	10 kHz		– 73		
			100 kHz		– 100		
			1 MHz		– 122		
			10 MHz		– 143		
			90 MHz		– 155		
		VCO7 f_{VCO} = 14.5 GHz	10 kHz		– 73		
			100 kHz		–99		
			1 MHz		– 121		
			10 MHz		– 143		
			90 MHz		– 152		
t_{VCOCAL}	VCO Calibration Speed, Switch Across the entire frequency Band, f_{OSC} = 200 MHz, f_{PD} = 100 MHz (4)	No assist			50		µs
		Partial assist			35		
		Close frequency			20		
		Full assist			5		

(4) See *Application and Implementation* for more details on the different VCO calibration modes.

Electrical Characteristics (continued)

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ +85°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
K_{VCO}	VCO Gain	8.0 GHz			73		MHz/V
		9.2 GHz			76		
		10.3 GHz			94		
		11.3 GHz			86		
		12.5 GHz			149		
		13.3 GHz			135		
		14.5 GHz			154		
$\lvert \Delta T_{CL} \rvert$	Allowable temperature drift when VCO is not re-calibrated	RAMP_EN = 0 or RAMP_MANUAL= 1			125		°C
H2	VCO second harmonic	f_{VCO} = 8 GHz, divider disabled			–20		dBc
H3	VCO third haromonic	f_{VCO} = 8 GHz, divider disabled			–50		
SYNC PIN AND PHASE ALIGNMENT							
f_{OSCin}SYNC	Maximum usable OSCin with sync pin Figure 22	Category 3		0		100	MHz
		Categories1 and 2		0		1400	
DIGITAL INTERFACE, Applies to SCLK, SDA, CSB, RampDir, RampCLK, MUXout, SYNC (CMOS Mode), SysRefReq (CMOS Mode)							
V_{IH}	High level input voltage			1.4		Vcc	V
V_{IL}	Low level input voltage			0		0.4	V
I_{IH}	High level input current			–25		25	µA
I_{IL}	Low level input current			–25		25	µA
V_{OH}	High level output voltage	MUXout pin	Load current = –10 mA			V_{CC} – 0.4	V
V_{OL}	High level output current		Load current = 10 mA	0.4			V

6.6 Timing Requirements

(3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ +85°C, except as specified. Nominal values are at V_{CC} = 3.3 V, T_A = 25°C)

			MIN	NOM	MAX	UNIT
SYNC, SYSRefReq, RampCLK, and RampDIR Pins						
t_{SETUP}	Setup time for pin relative to OSCin rising edge	SYNC pin	2.5			ns
		SysRefReq pin	2.5			
t_{HOLD}	Hold time for SYNC pin relative to OSCin rising edge	SYNC pin	2			ns
		SysRefReq pin	2			
DIGITAL INTERFACE WRITE SPECIFICATIONS						
f_{SPI}Write	SPI write speed	t_{CWL} + t_{CWH} > 13.333 ns			75	MHz
t_{ES}	Clock to enable low time	See Figure 1	5			ns
t_{CS}	Data to clock setup time		2			ns
t_{CH}	Data to clock hold time		2			ns
t_{CWH}	Clock pulse width high		5			ns
t_{CWL}	Clock pulse width low		5			ns
t_{CES}	Enable to clock setup time		5			ns
t_{EWH}	Enable pulse width high		2			ns

Timing Requirements (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ +85°C, except as specified. Nominal values are at V_{CC} = 3.3 V, T_A = 25°C)

			MIN	NOM	MAX	UNIT
DIGITAL INTERFACE READBACK SPECIFICATIONS						
f_{SPI}Readback	SPI readback speed	See Figure 2			50	MHz
t_{ES}	Clock to enable low time		10			ns
t_{CS}	Clock to data wait time				10	ns
t_{CWH}	Clock pulse width high		10			ns
t_{CWL}	Clock pulse width low		10			ns
t_{CES}	Enable to clock setup time		10			ns
t_{EWH}	Enable pulse width high		10			ns

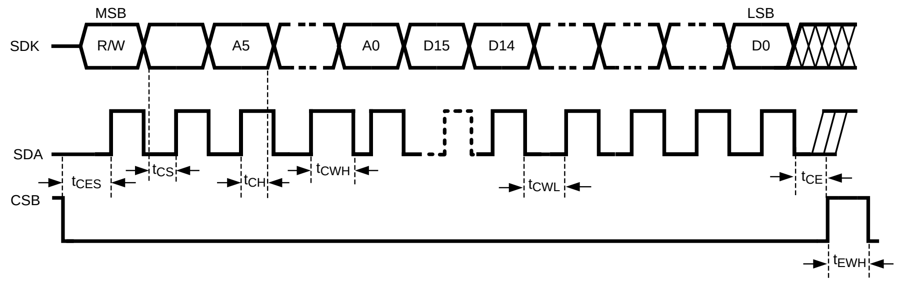


Figure 1. Serial Data Input Timing Diagram

There are several other considerations for writing on the SPI:

- The R/W bit must be set to 0.
- The data on SDA pin is clocked into a shift register on each rising edge on the SCK pin.
- The CSB must be held low for data to be clocked. Device will ignore clock pulses if CSB is held high.
- The CSB transition from high to low must occur when SCK is low.
- When SCK and SDA lines are shared between devices, TI recommends hold the CSB line high on the device that is not to be clocked.

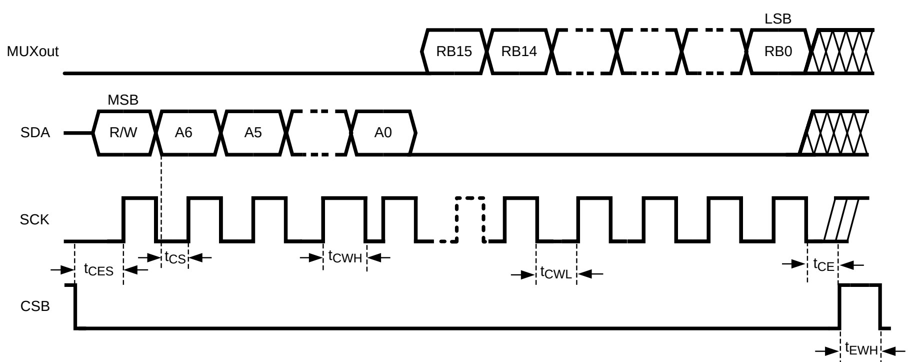


Figure 2. Serial Data Readback Timing Diagram

There are several other considerations for SPI readback:

- The R/W bit must be set to 1.
- The MUXout pin will always be low for the address portion of the transaction.
- The data on SDA is clocked out on the rising edge of SCK.
- The data portion of the transition on the SDA line is always ignored.

6.7 Typical Characteristics

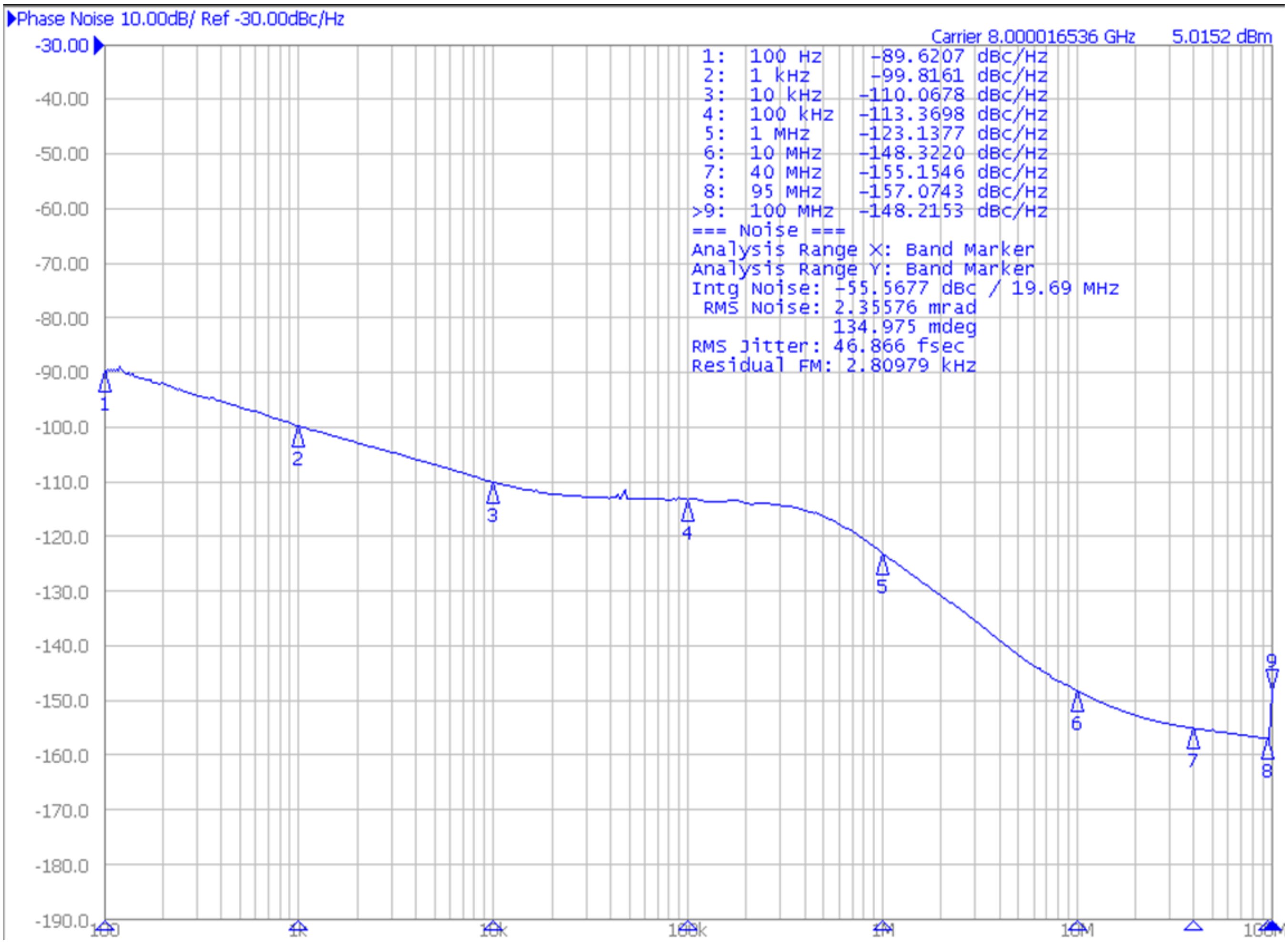


Figure 3. Closed Loop Phase Noise With f_{OSC} = 100 MHz and f_{PD} = 200 MHz

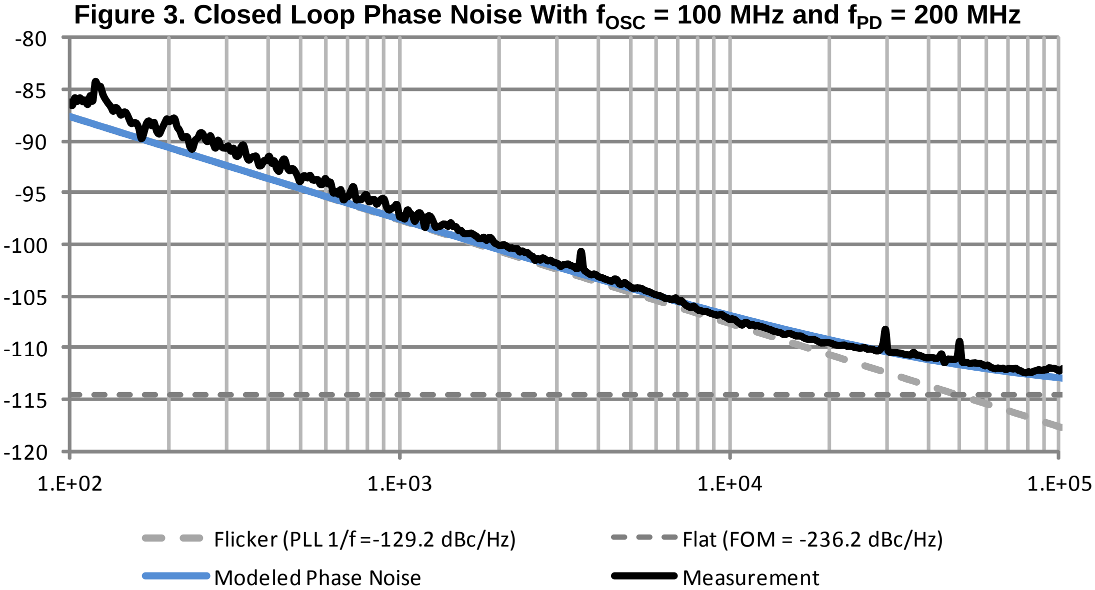


Figure 4. Calculation of PLL Noise Metrics of PLL f_{PD}=100 MHz, f_{VCO} = 12 GHz

Typical Characteristics (continued)

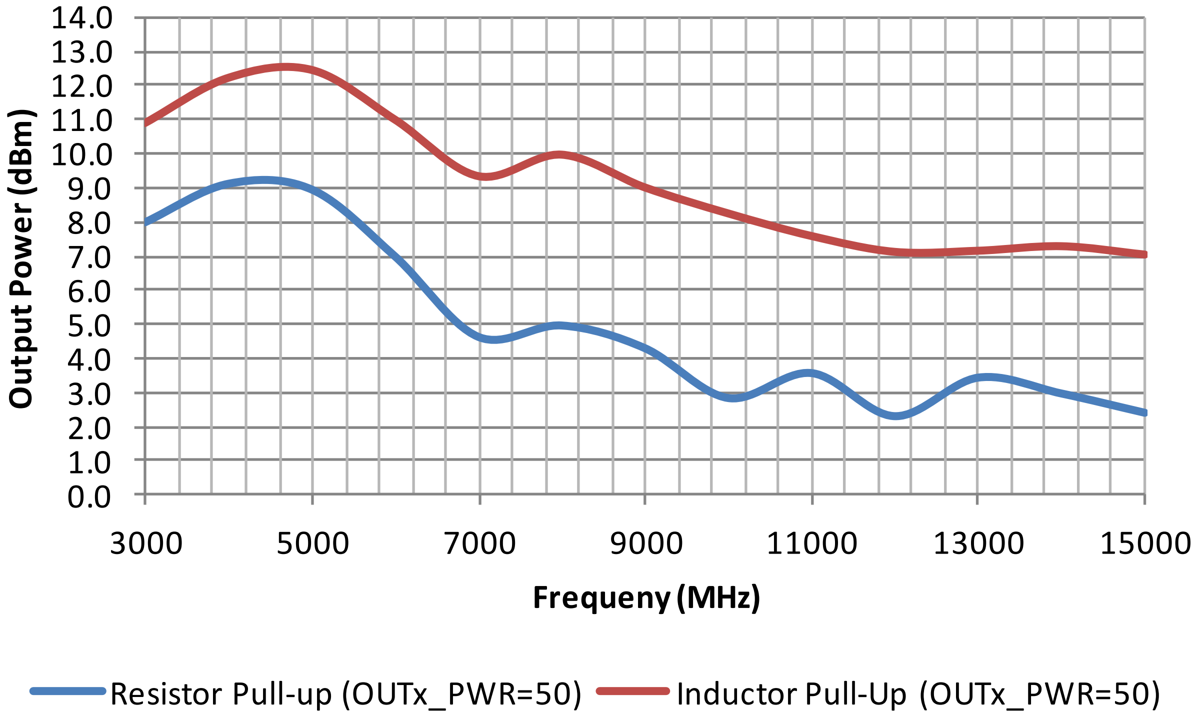


Figure 5. Output Power vs Pullup

Typical Characteristics (continued)

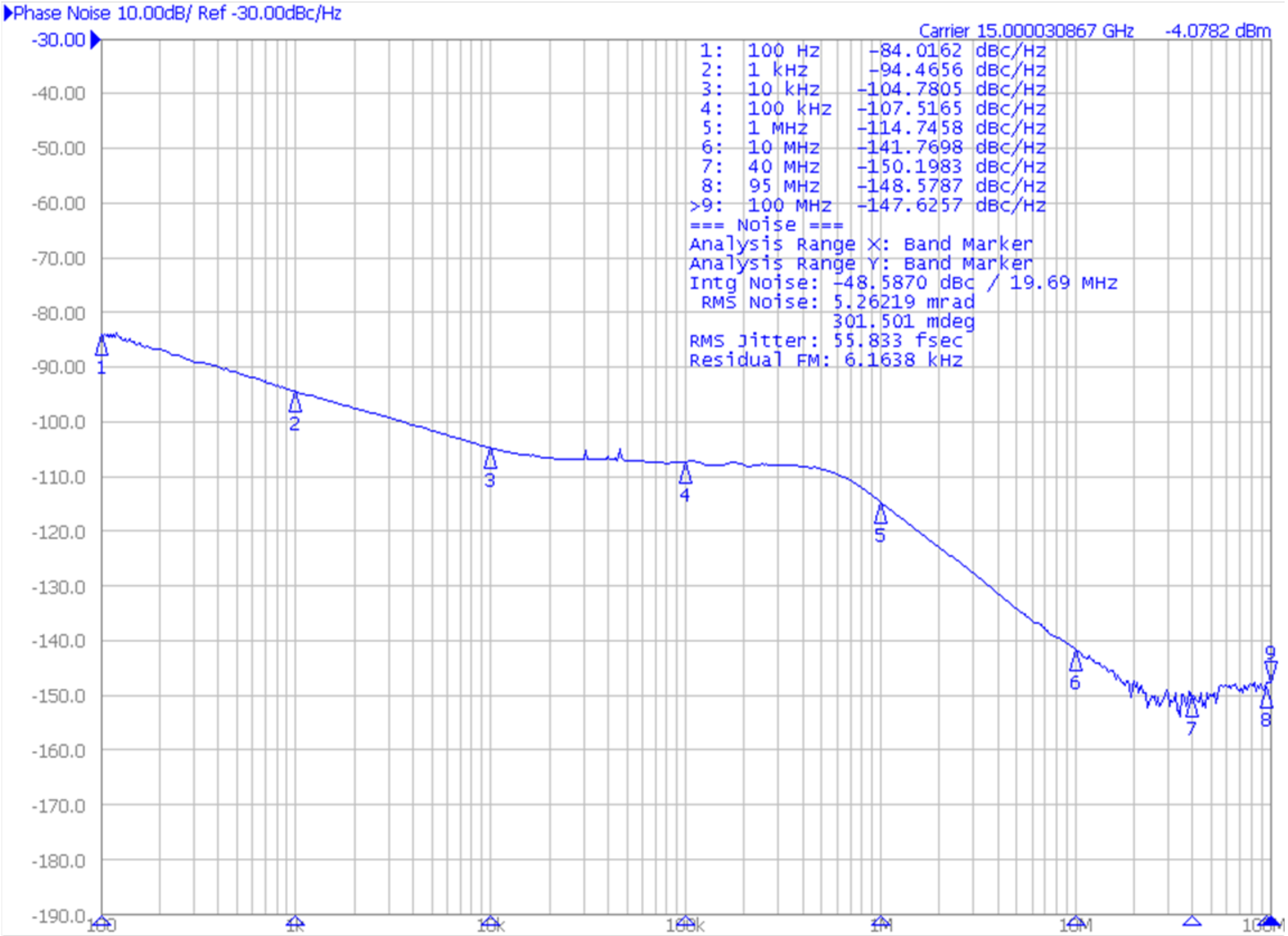


Figure 6. Closed Loop Phase Noise at 15 GHz With f_{OSC} = 100 MHz and f_{PD} = 200 MHz

Typical Characteristics (continued)

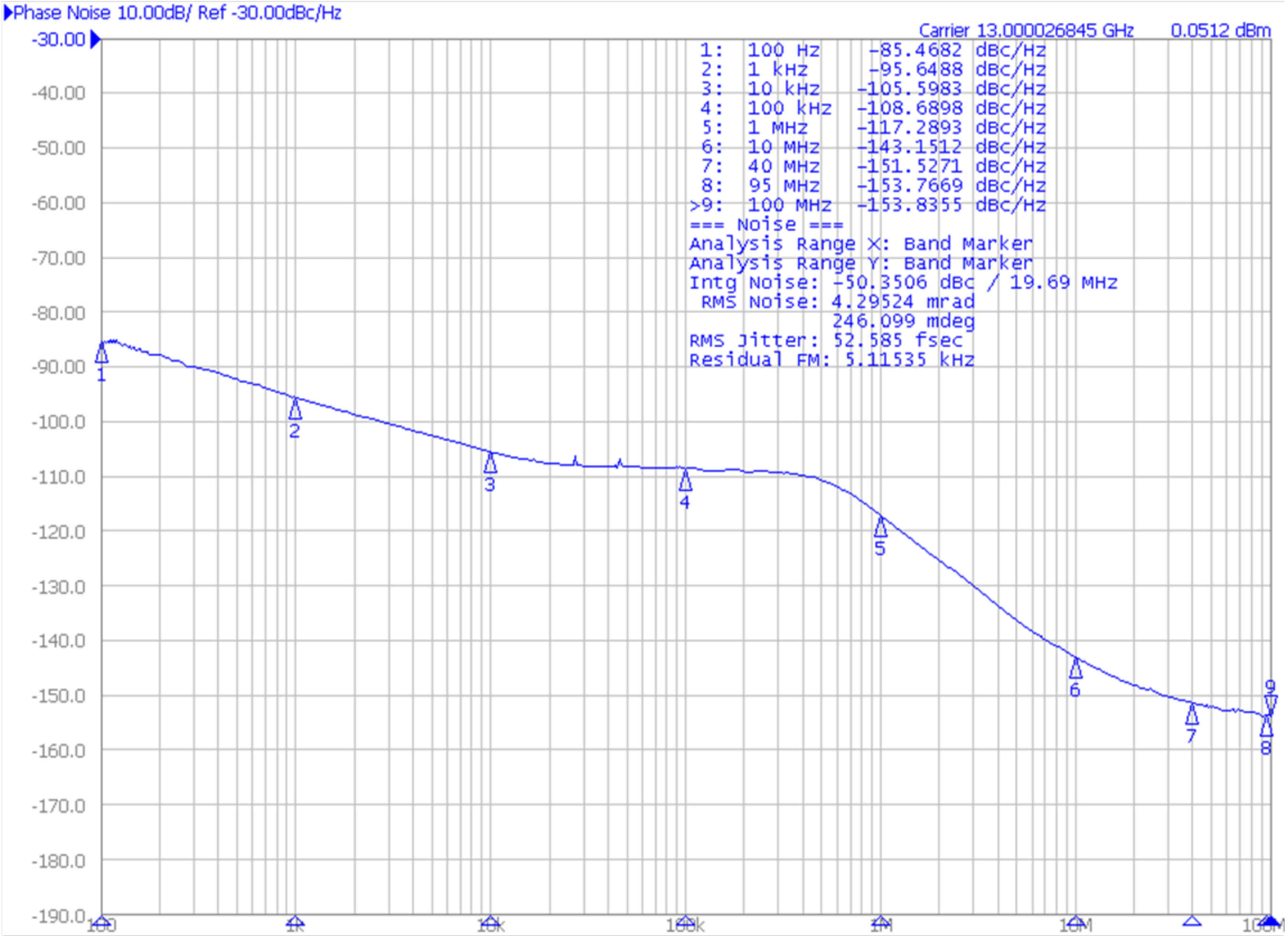


Figure 7. Closed Loop Phase Noise at 13 GHz With f_{OSC} = 100 MHz and f_{PD} = 200 MHz

Typical Characteristics (continued)

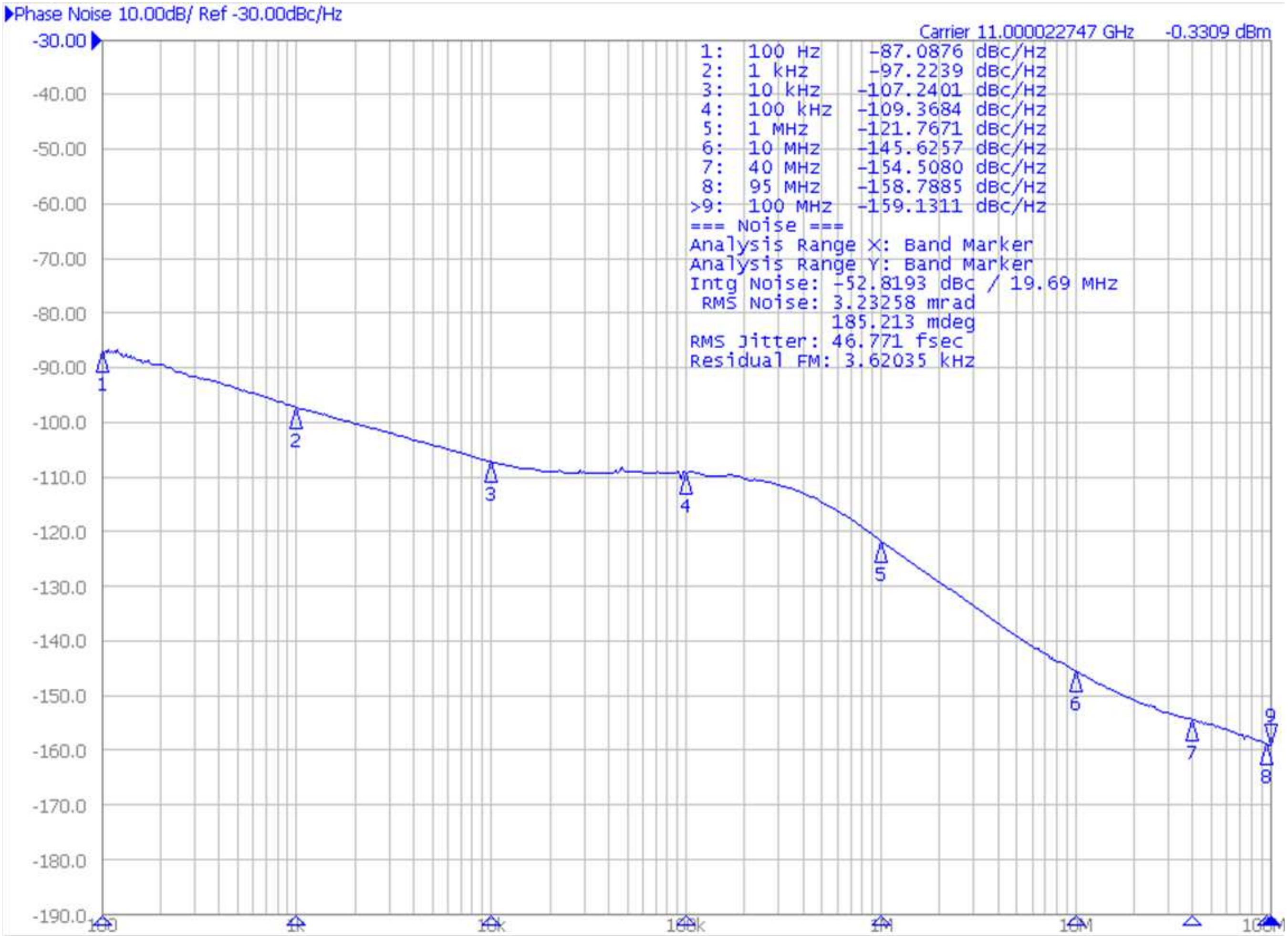


Figure 8. Closed Loop Phase Noise at 11 GHz With f_{OSC} = 100 MHz and f_{PD} = 200 MHz

Typical Characteristics (continued)

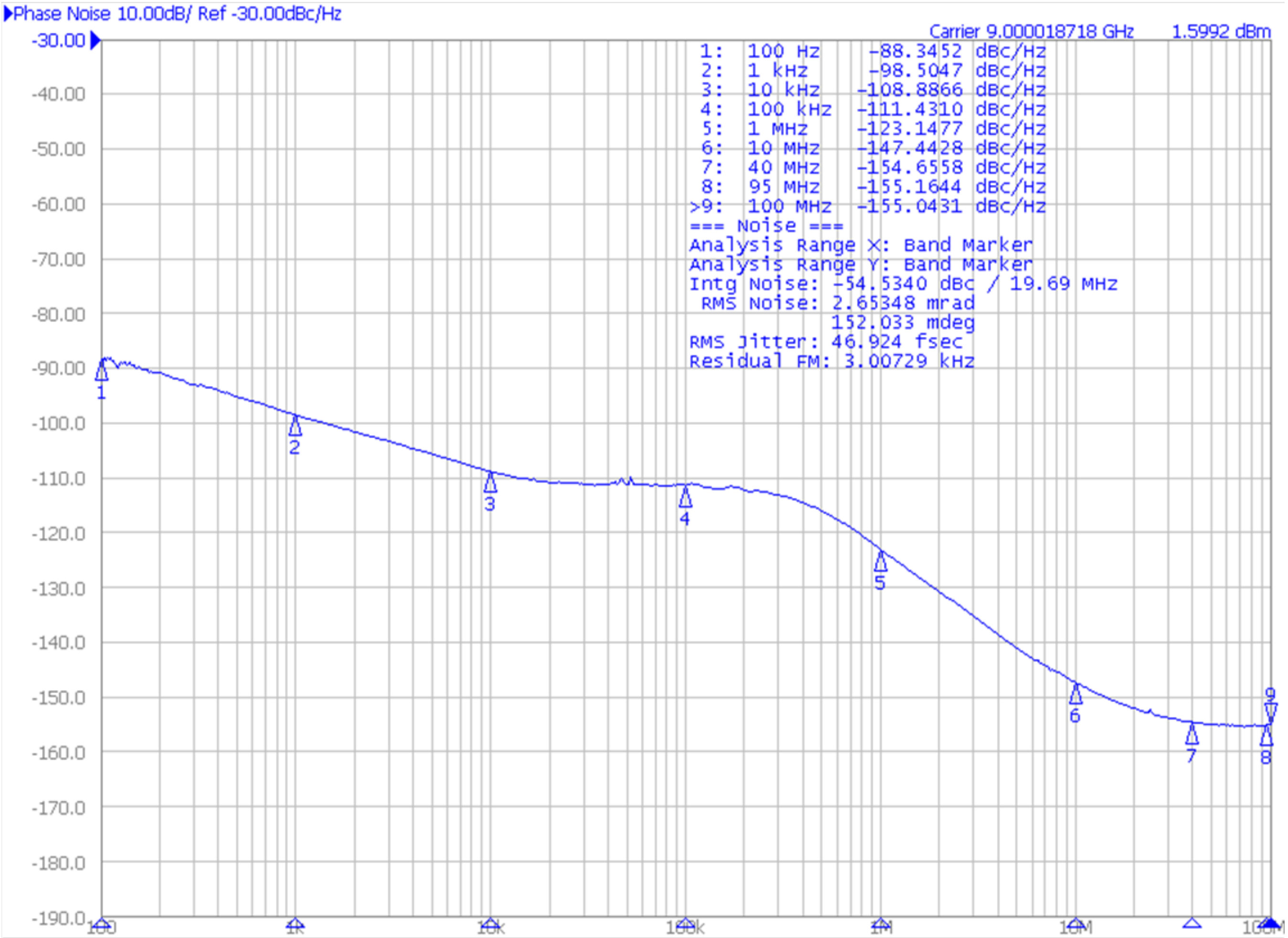


Figure 9. Closed Loop Phase Noise at 9 GHz With f_{OSC} = 100 MHz and f_{PD} = 200 MHz

Typical Characteristics (continued)

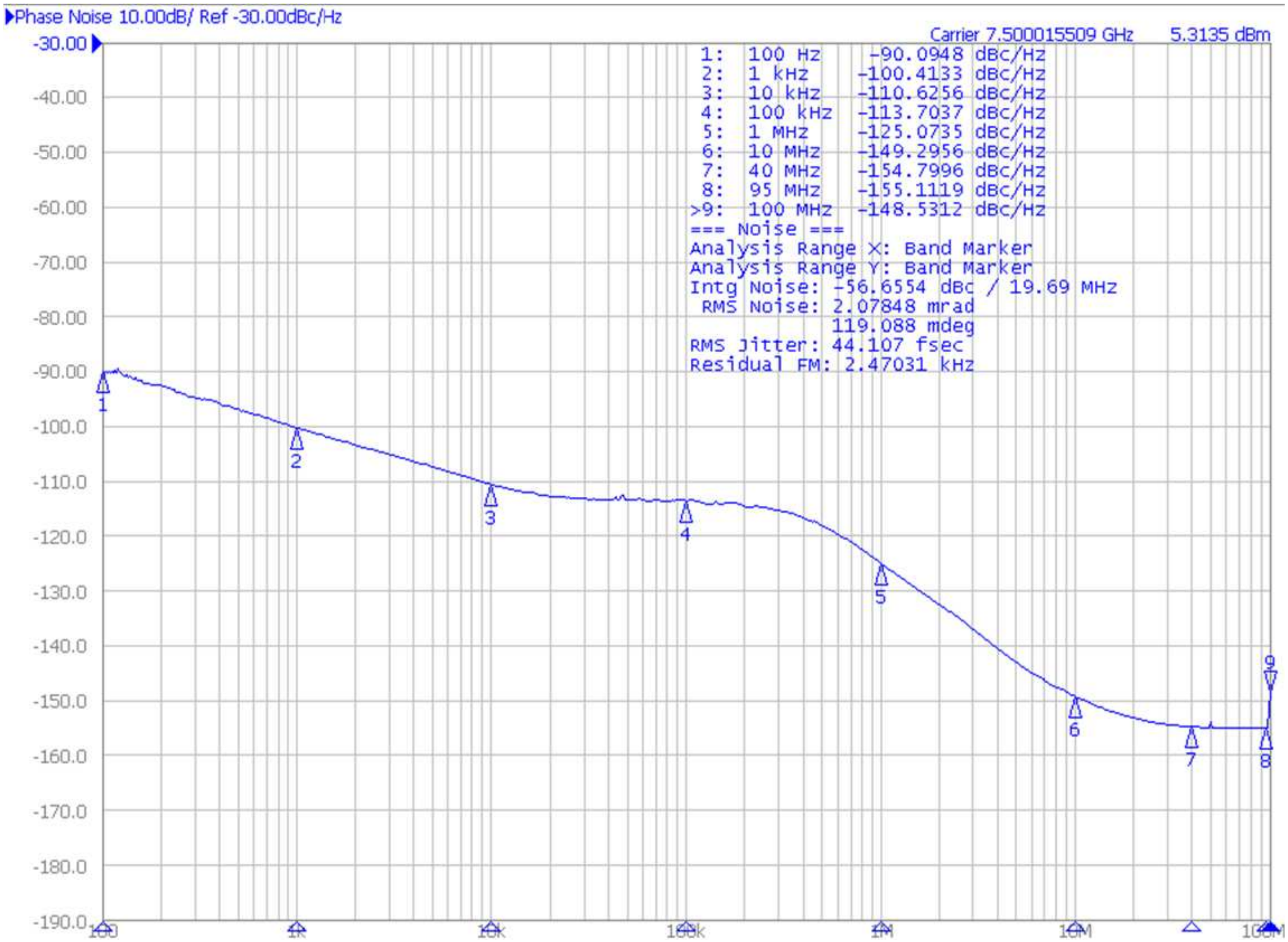


Figure 10. Closed Loop Phase Noise at 7.5 GHz With f_{OSC} = 100 MHz and f_{PD} = 200 MHz

Typical Characteristics (continued)

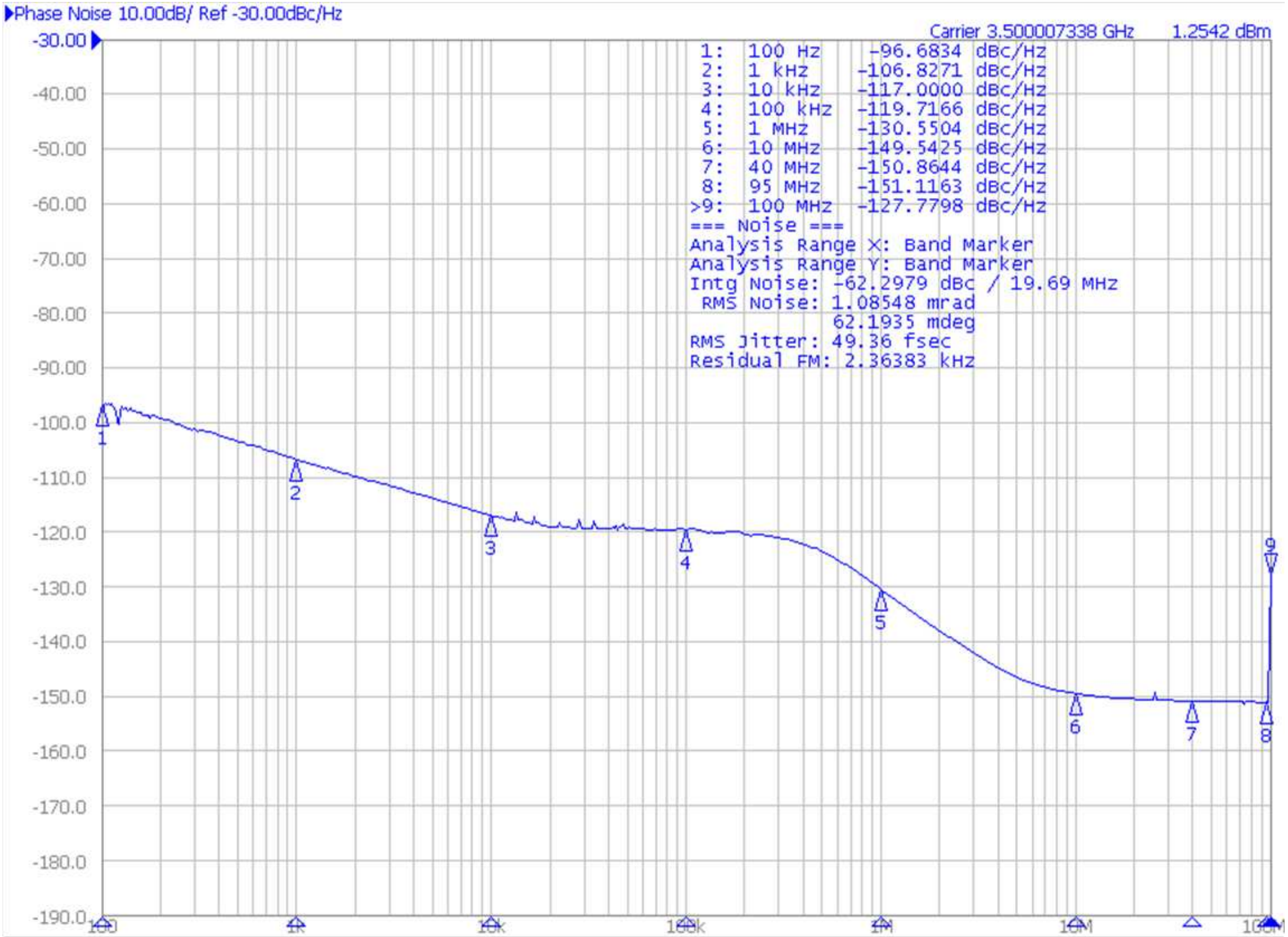


Figure 11. Closed Loop phase noise at 3.5 GHz With f_{VCO} = 100, f_{OSC} = 100 MHz, and f_{PD} = 200 MHz

Typical Characteristics (continued)

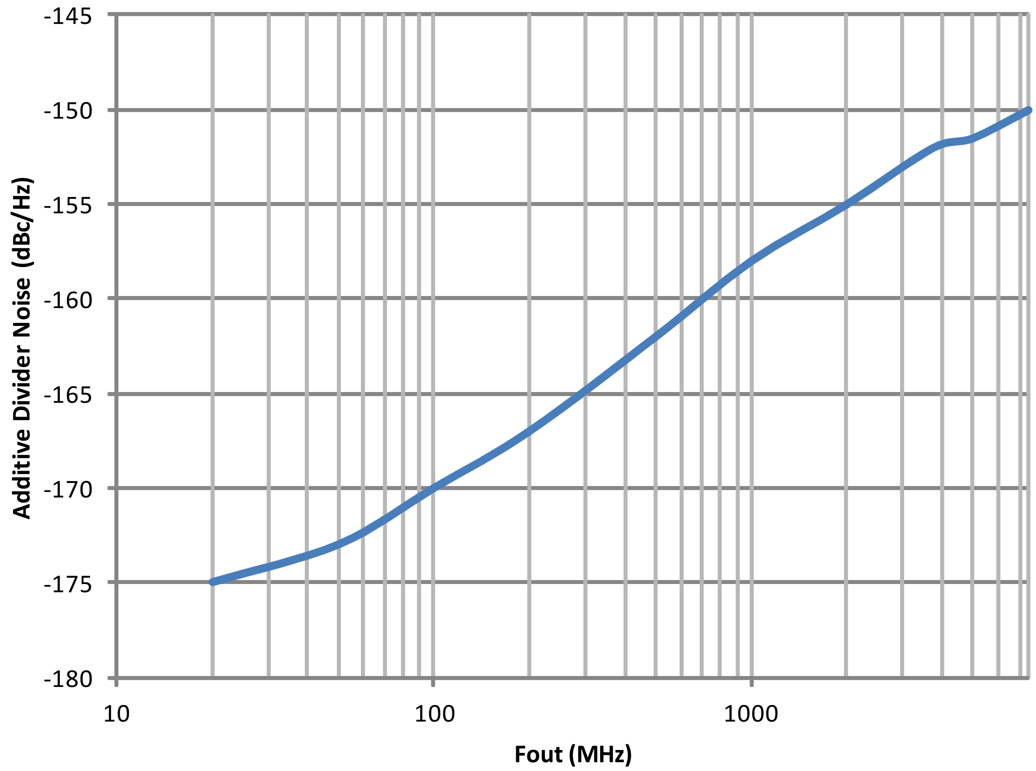


Figure 12. Additive VCO Divider Noise Floor (Adds to the divided far out VCO noise when output divider is used.)

Typical Characteristics (continued)

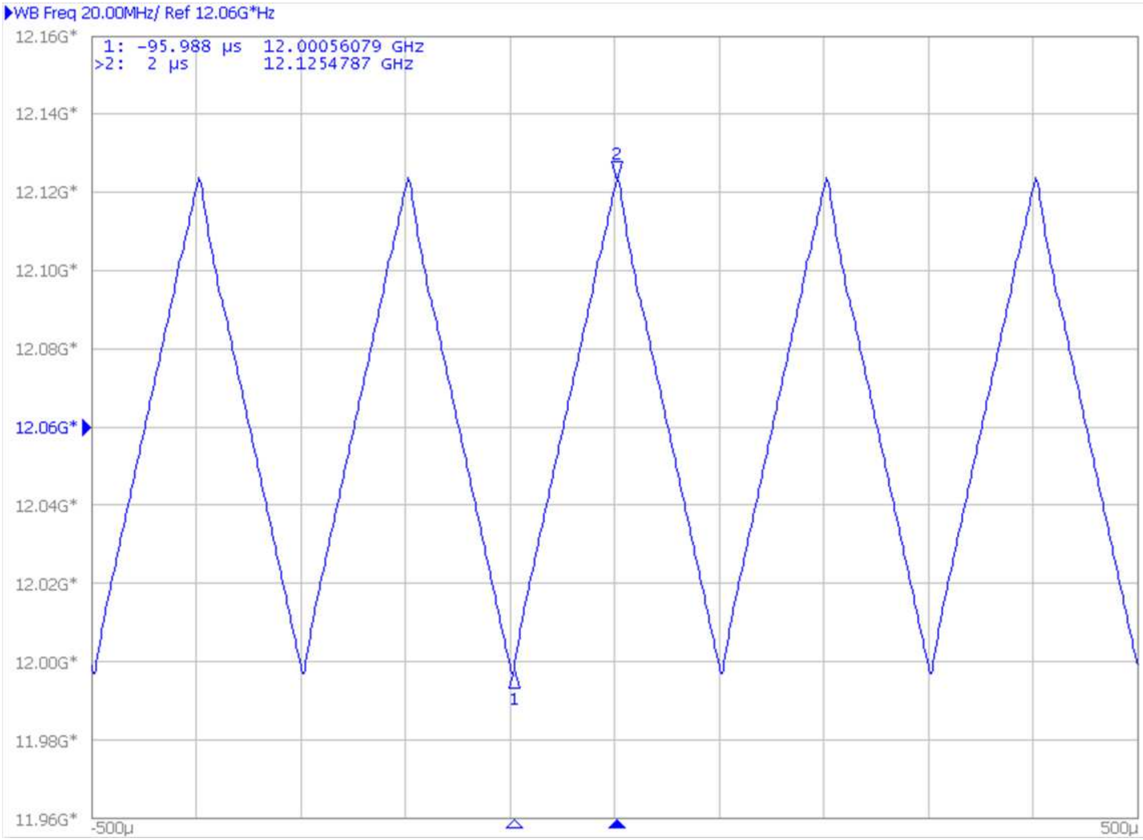


Figure 13. VCO Ramping 12 - 12.125 GHz Without Need to Calibrate

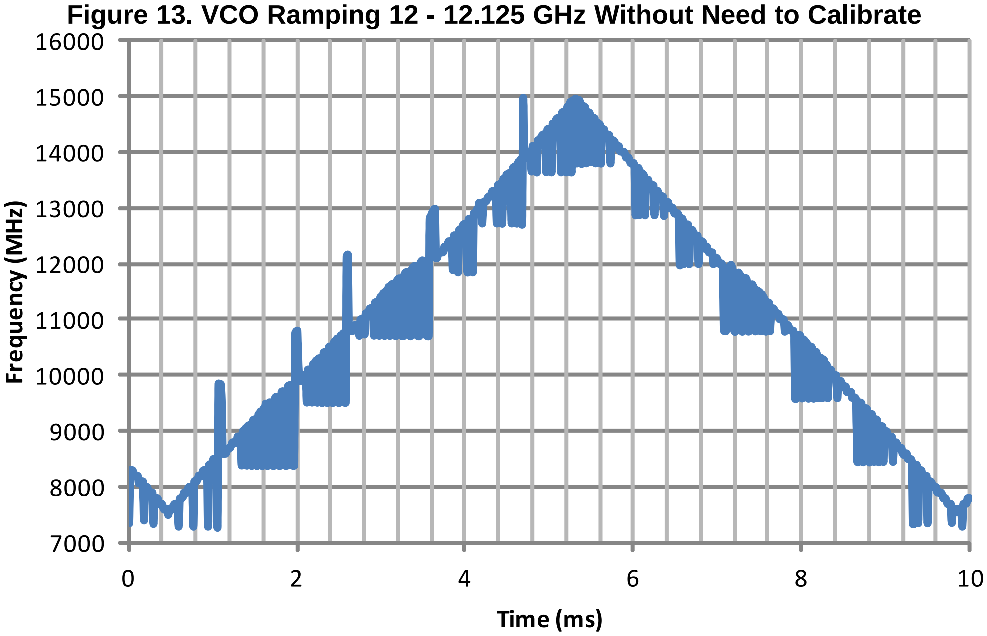


Figure 14. VCO Ramping 7.5 to 15 GHz Triangle Wave with VCO Calibration (The glitches in the plot are due to inability of the measurement equipment to track the VCO while calibrating.)

Typical Characteristics (continued)

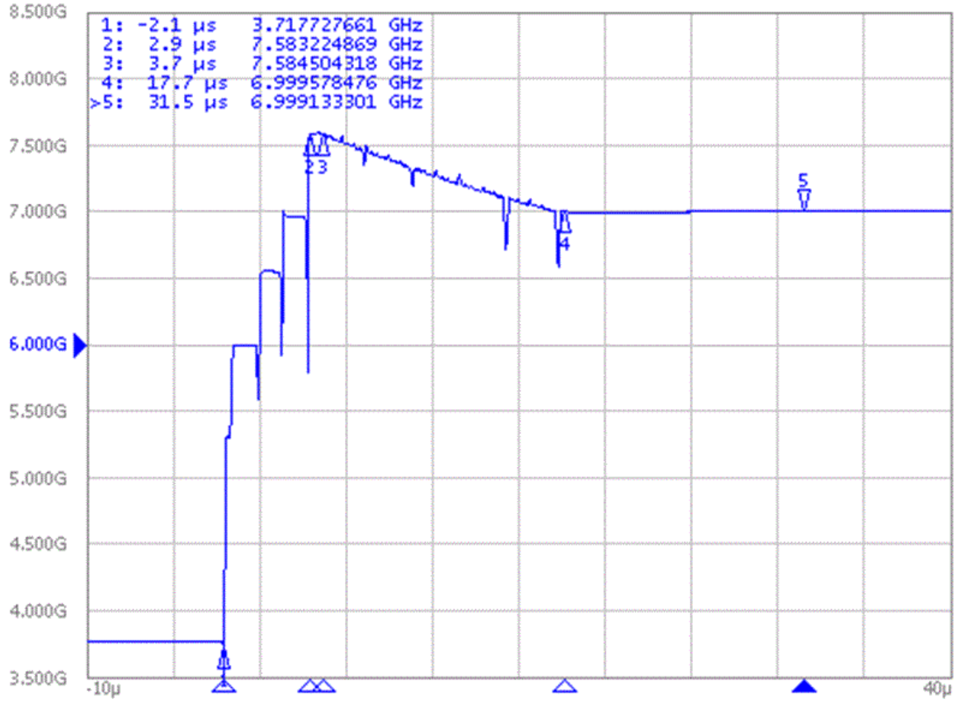


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Figure 15. VCO unassisted calibration from 7.5 - 14 GHz in 33.6 µs CHDIV=2, f_{OSC}=200 MHz, f_{PD}=100 MHz

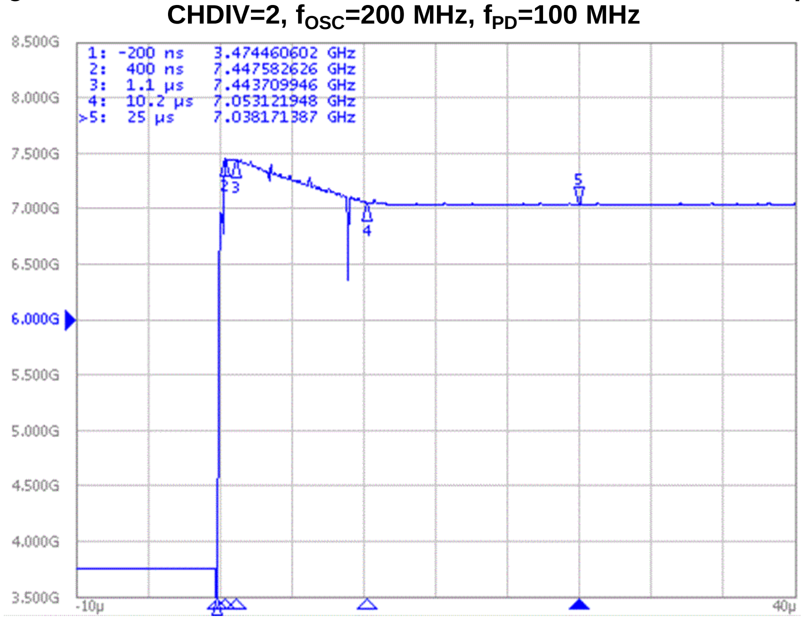

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Figure 16. VCO Calibration with partial assist from 7.5 - 14 GHz in 25.2 µs CHDIV=2, f_{OSC} = 200 MHz, f_{PD} = 100 MHz.

7 Detailed Description

7.1 Overview

The LMX2594 is a high-performance, wideband frequency synthesizer with integrated VCO and output divider. The VCO operates from 7.5 to 15 GHz and this can be combined with the output divider to produce any frequency in the range of 10 MHz to 15 GHz. Within the input path there are two dividers and a multiplier for flexible frequency planning. The multiplier also allows reduction of spurs by moving the frequencies away from the integer boundary.

The PLL is fractional-N PLL with programmable delta-sigma modulator up to 4^{th} order. The fractional denominator is a programmable 32-bit long, which can provide fine frequency steps easily below 1-Hz resolution as well as be used to do exact fractions like 1/3, 7/1000, and many others. The phase frequency detector goes up to 300 MHz in fractional mode or 400 MHz in integer mode, although minimum N divider values must also be taken into account.

For applications where deterministic or adjustable phase is desired, the SYNC pin can be used to get the phase relationship between the OSCin and RFout pins deterministic. Once this is done, the phase can be adjusted in very fine steps of the VCO period divided by the fractional denominator.

The ultra-fast VCO calibration is ideal for applications where the frequency must be swept or abruptly changed. The frequency can be manually programmed, or the device can be set up to do ramps and chirps.

The JESD204B support includes using the RFoutB output to create a differential SYSREF output that can be either a single pulse or a series of pulses that occur at a programmable distance away from the rising edges of the output signal.

The LMX2594 device requires only a single 3.3 V power supply. The internal power supplies are provided by integrated LDOs, eliminating the need for high performance external LDOs.

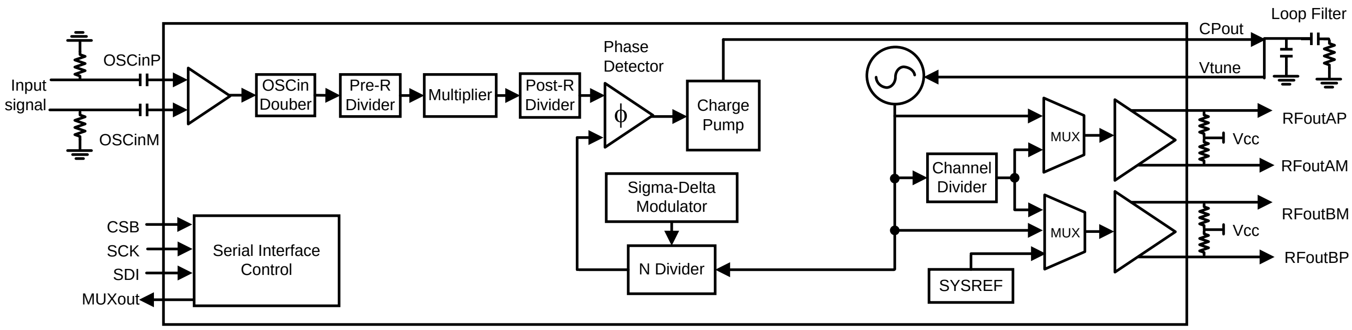
The digital logic for the SPI interface and is compatible with voltage levels from 1.8 to 3.3 V.

Table 1 shows the range of several of the dividers, multipliers, and fractional settings.

Table 1. Range of Dividers, Multipliers, and Fractional Settings

PARAMETER	MIN	MAX	COMMENTS
Outputs enabled	0	2	
OSCin doubler	0 (1X)	1 (2X)	The low noise doubler can be used to increase the phase detector frequency to improve phase noise and avoid spurs. This is in reference to the OSC_2X bit.
Pre-R divider	1 (bypass)	128	Only use the Pre R divider if the multiplier is used and the input frequency is too high for the multiplier.
Multiplier	3	7	This is in reference to the MULT word.
Post-R divider	1 (bypass)	255	The maximum input frequency for the post-R divider is 250 MHz. Use the Pre R divider if necessary.
N divider	≥ 28	524287	The minimum divide depends on modulator order and VCO frequency. See *N Divider and Fractional Circuitry* for more details.
Fractional numerator/ denominator	1 (Integer mode)	$2^{32} - 1 = 4294967295$	The fractional denominator is programmable and can assume any value between 1 and 2^{32}–1; it is not a fixed denominator.
Fractional order	0	4	Order 0 is integer mode and the order can be programmed
Channel divider	1 (bypass)	768	This is the series of several dividers. Also, be aware that above 10 GHz, the maximum allowable channel divider value is 6.
Output frequency	10 MHz	15 GHz	This is implied by the minimum VCO frequency divided by the maximum channel divider value.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reference Oscillator Input

The OSCin pins are used as a frequency reference input to the device. The input is high impedance and requires AC-coupling caps at the pin. The OSCin pins can be driven single-ended with a CMOS clock or XO. Differential clock input is also supported, making it easier to interface with high-performance system clock devices such as TI's LMK series clock devices. As the OSCin signal is used as a clock for the VCO calibration, a proper reference signal must be applied at the OSCin pin at the time of programming FCAL_EN.

7.3.2 Reference Path

The reference path consists of an OSCin doubler (OSC_2X), Pre-R divider, multiplier (MULT) and a Post-R divider.

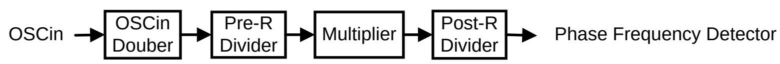


Figure 17. Reference Path Diagram

The OSCin doubler (OSC_2X) can double up low OSCin frequencies. Pre-R (PLL_R_PRE) and Post-R (PLL_R) dividers both divide frequency down while the multiplier (MULT) multiplies frequency up. The purposes of adding a multiplier is to reduce integer boundary spurs or to increase the phase detector frequency. Note that the multiplier cannot be used if the OSCin doubler is used. The phase detector frequency, f_{PD}, is calculated as follows:

$$f_{PD} = f_{OSC} \times OSC\_2X \times MULT / (PLL\_R\_PRE \times PLL\_R) \quad (1)$$

Feature Description (continued)

7.3.2.1 OSCin Doubler (OSC_2X)

The OSCin doubler allows one to double the input reference frequency up to 400 MHz. This doubler adds minimal noise and is useful for raising the phase detector frequency for better phase noise and also to avoid spurs. When the phase-detector frequency is increased, the flat portion of the PLL phase noise improves.

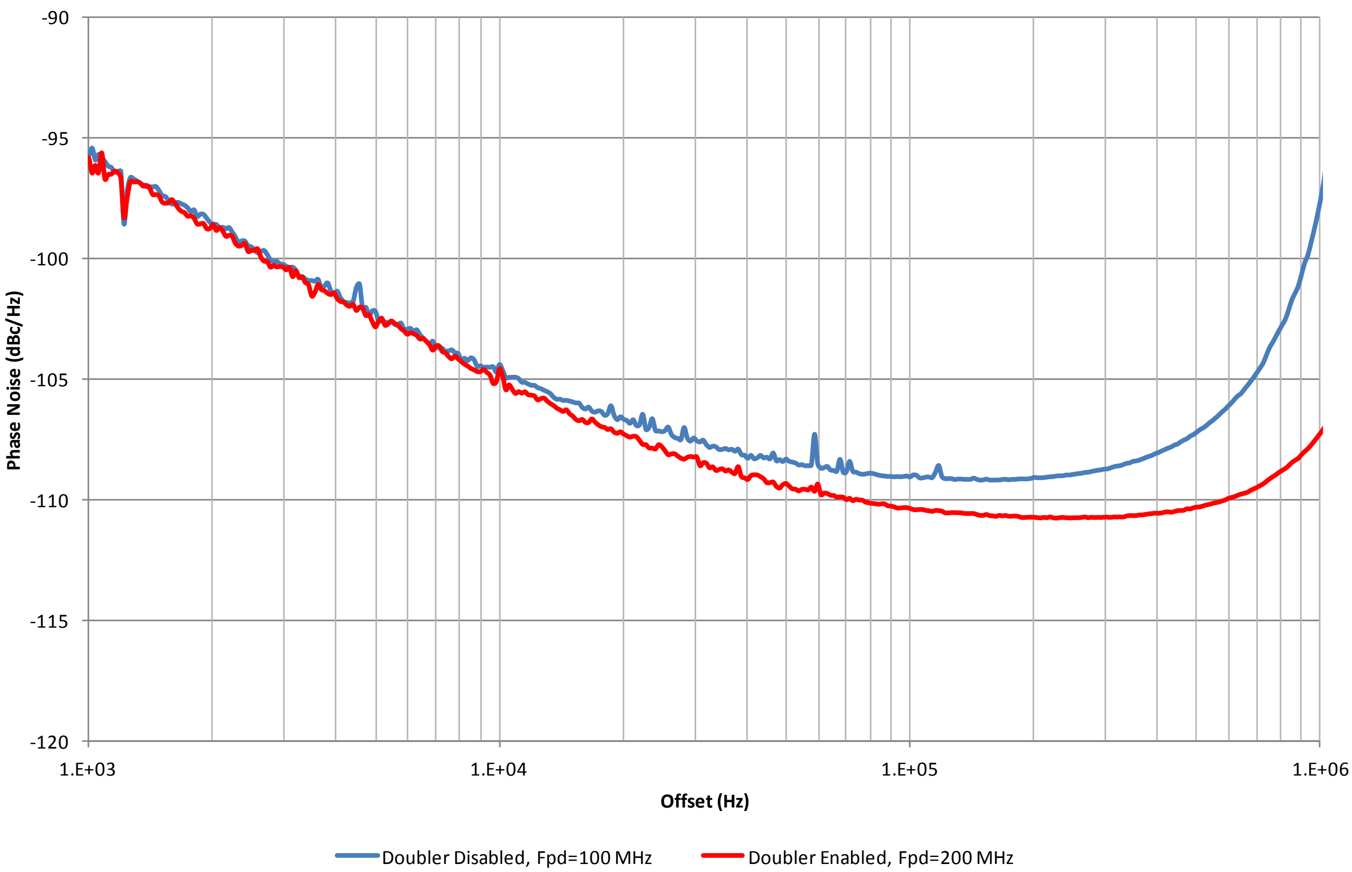


Figure 18. Benefit of Using the OSC_2X Doubler at 14 GHz

7.3.2.2 Pre-R Divider (PLL_R_PRE)

The pre-R divider is useful for reducing the input frequency so that the programmable multiplier (MULT) can be used or to help meet the maximum 250 MHz input frequency limitation to the PLL-R divider. Otherwise, it does not have to be used.

7.3.2.3 Programmable Multiplier (MULT)

The MULT is useful for shifting the phase-detector frequency to avoid integer boundary spurs. The multiplier allows a multiplication of 3, 4, 5, 6, or 7. Be aware that unlike the doubler, the programmable multiplier degrades the PLL figure of merit; however, this only would matter for a clean reference and if the loop bandwidth was wide.

7.3.2.4 Post-R Divider (PLL_R)

The post-R divider can be used to further divide down the frequency to the phase detector frequency. When it is used (PLL_R > 1), the input frequency to this divider is limited to 250 MHz.

Feature Description (continued)

7.3.3 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the Post-R divider and N divider and generates a correction current corresponding to the phase error until the two signals are aligned in phase. This charge-pump current is software programmable to many different levels, allowing modification of the closed loop bandwidth of the PLL. See application section on phase noise due to the charge pump.

7.3.4 N Divider and Fractional Circuitry

The N divider includes fractional compensation and can achieve any fractional denominator from 1 to (2^{32} – 1). The integer portion of N is the whole part of the N divider value, and the fractional portion, N_{frac} = NUM / DEN, is the remaining fraction. In general, the total N divider value is determined by N + NUM / DEN. The N, NUM and DEN are software programmable. The higher the denominator, the finer the resolution step of the output. For example, even when using f_{PD} = 200 MHz, the output can increment in steps of 200 MHz / 2^{32} = 0.047 Hz. Equation 2 shows the relationship between the phase detector and VCO frequencies. Note that in SYNC mode, there is an extra divider that is not shown in Equation 2.

$$f_{VCO} = f_{pd} \times \left(N + \frac{NUM}{DEN} \right) \quad (2)$$

The sigma-delta modulator that controls this fractional division is also programmable from integer mode to fourth order. To make the fractional spurs consistent, the modulator is reset any time that the R0 register is programmed.

The N divider has minimum value restrictions based on the modulator order and VCO frequency. Furthermore, the PFD_DLY_SEL bit must be programmed in accordance to the Table 2.

Table 2. Minimum N Divider Restrictions

FRAC_ORDER	f_{VCO} (MHz)	MINIMUM N	PFD_DLY_SEL
0	≤ 12500	28	1
	> 12500	32	2
1	≤ 10000	28	1
	10000-12500	32	2
	>12250	36	3
2	≤ 10000	32	2
	>10000	36	3
3	≤ 10000	36	3
	>10000	40	4
4	≤ 10000	44	5
	>10000	48	6

7.3.5 MUXout Pin

The MUXout pin can be used to readback programmable states of the device or for lock detect.

Table 3. MUXout Pin Configurations

MUXOUT_SEL	FUNCTION
0	Readback
1	Lock Detect

7.3.5.1 Lock Detect

The MUXout pin can be configured for lock detect done in by reading back the rb_LD_VTUNE field or using the pin as shown in the Table 4.

Table 4. Configuring the MUXout Pin for Lock Detect

FIELD	PROGRAMMING	DESCRIPTION
LD_TYPE	0 = VCO Calibration Status 1 = Vtune	This determines if the lock detect is based on the VCO tuning voltage or at the VCO calibration.
LD_DLY	0 to 65535	Only valid for Vtune lock detect. This is a delay in state machine cycles. The state machine clock frequency is equal to f_{OSC}/CAL_CLK_DIV
OUT_MUTE	0 = Disabled 1 = Enabled	Turns off outputs when lock detect is low.

VCO calibration status lock detect works by indicating a low signal whenever the VCO is calibrating or the LD_DLY counter is running.

Vtune lock detect works by checking the Vtune voltage. Whenever the Vtune voltage is within an acceptable range and the VCO is not calibrating, then Vtune lock detect is high.

7.3.5.2 Readback

The MUXout pin can be configured for to read back useful information from the device. Common uses for readback are:

1. Read back registers to ensure that they have been programmed to the correct value.
2. Read back the lock detect status to determine if the PLL is in lock.
3. Read back VCO calibration information so that it can be used to improve the lock time.
4. Read back information to help troubleshoot.

VCO calibration status lock detect works by indicating a low signal whenever the VCO is calibrating or the LD_DLY counter is running. The delay from the LD_DLY added to the true VCO calibration time (t_{VCOCAL}) so it can be used to account for the analog lock time of the PLL.

Vtune lock detect works by checking the Vtune voltage. Whenever the Vtune voltage is within an acceptable range and the VCO is not calibrating, then Vtune lock detect is high.

7.3.6 VCO (Voltage Controlled Oscillator)

The LMX2594 includes a fully integrated VCO. The VCO takes the voltage from the loop filter and converts this into a frequency. The VCO frequency is related to the other frequencies and as follows:

$$f_{VCO} = f_{PD} \times N \text{ divider} \quad (3)$$

7.3.6.1 VCO Calibration

To reduce the VCO tuning gain and therefore improve the VCO phase-noise performance, the VCO frequency range is divided into several different frequency bands. The entire range, 7.5 to 15 GHz, covers an octave that allows the divider to take care of frequencies below the lower bound. This creates the need for frequency calibration to determine the correct frequency band given a desired output frequency. The frequency calibration routine is activated any time that the R0 register is programmed with the FCAL_EN = 1. It is important that a valid OSCin signal must present before VCO calibration begins.

The VCO also has an internal amplitude calibration algorithm to optimize the phase noise which is also activated any time the R0 register is programmed.

The optimum internal settings for this are temperature dependent. If the temperature is allowed to drift too much without being re-calibrated, some minor phase noise degradation could result. The maximum allowable drift for continuous lock, ΔT_{CL}, is stated in the electrical specifications. For this device, a number of 125°C means the device never loses lock if the device is operated under recommended operating conditions.

The LMX2594 allows the user to assist the VCO calibration. In general, there are three kinds of assistance, as shown in Table 5:

Table 5. Assisting the VCO Calibration Speed

ASSISTANCE LEVEL	DESCRIPTION	PROGRAMMABLE SETTINGS
No assist	User does nothing to improve VCO calibration speed.	QUICK_RECAL_EN=0
Partial assist	Upon every frequency change, before the FCAL_EN bit is checked, the user provides the initial starting point for the VCO core (VCO_SEL), band (VCO_CAPCTRL_STRT), and amplitude (VCO_DACISET_STRT) based on Table 6.	QUICK_RECAL_EN=0
Close Frequency Assist	Upon initialization of the device, user enables QUICK_RECAL_EN bit. The VCO uses the current VCO_CAPCTRL and VCO_AMPCAL settings as the initial starting point.	QUICK_RECAL_EN=1
Full assist	The user forces the VCO core (VCO_SEL), amplitude settings (VCO_DACISET), and frequency band (VCO_CAPCTRL) and manually sets the value.	VCO_SEL_FORCE=1 VCO_DACISET_FORCE=1 VCO_CAPCTRL_FORCE=1

To do the partial assist for the VCO calibration, follow this procedure:

1. Determine VCO Core

   Find a VCO Core that includes the desired VCO frequency. If at the boundary of two cores, choose based on phase noise or performance.

2. Calculate the VCO CapCode as follows

   $VCO\_CAPCTRL\_STRT = round\ (C_{CoreMin} – (C_{CoreMin} – C_{CoreMax}) \times (f_{VCO} – f_{CoreMin}) / (f_{CoreMax} – f_{CoreMin}))$

3. Get the AMPCal Setting from the table

   $VCO\_AMPCAL = round\ (A_{CoreMin} + (A_{CoreMax} – A_{CoreMin}) \times (f_{VCO} – f_{CoreMin})/(f_{CoreMax} – f_{CoreMin}))$

Table 6. VCO Core Ranges

VCO Core	$f_{CoreMin}$	$f_{CoreMax}$	$C_{CoreMin}$	$C_{CoreMax}$	$A_{CoreMin}$	$A_{CoreMax}$
VCO 1	7500	8600	164	12	299	240
VCO 2	8600	9800	165	16	356	247
VCO 3	9800	10800	158	19	324	224
VCO 4	10800	12000	140	0	383	244
VCO 5	12000	12900	183	36	205	146
VCO 6	12900	13900	155	6	242	163
VCO 7	13900	15000	175	19	323	244

NOTE

In the range of 11900 to 12100 MHz, VCO assistance cannot be used, and the settings must be VCO_SEL = 4, VCO_DACISET_STRT = 300, and VCO_CAPCTRL_STRT = 1. Outside this range, in the partial assist for the VCO calibration, the VCO calibration is run. This means that if the settings are incorrect, the VCO still locks with the correct settings; the only consequence is that the calibration time might be a little longer. The closer the calibration settings are to the true final settings, the faster the VCO calibration will be.

7.3.6.2 Determining the VCO Gain

The VCO gain varies between the seven cores and is the lowest at the lowest end of the band and highest at the highest end of each band. For a more accurate estimation, use Table 7:

Table 7. VCO Gain

f1	f2	Kvco1	Kvco2
7500	8600	79	113
8600	9800	81	99
9800	10800	88	130
10800	12000	182	225
12000	12900	195	250
12900	13900	250	250

Based in this table, the VCO gain can be estimated for an arbitrary VCO frequency of f_{VCO} as:

$$Kvco = Kvco1 + (Kvco2 - Kvco1) \times (f_{VCO} – f1) / (f2 – f1) \quad (4)$$

7.3.7 Channel Divider

To go below the VCO lower bound of 7.5 GHz, the channel divider can be used. The channel divider consists of four segments, and the total division value is equal to the multiplication of them. Therefore, not all values are valid.

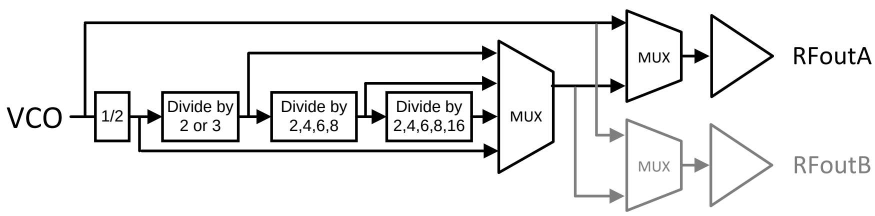


Figure 19. Channel Divider

When the channel divider is used, there are limitations on the values. Table 8 shows how these values are implemented and which segments are used.

Table 8. Channel Divider Segments

EQUIVALENT DIVISION VALUE	FREQUENCY LIMITATION	OutMin (MHz)	OutMax (MHz)	CHDIV[4:0]	SEG0	SEG1	SEG2	SEG3
2	None	3750	7500	0	2	1	1	1
4		1875	3750	1	2	2	1	1
6		1250	2500	2	2	3	1	1

Table 8. Channel Divider Segments (continued)

EQUIVALENT DIVISION VALUE	FREQUENCY LIMITATION	OutMin (MHz)	OutMax (MHz)	CHDIV[4:0]	SEG0	SEG1	SEG2	SEG3
8	$f_{VCO} \leq 10$ GHz	937.5	1250	3	2	2	2	1
12		625	833.333	4	2	3	2	1
16		468.75	625	5	2	2	4	1
24		312.5	416.667	6	2	2	6	1
32		234.375	312.5	7	2	2	8	1
48		125.25	208.333	8	2	3	8	1
64		117.1875	156.25	9	2	2	8	2
72		104.157	138.889	10	2	3	6	2
96		78.125	104.167	11	2	3	8	2
128		58.594	78.125	12	2	2	8	4
192		39.063	52.083	13	2	2	8	6
256		29.297	39.063	14	2	2	8	8
384		19.531	26.042	15	2	3	8	8
512		14.648	19.531	16	2	2	8	16
768		9.766	13.021	17	2	3	8	16
Invalid	n/a	n/a	n/a	18-31	n/a	n/a	n/a	n/a

The channel divider is powered up whenever an output (OUTx_MUX) is selected to the channel divider or SysRef, regardless of whether it is powered down or not. When an output is not used, TI recommends selecting the VCO output to ensure that the channel divider is not unnecessarily powered up.

Table 9. Channel Divider

OUTA MUX	OUTB MUX	CHANNEL DIVIDER
Channel Divider	X	Powered up
X	Channel Divider or SYSREF	Powered up
All Other Cases		Powered down

7.3.8 Output Buffer

The RF output buffer type is open collector so it requires an external pullup to Vcc. This component may be a 50-Ω resistor to give a nice 50-Ω output impedance, or an inductor. The inductor has poor output impedance, but allows higher output power. The output power can be programmed to various levels or disabled while still keeping the PLL in lock. If using a resistor, limit OUTx_PWR setting to 40; higher than this tends to actually reduce power.

7.3.9 Powerdown Modes

The LMX2594 can be powered up and down using the CE pin or the POWERDOWN bit. When the device comes out of the powered down state, either by resuming the POWERDOWN bit to zero or by pulling back CE pin HIGH (if it was powered down by CE pin), register R0 must be programmed with FCAL_EN high again to re-calibrate the device.

7.3.10 Phase Synchronization

7.3.10.1 General Concept

The SYNC pin allows one to synchronize the LMX2594 such that the delay from the rising edge of the OSCin signal to the output signal is deterministic. Initially, the devices are locked to the input, but are not synchronized. The user sends a synchronization pulse that is reclocked to the next rising edge of the OSCin pulse. After a given time, t_1, the phase relationship from OSCin to f_{OUT} will be deterministic. This time is dominated by the sum of the VCO calibration time, the analog setting time of the PLL loop, and the MASH_RST_CNT if used in fractional mode.

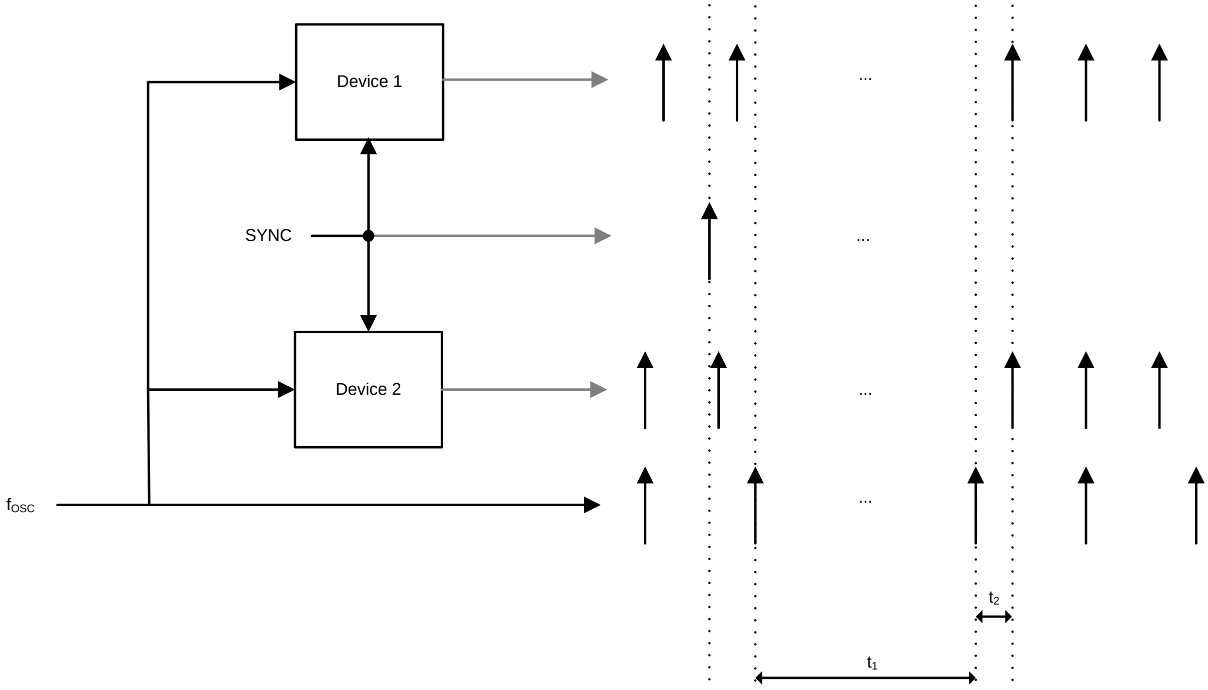


Figure 20. Devices Are Now Synchronized to OSCin Signal

When the SYNC feature is enabled, part of the channel divide is included in the feedback path.

Table 10. Included Divide

OUTA_MUX / OUTB_MUX	CHANNEL DIVIDER	INCLUDED DIVIDE
Neither one has the channel divider or SysRef selected	x	None
At least one is selecting the channel divider or SYSREF	Divisible by 3, but NOT 24 or 192	SEG0 × SEG1 = 6
	All other values	SEG0 × SEG1 = 4

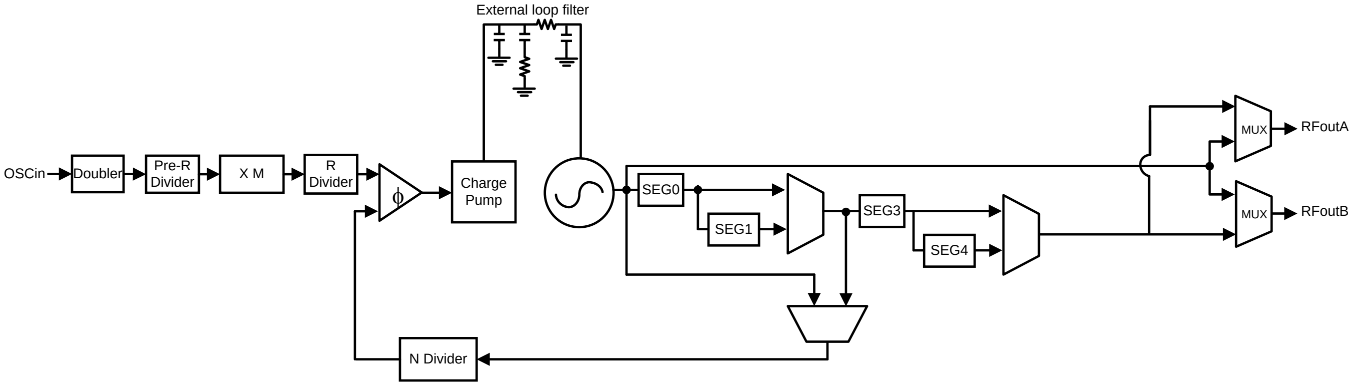


Figure 21. Phase SYNC Diagram

7.3.10.2 Categories of Applications for SYNC

The requirements for SYNC depend on certain setup conditions. In cases that the SYNC is not timing critical, it can be done through software by toggling the VCO_PHASE_SYNC bit from 0 to 1. When it is timing critical, then it must be done through the pin and the setup and hold times for the OSCin pin are critical. The Figure 22 gives the different categories.

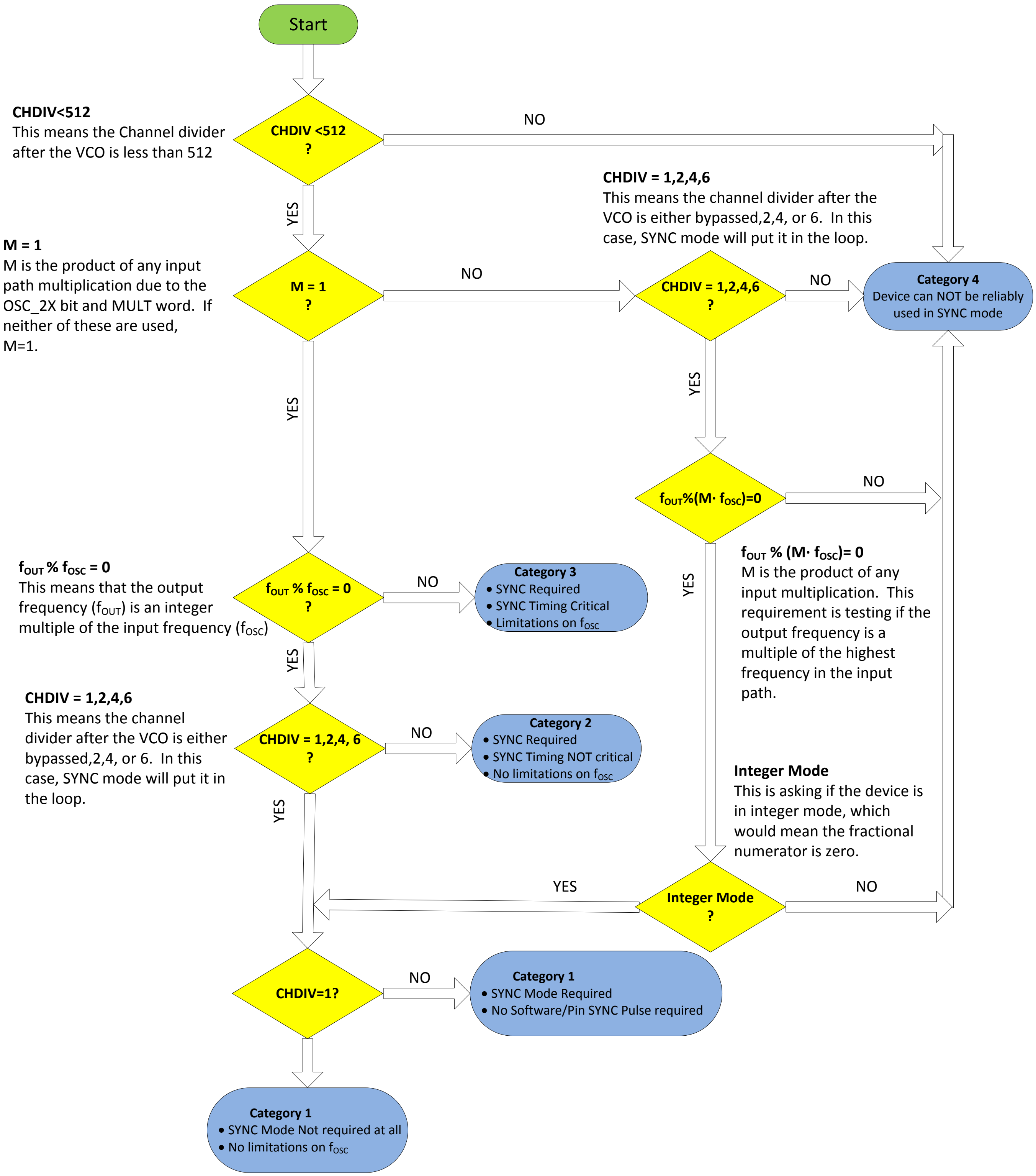


Figure 22. Determining the SYNC Category

7.3.10.3 Procedure for Using SYNC

This procedure must be used to put the device in SYNC mode.

1. Use the flowchart to determine the SYNC category.
2. Make determinations for OSCin and using SYNC based on the category
   (a) If Category 4, SYNC cannot be performed in this setup.
   (b) If category 3, ensure that the maximum f_{OSC} frequency for SYNC is not violated and there are hardware accommodations to use the SYNC pin.
3. If the channel divide is used, determine the included channel divide value which will be 2 × SEG0 of the channel divide:
   (a) If neither OUTA_MUX nor OUTB_MUX is selected to channel divider, then the included divide is one.
   (b) If one of them is, then the included channel divide value will be 2 × SEG0.
4. If not done already, divide the N divider and fractional values by the included channel divide to account for the included channel divide.
5. Program the device with the VCO_PHASE_SYNC = 1. Note that this does not count as applying a SYNC to device (for category 2).
6. Apply the SYNC, if required
   (a) If category 2, VCO_PHASE_SYNC can be toggled from 0 to 1. Alternatively, a rising edge can be sent to the SYNC pin and the timing of this is not critical.
   (b) If category 3, the SYNC pin must be used, and the timing must be away from the rising edge of the OSCin signal.

7.3.10.4 SYNC Input Pin

The SYNC input pin can be driven either in CMOS or LVDS mode. However, if not using SYNC mode (VCO_PHASE_SYNC = 0), then the INPIN_IGNORE bit must be set to one, otherwise it causes issues with lock detect. If the pin is desired for to be used and VCO_PHASE_SYNC=1, then set INPIN_IGNORE = 0. LVDS or CMOS mode may be used. LVDS works to 250 mVPP, but is not ensured in production.

7.3.11 Phase Adjust

The LMX2594 can use the sigma-delta modulator to adjust the output signal phase with respect to the input reference. The phase shift every time you write the value of MASH SEED is:

$$\text{Phase shift in degrees} = 360 \times (\text{MASH\_SEED} / \text{PLL\_DEN}) \times (\text{IncludedDivide}/\text{CHDIV}) \quad (5)$$

Example:

Mash seed = 1

Denominator = 12

Channel divider = 16

Phase shift (VCO_PHASE_SYNC=1) = 360 × (1/12) × (1/16) = 1.875 degrees

Phase Shift (VCO_PHASE_SYNC=1) = 360 × (1/12) × (4/16) = 7.5 degrees

Phase shift can be done with a FRAC_NUM=0, but FRAC_ORDER must be greater than zero. In the case of one output being set to the VCO and the other output unused, the unused output can powered down but directed to the channel divider to put part of this in the loop, which can sometimes be used to create a fraction. For the phase adjust, the condition PLL_DEN > PLL_NUM + MASH_SEED must be satisfied.

7.3.12 Ramping Function

The LMX2594 supports the ability to make ramping waveforms using manual mode or automatic mode. In manual mode, the user defines a step and uses the RampClk and RampDir pins to create the ramp. In automatic mode, the user sets up the ramp with up to two linear segments in advance and the device automatically creates this ramp. Table 11 fields apply in both automatic mode and manual pin mode.

Table 11. Ramping Field Descriptions

FIELD	PROGRAMMING	DESCRIPTION
GENERAL COMMANDS		
RAMP_EN	0 = Disabled 1 = Enabled	RAMP_EN must be 1 for any ramping functions to work.
RAMP_MANUAL	0 = Automatic ramping mode 1 = Manual pin ramping mode	In automatic ramping mode, the ramping is automatic and the clock is based on the phase detector. In manual pin ramping mode, the clock is based on rising edges on the RampCLk pin.
RAMPx_INC	0 to $2^{30} – 1$	This is the amount the fractional numerator is increased for each phase detector cycle in the ramp.
RAMPx_DLY	0 to 65535	This is the length of the ramp in phase detector cycles.
DEALING WITH VCO CALIBRATION		
RAMP_THRESH	0 to $\pm 2^{32}$	Whenever the fractional numerator changes this much (either positive or negative) because the VCO was last calibrated, the VCO is forced to recalibrate.
RAMP_TRIG_CAL	0 = Disabled 1 = Enabled	When enabled, the VCO is forced to re-calibrate at the beginning each ramp. This only applies in automatic ramping mode.
PLL_DEN	4294967295	In ramping mode, the denominator must be fixed to this forced value of $2^{32} – 1$. However, the effective denominator in ramping mode is 2^{24}.
LD_DLY	0	This must be zero to avoid interfering with calibration.
RAMP LIMITS		
RAMP_LIMIT_LOW RAMP_LIMIT_HIGH	0 to 2^{31}	2's complement of the total value of the ramp low and high limits can never go beyond. If this value is exceeded, then the frequency is limited.

Table 12. General Restrictions for Ramping

RULE	RESTRICTION	EXPLANATION
Phase Detector Frequency	$f_{OSC} / 2^{CAL\_CLK\_DIV} \leq f_{PD} \leq 125$ MHz	**Minimum Phase Detector Frequency when Ramping** The phase detector frequency cannot be less than the state machine clock frequency. The state machine clock frequency is calculated from expression on the left-hand side of the inequality. This is satisfied provided there is no division in the input path. However, if the PLL R divider is used, it is necessary to adjust CAL_CLK_DIV to satisfy this constraint. Also, this implies a maximum total division in the input path of 8. **Maximum Phase Detector Frequency** TI recommends that phase-detector frequency be less or equal than 125 MHz because if the phase detector frequency is too high, it can lead to distortion in the ramp. Higher phase-detector frequency frequencies may be possible, but this distortion is application specific.

7.3.12.1 Manual Pin Ramping

Manual pin ramping is enabled by setting RAMP_EN = 1 and RAMP_MODE = 1. In this mode, the ramp is clocked by rising edges applied to the RampCLk pin, and the RampDir pin controls the size of the change. If a rising edge is seen on the RampCLk pin while the VCO is calibrating, then this rising edge is ignored. The frequency for the RampCLK must be limited to a frequency of 250 kHz or less, and the rising edge of the RampDir signal must be targeted to the falling edge of the RampCLK pin.

Table 13. RAMP_INC

RampDir PIN	STEP SIZE
Low	Add RAMP0_INC
High	Add RAMP1_INC

7.3.12.1.1 Manual Pin Ramping Example

In this ramping example, assume that we want to use the pins for UP/Down control of the ramp for 10 MHz steps and the phase detector is 100 MHz.

Table 14. Step Ramping Example

FIELD	PROGRAMMING	DESCRIPTION
RAMP_EN	1 = Enabled	
RAMP_MANUAL	1 = Manual pin ramping mode	
RAMP0_INC	1677722	(10 MHz)/ (100 MHz) × 16777216 = 1677722 2's complement = 1677722
RAMP1_INC	1072064102	(–10 MHz)/ (100 MHz) × 16777216 = –1677722 2's complement = 2^30 – 1677722 = 1072064102
RAMP_TRIG_CAL	1	Re-calibrate at every clock cycle

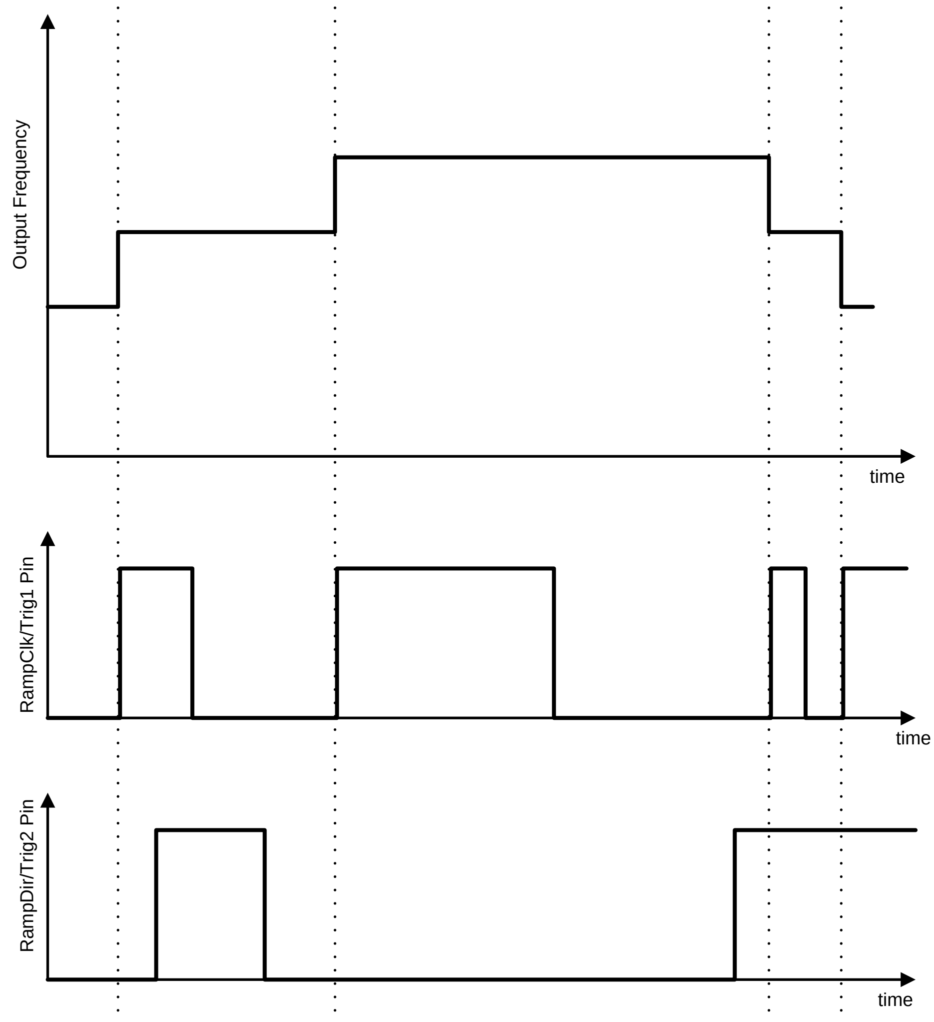


Figure 23. Step Ramping Example

7.3.12.2 Automatic Ramping

Automatic ramping is enabled when RAMP_EN=1 and RAMP_MODE = 0. The action of programming FCAL = 1 starts the ramping. In this mode, there are two ramps that one can set the length and frequency change. In addition to this, there are ramp limits that can be used to create more complicated waveforms.

Automatic ramping can really be divided into two classes depending on if the VCO must calibrate in the middle of the ramping waveform or not. If the VCO can go the entire range without calibrating, this is calibration-free ramping, which is shown in *Typical Characteristics*. Note that this range is less at hot temperatures and for lower frequency VCOs. This range is not ensured, so margin must be built into the design.

For waveforms that are NOT calibration free, the slew rate of the ramp must be kept less than 250 kHz/µs. Also, for all automatic ramping waveforms, be aware that there is a very small phase disturbance as the VCO crosses over the integer boundary, so one might consider using the input multiplier to avoid these or timing the VCO calibrations at integer boundaries.

Table 15. Automatic Ramping Field Descriptions

FIELD	PROGRAMMING	DESCRIPTION
RAMP_DLY	0 = One clock cycle 1 = Two clock cycles	Normally the ramp clock is equal to the phase detector frequency. When this feature is enabled, it reduces the ramp clock by a factor of 2.
RAMP0_LEN RAMP1_LEN	0 to 65535	This is the length of the ramp in clock cycles. Note that the time that the VCO is calibrating is added to this time.
RAMP0_INC RAMP1_INC	0 to 2^{30}	2's complement of the value for the ramp increment.
RAMP0_NEXT RAMP1_NEXT	0 = RAMP0 1 = RAMP1	Defines which ramp comes after the current ramp.
RAMP0_NEXT_TRIG RAMP1_NEXT_TRIG	0 = Timeout counter 1 = Trigger A 2 = Trigger B 3 = Reserved	Determines what triggers the action of the next ramp occurring.
RAMP_TRIG_A RAMP_TRIG_B	0 = Disabled 1 = RampCLk rising edge 2 = RampDir rising edge 4 = Always triggered 9 = RampCLk falling edge 10 = RampDir falling edge All other States = invalid	This field defines what the ramp trigger is.
RAMP0_RST RAMP1_RST	0 = Disabled 1 = Enabled	Enabling this bit causes the ramp to reset to the original value when the ramping started. This is useful for roundoff errors.
RAMP_BURST_COUNT	0 to 8191	This is the number the ramping pattern repeats and only applies for a terminating ramping pattern.
RAMP_BURST_TRIG	0 = Ramp Transition 1 = Trigger A 2 = Trigger B 3 = Reserved	This defines what causes the RAMP_COUNT to increment.

7.3.12.2.1 Automatic Ramping Example (Triangle Wave)

Suppose user wants to generate a sawtooth ramp that goes from 8 to 10 GHz in 2 ms (including calibration breaks) with a phase-detector frequency of 50 MHz. Divide this into segments of 50 MHz where the VCO ramps for 25 µs, then calibrates for 25 µs, for a total of 50 µs. There would therefore be 40 such segments which span over a 2-GHz range and would take 2 ms, including calibration time.

Table 16. Sawtooth Ramping Example

FIELD	PROGRAMMING	DESCRIPTION
RAMP_EN	1 = Enabled	
RAMP_MANUAL	0 = Automatic ramping mode	
RAMP_TRIG_CAL	0 = Disabled	
RAMP_THRESH	8388608	50 MHz / 50 MHz × 2^{24} = 16777216
RAMP_DLY	0 = 1 clock cycle	
RAMPx_LEN	13422	1000 µs × 50 MHz = 50000
RAMP0_INC	13422	(2000 MHz) / (50 MHz) × 2^{24} / 50000 = 13422
RAMP1_INC	1073740146	(–2000 MHz) / (50 MHz) × 2^{24} / 50000 = –13422 2's complement = 2^{30} – 13422 = 1073728402
RAMP0_NEXT	1 = RAMP1	
RAMP1_NEXT	0 = RAMP0	
RAMPx_NEXT_TRIG	0 = Timeout counter	
RAMP_TRIG_x	0 = Disabled	
RAMP0_RST	1 = Enabled	Not necessary, but good practice to reset.
RAMP1_RST	0 = Disabled	Do not reset this, or ramp does not work.
RAMP_BURST_COUNT	0	
RAMP_BURST_TRIG	0 = Ramp Transition	

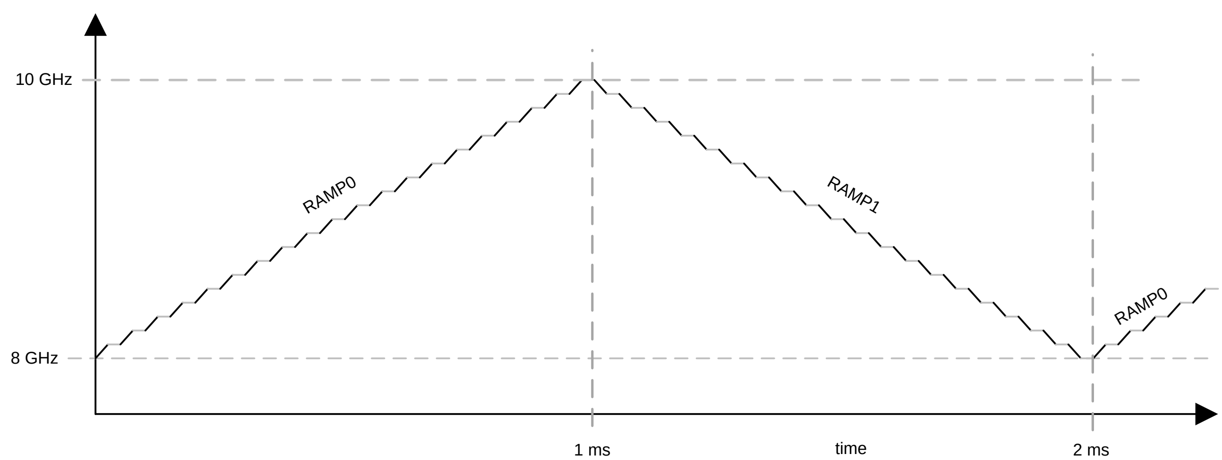


Figure 24. Triangle Waveform Example

7.3.13 SYSREF

The LMX2594 can used to a SYSREF output signal that synchronized to the output with a programmable delay. This output can be a single pulse, series of pulse, or a continuous stream of pulses. To use the SYSREF capability, the PLL must be in SYNC mode with VCO_PHASE_SYNC = 1.

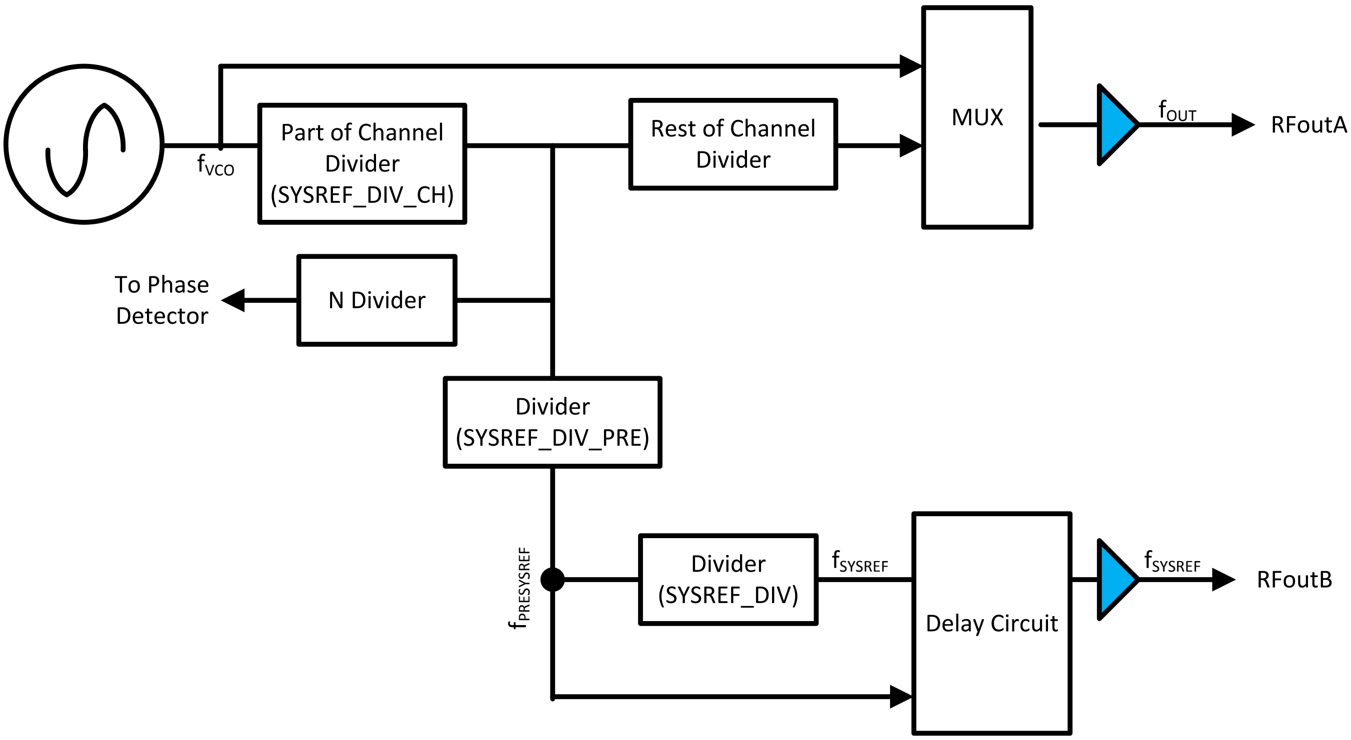


Figure 25. SYSREF Setup

As Figure 25 shows, the SYSREF feature shares parts of the channel divide and puts a pre-divider in front of the N divider; this must be taken into consideration when using the SYSREF feature.

When configured for this mode, a rising edge is sent to the SysRefReq pin, which causes the device to output either a single pulse or a series of pulses to the RFoutB pins. These pulses are synchronous with the RFoutA signal with an adjustable delay.

Table 17. SYSREF Setup

PARAMETER	MIN	TYP	MAX	UNIT
f_{VCO}	7.5		15	GHz
$f_{INTERPOLATOR}$	0.8		1.5	GHz
SYSREF_DIV_CH (Part of channel divider)		2, 4, or 6		
SYSREF_DIV_PRE	1, 2, or 4			
SYSREF_DIV	1 to 2047, but maybe not all values can be used			
$f_{INTERPOLATOR}$	$f_{PRESYSREF} = f_{VCO}$ /(SYSREF_DIV_CH × SYSREF_DIV_PRE)			
f_{SYSREF}	$f_{SYSREF} = f_{INTERPOLATOR}$ / (2 × SYSREF_DIV)			
Delay step size		9		ps
Pulses for pulsed mode (SYSREF_PULSE_CNT)	0		15	n/a

The delay can be programmed using the JESD_DAC1_CTRL, JESD_DAC2_CTRL, JESD_DAC3_CTRL, and JESD_DAC4_CTRL words. By concatenating these words into a larger word called "SysRefPhaseShift", the relative delay can be found. The sum of these words should always be 63.

Table 18. SysRef Delay

SysRef DELAY	DELAY	JESD_DAC1	JESD_DAC2	JESD_DAC3	JESD_DAC4
0	Minimum	36	27	0	0
...				0	0
36		0	63	0	0
37		62	1	0	0
...					
99		0	0	63	0
100		0	0	62	1
...					
161		0	0	1	62
162		0	0	0	63
163		1	0	0	62
224		63	0	0	0
225		62	1	0	0
247	Maximum	41	22	0	0
> 247	Invalid	Invalid	Invalid	Invalid	Invalid

7.3.13.1 Programmable Fields

Table 19 has the programmable fields for the SYSREF functionality.

Table 19. SYSREF Programming Fields

FIELD	PROGRAMMING	DEFAULT	DESCRIPTION
SYSREF_EN	0 = Disabled 1 = enabled	0	Enables the SYSREF mode
SYSREF_DIV_PRE	1: DIV1 2: DIV2 4: DIV4 Other states: invalid		The output of this divider is the $f_{PRESYSREF}$.
SYSREF_REPEAT	0 = Generator 1 = Repeater	0	In generator mode, the device creates a series of SYSREF pulses. In repeater mode, SYSREF pulses are generated with the SysRefReq pin.
SYSREF_PULSE	0 = Continuous mode 1 = Pulsed mode	0	Continuous mode continuously makes SYSREF pulses, where pulsed mode makes a series of SYSREF_PULSE_CNT pulses
SYSREF_PULSE_CNT	0 to 15	4	In the case of using pulsed mode, this is the number of pulses. Setting this to zero is an allowable, but not practical state.
SYSREF_DIV	170 to 2047	0	The SYSREF frequency is at the VCO frequency divided by this value.

7.3.13.2 Input and Output Pin Formats

7.3.13.2.1 Input Format for SYNC and SYSREF Pins

These pins are single-ended but a differential signal can be converted to drive them. In the LVDS mode, if the INPIN_FMT is set to LVDS mode, then the bias level can be adjusted with INPIN_LVL and the hysteresis can be adjusted with INPIN_HYST.

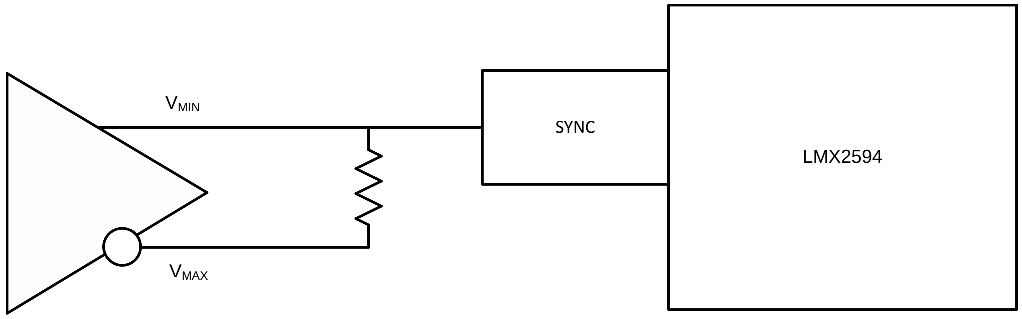


Figure 26. Driving SYNC/SYSREF with Differential Signal

7.3.13.2.2 SYSREF Output Format

The SYSREF output comes in differential format through RFoutB. This will have a minimum voltage of about 2.3 V and a maximum of 3.3 V. If DC coupling cannot be used, there are two strategies for AC coupling.

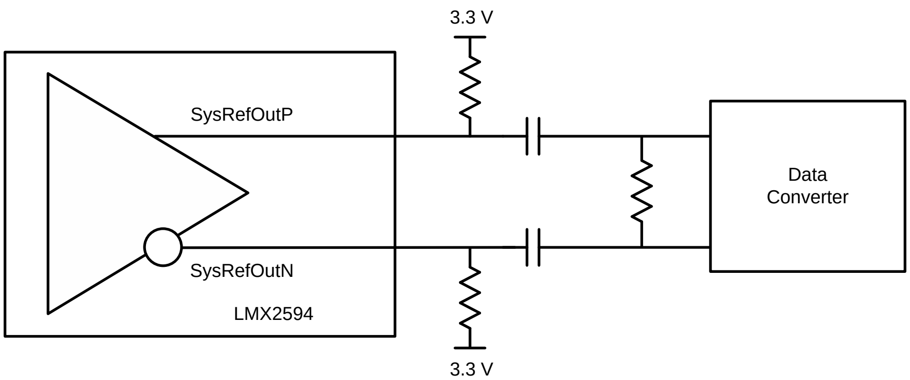


Figure 27. SYSREF Output

1. Send a series of pulses to establish a DC-bias level across the AC-coupling capacitor.
2. Establish a bias voltage at the data converter that is below the threshold voltage by using a resistive divider.

7.3.13.3 Examples

The SYSREF can be used in a repeater mode, which just echos the input, after being reclocked to OSCin and then RFout, or it can be used in a repeater. In either mode, there is a phase adjustment with resolution of 1/16 of the output phase up to a maximum of 1 ns. In repeater mode, it can repeat 1,2,4,8, or infinite (continuous) pulses. The frequency for repeater mode is equal to the RFout frequency divided by the SYSREF divider.

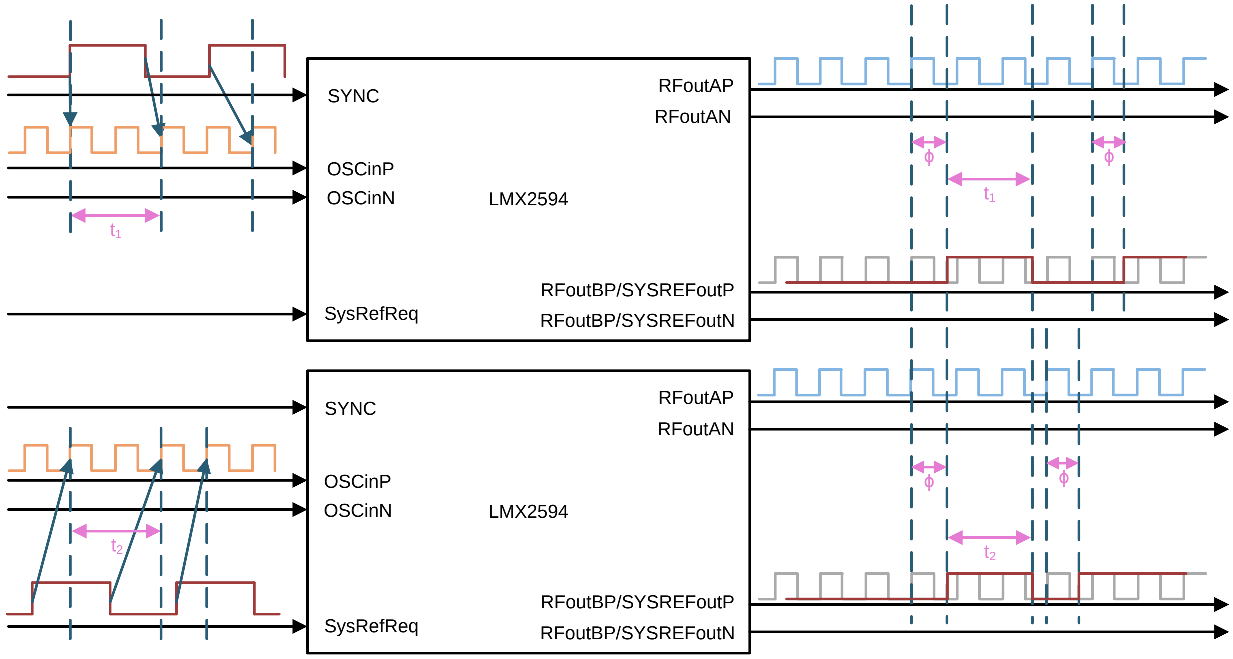


Figure 28. SYSREF Out In Repeater Mode

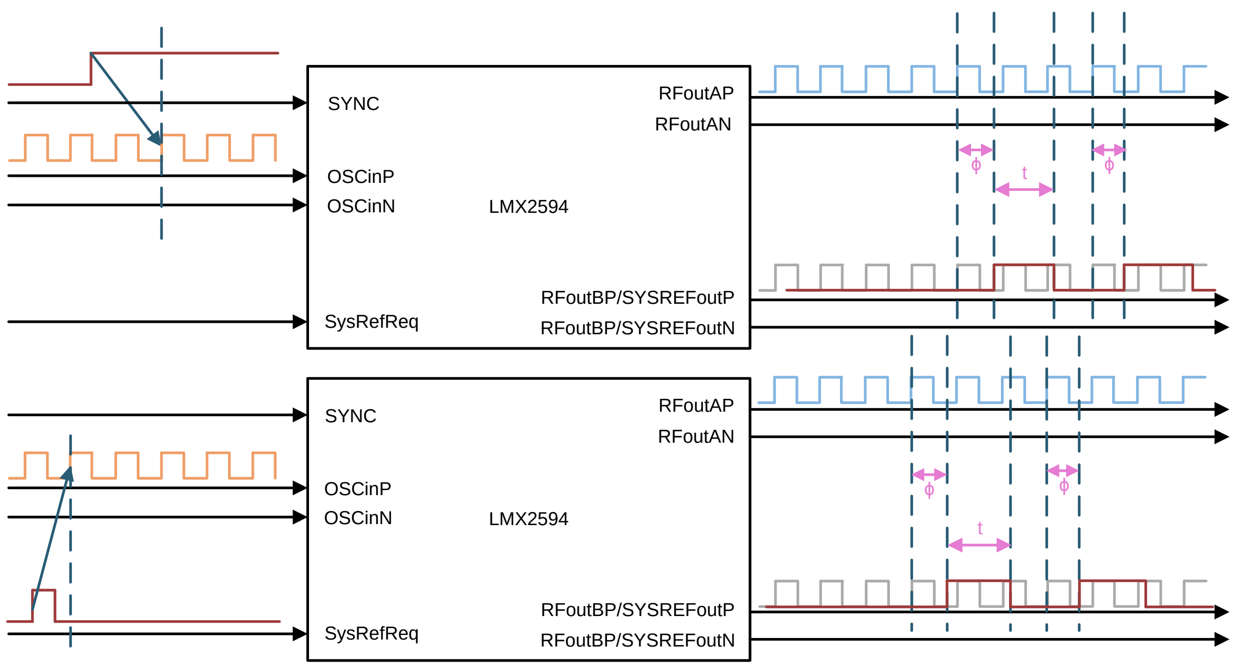


Figure 29. Figure 1. SYSREF Out In Pulsed/Continuous Mode

7.3.13.4 SYSREF Procedure

To use SYSREF, do the these steps:

1. Put the device in SYNC mode using the procedure already outlined.
2. Figure out the included channel divide the same way it is done for SYNC mode.
3. Calculate the SYSREF_DIV_PRE value such that the interpolator frequency ($f_{INTERPOLATOR}$) is in the range of 800 to 1500 MHz. $f_{INTERPOLATOR} = f_{VCO}$/IncludedDivide/SYSREF_DIV_PRE
4. If using master mode (SYSREF_REPEAT=0), ensure SysRefReq pin is high, ensure the SysRefReq pin is high.
5. If using repeater mode (SYSREF_REPEAT=1), set up the pulse count if desired. Pulses are created by toggling the SysRefReq pin.
6. Adjust the delay between the RFoutA and RFoutB signal using the JESD_DACx_CTL fields.

7.3.14 SysRefReq Pin

The SysRefReq pin can be used in CMOS all the time, or LVDS mode is also optional if SYSREF_REPEAT = 1. LVDS mode cannot be used in master mode.

7.4 Device Functional Modes

Although there is a vast number of ways to configure this device, there is really only one functional.

Table 20. Device Functional Modes

MODE	DESCRIPTION	SOFTWARE SETTINGS
RESET	Registers are held in their reset state. This device does have a power on reset, but it is good practice to also do a software reset if there is any possibility of noise on the programming lines, especially if there is sharing with other devices. Also realize that there are registers not disclosed in the data sheet that are reset as well.	RESET = 1, POWERDOWN = 0
POWERDOWN	Device is powered down.	POWERDOWN = 1 or CE Pin = Low
Normal operating mode	This is used with at least one output on as a frequency synthesizer.	
SYNC mode	This is used where part of the channel divider is in the feedback path to ensure deterministic phase.	VCO_PHASE_SYNC = 1
SYSREF mode	In this mode, RFoutB is used to generate pulses for SYSREF.	VCO_PHASE_SYNC =1, SYSREF_EN = 1

7.5 Programming

The LMX2594 is programmed using 24-bit shift registers. The shift register consists of a R/W bit (MSB), followed by a 7-bit address field and a 16-bit data field. For the R/W bit, 0 is for write, and 1 is for read. The address field ADDRESS[6:0] is used to decode the internal register address. The remaining 16 bits form the data field DATA[15:0]. While CSB is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When CSB goes high, data is transferred from the data field into the selected register bank. See Figure 1 for timing details.

7.5.1 Recommended Initial Power-Up Sequence

For the most reliable programming, TI recommends this procedure:

1. Apply power to device.
2. Program RESET = 1 to reset registers.
3. Program RESET = 0 to remove reset.
4. Program registers as shown in the register map in REVERSE order from highest to lowest.
5. Program register R0 one additional time with FCAL_EN = 1 to ensure that the VCO calibration runs from a stable state.

7.5.2 Recommended Sequence for Changing Frequencies

The recommended sequence for changing frequencies is as follows:

1. Change the N divider value.
2. Program the PLL numerator and denominator.
3. Program FCAL_EN (R0[3]) = 1.

7.6 Register Maps and Descriptions

Note that for registers that have numbers, but defined programmable bits, it is necessary to program these values just as shown in the register map. Registers must be programmed from highest to lowest (R0 Last)

Table 21. Full Register Map

	R/W	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	RAMP_EN	VCO_PHASE_SYNC_EN	1	0	0	1	OUT_MUTE	FCAL_HPFD_ADJ		FCAL_LPFD_ADJ		1	FCAL_EN	MUXOUT_LD_SEL	RESET	POWERDOWN
R1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	CAL_CLK_DIV		
R2	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R3	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0
R4	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1
R5	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0
R6	0	0	0	0	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0
R7	0	0	0	0	0	1	1	1	0	OUT_FORCE	0	0	0	0	0	0	1	0	1	1	0	0	1	0
R8	0	0	0	0	1	0	0	0	0	VCO_DACISET_FORCE	1	0	VCO_CAPCTRL_FORCE	0	0	0	0	0	0	0	0	0	0	0
R9	0	0	0	0	1	0	0	1	0	0	0	OSC_2X	0	1	1	0	0	0	0	0	0	1	0	0
R10	0	0	0	0	1	0	1	0	0	0	0	1	MULT					1	0	1	1	0	0	0
R11	0	0	0	0	1	0	1	1	0	0	0	0	PLL_R								1	0	0	0
R12	0	0	0	0	1	1	0	0	0	1	0	1	PLL_R_PRE											
R13	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R14	0	0	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	CPG			0	0	0	0
R15	0	0	0	0	1	1	1	1	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1
R16	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	VCO_DACISET								
R17	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	VCO_DACISET_STRT								
R18	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
R19	0	0	0	1	0	0	1	1	0	0	1	0	0	1	1	1	VCO_CAPCTRL							
R20	0	0	0	1	0	1	0	0	1	0	VCO_SEL			VCO_SEL_FORCE	0	0	0	1	0	0	1	0	0	0
R21	0	0	0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
R22	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 21. Full Register Map (continued)

	R/W	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R23	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0
R24	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	0	1	0
R25	0	0	0	1	1	0	0	1	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	0
R26	0	0	0	1	1	0	1	0	0	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0
R27	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R28	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0
R29	0	0	0	1	1	1	0	1	0	0	1	1	0	0	0	1	1	0	0	0	1	1	0	0
R30	0	0	0	1	1	1	1	0	0	0	1	1	0	0	0	1	1	0	0	0	1	1	0	0
R31	0	0	0	1	1	1	1	1	0	1	0	0	0	0	1	1	1	1	1	0	1	1	0	0
R32	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1
R33	0	0	1	0	0	0	0	1	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1
R34	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PLL_N[18:16]		
R35	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R36	0	0	1	0	0	1	0	0	PLL_N															
R37	0	0	1	0	0	1	0	1	MASH_SEED_EN	0	PFD_DLY_SEL						0	0	0	0	0	1	0	0
R38	0	0	1	0	0	1	1	0	PLL_DEN[31:16]															
R39	0	0	1	0	0	1	1	1	PLL_DEN[15:0]															
R40	0	0	1	0	1	0	0	0	MASH_SEED[31:16]															
R41	0	0	1	0	1	0	0	1	MASH_SEED[15:0]															
R42	0	0	1	0	1	0	1	0	PLL_NUM[31:16]															
R43	0	0	1	0	1	0	1	1	PLL_NUM[15:0]															
R44	0	0	1	0	1	1	0	0	0	0	OUTA_PWR						OUTB_PD	OUTA_PD	MASH_RESET_N	0	0	MASH_ORDER		
R45	0	0	1	0	1	1	0	1	1	1	0	OUTA_MUX		OUT_ISET		0	1	1	OUTB_PWR					
R46	0	0	1	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	OUTB_MUX	
R47	0	0	1	0	1	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
R48	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
R49	0	0	1	1	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0
R50	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R52	0	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
R53	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 21. Full Register Map (continued)

	R/W	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R54	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R55	0	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R56	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R57	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R58	0	0	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R59	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LD_TYPE
R60	0	0	1	1	1	1	0	0	LD_DLY															
R61	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
R62	0	0	1	1	1	1	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0
R63	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R64	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0
R65	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R66	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0
R67	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R68	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0
R69	0	1	0	0	0	1	0	1	MASH_RST_COUNT[31:16]															
R70	0	1	0	0	0	1	1	0	MASH_RST_COUNT[15:0]															
R71	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	SYSREF_DIV_PRE			SYSREF_PULSE	SYSREF_EN	SYSREF_REPEAT	0	1
R72	0	1	0	0	1	0	0	0	0	0	0	0	0	SYSREF_DIV										
R73	0	1	0	0	1	0	0	1	0	0	0	0	JESD_DAC2_CTRL						JESD_DAC1_CTRL					
R74	0	1	0	0	1	0	1	0	SYSREF_PULSE_CNT				JESD_DAC4_CTRL						JESD_DAC3_CTRL					
R75	0	1	0	0	1	0	1	1	0	0	0	0	1	CHDIV					0	0	0	0	0	0
R76	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R77	0	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R78	0	1	0	0	1	1	1	0	0	0	0	0	RAMP_THRESH[32]	0	QUICK_RECAL_EN	VCO_CAPCTRL_STRT								1
R79	0	1	0	0	1	1	1	1	RAMP_THRESH[31:16]															
R80	0	1	0	1	0	0	0	0	RAMP_THRESH[15:0]															

Table 21. Full Register Map (continued)

	R/W	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R81	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_LIMIT_HIGH[32]
R82	0	1	0	1	0	0	1	0	RAMP_LIMIT_HIGH[31:16]															
R83	0	1	0	1	0	0	1	1	RAMP_LIMIT_HIGH[15:0]															
R84	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_LIMIT_LOW[32]
R85	0	1	0	1	0	1	0	1	RAMP_LIMIT_LOW[31:16]															
R86	0	1	0	1	0	1	1	0	RAMP_LIMIT_LOW[15:0]															
R87	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R88	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R89	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R90	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R91	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R92	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R93	0	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R94	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R95	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R96	0	1	1	0	0	0	0	0	RAMP_BURST_EN	RAMP_BURST_COUNT													0	0
R97	0	1	1	0	0	0	0	1	RAMP0_RST	0	0	0	1	RAMP_TRIGB				RAMP_TRIGA				0	RAMP_BURST_TRIG	
R98	0	1	1	0	0	0	1	0	RAMP0_INC[29:16]														RAMP0_FL	RAMP0_DLY
R99	0	1	1	0	0	0	1	1	RAMP0_INC[15:0]															
R100	0	1	1	0	0	1	0	0	RAMP0_LEN															
R101	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	RAMP1_DLY	RAMP1_RST	RAMP0_NEXT	0	0	RAMP0_NEXT_TRIG	
R102	0	1	1	0	0	1	1	0	0	0	RAMP1_INC[29:16]													
R103	0	1	1	0	0	1	1	1	RAMP1_INC[15:0]															

Table 21. Full Register Map (continued)

	R/W	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R104	0	1	1	0	1	0	0	0	RAMP1_LEN															
R105	0	1	1	0	1	0	0	1	RAMP_DLY_CNT										RAMP_MANUAL	RAMP1_NEXT	0	0	RAMP1_NEXT_TRIG	
R106	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_TRIG_CAL	0	RAMP_SCALE_COUNT		
R107	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R108	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R109	0	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R110	0	1	1	0	1	1	1	0	0	0	0	0	0	rb_LD_VTUNE		0	rb_VCO_SEL			0	0	0	0	0
R111	0	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	rb_VCO_CAPCTRL							
R112	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	rb_VCO_DACISET								

7.6.1 General Registers R0, R1, & R7

Figure 30. Registers Excluding Address

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	RAMP_EN	VCO_PHASE_SYNC_EN	1	0	0	1	OUT_MUTE	FCAL_HPFD_ADJ		FCAL_LPFD_ADJ		1	FCAL_EN	MUXOUT_LD_SEL	RESET	POWERDOWN
R1	0	0	0	0	1	0	0	0	0	0	0	0	1	CAL_CLK_DIV		
R7	0	OUT_FORCE	0	0	0	0	0	0	1	0	1	1	0	0	1	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. Field Descriptions

Location	Field	Type	Reset	Description
R0[15]	RAMP_EN	R/W	0	0 : Disable frequency ramping mode 1 : Enable frequency ramping mode
R0[14]	VCO_PHASE_SYNC	R/W	0	0 : Disable phase SYNC mode 1 : Enable phase SYNC mode
R0[9]	OUT_MUTE	R/W	0	Mute the outputs when the VCO is calibrating. 0 : Disabled. If disabled, also be sure to enable OUT_FORCE 1 : Enabled. If enabled, also be sure to disable OUT_FORCE
R0[8:7]	FCAL_HPFD_ADJ	R/W		Set this field in accordance to the phase-detector frequency for optimal VCO calibration. 0 : f_{PD} ≤ 100 MHz 1: 100 MHz < f_{PD} ≤ 150 MHz 2 : 150 MHz < f_{PD} ≤ 200 MHz 3: f_{PD} >200 MHz
R0[6:5]	FCAL_LPFD_ADJ	R/W	0	Set this field in accordance to the phase detector frequency for optimal VCO calibration. 0: f_{PD} ≥ 10 MHz 1: 10 MHz > f_{PD} ≥ 5 MHz 2: 5 MHz > f_{PD} ≥ 2.5 MHz 3: f_{PD} < 2.5 MHz
R0[3]	FCAL_EN	R/W	0	Enablie the VCO frequency calibration. Also note that the action of programming this bit to a 1 activates the VCO calibration
R0[2]	MUXOUT_LD_SEL	R/W	0	Selects the state of the function of the MUXout pin 0: Readback 1: Lock detect
R0[1]	RESET	R/W	0	Resets and holds all state machines and registers to default value. 0: Normal operation 1: Reset
R0[0]	POWERDOWN	R/W	0	Powers down entire device 0: Normal operation 1: Powered down
R1[2:0]	CAL_CLK_DIV	R/W	3	Sets divider for VCO calibration state machine clock based on input frequency. 0: f_{OSC} ≤ 200 MHz 1: 200 MHz < f_{OSC} ≤ 400 MHz 2: 400 MHz < f_{OSC} ≤ 800 MHz 3: f_{OSC} > 800 MHz
R7[14]	OUT_FORCE	R/W	0	Works with OUT_MUTE in disabling outputs when VCO calibrating.

7.6.2 Input Path Registers

Figure 31. Registers excluding address

<table>
<tr><th></th><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>R9</td><td>0</td><td>0</td><td>0</td><td>OSC_ 2X</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>R10</td><td>0</td><td>0</td><td>0</td><td>1</td><td colspan="5">MULT</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>R11</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="8">PLL_R</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>R12</td><td>0</td><td>1</td><td>0</td><td>1</td><td colspan="12">PLL_R_PRE</td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. Field Descriptions

Location	Field	Type	Reset	Description
R9[12]	OSC_2X	R/W	0	Low=noise OSCin frequency doubler. 0: Disabled 1: Enabled
R10[11:7]	MULT	R/W	1	Programmable input frequency multiplier 0,2,,8-31: Reserved 1: Byapss 3: 3X ... 7: 7X
R11[11:4]	PLL_R	R/W	1	Programmable input path divider after the programmable input frequency multiplier.
R12[11:0]	PLL_R_PRE	R/W	1	Programmable input path divider before the programmable input frequency multiplier.

7.6.3 Charge Pump Registers (R13, R14)

Figure 32. Registers excluding address

<table>
<tr><th></th><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>R14</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td colspan="3">CPG</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. Field Descriptions

Location	Field	Type	Reset	Description
R14[6:4]	CPG	R/W	7	Effective charge-pump current. This is the sum of up and down currents. 0: 0 mA 1: 6 mA 2: Reserved 3: 12 mA 4: 3 mA 5: 9 mA 6: Reserved 7: 15 mA

7.6.4 VCO Calibration Registers

Figure 33. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R8	0	VCO_DACISET_FORCE	1	0	VCO_CAPCTRL_FORCE	0	0	0	0	0	0	0	0	0	0	0
R16	0	0	0	0	0	0	0	VCO_DACISET								
R17	0	0	0			0	0	0	0	VCO_DACISET_STRT	0	0	1	1	0	0
R19	0	0	1			0	0	1	1	1	VCO_CAPCTRL					
R20	1	VCO_SEL_STRT_EN	VCO_SEL			VCO_SEL_FORCE	0	0	0	1	0	0	1	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. Field Descriptions

Location	Field	Type	Reset	Description
R8[14]	VCO_DACISET_FORCE	R/W	0	This forces the VCO_DACISET value
R8[11]	VCO_CAPCTRL_FORCE	R/W	0	This forces the VCO_CAPCTRL value
R16[8:0]	VCO_DACISET	R/W	128	This sets the final amplitude for the VCO calibration in the case that amplitude calibration is forced.
R17[8:0]	VCO_DACISET_STRT	R/W	250	This sets the initial starting point for the VCO amplitude calibration.
R19[7:0]	VCO_CAPCTRL	R/W	183	This sets the final VCO band when VCO_CAPCTRL is forced.
R20[13:11]	VCO_SEL	R/W	7	This sets the VCO that is used when VCO_SEL_STRT_EN=1 or VCO_SEL_FORCE=1 0: Not Used 1: VCO1 2: VCO2 3: VCO3 4: VCO4 5: VCO5 6: VCO6 7: VCO7
R20[10]	VCO_SEL_FORCE	R/W	0	This forces the VCO to use the core specified by VCO_SEL. It is intended mainly for diagnostic purposes. 0: Disabled (recommended) 1: Enabled

7.6.5 N Divider, MASH, and Output Registers

Figure 34. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R34	0	0	0	0	0	0	0	0	0	0	0	0	0	PLL_N[18:16]		
R36	PLL_N															
R37	MASH_SEED_EN	0	PFD_DLY_SEL						0	0	0	0	0	1	0	0
R38	PLL_DEN[31:16]															
R39	PLL_DEN[15:0]															
R40	MASH_SEED[31:16]															
R41	MASH_SEED[15:0]															
R42	PLL_NUM[31:16]															
R43	PLL_NUM[15:0]															
R44	0	0	OUTA_PWR						OUTB_PD	OUTA_PD	MASH_RESET_N	0	0	MASH_ORDER		
R45	1	1	0	OUTA_MUX		OUT_ISET		0	1	1	OUTB_PWR					
R46	0	0	0	0	0	1	1	1	1	1	1	1	1	1	OUTB_MUX	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. Field Descriptions

Location	Field	Type	Reset	Description
R34[2:0] R36[15:0]	PLL_N	R/W	100	The PLL_N divider value is in the feedback path and divides the VCO frequency. 0: Disabled 1: Enabled
R37[15]	MASH_SEED_EN	R/W	0	Enabling this bit allows the MASH_SEED to be applied to shift the phase at the output or optimize spurs.
R37[13:8]	PFD_DLY_SEL	R/W	2	The PFD_DLY_SEL must be adjusted in accordance to the N divider value. This is with the functional description for the N divider.
R38[15:0] R39[15:0]	PLL_DEN	R/W	4294967295	The fractional denominator.
R40[15:0] R41[15:0]	MASH_SEED	R/W	0	The initial state of the MASH engine first accumulator. Can be used to shift phase or optimize fractional spurs. Every time the MASH_SEED field is programmed, it ADDS this MASH seed to the existing one. To reset it, use the MASH_RESET_N bit.
R42[15:0] R43[15:0]	PLL_NUM	R/W	0	The fractional numerator
R44[13:8]	OUTA_PWR	R/W	31	Adjusts output power. Higher numbers give more output power to a point, depending on the pullup component used.
R44[7]	OUTB_PD	R/W	1	Powers down output B 0: Output B active 1: Output B powered down
R44[6]	OUTA_PD	R/W	0	Powers down output A 0: Output A Active 1: Output A powered down
R44[5]	MASH_RESET_N	R/W	1	Resets MASH circuitry to an initial state 0: Disabled. Fractional mode enabled. 1: Enabled. All fractions are ignored and MASH engine is reset.
R44[2:0]	MASH_ORDER	R/W	0	Sets the MASH order 0: Integer mode 1: First order modulator 2: Second order modulator 3: Third order modulator 4: Fourth order modulator 5-7: Reserved

Table 26. Field Descriptions (continued)

Location	Field	Type	Reset	Description
R45[12:11]	OUTA_MUX	R/W	1	Selects what signal goes to RFoutA 0: Channel divider 1: VCO 2: Reserved 3: High impedance
R45[10:9]	OUT_ISEL	R/W	0	Setting to a lower value allows slightly higher output power at higher frequencies at the expense of higher current consumption. 0: Maximum output power boost ... 3: No output power boost
R45[5:0]	OUTB_PWR	R/W	31	Output power setting for RFoutB.
R46[1:0]	OUTB_MUX	R/W	1	Selects what signal goes to RFoutB 0: Channel divider 1: VCO 2: Sysref 3: High impedance

7.6.6 Lock Detect Registers

Figure 35. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R59	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LD_TYPE
R60	LD_DLY															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. Field Descriptions

Location	Field	Type	Reset	Description
R59[0]	LD_TYPE	R/W	1	Lock detect type 0: VCO calibration status 1: VCO calibration status and Vtune
R60[15:0]	LD_DLY	R/W	1000	This is the delay added to the lock detect after the VCO calibration is successful. It is in phase-detector cycles.

7.6.7 MASH_RESET

Figure 36. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R69	MASH_RST_COUNT[31:16]															
R70	MASH_RST_COUNT[15:0]															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. Field Descriptions

Location	Field	Type	Reset	Description
R69[15:0] R70[15:0]	MASH_RST_COUNT	R/W	50000	If not using this device in fractional mode with VCO_PHASE_SYNC=1, then this field can be set to 0. In phase-sync mode with fractions, this bit is used so that there is a delay for the VCO divider after the MASH is reset. This delay must be set to greater than the lock time of the PLL. It does impact the latency time of the SYNC feature.

7.6.8 SysREF Registers

Figure 37. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R71	0	0	0	0	0	0	0	0	SYSREF_DIV_PRE			SYSREF_PULSE	SYSREF_EN	SYSREF_REPEAT	0	1
R72	0	0	0	0	0	SYSREF_DIV										
R73	0	0	0	0	JESD_DAC2_CTRL						JESD_DAC1_CTRL					
R74	SYSREF_PULSE_CNT				JESD_DAC4_CTRL						JESD_DAC3_CTRL					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. Field Descriptions

Location	Field	Type	Reset	Description
R71[7:5]	STSREF_DIV_PRE	R/W	4	Pre divider for SYSREF 2: Divide by 2 4: Divide by 4 All other states: invalid
R71[4]	SYSREF_PULSE	R/W	0	Enable pulser mode in master mode 0: Disabled 1: Enabled
R71[3]	SYSREF_EN	R/W	0	Enable SYSREF
R71[2]	SYSREF_REPEAT	R/W	0	Enable repeater mode 0: Master mode 1: Repeater mode
R72[10:0]	SYSREF_DIV	R/W	0	Divider for the SYSREF Fout = Fin / (2 × SYSREF_DIV + 4)
R73[5:0]	JESD_DAC1_CTRL	R/W	63	These are the adjustments for the delay for the SYSREF. Two of these must be zero and the other two values must sum to 63.
R73[11:6]	JESD_DAC2_CTRL	R/W	0	
R74[5:0]	JESD_DAC3_CTRL	R/W	0	
R74[11:6]	JESD_DAC4_CTRL	R/W	0	
R74[15:12]	SYSREF_PULSE_CNT	R/W	0	Number of pulses in pulse mode in master mode

7.6.9 CHANNEL Divider Registers

Figure 38. Registers Excluding Address

Reg	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R75	0	0	0	0	1	CHDIV					0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. Field Descriptions

Location	Field	Type	Reset	Description
R75[10:6]	CHDIV	R/W	0	VCO divider value 0: 2 1: 4 2: 6 3: 8 4: 12 5: 16 6: 24 7: 32 8: 48 9: 64 10: 72 11: 96 12: 128 13: 192 14: 256 15: 384 16: 512 17: 768 18-31: Reserved

7.6.10 Ramping and Calibration Fields

Figure 39. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R78	0	0	0	0	RAMP_THRESH[32]	0	QUICK_RECAL_EN	VCO_CAPCTRL_STRT								1
R79	RAMP_THRESH[31:16]															
R80	RAMP_THRESH[15:0]															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. Field Descriptions

Location	Field	Type	Reset	Description
R78[11] R79[15:0] R80[15:0]	RAMP_THRESH	R/W	0	This sets how much the ramp can change the VCO frequency before calibrating. If this frequency is chosen to be Δf, then it is calculated as follows: RAMP_THRESH = $(\Delta f / f_{PD}) \times 16777216$
R78[9]	QUICK_RECAL_EN	R/W	0	Causes the initial VCO_CORE, VCO_CAPCTRL, and VCO_DACISET to be based on the last value. Useful if the frequency change is small, as is often the case for ramping. 0: Disabled 1: Enabled
R78[8:1]	VCO_CAPCTRL_STRT	R/W	0	This is the capcode that is used for the calibration when VCO_CAPCTRL_STRT_EN = 1. Smaller values yield a higher frequency band within a VCO core. Valid number range is 0 to 183.

7.6.11 Ramping Registers

These registers are only relevant for ramping functions and are enabled if and only if RAMP_EN (R0[15]) = 1.

7.6.11.1 Ramp Limits

Figure 40. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R81	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_LIMIT_HIGH[32]
R82	RAMP_LIMIT_HIGH[31:16]															
R83	RAMP_LIMIT_HIGH[15:0]															
R84	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_LIMIT_LOW[32]
R85	RAMP_LIMIT_LOW[31:16]															
R86	RAMP_LIMIT_LOW[15:0]															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. Field Descriptions

Location	Field	Type	Reset	Description
R81[0] R82[15:0] R83[15:0]	RAMP_LIMIT_HIGH	R/W	0	This sets a maximum frequency that the ramp can not exceed so that the VCO does not get set beyond a valid frequency range. Suppose f_{HIGH} is this frequency and f_{VCO} is the starting VCO frequency then: For $f_{MAX} \geq f_{VCO}$: RAMP_LIMIT_HIGH = $(f_{HIGH} - f_{VCO})/f_{PD} \times 16777216$ For $f_{MAX} < f_{VCO}$ this is not a valid condition to choose.
R84[0] R85[15:0] R86[15:0]	RAMP_LIMIT_LOW	R/W	0	This sets a minimum frequency that the ramp can not exceed so that the VCO does not get set beyond a valid frequency range. Suppose f_{LOW} is this frequency and f_{VCO} is the starting VCO frequency then: For $f_{LOW} \leq f_{VCO}$: RAMP_LIMIT_LOW =$2^{32} - (f_{LOW} - f_{VCO}) / f_{PD} \times 16777216$ For $f_{LOW} > f_{VCO}$ this is not a valid condition to choose.

7.6.11.2

7.6.11.3 Ramping Triggers, Burst Mode, and RAMP0_RST

Figure 41. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R96	RAMP_BURST_EN	RAMP_BURST_COUNT													0	0
R97	RAMP0_RST	0	0	0	1	RAMP_TRIGB				RAMP_TRIGA				0	RAMP_BURST_TRIG	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. Field Descriptions

Location	Field	Type	Reset	Description
R96[15]	RAMP_BURST_EN	R/W	0	Enables burst ramping mode. In this mode, a RAMP_BURST_COUNT ramps are sent out when RAMP_EN is set from 0 to 1. 0: Disabled 1: Enabled
RAMP96[14:2]	RAMP_BURST_COUNT	R/W	0	Sets how many ramps are run in burst ramping mode.
R97[15]	RAMP0_RST	R/W	0	Resets RAMP0 at start of ramp to eliminate round-off errors. Must only be used in automatic ramping mode. 0: Disabled 1: Enabled
R97[6:3]	RAMP_TRIGA	R/W	0	Multipurpose Trigger A definition: 0: Disabled 1: RampCLK pin rising edge 2: RampDIR pin rising edge 4: Always triggered 9: RampCLK pin falling edge 10: RampDIR pin falling edge All other states: reserved
R97[10:7]	RAMP_TRIGB	R/W	0	Multipurpose trigger B definition: 0: Disabled 1: RampCLK pin Rising Edge 2: RampDIR pin Rising Edge 4: Always Triggered 9: RampCLK pin Falling Edge 10: RampDIR pin Falling Edge All other states: Reserved
R97[1:0]	RAMP_BURST_TRIG	R/W	0	Ramp burst trigger definition that triggers the next ramp in the count. Note that RAMP_EN starts the count, not this word. 0: Disabled 1: RampCLK pin rising edge 5: CMP0 detected 8: Always triggered All other states: reserved

7.6.11.4 Ramping Configuration

Figure 42. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R98	RAMP0_INC[29:16]														0	RAMP0_DLY
R99	RAMP0_INC[15:0]															
R100	RAMP0_LEN															
R101	0	0	0	0	0	0	0	0	0	RAMP1_DLY	RAMP1_RST	RAMP0_NEXT	0	RAMP0_NEXT_TRIG	RAMP0_NEXT_TRIG	
R102	0	0	RAMP1_INC[29:16]													
R103	RAMP1_INC[15:0]															
R104	RAMP1_LEN															
R105	RAMP_DLY_CNT										RAMP_MANUAL	RAMP1_NEXT	0	0	RAMP1_NEXT_TRIG	
R106	0	0	0	0	0	0	0	0	0	0	0	RAMP_TRIG_CAL	0	RAMP_SCALE_COUNT		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. Field Descriptions

Location	Field	Type	Reset	Description
R98[15:2] R99[15:0]	RAMP0_INC	R/W	0	2's complement of the amount the RAMP0 is incremented in phase detector cycles.
R98[0]	RAMP0_DLY	R/W	0	Enabling this bit uses two clocks instead of one to clock the ramp. Effectively doubling the length. 0: Normal ramp length 1: Double ramp length
R100[15:0]	RAMP0_LEN	R/W	0	Length of RAMP0 in phase detector cycles
R101[6]	RAMP1_DLY	R/W	0	Enabling this bit uses two clocks instead of one to clock the ramp. Effectively doubling the length. 0: Normal ramp length 1: Double ramp length
R101[5]	RAMP1_RST	R/W	0	Resets RAMP1 to eliminate rounding errors. Must be used in automatic ramping mode. 0: Disabled 1: Enabled
R101[4]	RAMP0_NEXT	R/W	0	Defines what ramp comes after RAMP0 0: RAMP0 1: RAMP1
R101[1:0]	RAMP0_NEXT_TRIG	R/W	0	Defines what triggers the next ramp 0: RAMP0_LEN timeout counter 1: Trigger A 2: Trigger B 3: Reserved
R102[13:0] R103[15:0]	RAMP1_INC	R/W	0	2's complement of the amount the RAMP0 is incremented in phase detector cycles.
R104[15:0]	RAMP1_LEN	R/W	0	Length of RAMP1 in phase detector cycles
R105[15:6]	RAMP_DLY_CNT	R/W	0	This is the amount of time for the VCO calibration in automatic mode. If the VCO calibration is less, then it is this time. if it is more then the time is the VCO caliabration time.
R105[5]	RAMP_MANUAL	R/W	0	Enables manual ramping mode, otherwise automatic mode 0: Automatic ramping mode 1: Manual ramping mode
R105[4]	RAMP1_NEXT	R/W	0	Determines what ramp comes after RAMP1: 0: RAMP0 1: RAMP1

Table 34. Field Descriptions (continued)

Location	Field	Type	Reset	Description
R105[1:0]	RAMP_NEXT_TRIG	R/W	0	Defines what triggers the next ramp 0: RAMP1_LEN timeout counter 1: Trigger A 2: Trigger B 3: Reserved
R106[4]	RAMP_TRIG_CAL	R/W	0	Enabling this bit forces the VCO to calibrate after the ramp.
R106[2:0]	RAMP_SCALE_COUNT	R/W	7	Multiplies RAMP_DLY count by $2^{RAMP\_SCALE\_COUNT}$

7.6.12 Readback Registers

Figure 43. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R110	0	0	0	0	0	rb_LD_VTUNE		0	rb_VCO_SEL			0	0	0	0	0
R111	0	0	0	0	0	0	0	0	rb_VCO_CAPCTRL							
R112	0	0	0	0	0	0	0	rb_VCO_DACISET								

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. Field Descriptions

Location	Field	Type	Reset	Description
R110[10:9]	rb_LD_VTUNE	R	0	Readback of Vtune lock detect 0: Unlocked (Vtune low) 1: Unlocked (Vtune high) 2: Locked 3: Invalid State
R110[7:5]	rb_VCO_SEL	R	0	Reads back the actual VCO that the calibration has selected. 0: Invalid 1: VCO1 ... 7: VCO7
R111[7:0]	rb_VCO_CAPCTRL	R	183	Reads back the actual CAPCTRL capcode value the VCO calibration has chosen.
R112[8:0]	rb_VCO_DACISET	R	170	Reads back the actual amplitude (DACISET) value that the VCO calibration has chosen.

8 Application and Implementation

NOTE

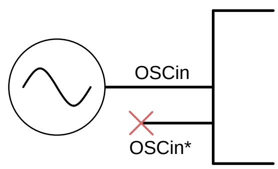
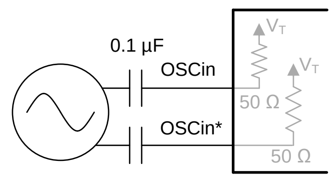
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 OSCin Configuration

OSCin supports single or differential-ended clock.

Table 36. OSCin Configuration

OSCin TYPE	SINGLE-ENDED CLOCK	DIFFERENTIAL CLOCK
Connection diagram		

Input clock definitions are shown in Figure 44:

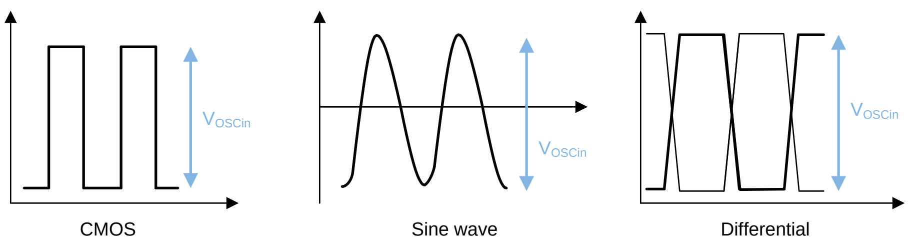


Figure 44. Input Clock Definitions

8.1.2 OSCin Slew Rate

The slew rate of the OSCin signal can have an impact on the spurs and phase noise of the LMX2594 if it is too low. In general, the best performance is for a high slew rate, but lower amplitude signal, such as LVDS.

8.1.3 RF Output Buffer Power Control

The OUTA_PWR and OUTB_PWR registers can be used to control the output power of the output buffers. The setting for optimal power may depend on the pullup component, but typically is around 50. The higher the setting, the higher the current consumption of the output buffer.

8.1.4 RF Output Buffer Pullup

The choice of output buffer components is very important and can have a profound impact on the output power. Table 37 shows how to treat each pin. If using single-ended, the pullup is still needed, and user puts a 50-Ω resistor after the capacitor.

Table 37. Different Methods for Pullup on Outputs

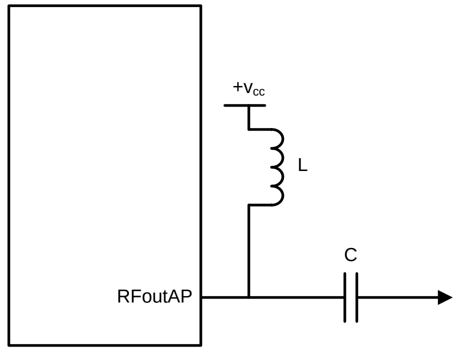
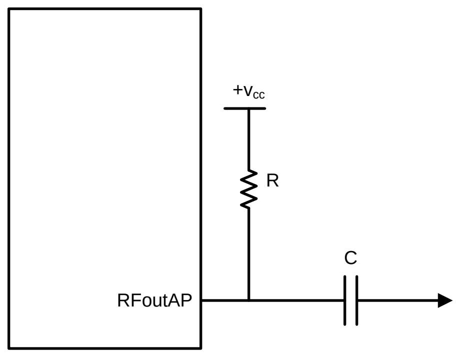
PULLUP STYLE	DIAGRAM	COMMENTS
Inductor		Potentially higher output power, but output impedance is far from 50 Ω. Consider also using with a resistive pad.
Resistor		More consistent matching

Table 38. Output Pullup Configuration

COMPONENT	VALUE	PART NUMBER
Inductor	Varies with frequency	
Resistor	50 Ω	Vishay FC0402E50R0BST1
Capacitor	Varies with frequency	ATC 520L103KT16T ATC 504L50R0FTNCFT

8.2 Typical Application

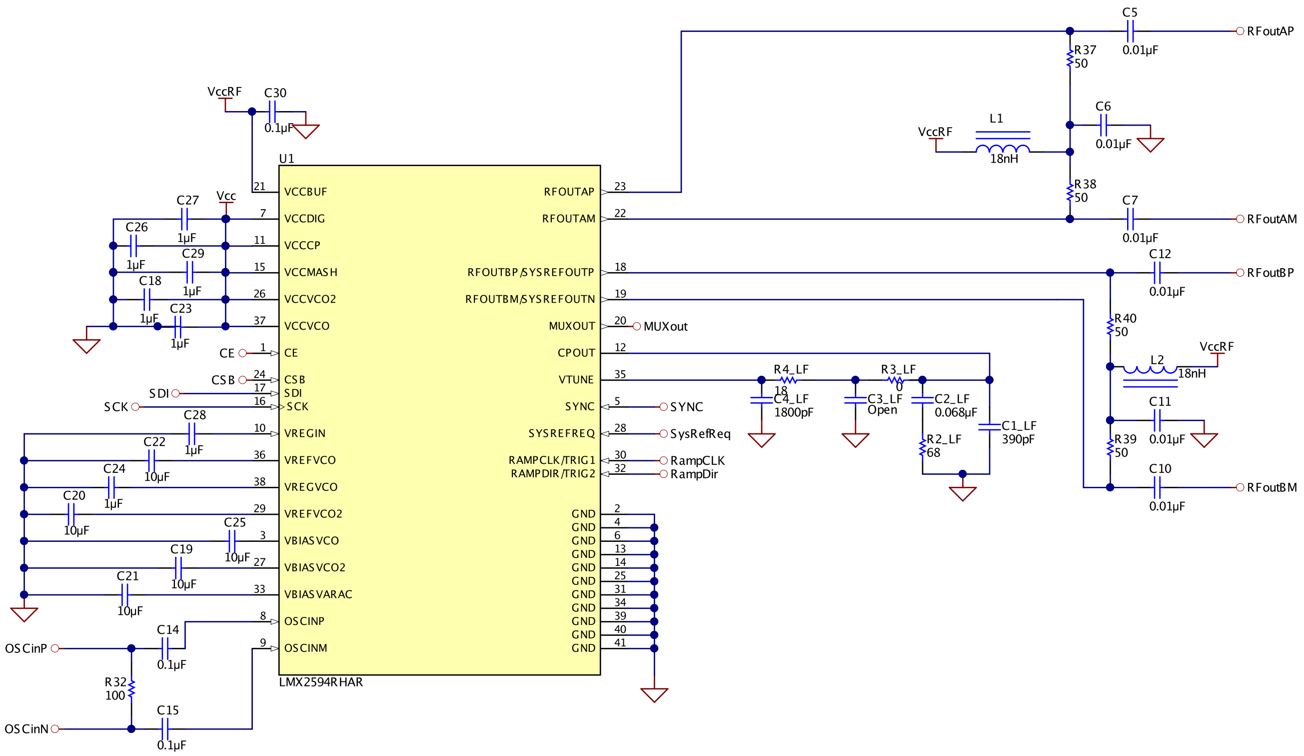


Figure 45. Typical Application Schematic

8.2.1 Design Requirements

The design of the loop filter is complex and is typically done with software. The PLLatinum Sim software is an excellent resource for doing this and the design is shown in the Figure 46. For those interested in the equations involved, the *PLL Performance, Simulation, and Design Handbook* listed in the end of this document goes into great detail as to theory and design of PLL loop filters.

Typical Application (continued)

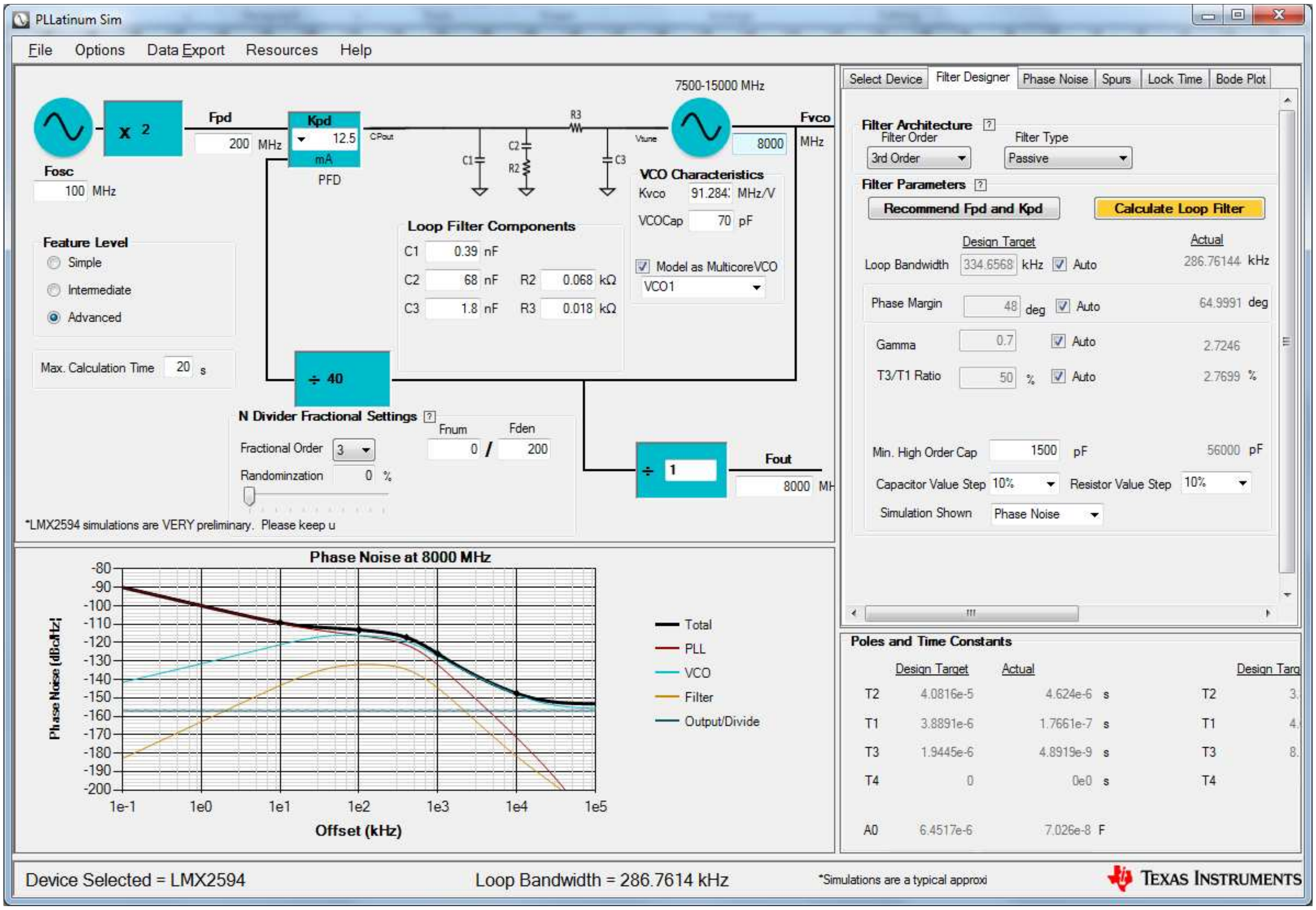


Figure 46. PLLatinum Sim Design Screen

8.2.2 Detailed Design Procedure

The integration of phase noise over a certain bandwidth (jitter) is an performance specification that translates to signal-to-noise ratio. Phase noise inside the loop bandwidth is dominated by the PLL, while the phase noise outside the loop bandwidth is dominated by the VCO. Generally, jitter is lowest if loop bandwidth is designed to the point where the two intersect. A higher phase margin loop filter design has less peaking at the loop bandwidth and thus lower jitter. The tradeoff with this is longer lock times and spurs must be considered in design as well.

Typical Application (continued)

8.2.3 Application Curves

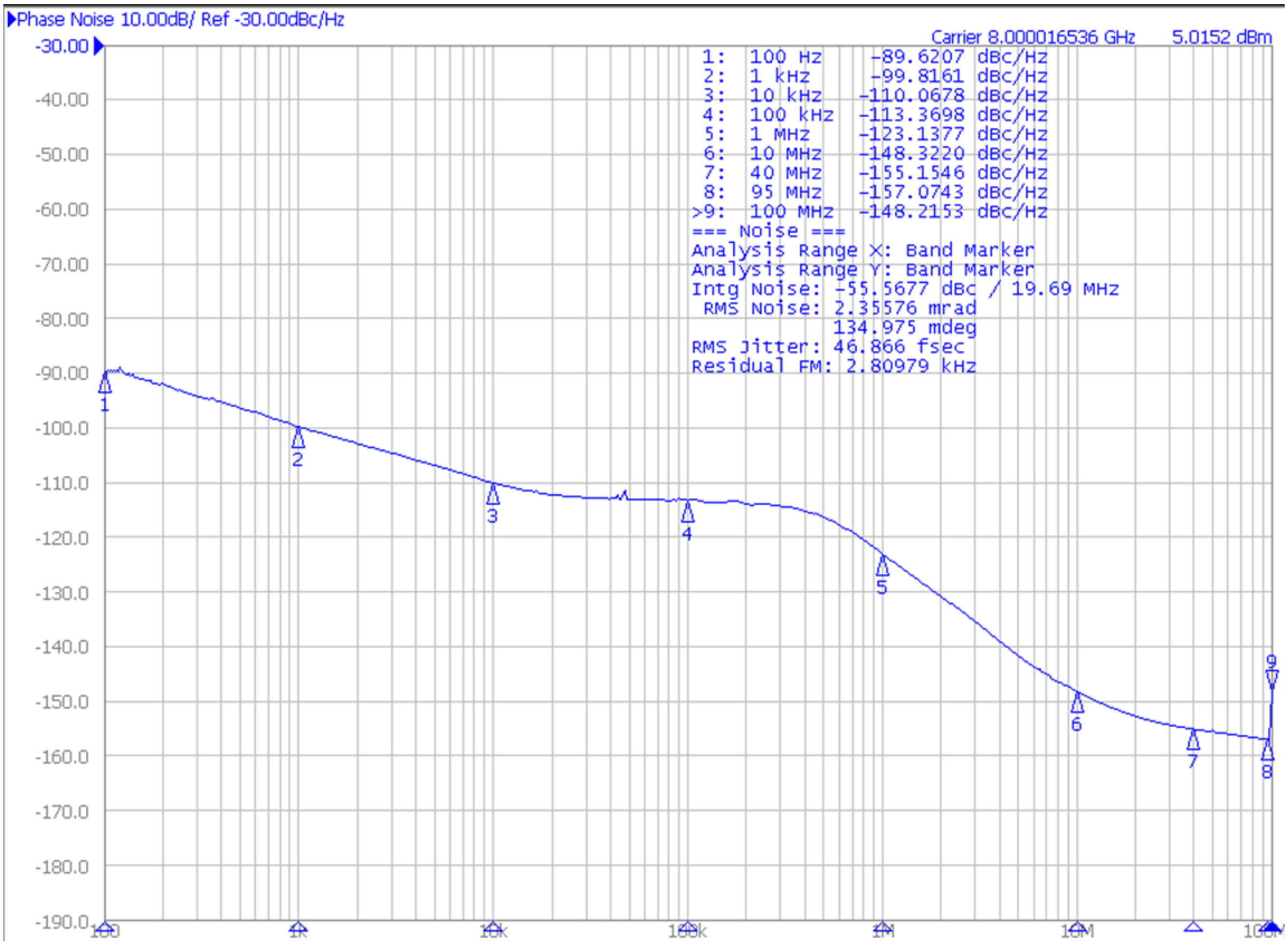


Figure 47. Typical Jitter

9 Power Supply Recommendations

TI recommends placement of 100 nF close to each of the power supply pins. If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins can reduce spurs to a small degree. This device has integrated LDOs, which improves the resistance to power supply noise. However, the pullup components on the RFoutA and RFoutB pins on the outputs have a direct connection to the power supply, so extra care must be made to ensure that the voltage is clean for these pins. Figure 48 is a typical application example.

This device can be powered by an external DC-DC buck converter, such as the TPS62150. Note that although Rtps, Rtps1, and Rtps2 are 0 Ω in the schematic, they could be potentially replaced with a larger resistor value or inductor value for better power supply filtering.

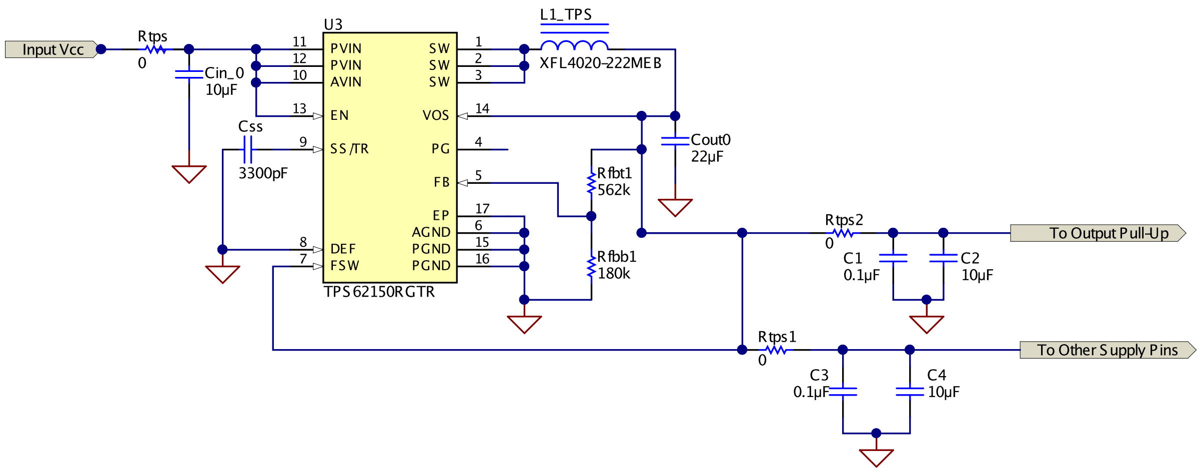


Figure 48. Using the TPS62150 as a Power Supply

10 Layout

10.1 Layout Guidelines

In general, the layout guidelines are similar to most other PLL devices. Here are some specific guidelines.

- GND pins may be routed on the package back to the DAP.
- The OSCin pins, these are internally biased and must be AC coupled.
- If not used, RampCLK, RampDIR, and SysRefReq can be grounded to the DAP.
- For the Vtune pin, try to get a loop filter capacitor as close to this as possible. This may mean separating it from the rest of the loop filter.
- For the outputs, keep the pullup component as close as possible to the pin and use the same component on each side of the differential pair.
- If a single-ended output is needed, the other side must have the same loading and pullup. However, the routing for the used side can be optimized by routing the complementary side through a via to the other side of the board. On this side, use the same pullup and make the load look equivalent to the side that is used.
- Ensure DAP on device is well-grounded with many vias, preferably copper filled.
- Have a thermal pad that is as large as the LMX2594 exposed pad. Add vias to the thermal pad to maximize thermal performance.
- Use a low loss dielectric material, such as Rogers 4003, for optimal output power.
- See instructions for the LMX2594EVM (*LMX2594 EVM Instructions, 15 GHz Wideband Low Noise PLL with Integrated VCO*) for more details on layout.

10.2 Layout Example

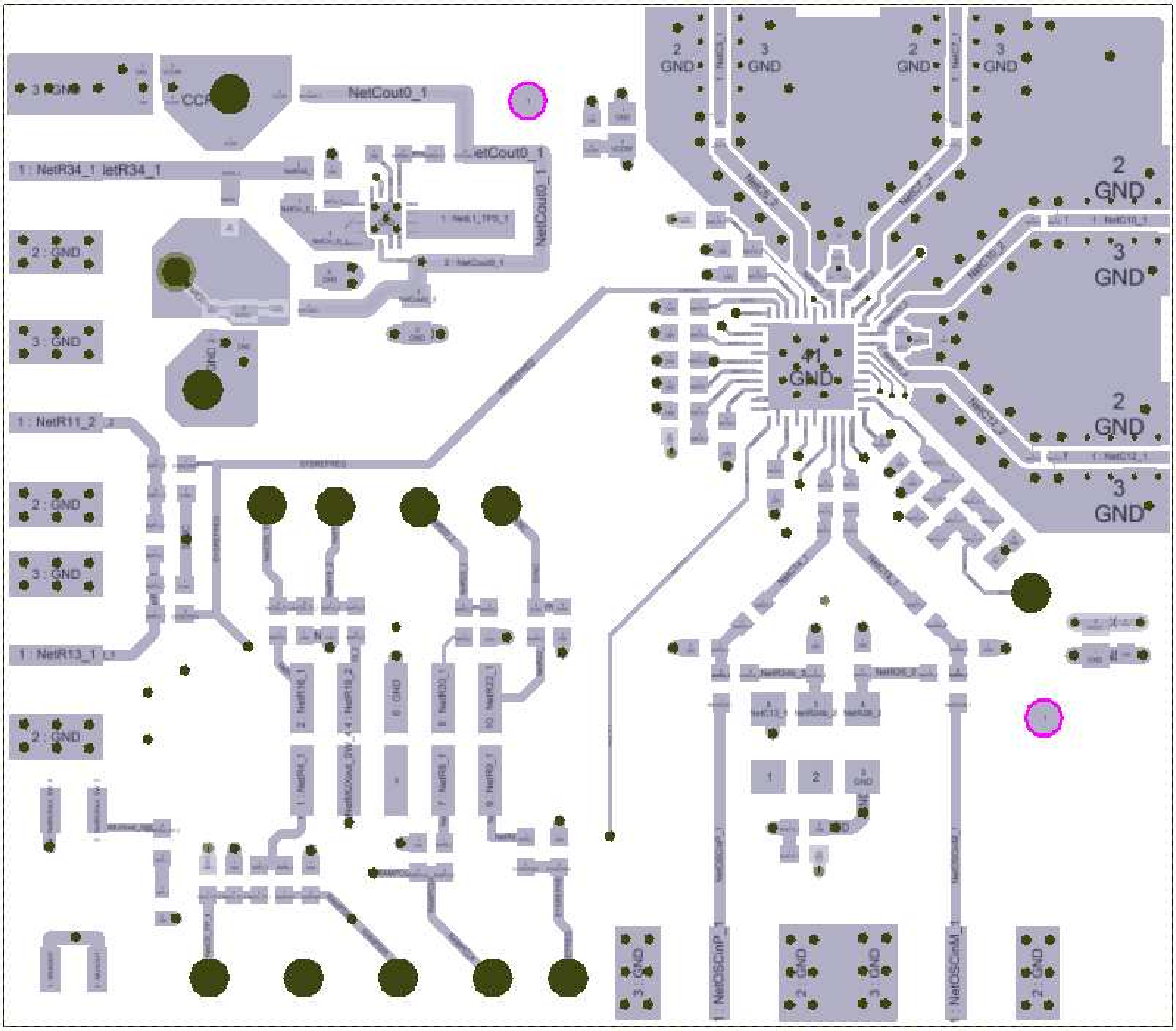


Figure 49. LMX2594 PCB Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

Texas Instruments has several software tools to aid in the development at www.ti.com. Among these tools are:

- EVM software to understand how to program the LMX2594 and for programming the EVM board.
- EVM board instructions for seeing typical measured data with detailed measurement conditions and a complete design.
- PLLatinum Sim program for designing loop filters, simulating phase noise, and simulating spurs on the LMX2594.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *AN-1879 Fractional N Frequency Synthesis*
- *PLL Performance, Simulation, and Design Handbook*
- *LMX2594 EVM Instructions, 15 GHz Wideband Low Noise PLL with Integrated VCO*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMX2594RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2594	Samples
LMX2594RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2594	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

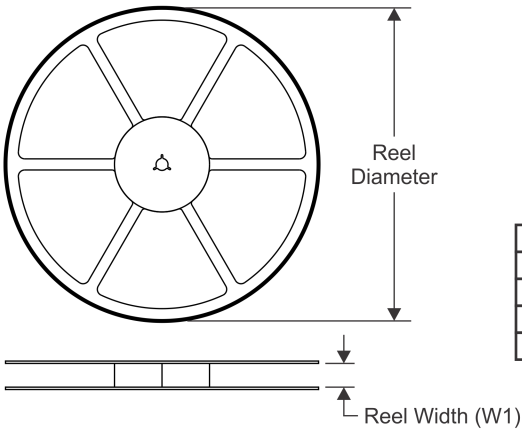
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

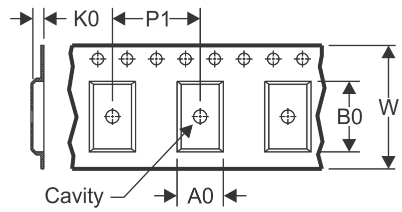
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

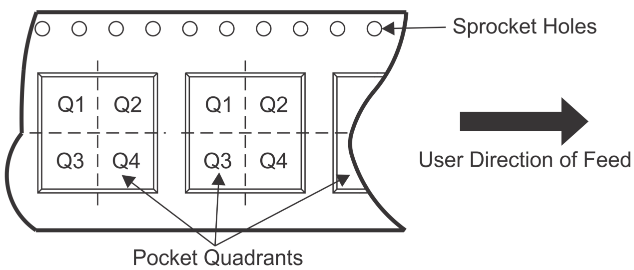


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

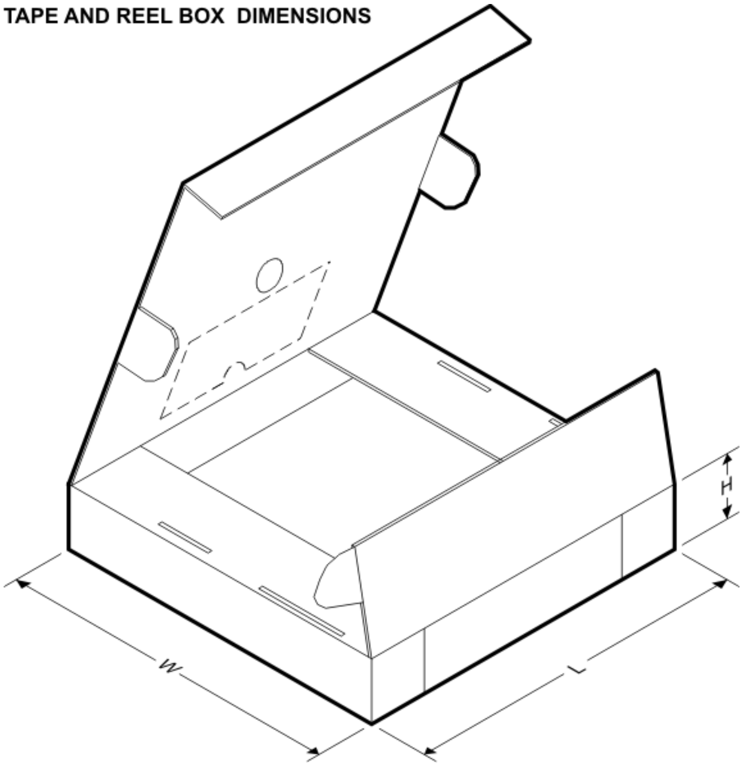
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX2594RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
LMX2594RHAT	VQFN	RHA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

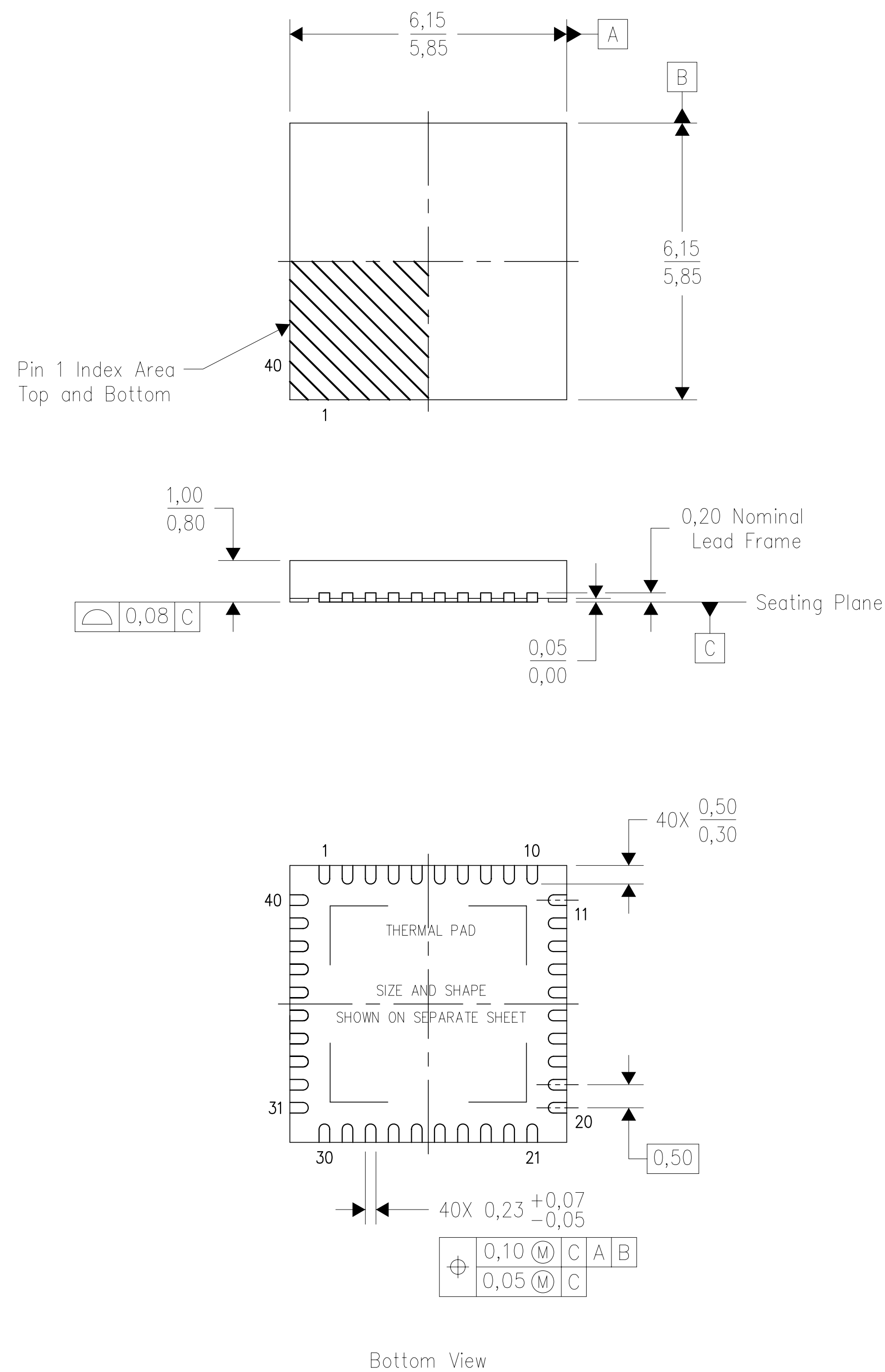
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX2594RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
LMX2594RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD



4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO-220 variation VJJD-2.