PAT9136E1-TXQT: Optical Tracking Chip

General Description

The PAT9136E1-TXQT is PixArt Imaging's latest optical tracking chip designed to enable navigation up to the speed of 5m/s on a wide range of surfaces. The chip is housed in a 6 x 6 x 1.35 mm^3 16-pin land-grid-array (LGA) package with an integrated laser illumination that provides X-Y motion data and consistent resolution. It is suitable for motion tracking in industrial applications.

Key Features

- Performance
  - Speed of up to 5m/s
  - Working Distance to Tracking Surface range of 5 to 50mm on glossy metal surfaces[*1]
  - Working Distance to Tracking Surface range of 10 to 27mm on glossy non-metal surfaces[*2]
  - Typical power consumption of 16.5mA
- No lens required
- Reports accurate XY motion data

Applications

- Devices that require high speed motion detection over a wide working range

Key Parameter

Parameter	Value
Supply Voltage	VDD: 1.8 to 2.1 V VDD_VCSEL: 2.8 to 3.3 V VDDIO: 1.8 to 3.3 V
Working Distance to Tracking Surface	5 to 50 mm*[1]
Frame Rate (max)	20,000 fps
Speed (max)	5 m/s
Acceleration	10 g; 98 m/s^2
Resolution (max)	20,000 cpi; 7,874 count/cm
Interface	4-Wire SPI @ 4 MHz
Package Size (mm^3)	6 x 6 x 1.35

Note*1: Aluminum and glossy stainless steel

Note*2: Glossy vinyl flooring, glossy gypsum board, glossy photo paper, green ESD mat and laminated wood.

Ordering Information

Part Number	Description	Package Type	Packing Type	MOQ
PAT9136E1-TXQT	Optical Tracking Chip	16-pin LGA Package	Tube	2000



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1.0 Introduction

1.1 Overview

The PAT9136E1-TXQT is based on Optical Navigation Technology, which measures changes in position by optically acquiring sequential picture elements and mathematically determining the direction and magnitude of movement. The chip contains a Picture Element Acquisition System (PEAS), a hard-coded Digital Signal Processing System (DSPS), and an integrated VCSEL illumination source.

The chip algorithm calculates the speed, direction, magnitude of motion and stores the motion data output information in the registers. Then, the host either uses the polling method or interrupts triggering for immediate access.

Note: Throughout this document, the PAT9136E1-TXQT is referred to as the "chip".

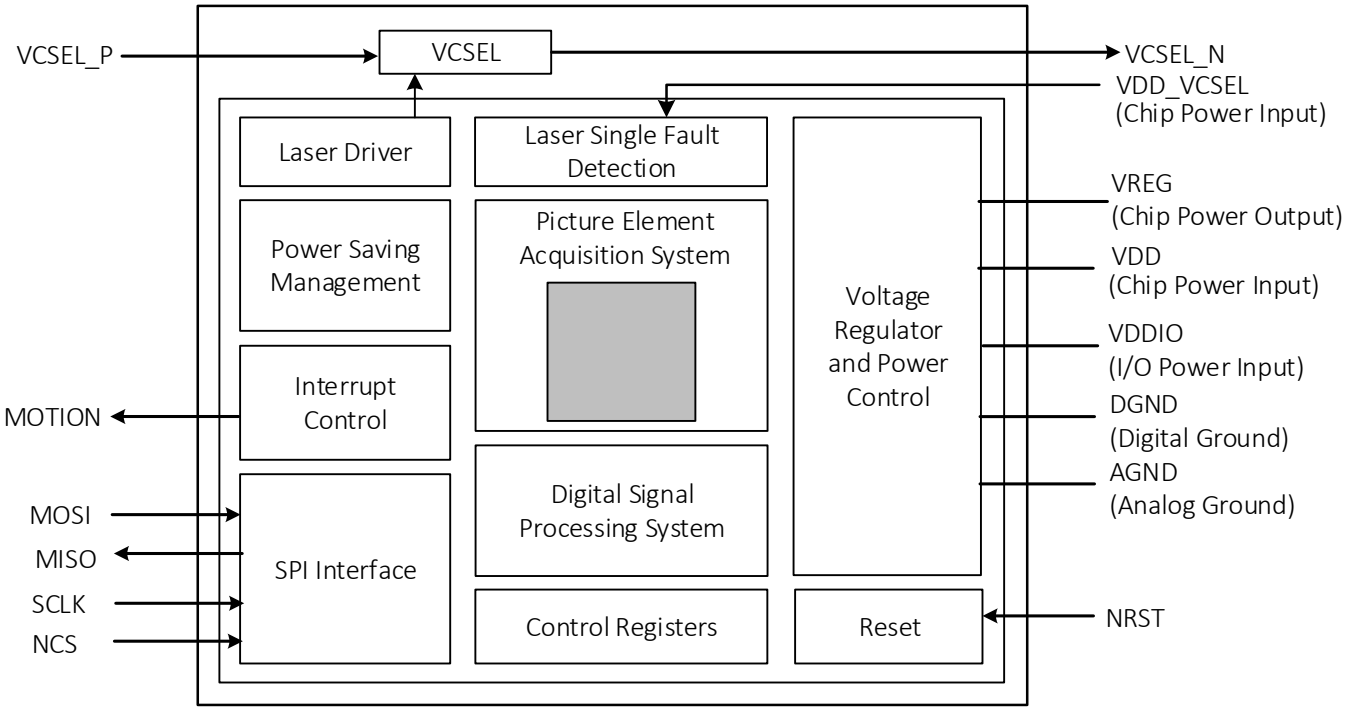

Figure 1. Block Diagram

1.2 Terminology

Term	Description
ESD	Electrostatic Discharge
I/O	Input / Output
VCSEL	Vertical Cavity Surface Emitting LASER
cpi	count per inch
fps	frame per second

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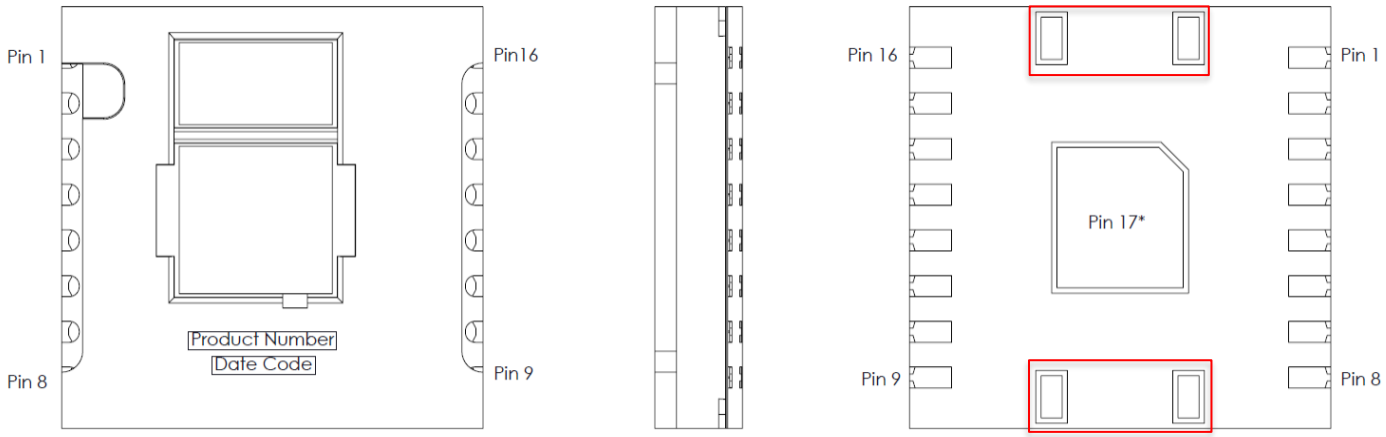
1.3 Signal Description



Note: The 4 pads in Figure 2 (red boxed) must be left unconnected.

Figure 2. Pin Configuration

Table 1. Signal Pins Description

Function	Pin No.	Signal Name	Type	Description
Power Supplies	8	DGND	Ground	Digital Ground
	13	AGND	Ground	Analog Ground
	9	VDDIO	Power	I/O power input
	11	VREG	Power	Chip power output
	12	VDD	Power	Chip power input
	15	VDD_VCSEL	Power	Chip power input
Control Interface	3	NCS	Input	Chip select (Active low)
	4	MISO	Output	Serial data output
	5	MOSI	Input	Serial data input
	6	SCLK	Input	Serial data clock
Functional I/O	2	NRST	Input	Hardware reset (Active low)
	7	MOTION	Output	Motion interrupt (Active low)
Special Function Pin	1	VCSEL_P	Input	Laser Anode
	10, 14	NC	NC	No connection (floating)
	16	VCSEL_N	Output	Laser Cathode
	17*	GND PADDLE	Ground	Bottom of LGA package must be connected to circuit ground.

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2.0 Operating Specification

2.1 Absolute Maximum Rating

Table 2. Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-40	85	°C	
Lead-Free Solder Temperature	T_{SOLDER}		260	°C	
Supply Voltage	VDD	-0.5	2.1	V	
	VDD_VCSEL	-0.5	3.3	V	
	VDDIO	-0.5	3.3	V	
Input Voltage	V_{IN}	-0.5	3.3	V	All I/O pins
ESD	ESD_{HBM}		2	kV	All pins (Human Body Model)

Notes:

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.

2.2 Recommended Operating Condition

Table 3. Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Temperature	T_A	0		60	°C	
Power Supply Voltage	VDD	1.8	1.9	2.1	V	Including supply noise
	VDD_VCSEL	2.8	3.0	3.3	V	Including supply noise
	VDDIO	1.8	1.9	3.3	V	Including supply noise
Power Supply Rise Time	t_{RT}	0.15		20	ms	0 to VDD, VDD_VCSEL & VDDIO min
Supply Noise (Sinusoidal)	V_{NA}			100	mV	Peak to peak noise voltage. 10 kHz to 75 MHz
Serial Port Clock Frequency	f_{SCLK}			4	MHz	50% duty cycle
Resolution	R			20,000	cpi	(7874 count/cm)
Speed[3]	S		3.6	5	m/s	Glossy metal surfaces*[1]
			3.6	5	m/s	Glossy non-metal surfaces*[2]
			1.0	1.5	m/s	Diffuse surface - white paper
Working Distance from Tracking Surface	Z	5		50	mm	Glossy metal surfaces*[1]
		10		27	mm	Glossy non-metal surfaces*[2]
		17		21	mm	Diffuse surface - white paper
Frame Rate	F_R			20,000	fps	
Acceleration	a			98	m/s^2	

Notes:

1. PixArt does not guarantee the performance of the system beyond the recommended operating condition limits.
2. Chip electrical characteristics over recommended operating conditions. Typical values at VDD = 1.9V, VDD_VCSEL = 3.0V, VDDIO = 1.9V, T_A = 25°C.
3. Maximum speed can be achieved when chip moves at 45° while typical speed can be achieved when chip moves at 0° and 90°. Below is the diagram of chip orientation vs chip moving direction.

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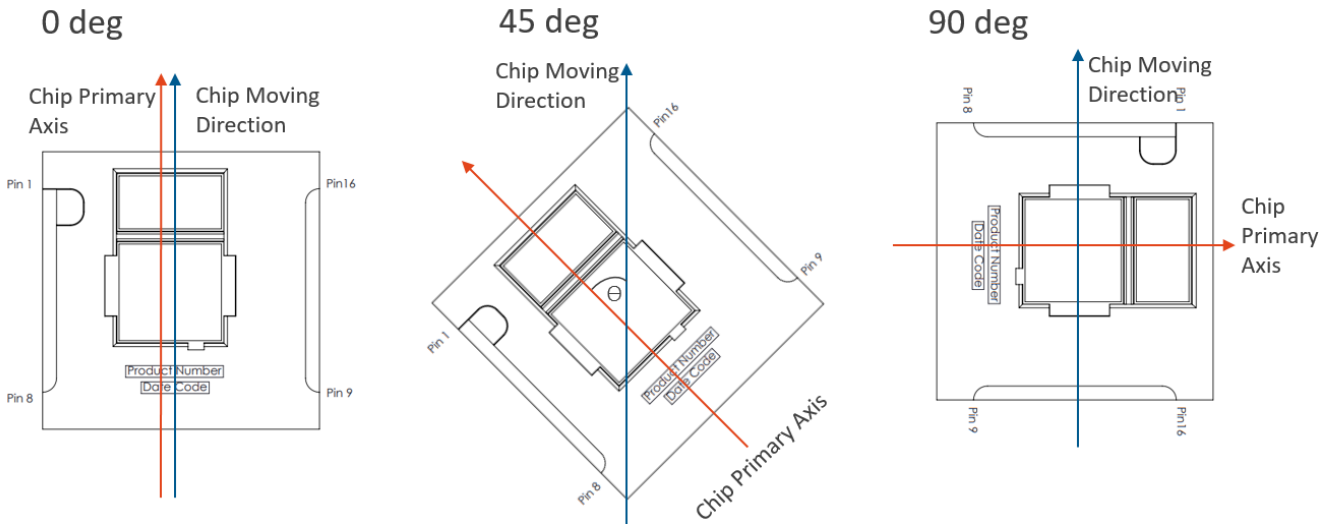

Figure 3. Chip Orientation vs Chip Moving Direction

4. *[1]: Tested on Aluminum and stainless steel.
5. *[2]: Tested on Glossy vinyl flooring, glossy gypsum board, glossy photo paper, green ESD mat and laminated wood.
6. For surfaces such as matte textured tiles, user may execute section 7.1.3 in order to improve the tracking performance. Please note that with the implementation of section 7.1.3, Resolution Variation RV_S% (over speed) will increase to 5%.

2.3 DC Characteristic

Table 4. DC Electrical Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Current	I_{DD_RUN}		14.5		mA	Average current (chip only) No load on MISO, MOTION
	$I_{DD_VCSEL_RUN}$		2		mA	Average current with laser pulsing @ 20k fps
Shutdown state Current	I_{PD}		4		µA	
Input Low Voltage	V_{IL}			0.3 x VDDIO	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	0.7 x VDDIO			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS
Input Leakage Current	I_{LEAK}		± 1	± 10	µA	V_{in} = VDDIO or 0V, SCLK, MOSI, NCS
Output Low Voltage	V_{OL}			0.45	V	I_{OUT} = 1mA for MISO I_{OUT} = 0.1mA for MOTION
Output High Voltage	V_{OH}	VDDIO -0.45			V	I_{OUT} = -1mA for MISO I_{OUT} = -0.1mA for MOTION

Note: Chip electrical characteristics over recommended operating conditions. Typical values at VDD = 1.9V, VDD_VCSEL = 3.0V, VDDIO = 1.9V, T_A = 25°C.

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2.4 AC Characteristic

Table 5. AC Electrical Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Motion Delay After Reset Time	$t_{MOT-RST}$	120			ms	From reset to valid motion, assuming motion is present.
Shutdown State Time	t_{STDWN}			500	ms	From Shutdown State active to low current.
Wake up from Shutdown State Time	t_{WAKEUP}	120			ms	From Shutdown State inactive to valid motion. Note: 1. A RESET must be asserted after a Shutdown State. 2. Refer to section 5.3, also note $t_{MOT-RST}$.
MISO Rise Time	t_{r-MISO}		6		ns	C_L = 20pF
MISO Fall Time	t_{f-MISO}		6		ns	C_L = 20pF
MISO Delay After SCLK	$t_{DLY-MISO}$			35	ns	From SCLK falling edge to MISO data valid. C_L = 20pF.
MISO Hold Time	$t_{hold-MISO}$	25			ns	Data held until next falling SCLK edge.
MOSI Hold Time	$t_{hold-MOSI}$	25			ns	Amount of time data is valid after SCLK rising edge.
MOSI Setup Time	$t_{setup-MOSI}$	25			ns	From data valid to SCLK rising edge.
SPI Time Between Write Commands	t_{SWW}	5			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI Time between Write and Read Commands	t_{SWR}	5			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI Time between Read and Subsequent Commands	t_{SRW}, t_{SRR}	2			µs	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI Read Address-Data Delay	t_{SRAD}	2			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
NCS Inactive After Motion Burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS To SCLK Active	$t_{NCS-SCLK}$	120			ns	From last NCS falling edge to first SCLK rising edge.
SCLK To NCS Inactive (For Read Operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer.

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
SCLK To NCS Inactive (For Write Operation)	$t_{SCLK-NCS}$	1			µs	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer.
NCS To MISO High-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state.
MOTION Rise Time	$t_{r-MOTION}$		300		ns	C_L = 20pF
MOTION Fall Time	$t_{f-MOTION}$		300		ns	C_L = 20pF
Input Capacitance	C_{in}		10		pF	SCLK, MOSI, NCS.
Load Capacitance	C_L			20	pF	MISO, MOTION
Transient Supply Current	I_{DDT}			70	mA	Maximum supply current during the supply ramp from 0V to VDD with minimum 150 µs and maximum 20 ms rise time (does not include charging currents for bypass capacitors).
	I_{DDTIO}			60	mA	Maximum supply current during the supply ramp from 0V to VDDIO with minimum 150 µs and maximum 20 ms rise time (does not include charging currents for bypass capacitors).

2.5 Performance Specification

Table 6. Resolution Variation Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Resolution Variation*	RV		1		%	At constant Speed and Working Distance from Tracking Surface @ 787 count/ cm.
Resolution Variation* (Over Height)	RV_H		3		%	At constant Speed, across Working Distance from Tracking Surface range @ 787 count/ cm.
Resolution Variation* (Over Speed)	RV_S		3		%	At constant Working Distance from Tracking Surface, up to max. Speed @ 787 count/ cm.

Note: *: Resolution Variation, RV = $\frac{(Rmax-Rmin)}{(Raverage)\ x\ 2}\ x\ 100\%$, chip mounted and tested at 45°.

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3.0 Mechanical Specification

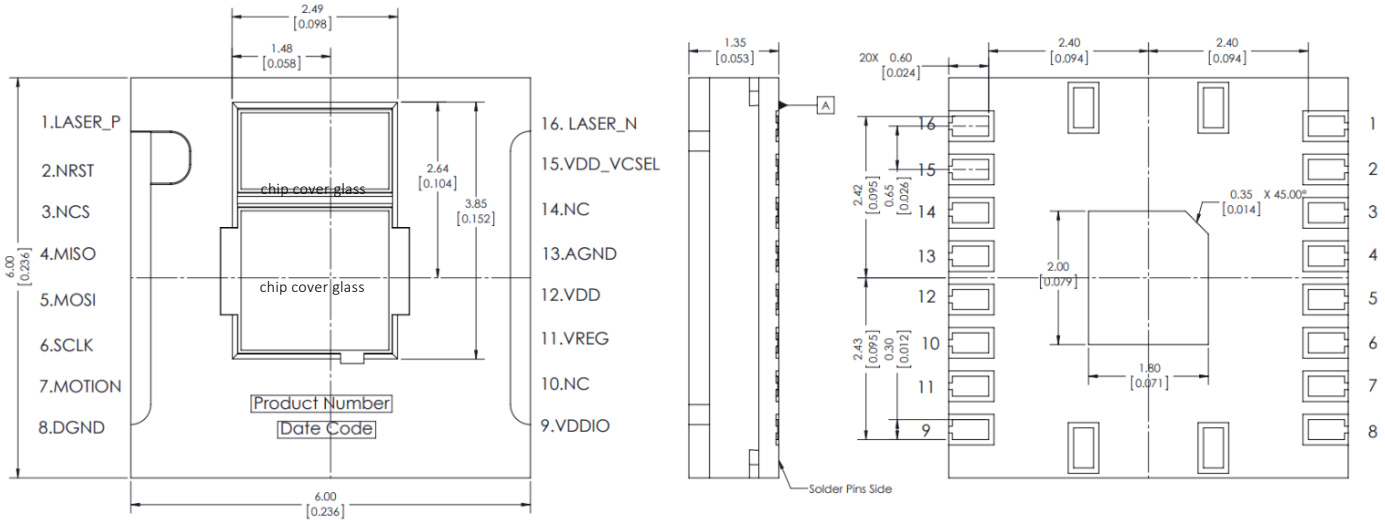
3.1 Package Marking

Refer to Figure 2. Pin Configuration for the code marking location on the device package.

Table 7. Code Identification

Label	Marking	Description
Product Number	P9136	Part number label
Date Code	YWX	Y: Year W: Week X: Reserved as PixArt reference

3.2 LGA Package Outline Drawing



Notes:

1. Dimensions in milimeter [inches]
2. Dimensional tolerance: ±0.1mm
3. Coplanarity of lead:0.1mm
4. Lead pitch tolerance: ±0.15mm

Notes:

5. Non-cumulative pitch tolerance: ±0.15mm
6. Maximum Burr:0.2mm
7. Angular tolerance: ±3°
8. Brackets () indicate reference dimension
9. Document Number:16L-6x6-LGA-G8

Note: It is advised that normal static discharge precautions be taken in handling and assembling of this component to prevent damage and/or degradation which may be induced by ESD.

Figure 4. LGA Package Outline Drawing

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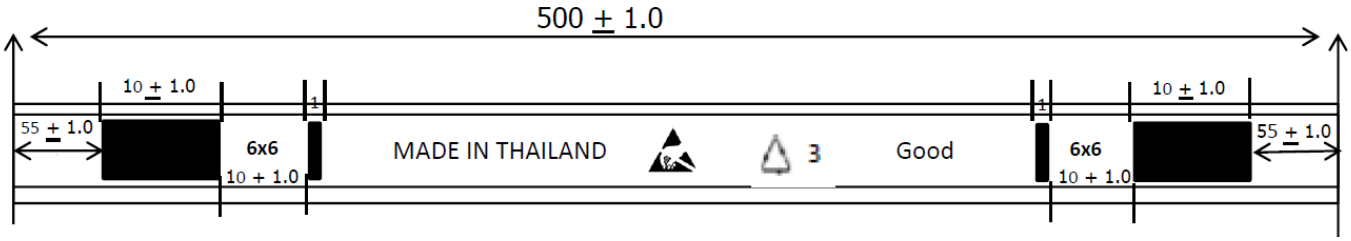
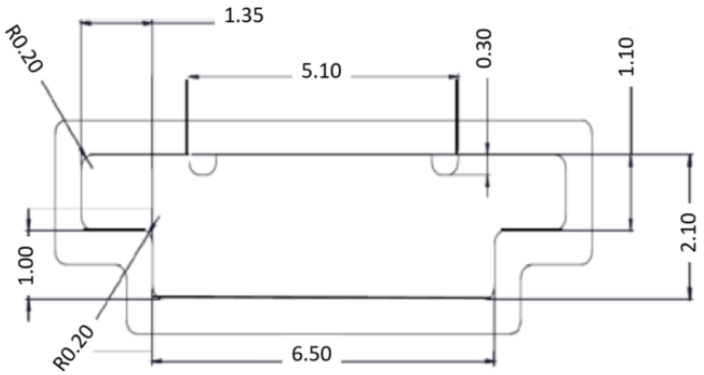
3.3 Packing Information

Parameter	Description
Part Number	PAT9136E1-TXQT
Package Type	16 Pins LGA
Tube Quantity	80 pcs
Packing	Vacuum Pack
Inner Box Quantity	2000 unit
Shipping Box Quantity	24,000 unit
Inner box size	89 x 540 x 58 mm^3
Shipping Box size	310 x 560 x 270 mm^3

Top View



Side View



Tube
Material: CLEAR PVC ANTISTATIC COATED
Marking: As above and add "MADE IN THAILAND" with ESD logo, PVC recycle logo and "Good" at center of tube.
Tolerance: ± 0.15mm unless specify.
Units are in mm.

Figure 5. Tube Dimension

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Figure 6. Moisture Barrier Bag

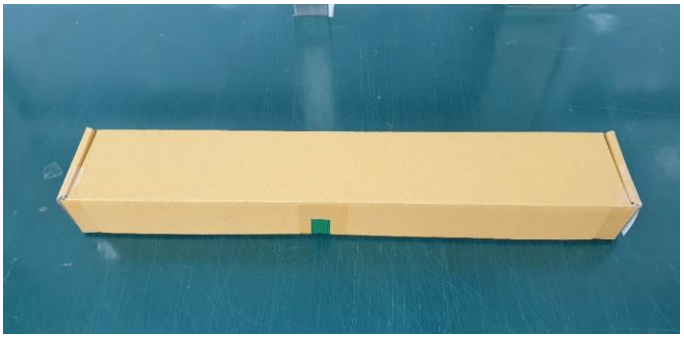

Figure 7. Inner Box

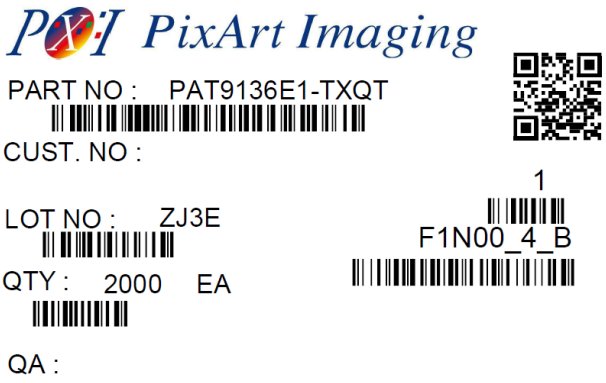

Figure 8. Inner Box Label



Figure 9. Shipping Box

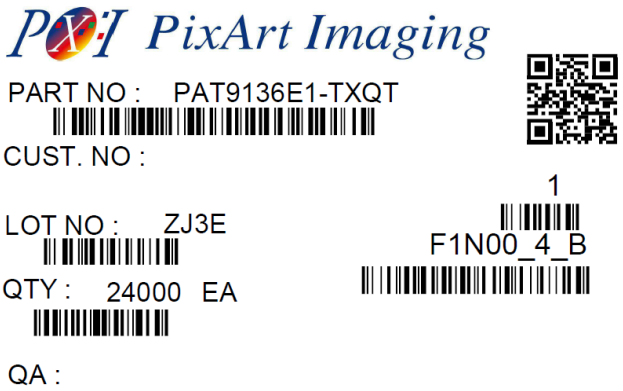

Figure 10. Shipping Box Label

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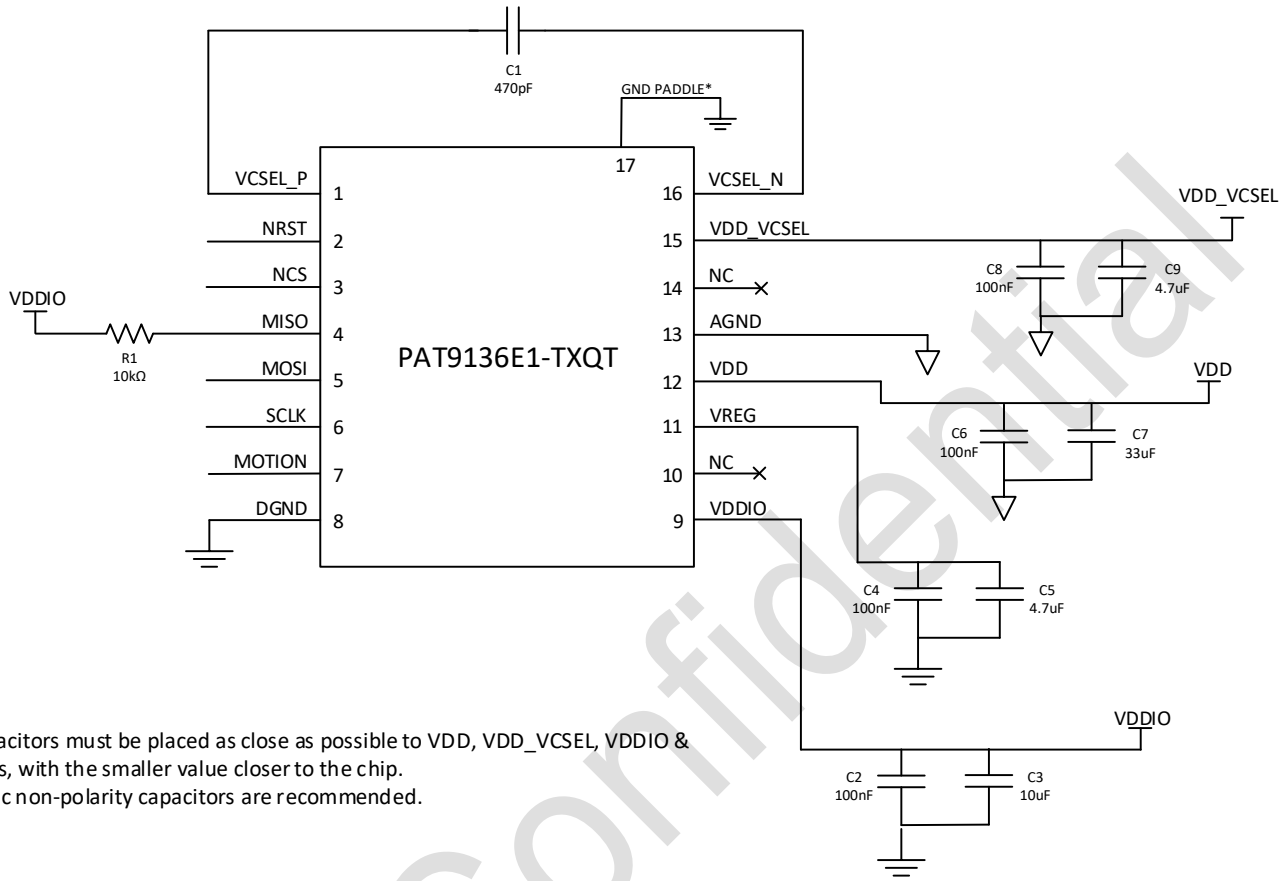
4.0 Design Reference

4.1 General Reference Schematic



Note:
1. All capacitors must be placed as close as possible to VDD, VDD_VCSEL, VDDIO & VREG pins, with the smaller value closer to the chip.
2. Ceramic non-polarity capacitors are recommended.

Figure 11. Reference Schematic

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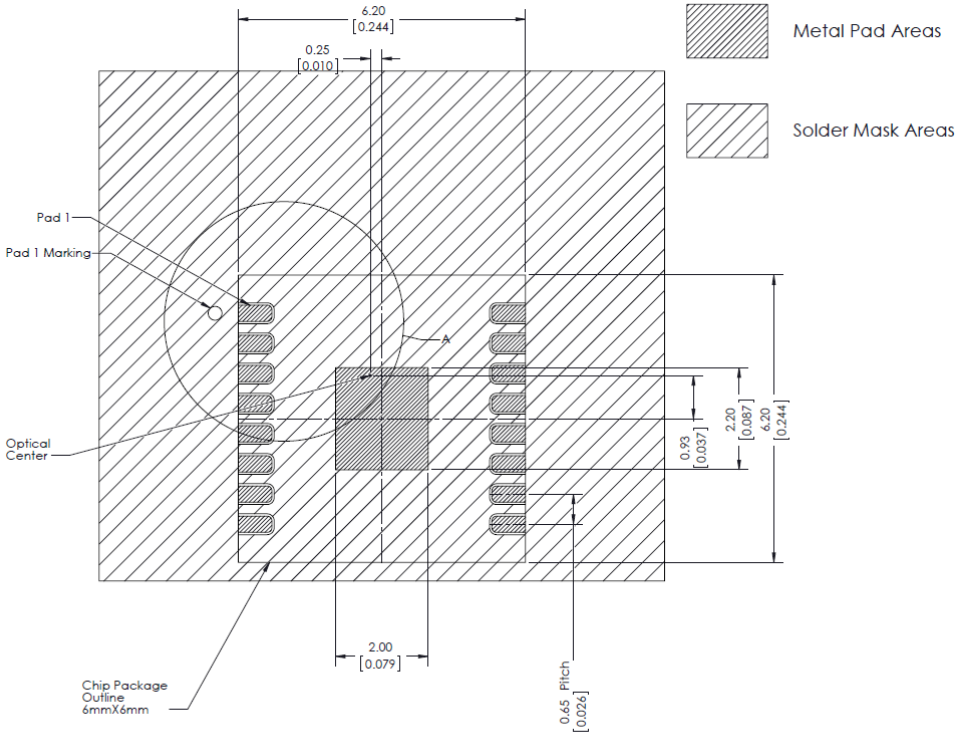
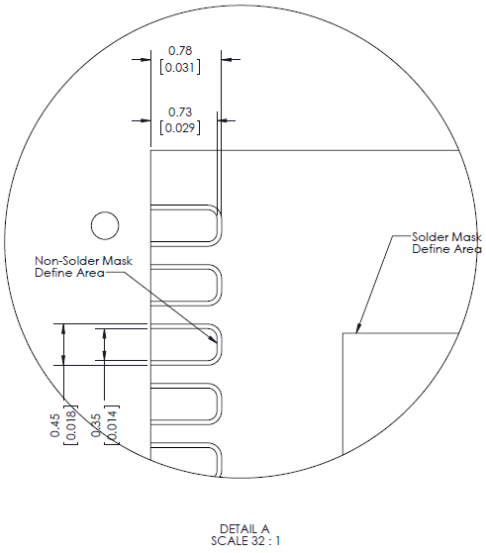
4.2 Recommended PCB Foot Print



Note: Bottom center pad of LGA package must be connected to circuit ground



Notes:

1. Dimensions in milimeter [inches]
2. Dimensional tolerance: ±0.1mm
3. Coplanarity of lead:0.1mm
4. Lead pitch tolerance: ±0.15mm
5. Non-cumulative pitch tolerance: ±0.15mm
6. Angular tolerance: ±3°
7. Brackets () indicate reference dimension

Figure 12. Recommended PCB Layout in mm [inch]

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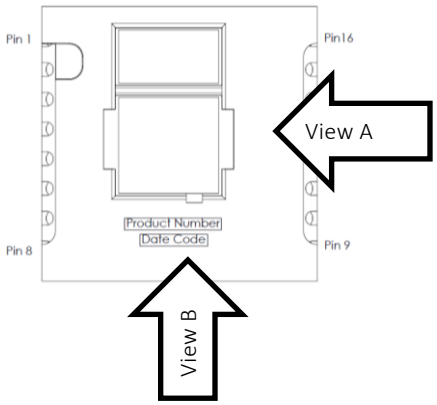
4.3 Chip Assembly Tilt

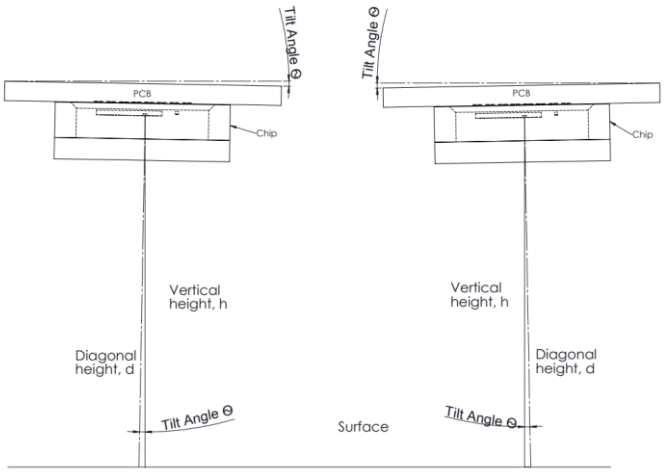
For optimal performance, there should be minimal tilt to the assembly of the chip on the PCB. The tilt should not be more than 3 degrees for trackable surfaces.

If the tilt angle is larger than 3 degrees, the Resolution Variation % will increase significantly over the working range stated in Table 3.

Chip Tilt Angles are defined per below drawings from view A and view B.



View A



View B

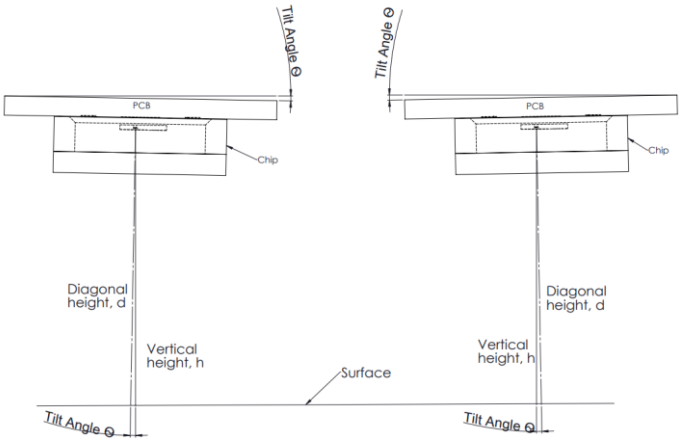


Figure 13. Tilt Definition

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4.4 Keep Out Area

A keep out area of 30° angle is recommended to ensure the optical path of the sensor is not blocked.

The 30° angle is from the top of the protective cover for the chip.

For protective cover design, please refer to Protection Cover Design Application Notes.

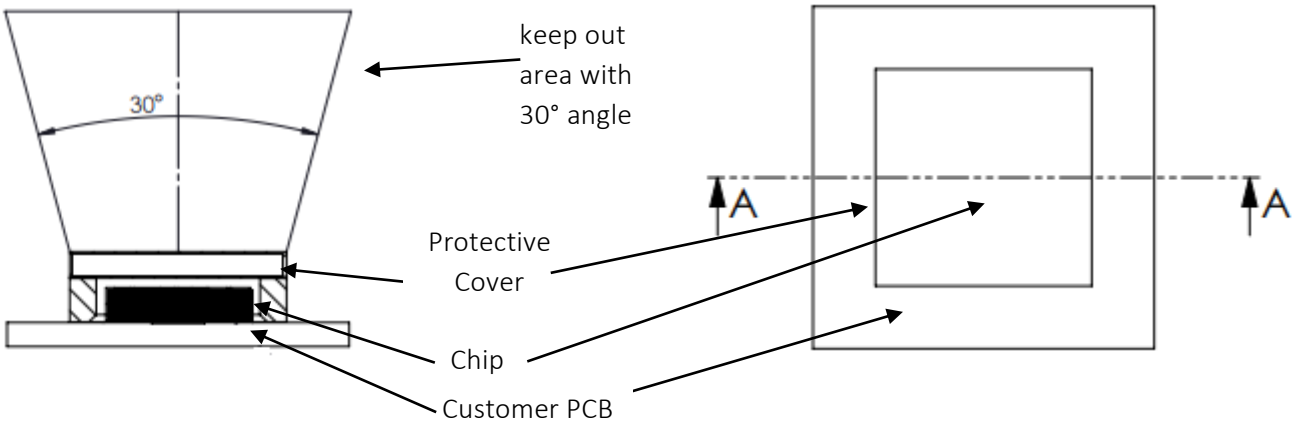

Figure 14. Side View and Top View of Keep Out Area

4.5 Assembly Guide

4.5.1 Handling Precaution of Moisture Sensitivity During Assembly Processes

This product is classified as moisture sensitivity device at Level 3 (MSL 3). Thus, the following moisture sensitive precaution and handling steps are required during the Assembly processes.

Storage Control of Unopened Box/ Seal Bag

This product is shipped in a vacuum sealed Moisture Barrier bag (MBB) together with desiccant and a moisture indicator card inside.

The shelf life in the unopened sealed bag is 12 months at storage condition of < 40°C/90% relative humidity (RH). It is advised that the vacuum sealed MBB only be opened at the START of assembly process.

Control of Opened Seal Bag

After the vacuum sealed MBB is opened, the product MUST be subjected to reflow solder and PCB mounting within 168 hours of the factory condition < 30°C/60% RH.

Control of Un-reflow Units

Any balance of un-reflow units need to be sealed back to the MBB with desiccant at < 5% RH.

The product requires Baking, before mounting, if the following conditions happen:

- Assembly floor life exceeded 168 hours after the sealed MBB is opened.
- Humidity Indicator Card (HIC) is > 10% when read at 23°C ± 5°C.

Recommended Baking condition is 125°C ± 10°C for 48 hours. Please refer to IPC/JEDEC J-STD-033 for Baking procedures.

Note: The shipping Tube cannot be subjected to high temperature baking. Transfer to an appropriate container for baking.

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4.5.2 Assembly Recommendation

For surface mount the chip and all other components onto PCB:

1. Reflow the entire assembly in a no-wash solder process.

   Note: Recommended to generate a stencil for the reflow process.

2. Remove the protective Kapton tape on top of the chip's package, which is meant to protect the cover glass in Figure 4. from contamination.

   Note: After the Kapton tape is removed, please take note to keep the cover glass (on the top of the chip's package) from contamination.

4.5.3 ESD Precaution

This chip is a sensitive device, ESD awareness is mandatory to prevent premature damage during handling.

Below are recommended procedures to prevent electrostatic discharge towards semiconductor devices:

- Equalize potentials of terminals during transportation or storage.
- Equalize the potentials of all electronic devices, work station, and operator's body that may have possible contact with the chip.
- Ensure maintaining an ESD free environment at all times. For example, maintain relative humidity in the work area to around 50%.

Operator

- Operators must wear wrist straps in contact with bare skin.
- Wear cotton or anti-static treated materials, clothing and gloves.
- Wear conductive shoes whenever a conductive mat is used.
- Do not touch the pins, hold the body of the chip instead.

Equipment and Tools

- Any electrical equipment and tool placed on the work bench must be isolated from the work bench's surface, and need to be grounded properly.
- Conductive mat (or conductive material) must be used on work bench's surface. These conductive materials must be grounded with a 1 MΩ resistor.

Transportation, Storage and Packing

- Use conductive or anti-static shielding bags to store chips.

Soldering Operation

- Use a soldering iron with a grounding wire.
- During manual soldering operation, the operator must wear wrist straps.
- Do not use the solder removal pump when detaching the chip from PCB. Use solder wick or equivalent tools.

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4.5.4 IR Reflow Soldering Profile

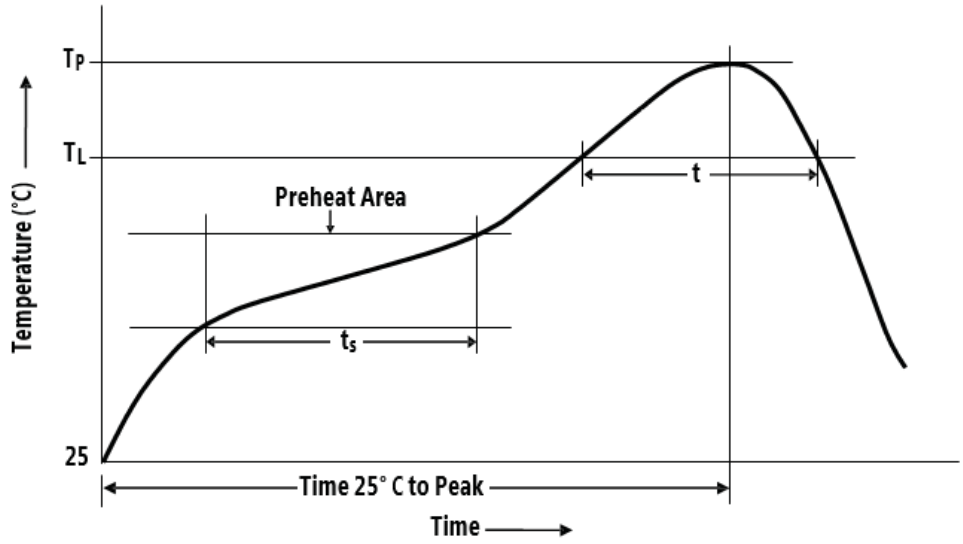

Figure 15. Solder Reflow Profile

Table 8. Soldering Profile

Parameter	Specification
Max. Rising Slope	0° – 3°C/sec
Preheat Duration (150 – 190°C), t_s	60 – 120 sec
Time above Reflow (T_L = 220°C), t	30 – 60 sec
Peak Temperature, T_p	230 – 260°C

Note: T_L is the Melting Temperature

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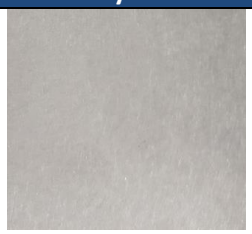
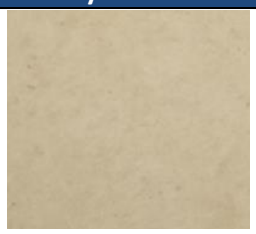
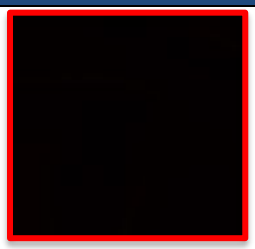
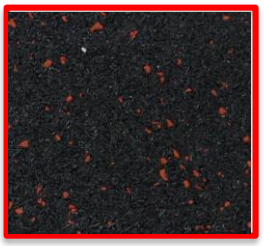
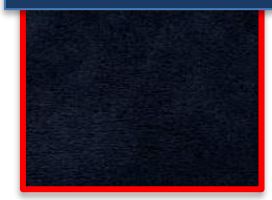
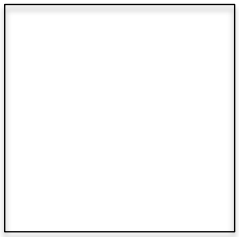
4.6 Surface Coverage

While the chip can track on a variety of common surfaces such as glossy metal, glossy non-metal and tiles, there are some challenges to track on dark, absorptive and very rough surfaces (highlighted in red below), where tracking performance or working range may be impacted. Refer to below figure for examples of the surfaces mentioned.

Glossy Metal	Glossy Non-Metal	Wood	Others
 Aluminum	 Glossy Gypsum Flooring	 Laminated Wood	 Dark Absorptive Art Paper
 Glossy Stainless Steel	 Glossy Grey Vinyl Flooring	 Light Brown Wood	 Very Rough Tiles
 Black Painted Metal	 Dark Granite	 Dark Plywood	 Dark Absoptive Rubber Mat (with or without Color Spots)
	 Glossy Photo Paper	Carpet  Black Carpet	 Rough Vinyl Flooring (Wood Pattern)
	 Green ESD Mat	 Crimson Carpet	 Diffuse A4 Paper

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5.0 Power Management

5.1 Power Supply

The chip has a total of three Power Supply input (VDD, VDDIO and VDD_VCSEL). VDD is the main power supply. VDDIO is the supply for I/O reference voltage. VDD_VCSEL is the power supply to the VCSEL.

5.2 Power Sequence

5.2.1 Power On

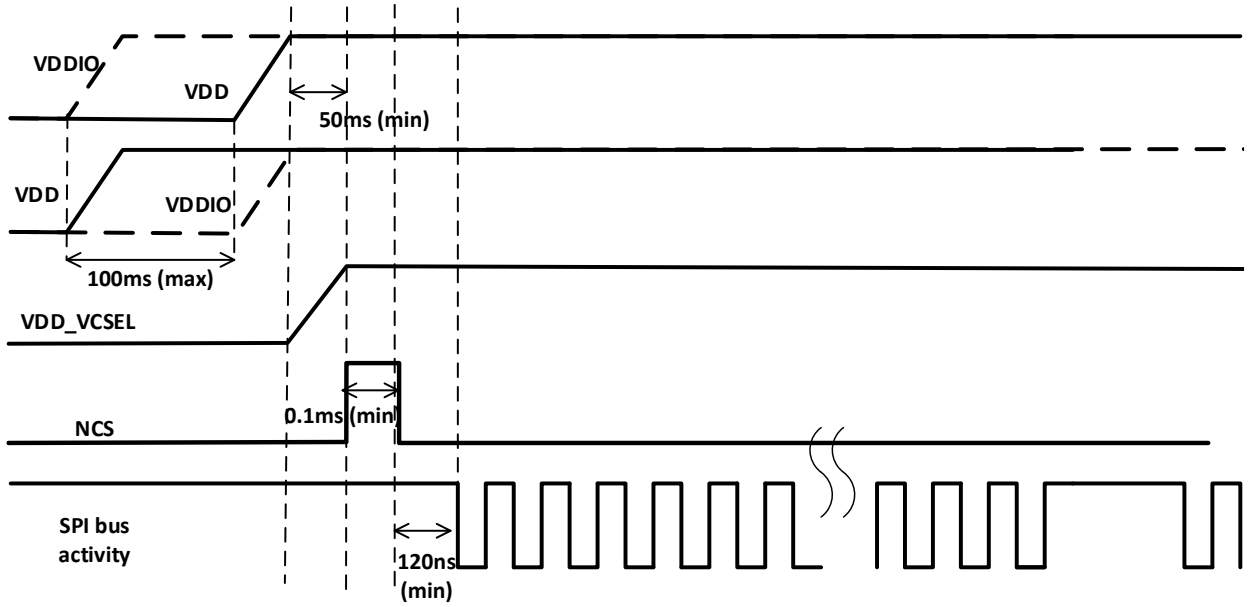

Figure 16. Power-on Sequence Requirement

The appropriate sequence is as below:

1. Apply power to VDD and VDDIO in any order, with a maximum of 100ms delay in between each supply. Ensure all supplies are stable.
2. Wait for at least 50 ms.
3. VDD_VCSEL power on after both VDD and VDDIO are stable.
4. Drive NCS to high state for 0.1ms, and then to low state to reset the SPI port.
5. SPI bus activity can be executed after waiting a min 120 ns after NCS reset.
6. Write 0x5A to register 0x3A (Power_Up_Reset) or alternatively toggle NRST pin for >20µs for hardware reset.

Refer to Section 7.1.2 Performance Optimization Setting to configure the required registers to achieve optimum performance of the chip.

5.2.2 Power Off

It is recommended to power off VDD, VDD_VCSEL and VDDIO at the same time.

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5.3 Power State

5.3.1 State Description

Table 9. Power State Description

State	Description
OFF	No power supply, all the voltage rails and clocks are gated.
Run	▪ Upon powered on, the chip enters Ready state mainly for loading the initial and customized chip parameter settings. The chip will not be activated until host command is fully executed. ▪ The chip enters Run state upon receiving the host commands to load its required setting. This is the state where the chip executes and deliver the required data according to the host command.
Shutdown	The chip enters this state for power saving purpose upon receiving Shutdown command.

5.3.2 State Diagram

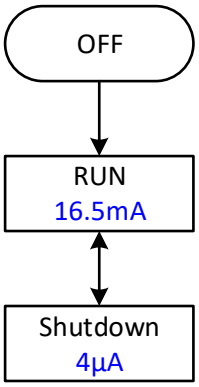

Figure 17. State Diagram

5.3.3 State Transition

Table 10. State Transition

State	Control Type	Description
OFF to Run	Power up	After power up the chip, the SPI interface will be ready in 50ms. Upon SPI interface is ready, initialize the chip by loading the performance optimization settings (refer to Section 7.1.2 for more details) from the host. When initialization is completed, the chip enters Run state automatically.
Run to Shutdown	Command	Shutdown of the chip can be achieved by Write 0xB6 to register 0x3B (Shutdown) to set the chip to Shutdown state. NCS pin is recommended to be pulled to high state during Shutdown.
Shutdown to Run	Command	To wake up from Shutdown state, write 0x5A to register 0x3A (Power_Up_Reset) through SPI interface. Initialize the chip by loading the initial settings (refer to Section 7.1.2 for more details) from the host. When the chip initialization is completed, it enters Run State automatically.

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5.4 Reset and Shutdown State

There are three approaches to trigger chip reset. All previous registers value will be cleared after each reset.

Table 11. State of Signal Pins during Reset and After Reset

State of Signal Pins after VDD & VDDIO are valid		
Pin	**During Reset**	**After Reset**
NRST	Functional	Functional
NCS	Ignored	Functional
MISO	Undefined	Depends on NCS
SCLK	Ignored	Depends on NCS
MOSI	Ignored	Depends on NCS
MOTION	Undefined	Functional

The table below shows the state of the various pins during Shutdown.

Table 12. State of Signal Pins during Shutdown

Pin	Status during Shutdown State
NRST	High
NCS	High
MISO	Hi-Z
SCLK	Ignore if NCS = 1
MOSI	Ignore if NCS = 1
MOTION	High

5.4.1 Power-on Reset

During power-on, the chip performs power-on reset. Refer to Section 2.2 for power supply specification detail to ensure power on reset is successful.

5.4.2 Hardware Reset

The NRST pin can be used to perform a complete chip reset. When the NRST pin is asserted, it performs the same function as the Power_Up_Reset register. The NRST pin needs to be asserted (held to logic 0) for at least 20µs. The NRST pin cannot be left floating or unconnected.

5.4.3 Software Reset

The chip can also be reset by writing value 0x5A to register 0x3A (Power_Up_Reset). Upon a software reset being executed, all register settings in Section 7.1.2 must be reloaded according to the selected Option.

Upon a software reset is executed, the host must wait for at least 120ms for next valid motion.

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5.5 Related Register

Usage	Name	Bank	Address
Enter Shutdown state	Shutdown	-	0x3B
Exit Shutdown state and reset	Power_Up_Reset	-	0x3A

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Revision History

Revision Number	Date	Description
0.8	15 Sept 2022	Initial release

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