Contents

Lect. 22: LTspice Tutorial

◆ LTspice ?

LTspice is a free circuit simulation program developed by Linear Technology, now a part of Analog Devices. It is widely used for power conversion, circuit, and power system design. It provides powerful features to help users model and analyze various types of circuits. Additionally, it is widely used among users, with many documents and resources available.

Installation

Lect. 22: LTspice Tutorial

◆ LTspice Installation

- Search for LTspice on Google or click the link below

  https://www.analog.com/en/lp/002/tools/ltspice-simulator-kr.html

Lect. 22: LTspice Tutorial

◆ LTspice Installation

- Download according to your OS version

LTspice 다운로드

사용 중인 운영 체제(OS)에 맞는 LTspice 시뮬레이션 소프트웨어를 다운로드하세요:

모델 업데이트 날짜 - 2023년 12월 12일

윈도우 10 64비트 및 그 이상 다운로드 버전 17.1.15

MacOS 10.15 및 그 이상 다운로드 버전 17.1.5

윈도우용 LTspice XVII 다운로드 (지원 종료)

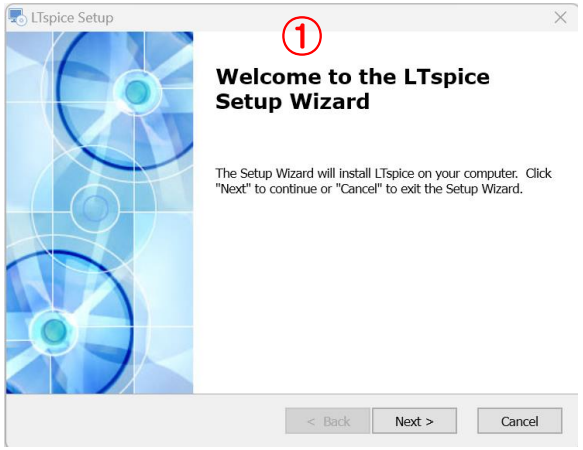
윈도우 XP 다운로드(지원 종료)

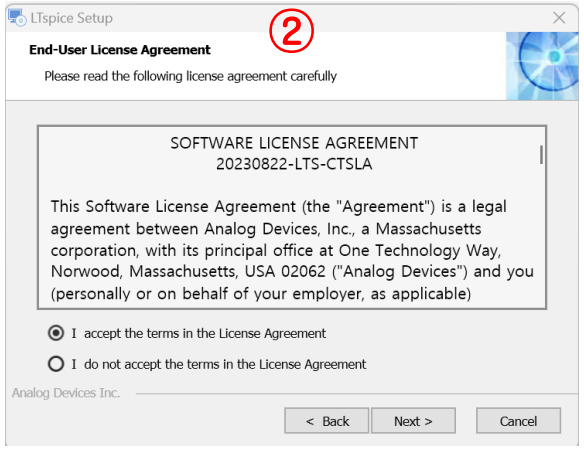
MacOS 10.9 다운로드(지원 종료)

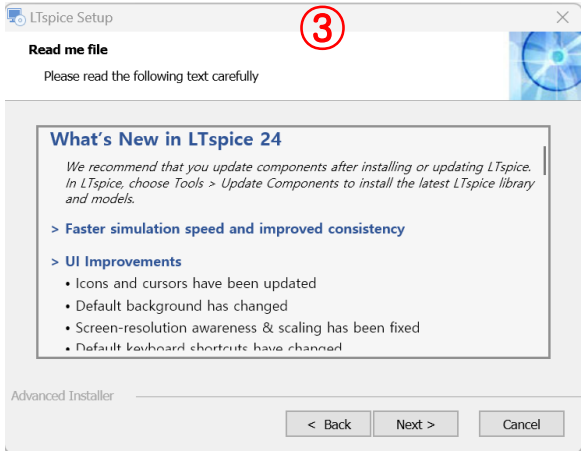
Lect. 22: LTspice Tutorial

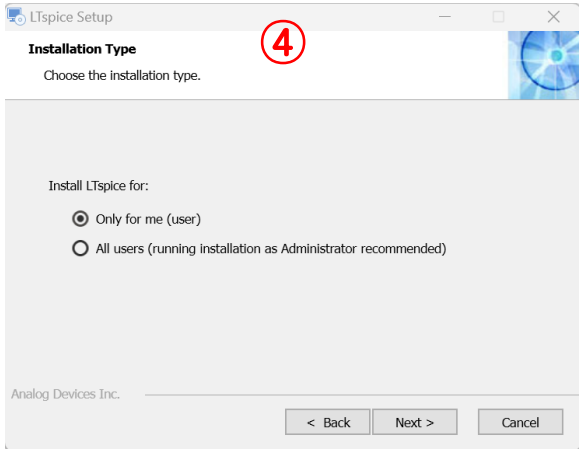
◆ LTspice Installation

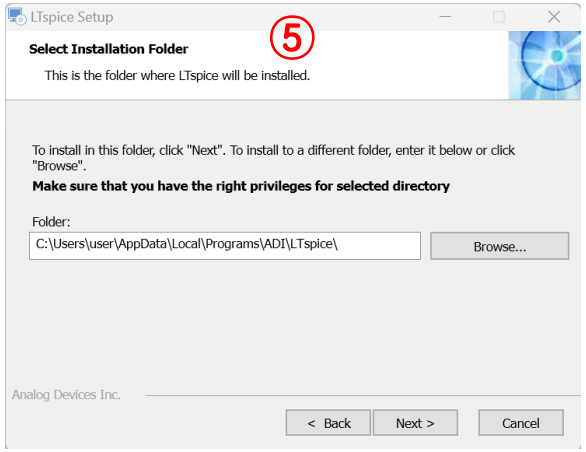
- Execute the downloaded file (LTspice64.msi)

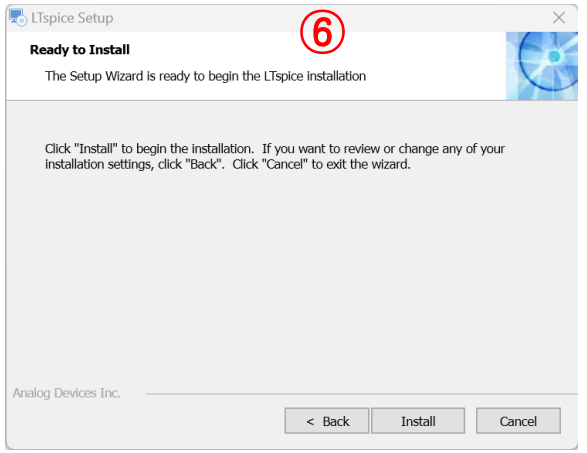








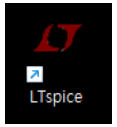




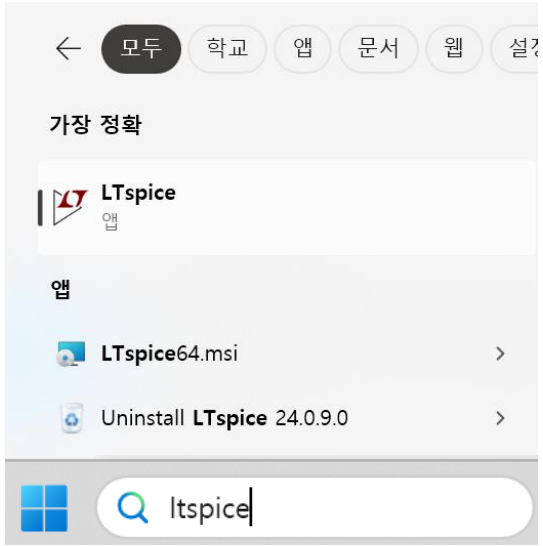
Lect. 22: LTspice Tutorial

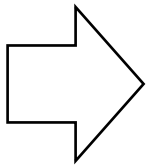
◆ LTspice Installation

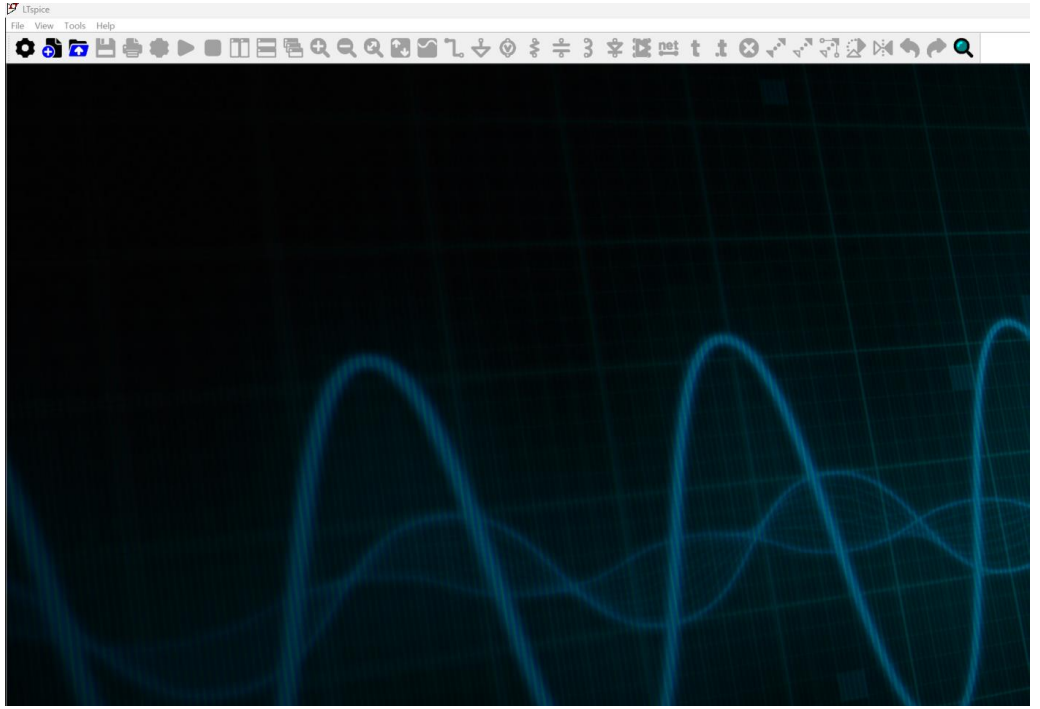
- Search or click the icon on the desktop



or







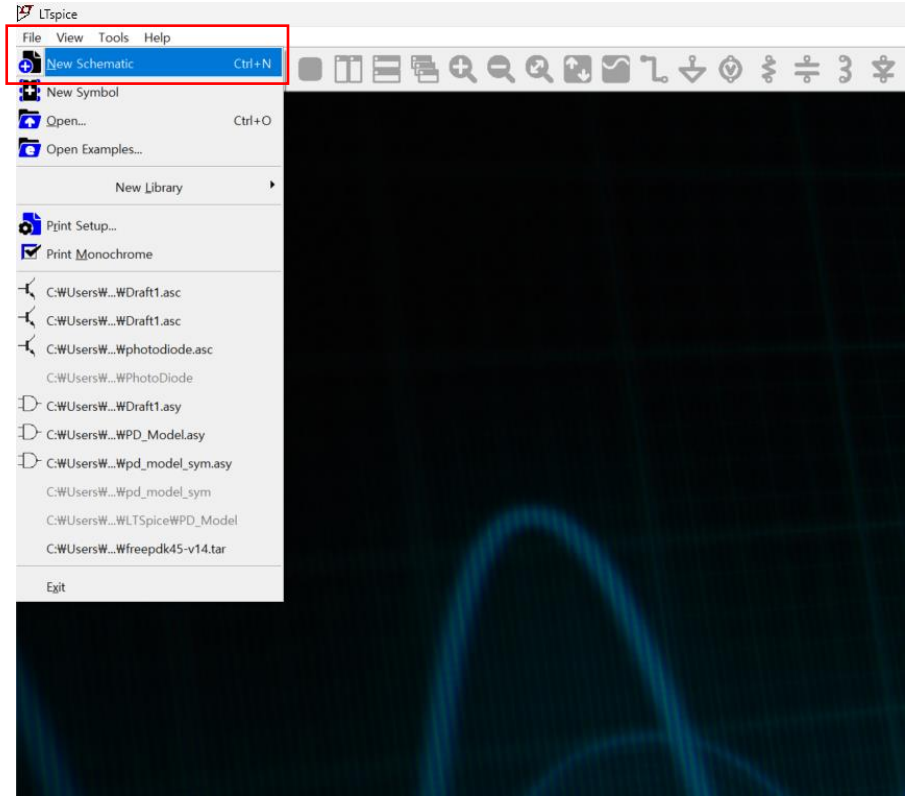
Success !

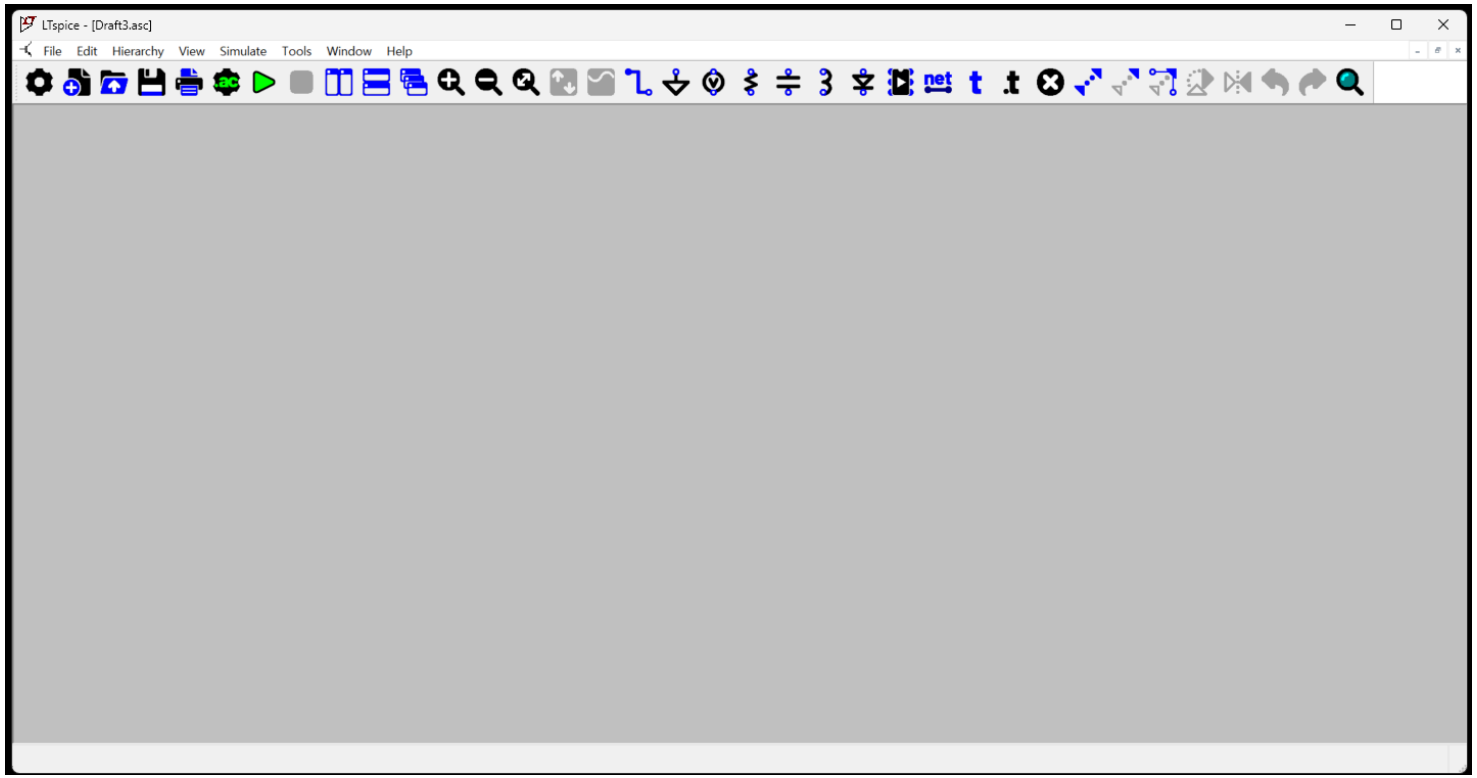
LTspice Basics

Lect. 22: LTspice Tutorial

◆ LTspice Basics

Click on **File** → **New Schematic**, an **empty schematic window will pop-up.**

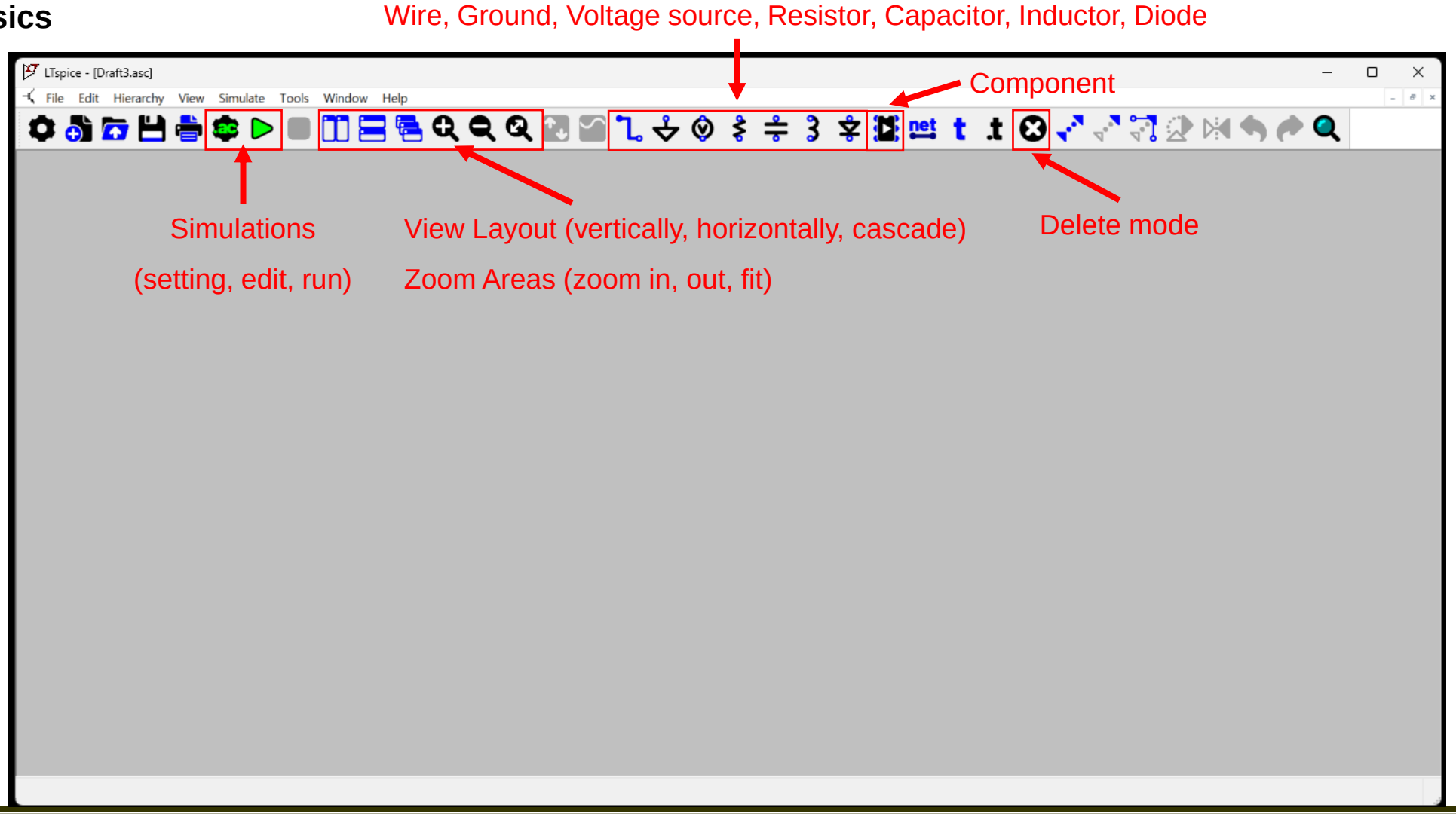




New Schematic Window

Lect. 22: LTspice Tutorial

◆ **LTspice Basics**



Lect. 22: LTspice Tutorial

◆ LTspice Basics – Key shortcuts

Description	Shortcut
Configure Analysis	A
Run/Pause Simulation	Alt + R
Stop Simulation	Alt + S
Zoom to Fit	Space
Place Component	P
Draw Wire	W
Place Ground	G
Place Voltage Source	V
Place Resistor	R
Place Capacitor	C
Place Inductor	L
Place Diode	D

Description	Shortcut
Place Net Name	N
Move Mode	M
Stretch Mode	S
Delete Mode	Del or Backspace
Duplicated Mode	Ctrl + C
Rotate	Ctrl + R
Mirror	Ctrl + E
Undo	Ctrl + Z
New Schematic	Ctrl + N
Save	Ctrl + S
SPICE Directive	.

Lect. 22: LTspice Tutorial

◆ LTspice Basics – Component Values (SI Unit)

K, k, kilo = 10^3

MEG, meg = 10^6

G, g, giga = 10^9

T, t, terra = 10^{12}

M, m, milli = 10^{-3}

U, u, micro = 10^{-6}

N, n, nano = 10^{-9}

P, p, pico = 10^{-12}

F, f, femto = 10^{-15}

Lect. 22: LTspice Tutorial

◆ LTspice Basics - NCSU 45nm CMOS Model Setup

In this semester, we will be using the NCSU 45nm CMOS Model.

The uploaded file (models_nom) contains the definitions of MOSFET's characteristics.

This is an open-source for 45nm CMOS technology node provided by North Carolina State University (NCSU).

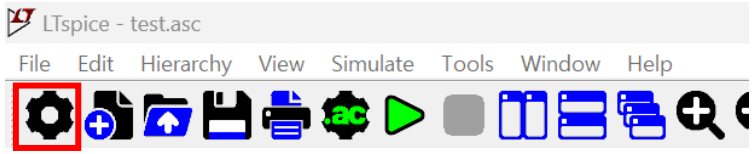
models_nom

```
* Customized PTM 45 NMOS NMOS_VTH

.model  NMOS_VTH  nmos  level = 54

* parameters related to the technology node
+tnom = 27    epsrox = 3.9
+eta0    = 0.008   nfactor = 1.6   wint = 5e-09
+cgso = 1.1e-010    cgdo = 1.1e-10

* parameters customized by the user
+toxe = 1.63e-09    toxp = 1.0e-09    toxm = 1.63e-09    toxref = 1.63e-09
+dtox = 6.3e-10    lint = 3.75e-09
+vth0 = 0.6078   k1 = 0.4   u0 = 0.05    vsat = 170000
+rdsw = 155    ndep = 3.24e+018   xj = 1.98e-08



+version = 4.0          binunit = 1          paramchk= 1          mobmod  = 0
+capmod  = 2          igcmod  = 1          igbmod  = 1          geomod  =
1
+diomod  = 1          rdsmod  = 0          rbodymod= 1          rgatemod=
1
+permod  = 1          acnqsmod= 0          trnqsmod= 0
```

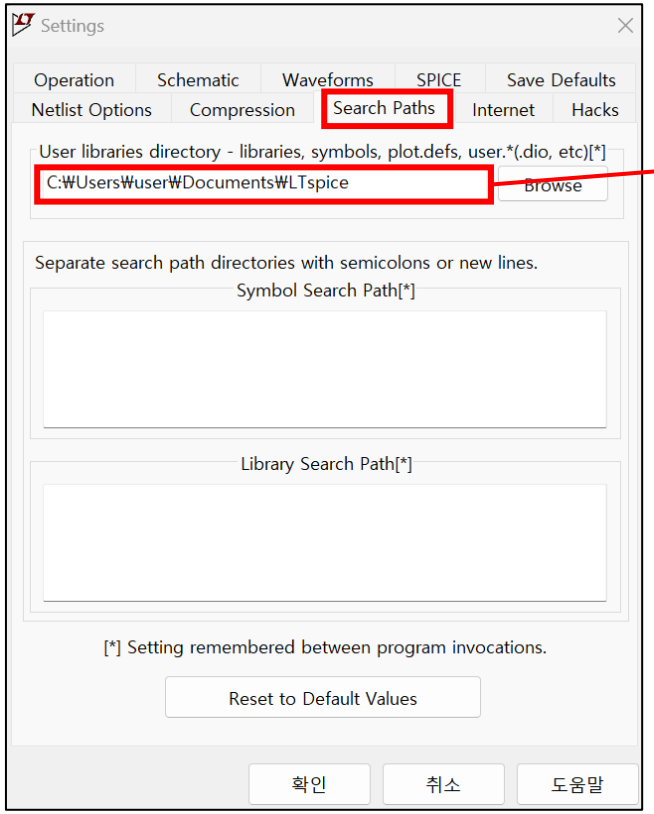
NMOS_VTL.inc

Lect. 22: LTspice Tutorial

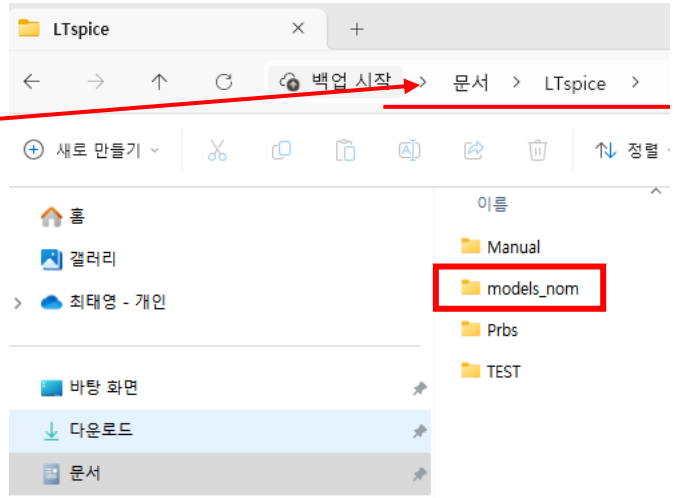
◆ LTspice Basics - NCSU 45nm CMOS Model Setup



1) To apply the PDK, click the **Settings**



2) **Search Paths → User libraries directory**
Check the existing library path



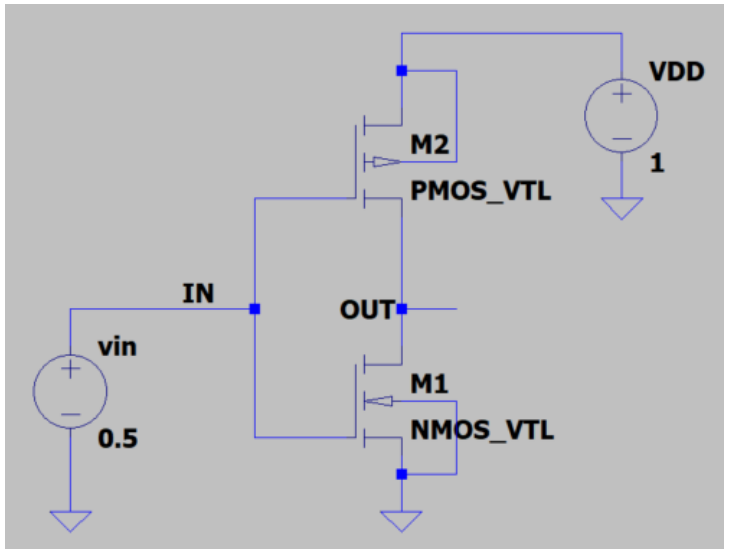
3) **Add 'models_nom'** folder to the library path

Finish !

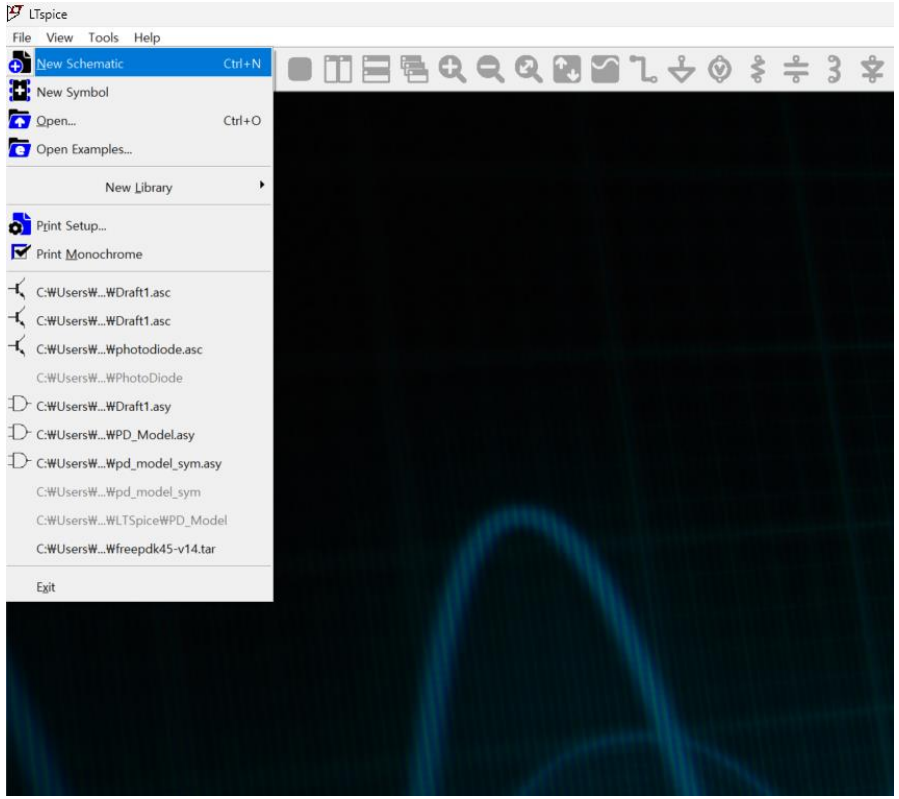
Inverter Design Example

Lect. 22: LTspice Tutorial

◆ **Inverter Design Using a NCSU 45nm CMOS Model**



Inverter Schematic

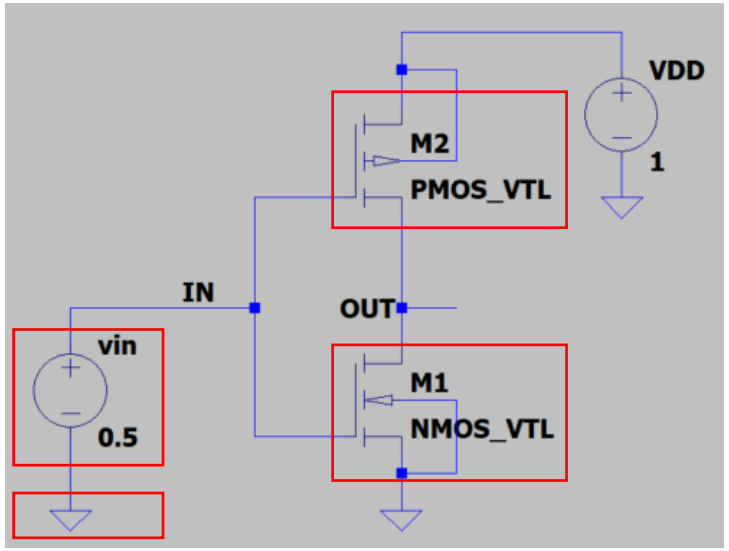


1) File → New Schematic (Ctrl + N)

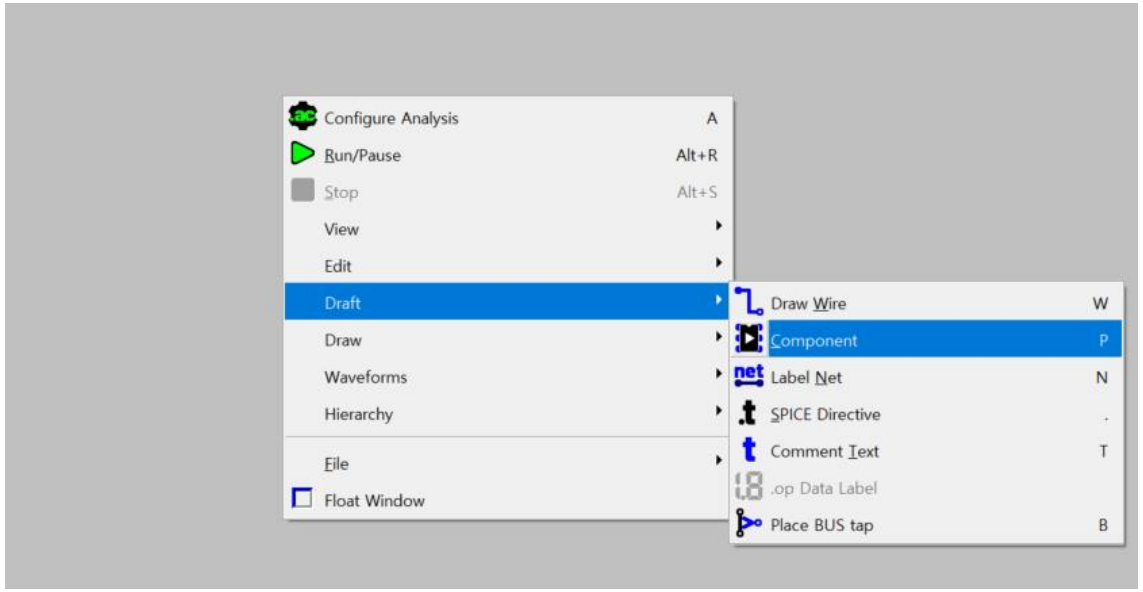
Lect. 22: LTspice Tutorial

◆ Inverter Design Using a NCSU 45nm CMOS Model

We want to place components such as **voltage sources**, **MOSFETs** and **GND**.



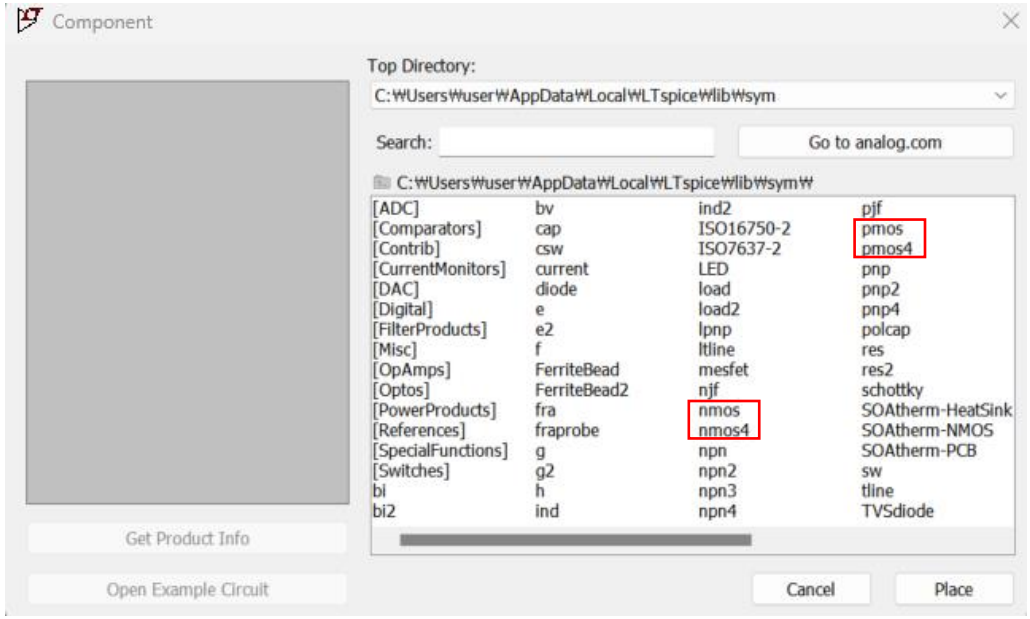
Inverter Schematic

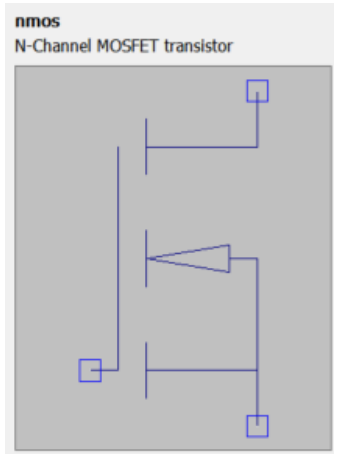


2) **Right-Click** on background→ **Draft** → **Component (P)**

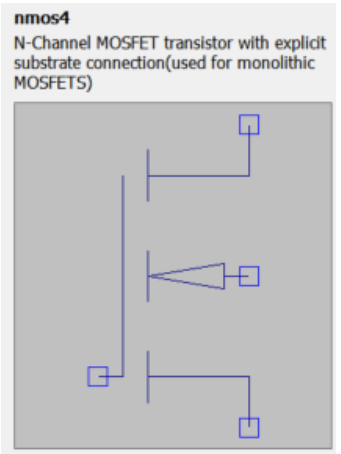
Lect. 22: LTspice Tutorial

◆ Inverter Design Using a NCSU 45nm CMOS Model

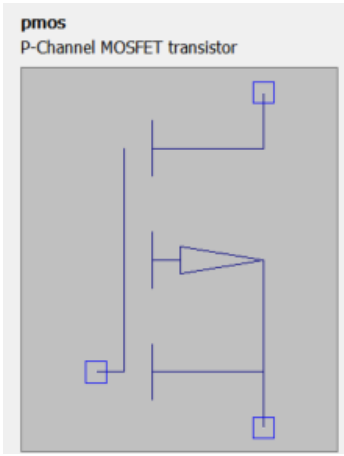




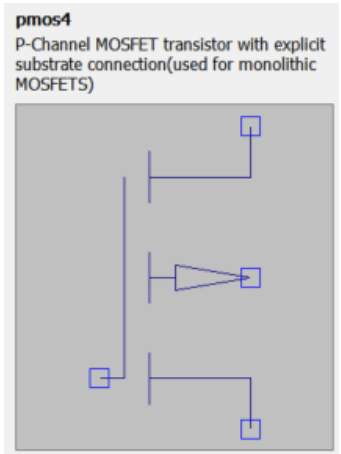
nmos



✓ nmos4



pmos

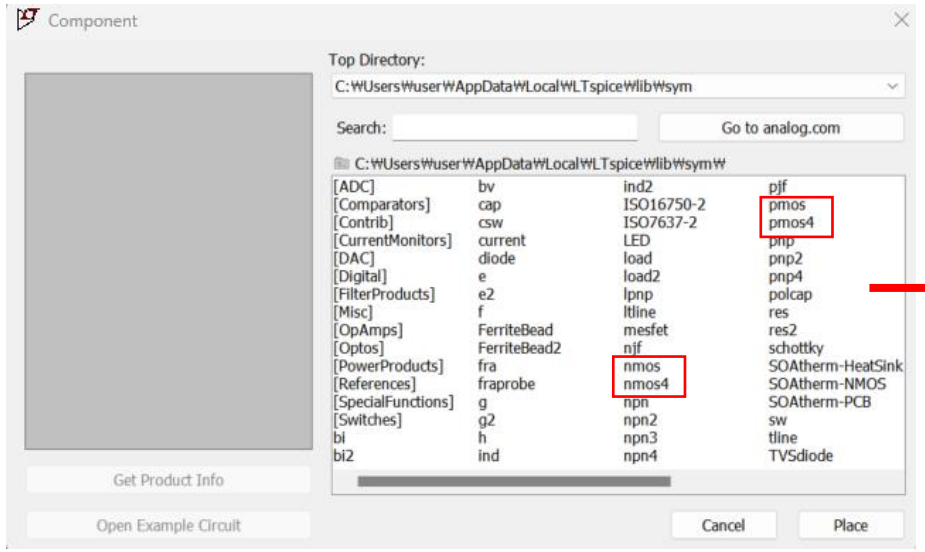


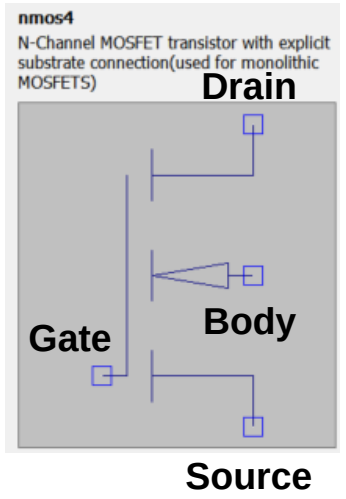
✓ pmos4

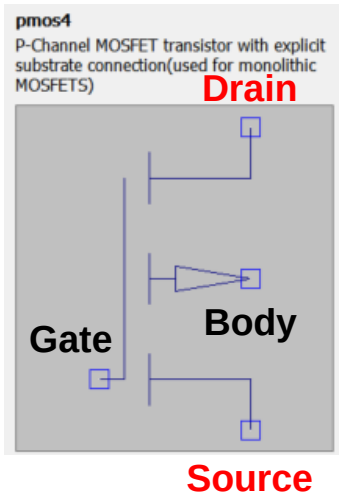
3) There are a total of 4 MOSFETs. We will be using **nmos4** and **pmos4** among them.

Lect. 22: LTspice Tutorial

◆ **Inverter Design Using a NCSU 45nm CMOS Model**







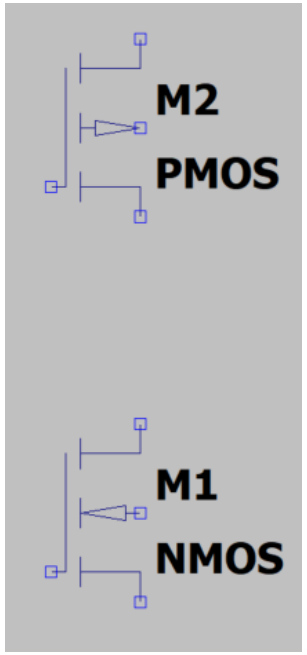
In the case of PMOS, typically, a symbol with **the drain terminal at the bottom** is used.

However, in LTspice, the symbol has the Drain terminal at the top.

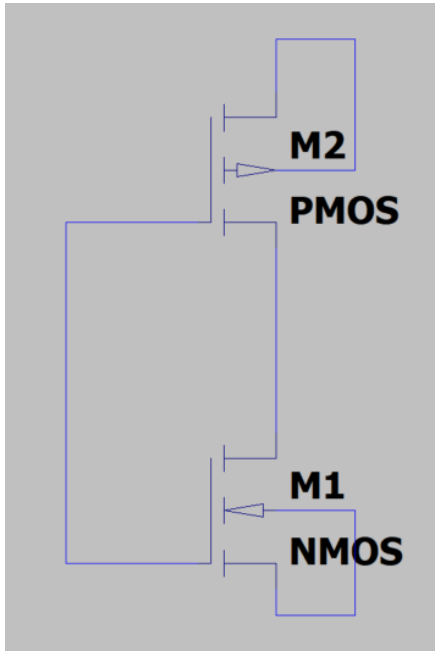
Nevertheless, since the drain and source of a MOSFET are symmetrical components, there is no functional issue. It's just important to be aware that the names of the source and drain may appear swapped in the simulation results.

Lect. 22: LTspice Tutorial

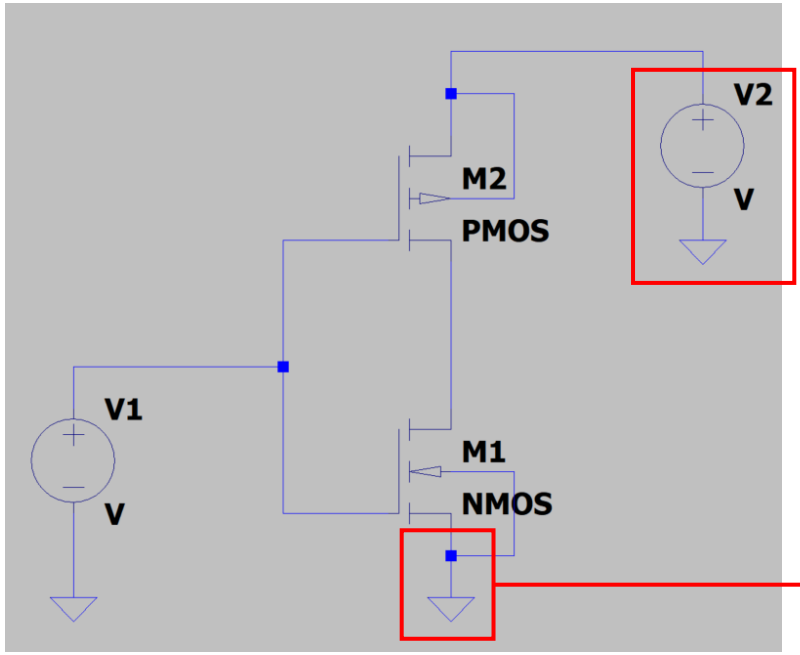
◆ **Inverter Design Using a NCSU 45nm CMOS Model**



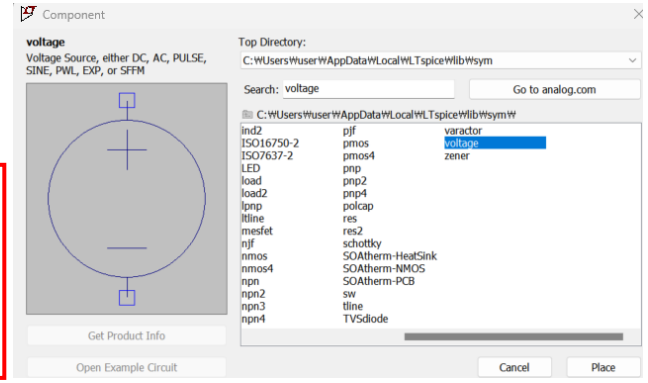
4) Place NMOS and PMOS



5) Draw Wires (W)



Ground (G)



voltage in Component (P)

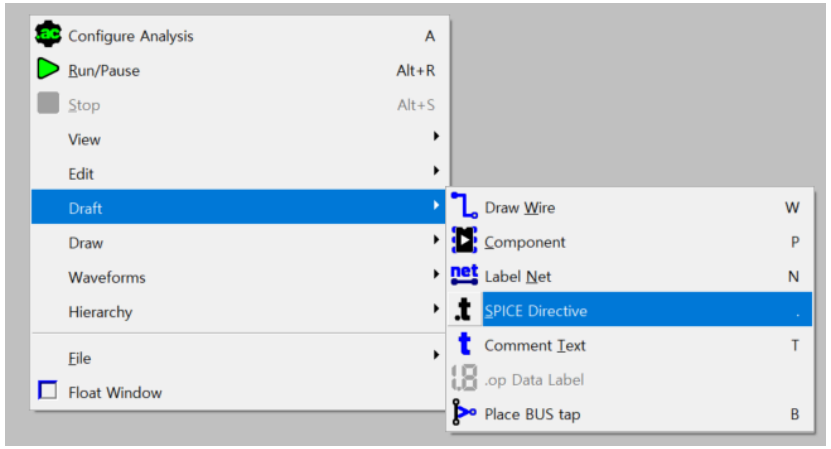
6) Place voltage source and Ground

NMOS body connected to Ground

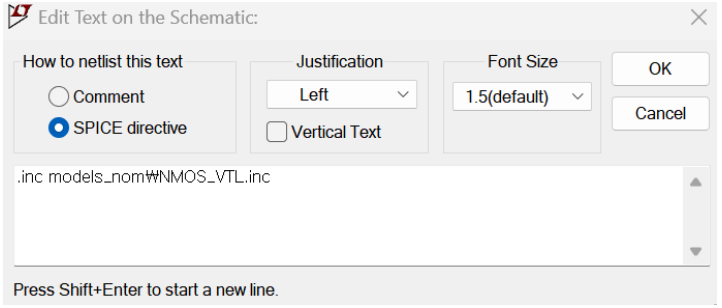
PMOS body connected to VDD

Lect. 22: LTspice Tutorial

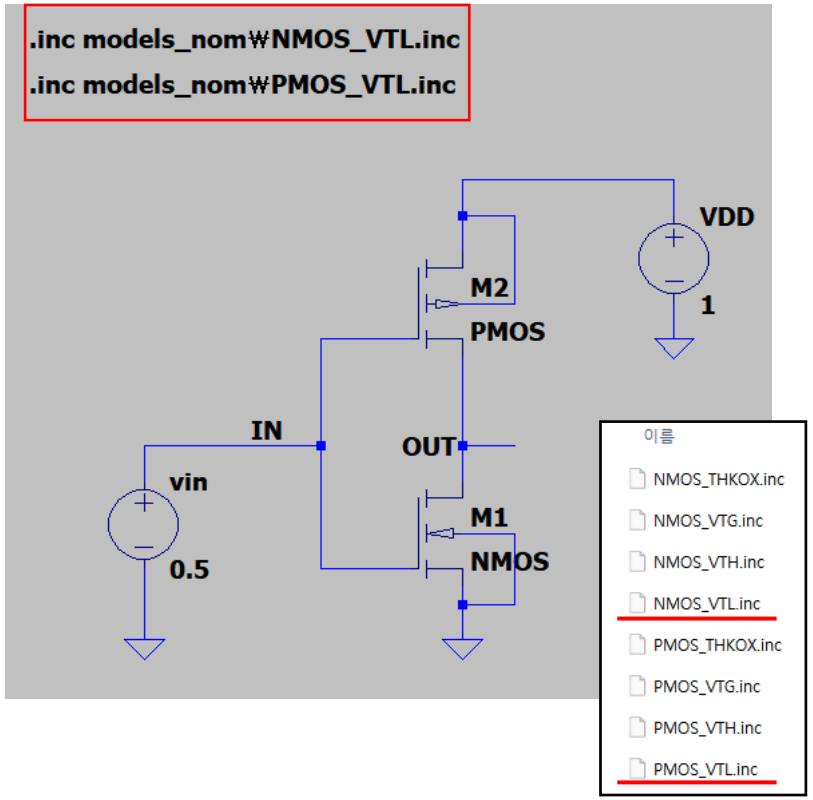
◆ Inverter Design Using a NCSU 45nm CMOS Model



7) Right-Click and **Draft → SPICE Directive (.)**

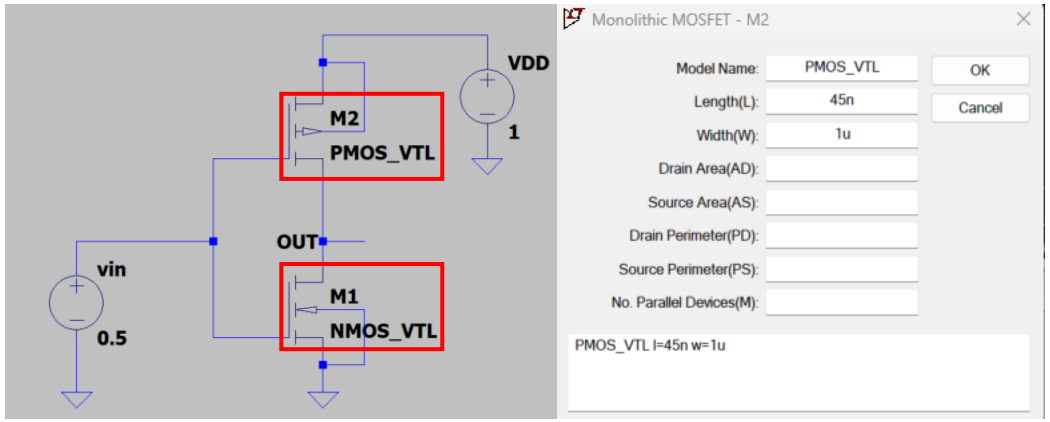


8) .inc + path of **model parameter file**



Lect. 22: LTspice Tutorial

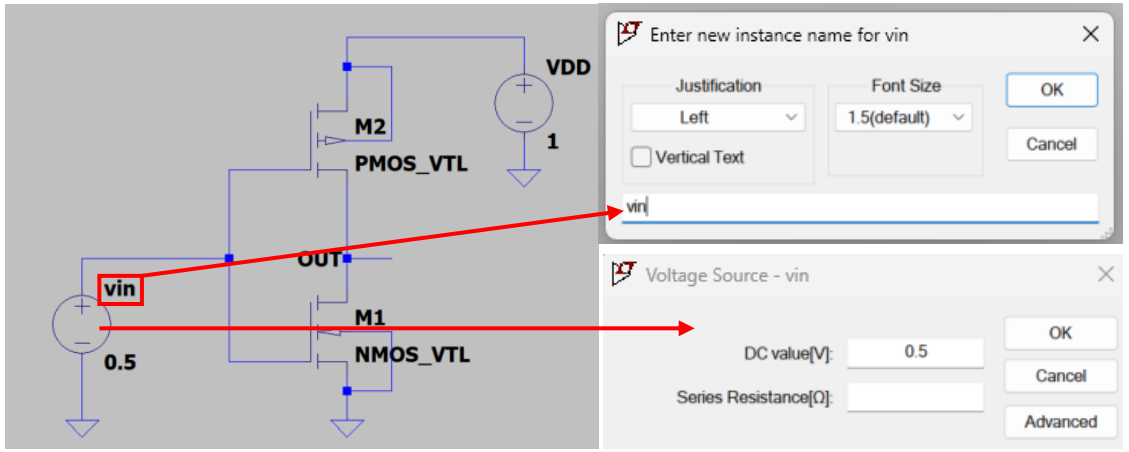
◆ Inverter Design Using a NCSU 45nm CMOS Model



9) Right-Click on **MOSFET instance (symbol)**

and **change the model name to PMOS_VTL and NMOS_VTL**

Set the length (≥ 45nm) and width values to what you desire



10) Right-Click on **voltage source name**

and change the instance name to vin

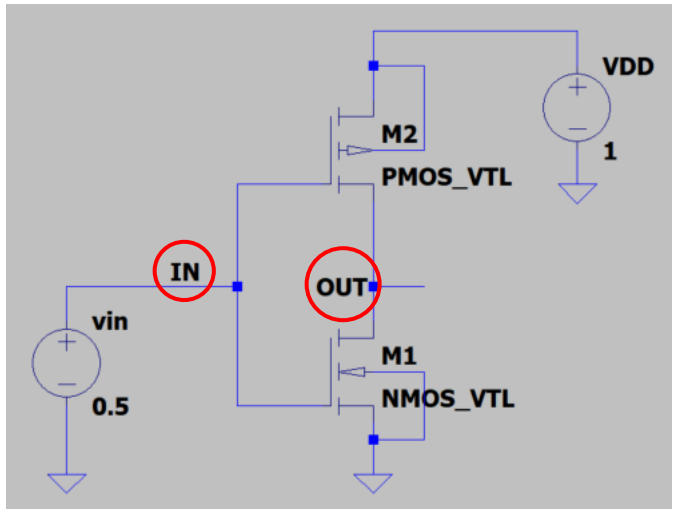
Right-Click on **voltage source instance (symbol)**

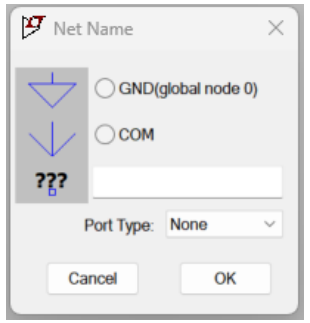
and change the DC value

* nominal voltage of this PDK is 1V, so VDD ⇒ 1V

Lect. 22: LTspice Tutorial

◆ **Inverter Design Using a NCSU 45nm CMOS Model**





Label Net (N)

11) Label Net (N) → **labeling IN** and **OUT**

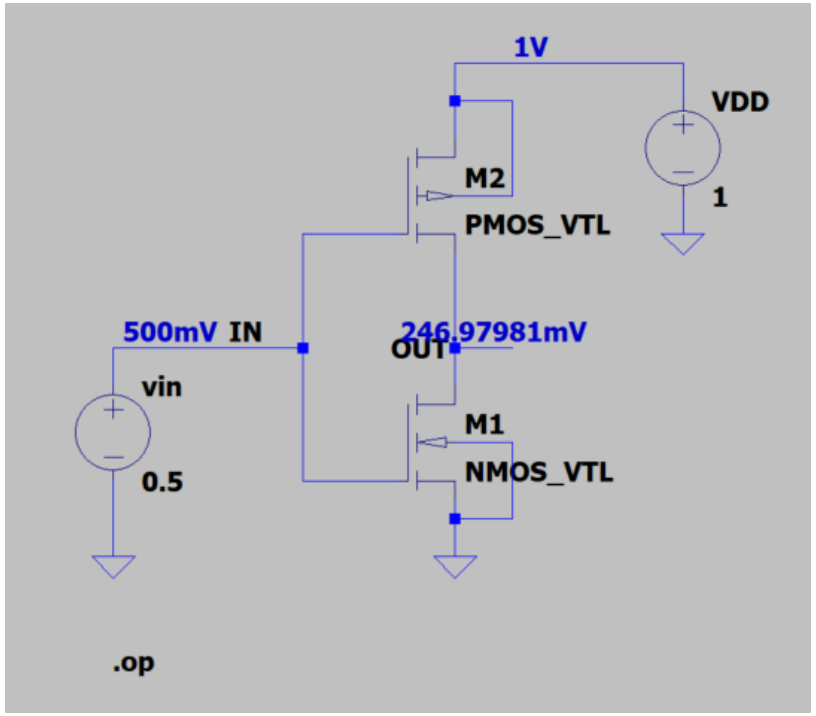
Simulation

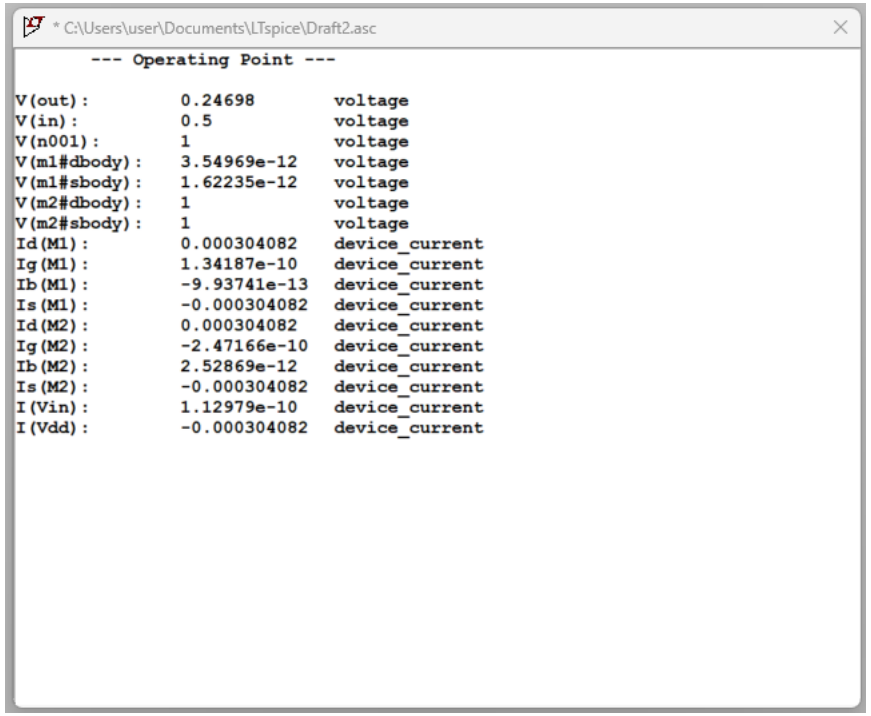
Lect. 22: LTspice Tutorial

◆ 1. DC Operating Point Simulation

DC operating point simulation is used for checking **each node's Voltage**, **Current.**

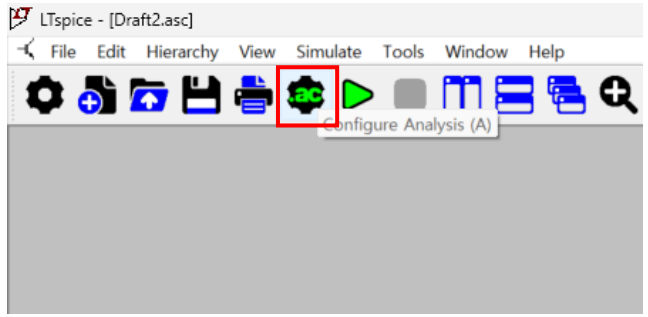
Capacitors are treated as open circuits, while inductors are treated as short circuits.



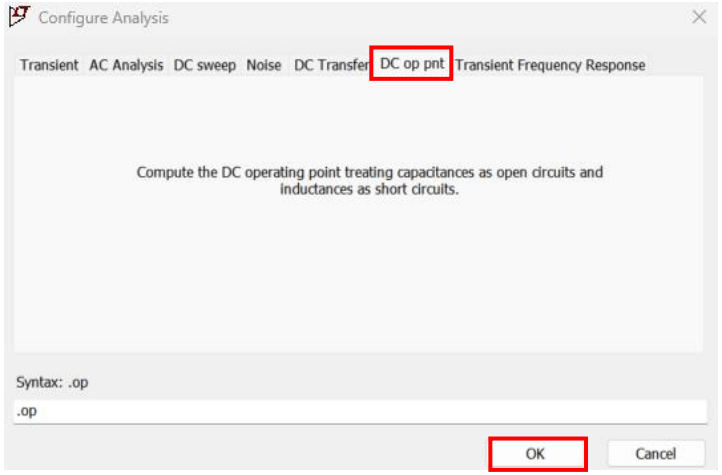


Lect. 22: LTspice Tutorial

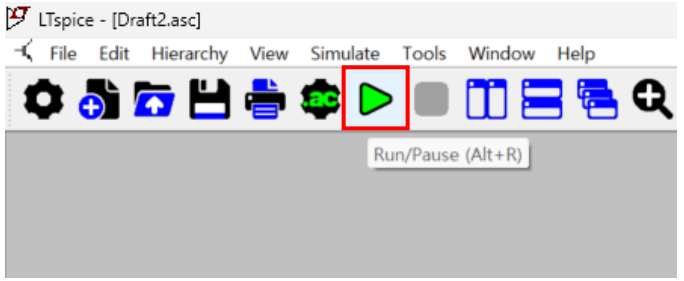
◆ 1. DC Operating Point Simulation



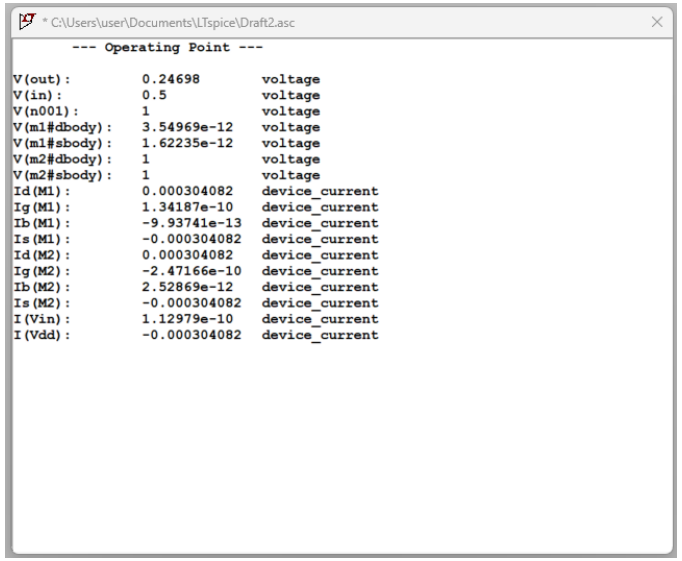
1) Click the **Configure Analysis (A)**



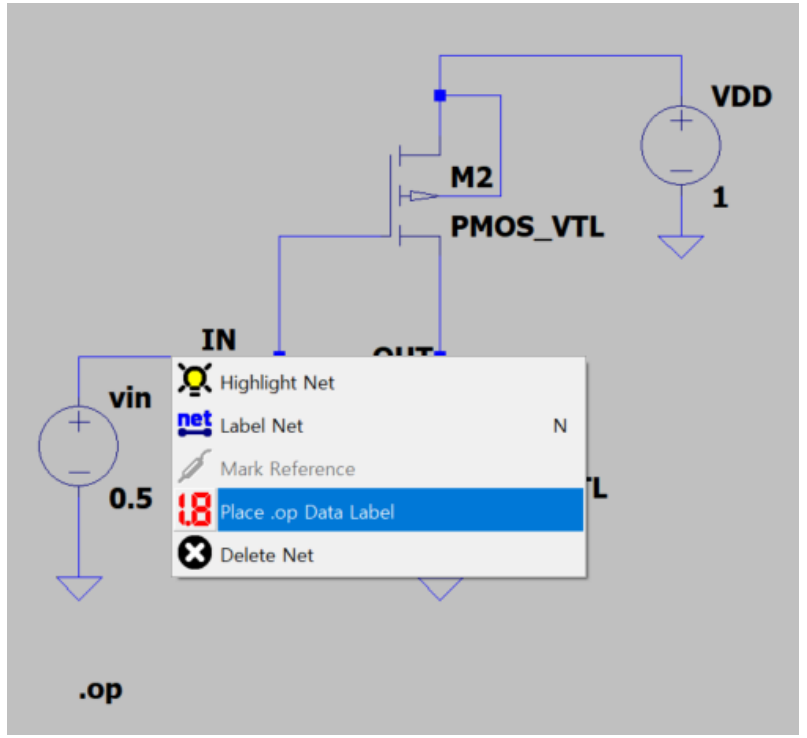
2) **DC op pnt → OK**



3) Click the **Run/Pause (Alt + R)**



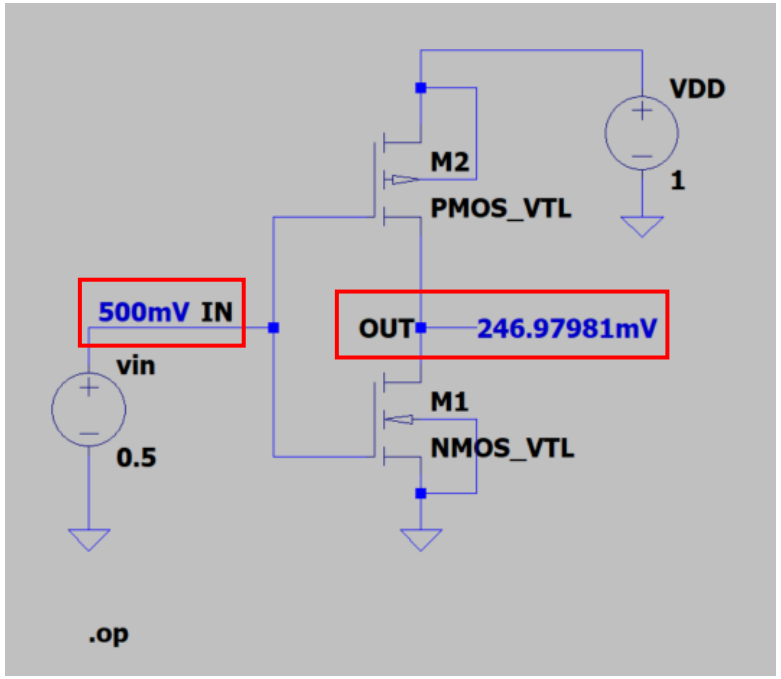
4) Get the results window

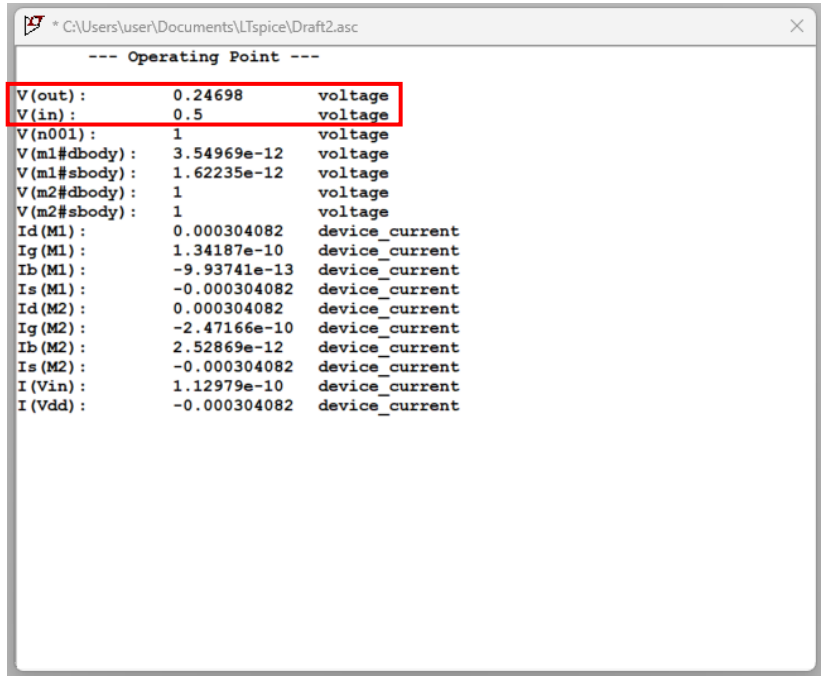


5) **Right-click on the node** you want to check and click **.op Data Label**

Lect. 22: LTspice Tutorial

◆ 1. DC Operating Point Simulation





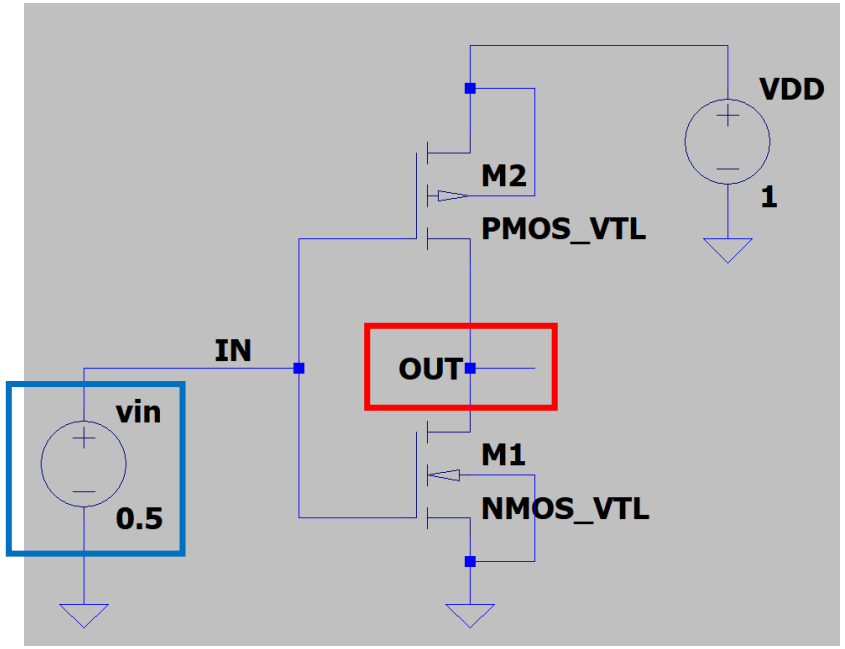
6) After running the simulation, you can check the results in two ways.

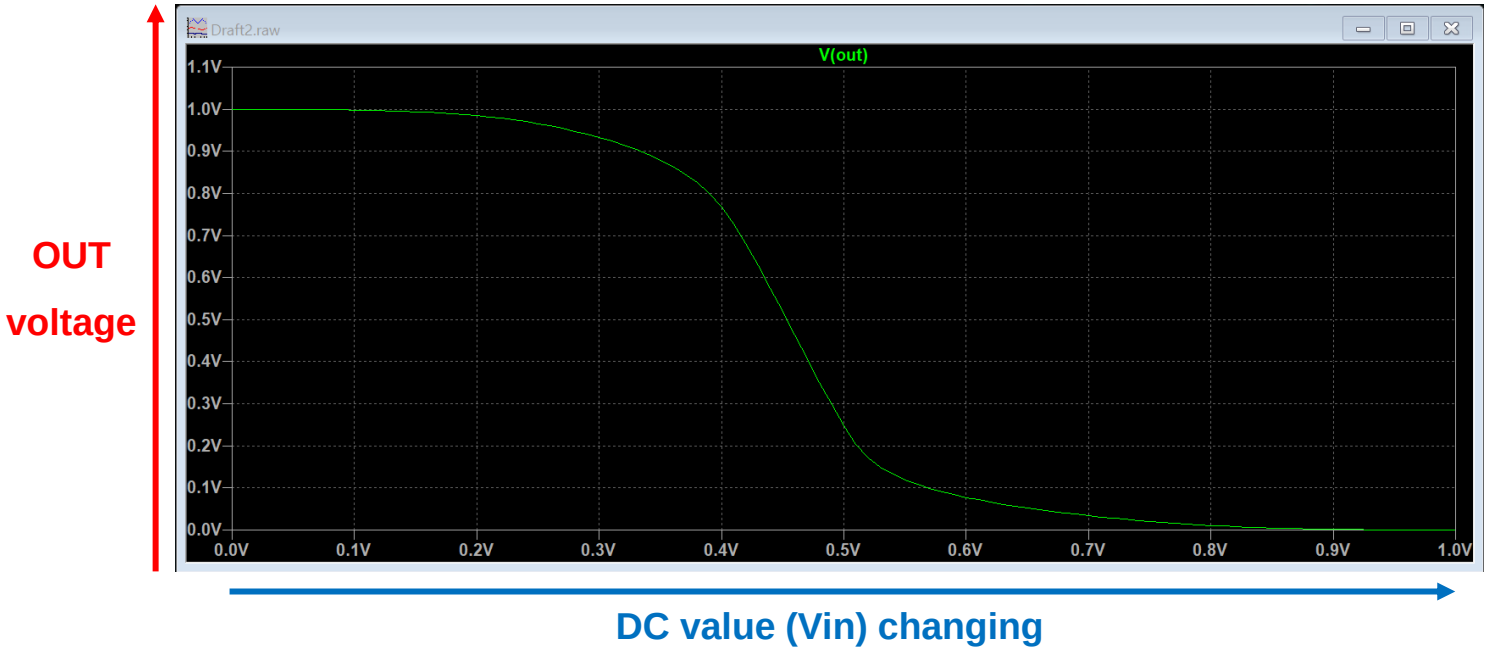
1. Directly probe nodes.
2. Check the data in the results window.

Lect. 22: LTspice Tutorial

◆ 2. DC sweep simulation

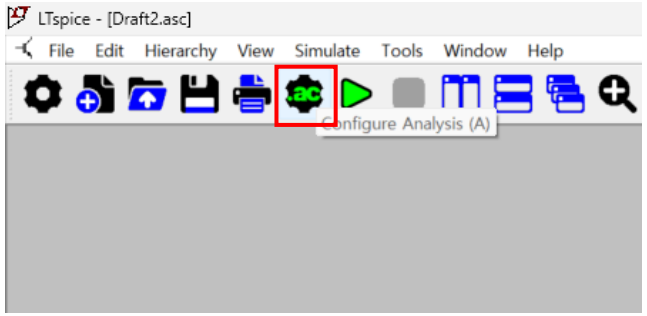
DC sweep simulation is used for seeing specific point's **voltage or current variation** when **changing DC value**



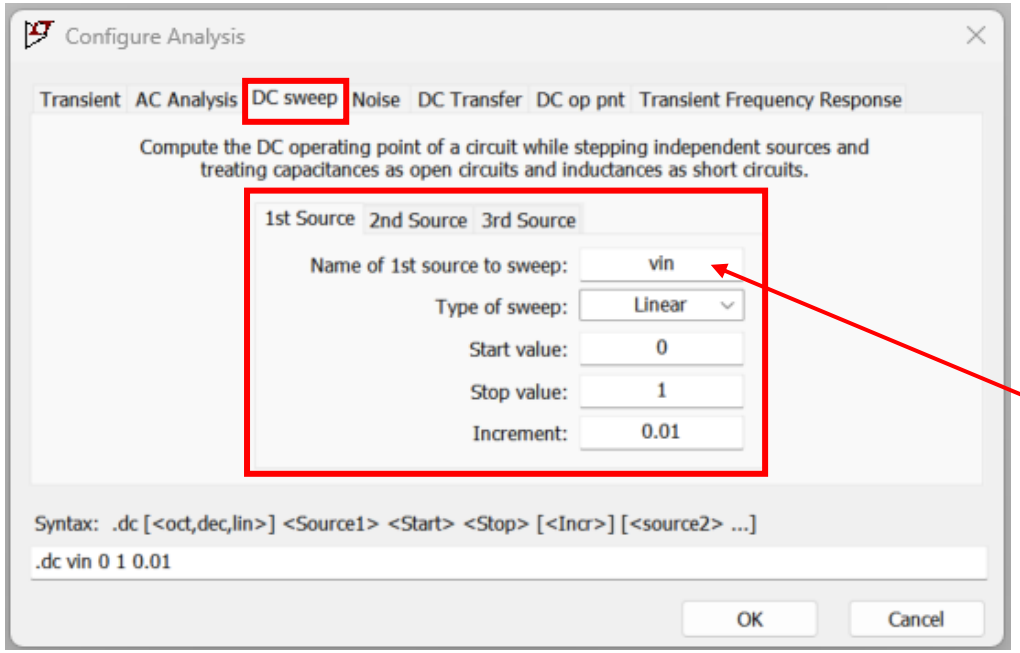


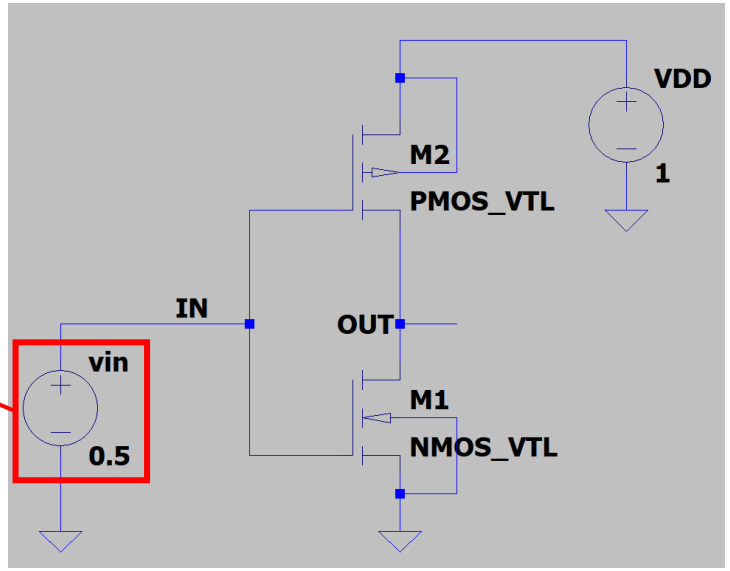
Lect. 22: LTspice Tutorial

◆ 2. DC sweep simulation



1) Click the **Configure Analysis (A)**

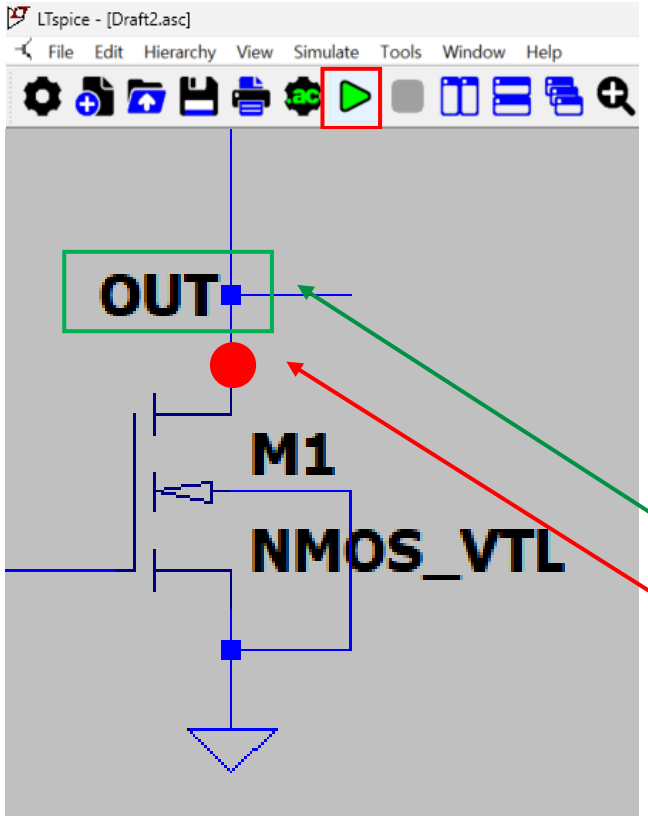




2) DC sweep → set up the simulation environment

Lect. 22: LTspice Tutorial

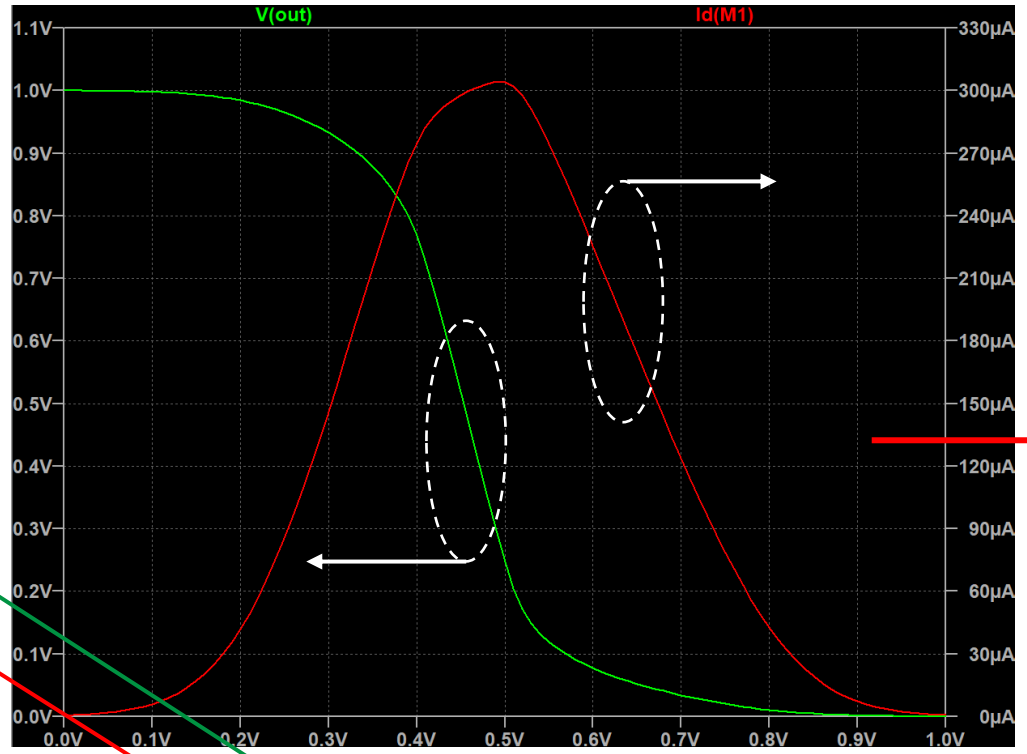
◆ 2. DC sweep simulation



3) Click the **Run/Pause (Alt + R)**

OUT node voltage

Drain current of M1



Grid option

⇒ **Ctrl + G**

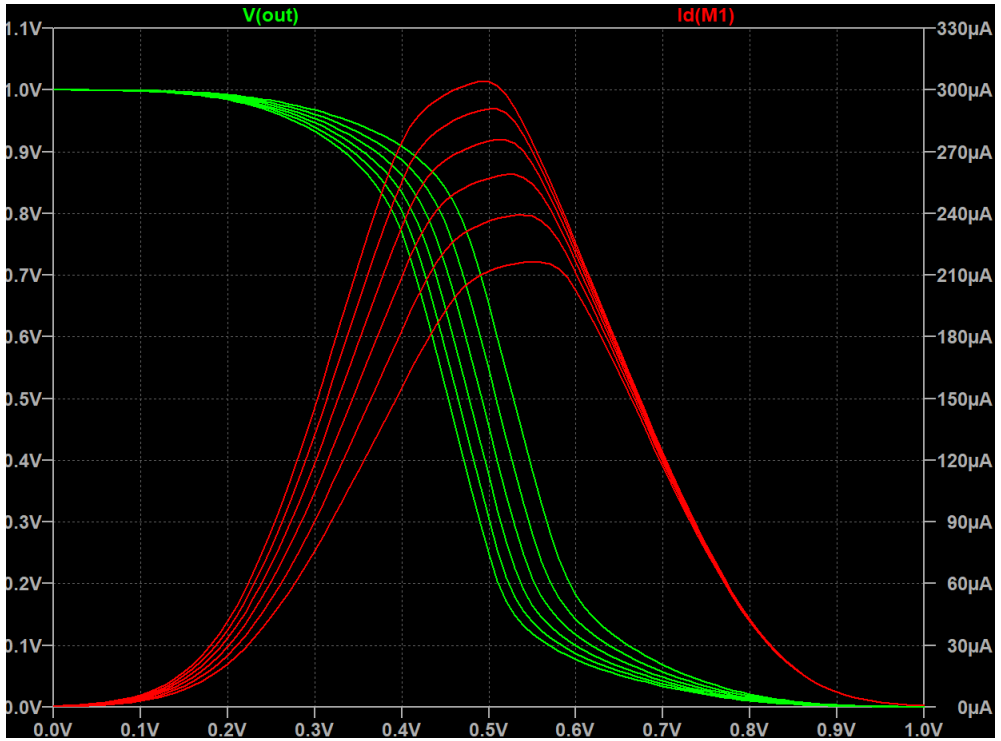
4) If you want to see **voltage, click on the node** in schematic

If you want to see **current**, **click on the terminal of instance** in schematic

Lect. 22: LTspice Tutorial

◆ 3. Parametric Simulation

Parametric Simulation is an option with which you can view simulation results for varying values of specific parameter.



Parametric Simulation can be used for not only **DC sweep** but also **AC sweep** and **Transient simulation**.

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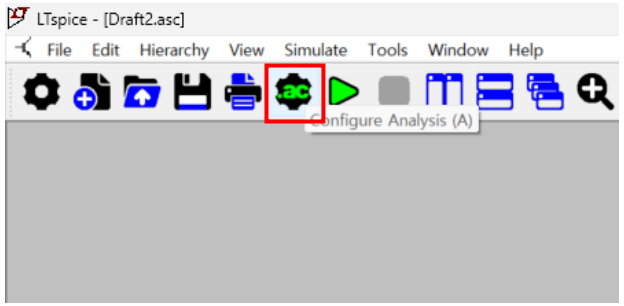
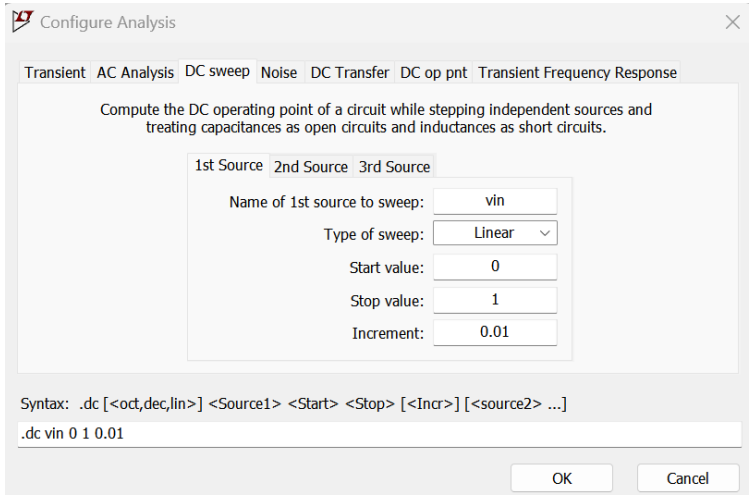
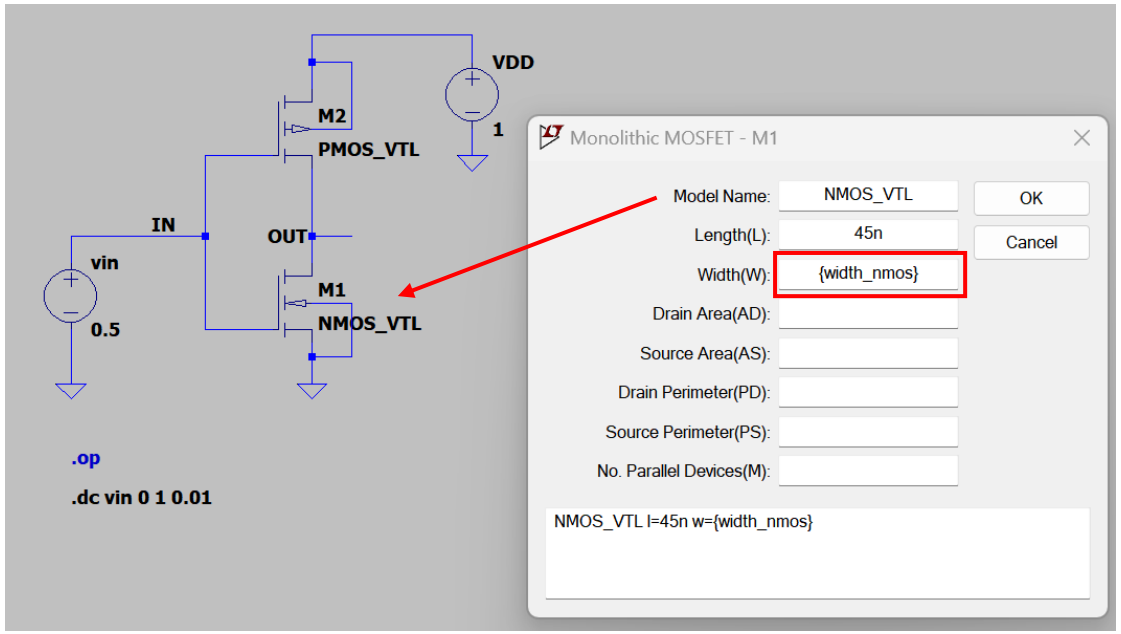
◆ 3. Parametric Simulation



1) Click the **Configure Analysis (A)**



2) **Choose simulation type** you want to view



3) **Assign a parameter name** to the desired value for the sweep (in this example, the width of the NMOS)

format : **{parameter name}**

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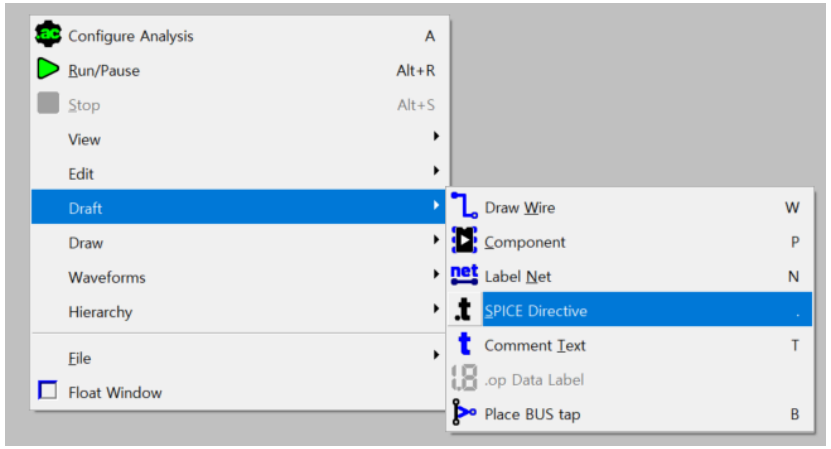
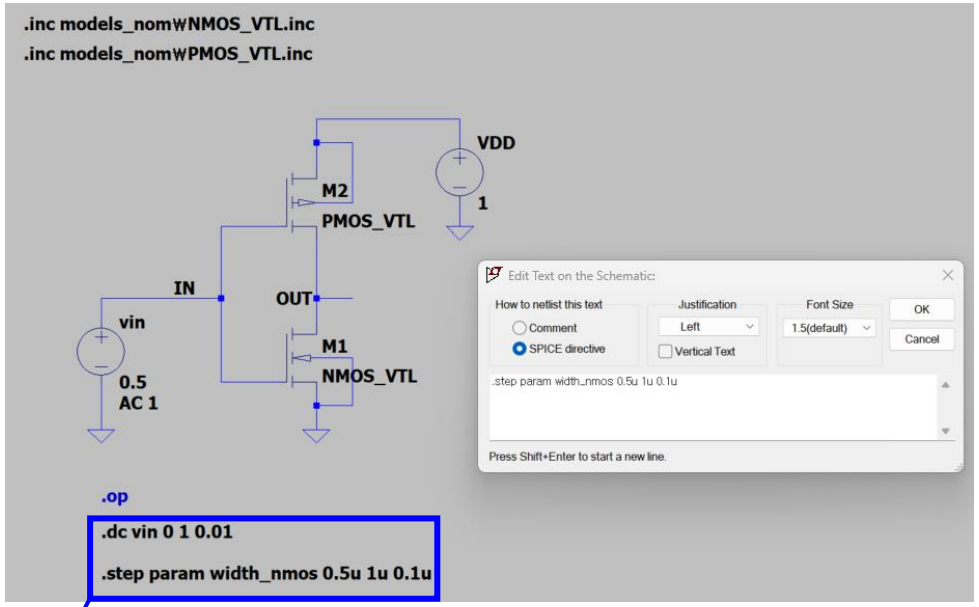
◆ 3. Parametric Simulation





4) **Enter the command** using **directives functions**.

SPICE Directive (.)

5) Enter **.step param width_nmos 0.5u 1u 0.1u**

<parameter name> <start value> <stop value> <increment>

The simulation option displayed in black text will be run.

If you want to change the simulation, **right click on text** and click OK.

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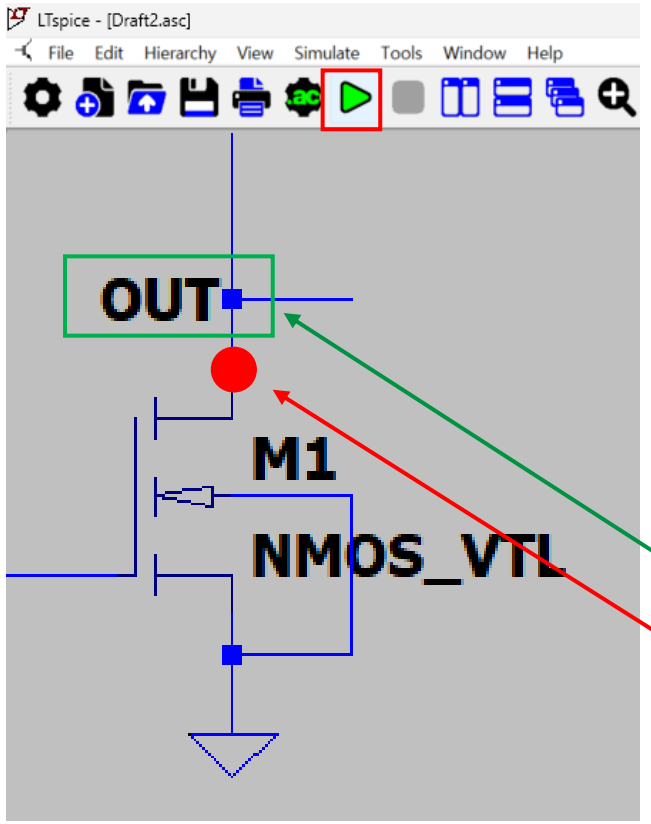
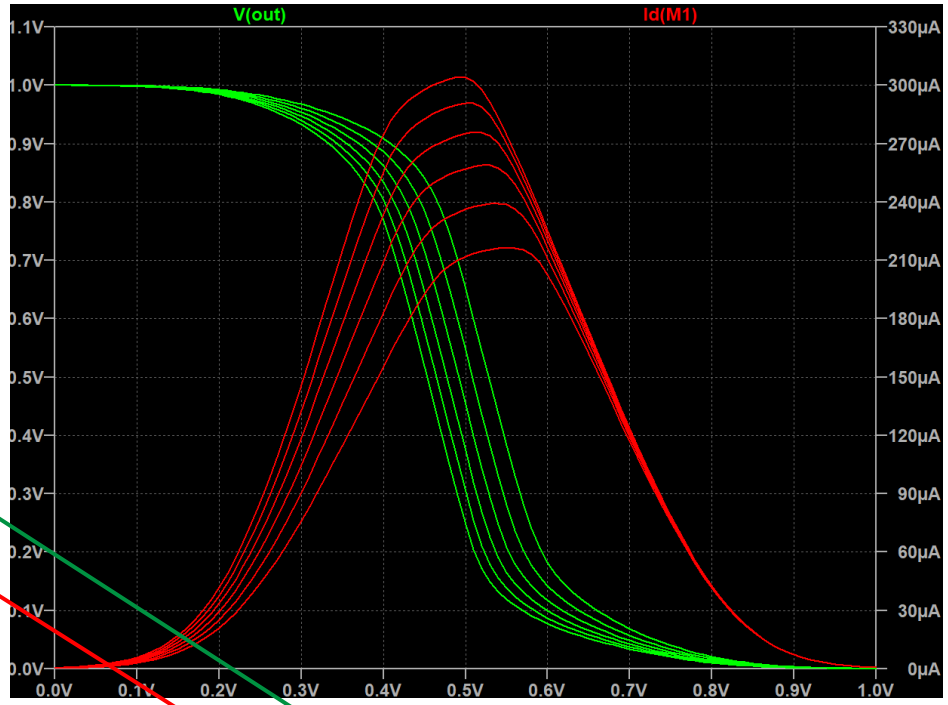
◆ 3. Parametric Simulation



6) Click the **Run/Pause (Alt + R)**



7) If you want to see **voltage, click on the node** in schematic

If you want to see **current, click on the terminal of instance** in schematic

The simulation results correspond to six values for nmos_width ranging from 0.5u to 1u in increments of 0.1u

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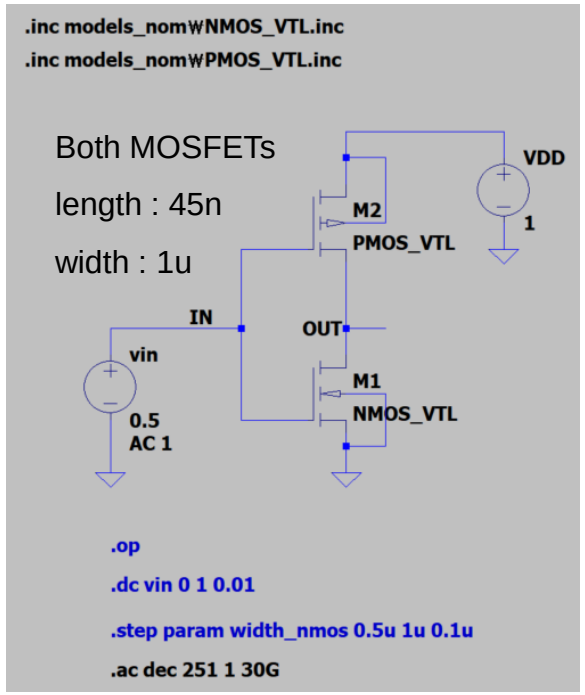
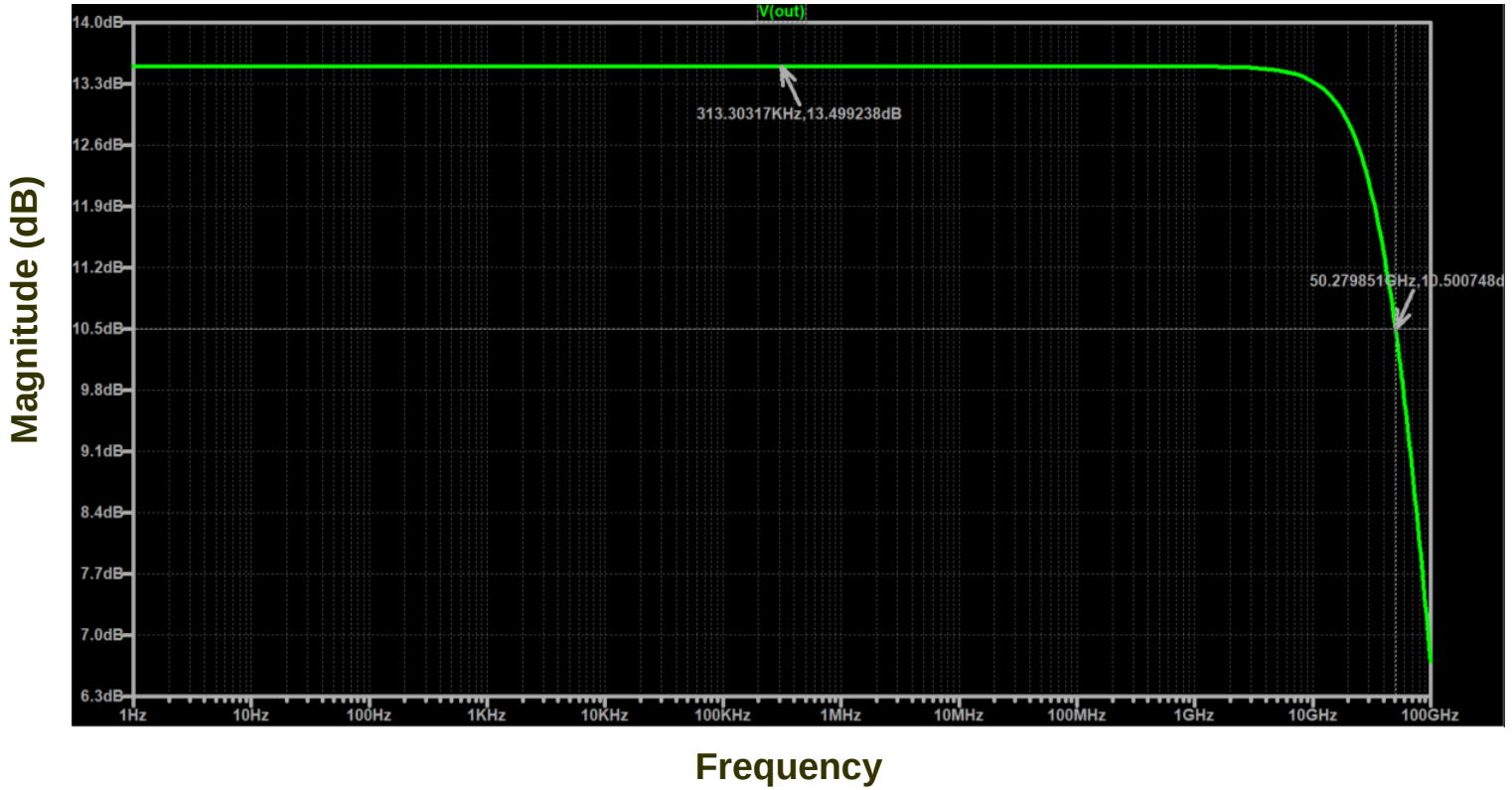
◆ 4. AC Simulation

AC sweep is used for seeing **frequency response** at a specific node.

(Do Not confuse it; it is not used for time-domain simulation)





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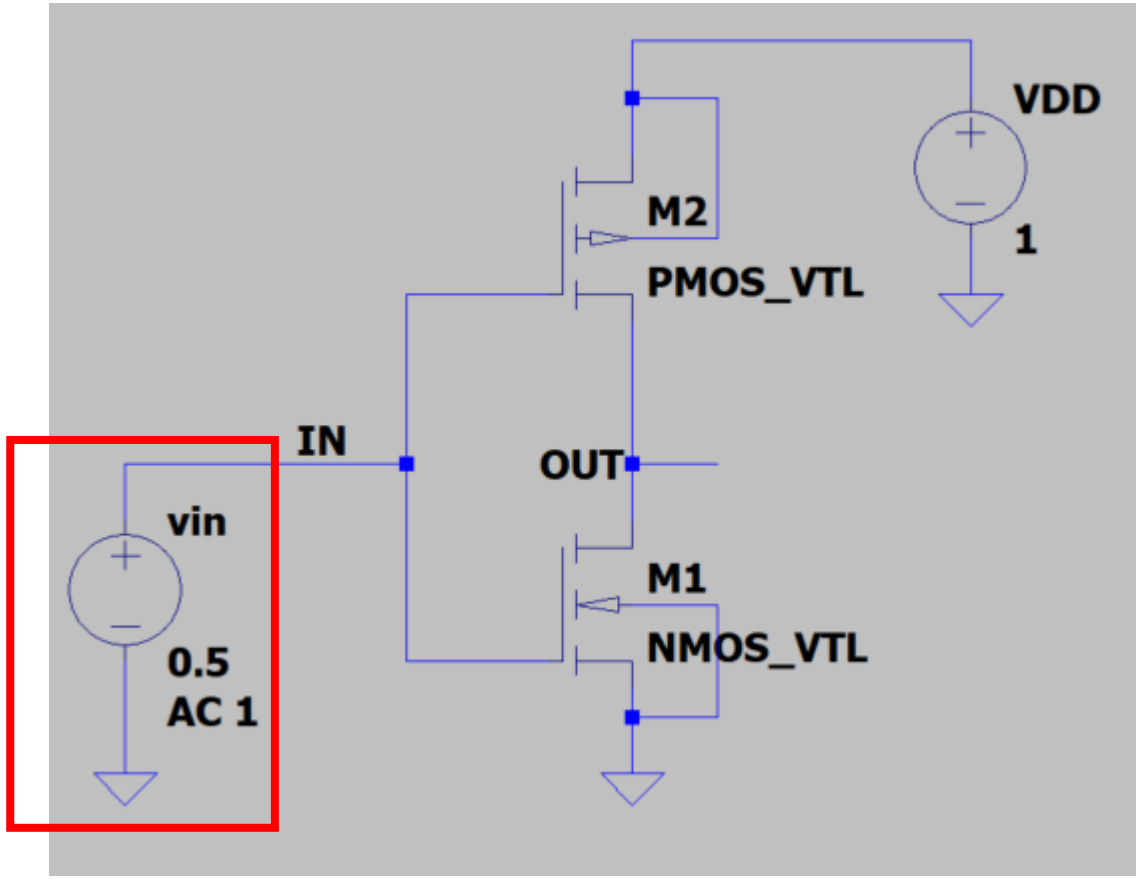
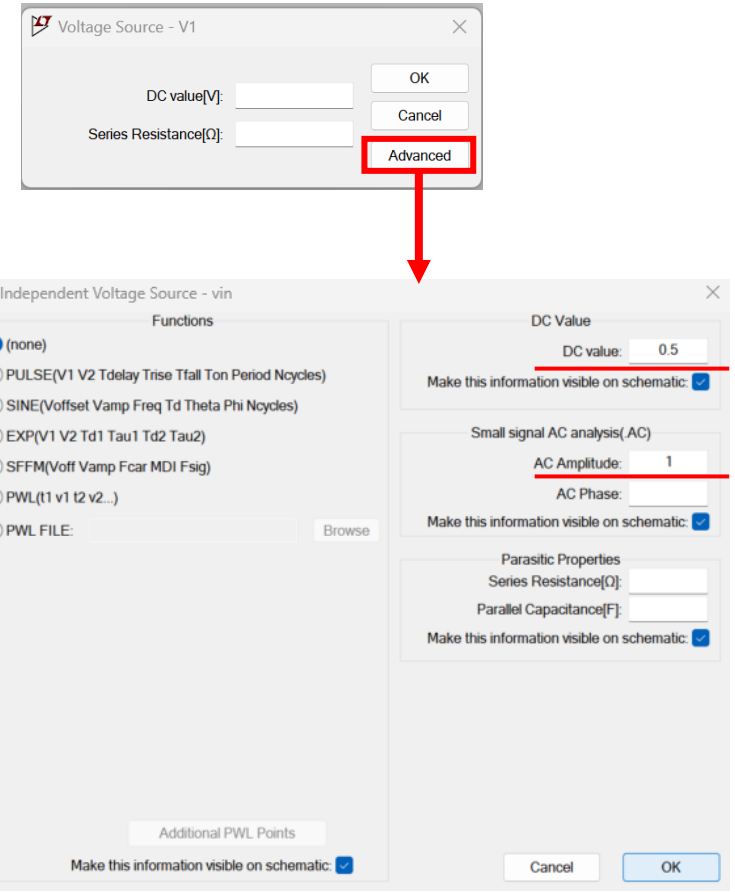
◆ 4. AC Simulation



1) Right click on voltage source



2) DC Value is what you desire.

Make sure that **Magnitude of AC Amplitude** is set to 1

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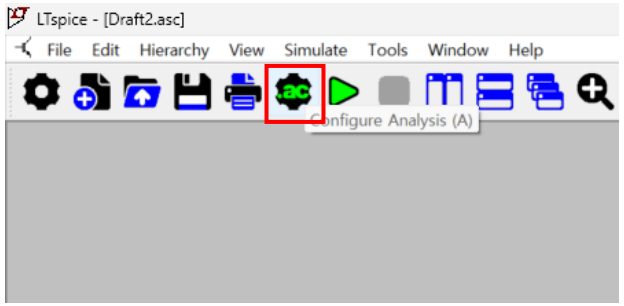
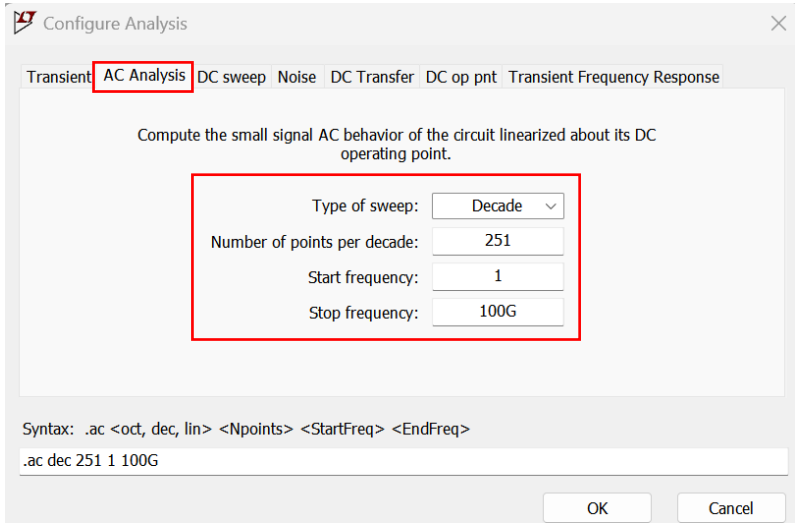
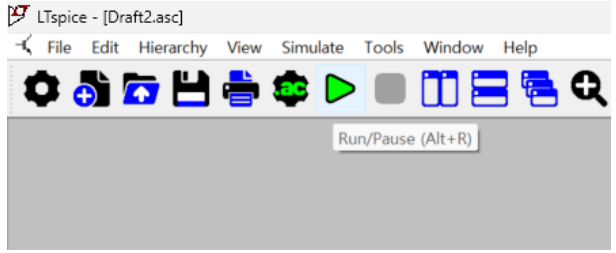
◆ 4. AC Simulation



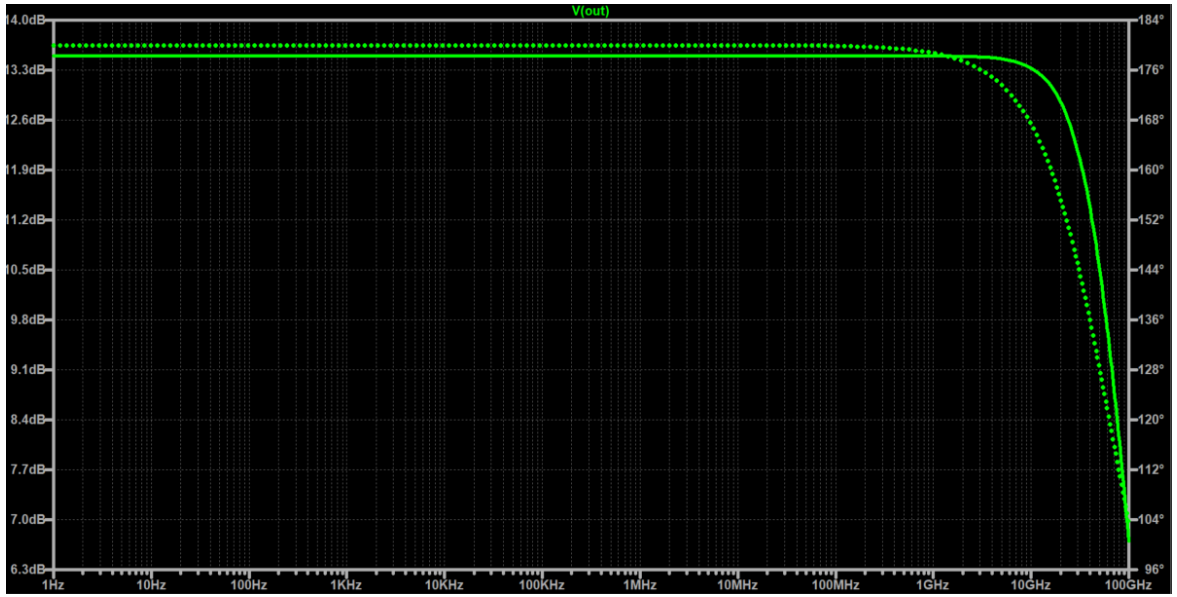
3) Click the **Configure Analysis (A)**



4) **Select AC Analysis** and **Configure the simulation settings.**



5) Click the **Run/Pause (Alt + R)**



6) If you want to see **voltage, click on the node(OUT)** in schematic

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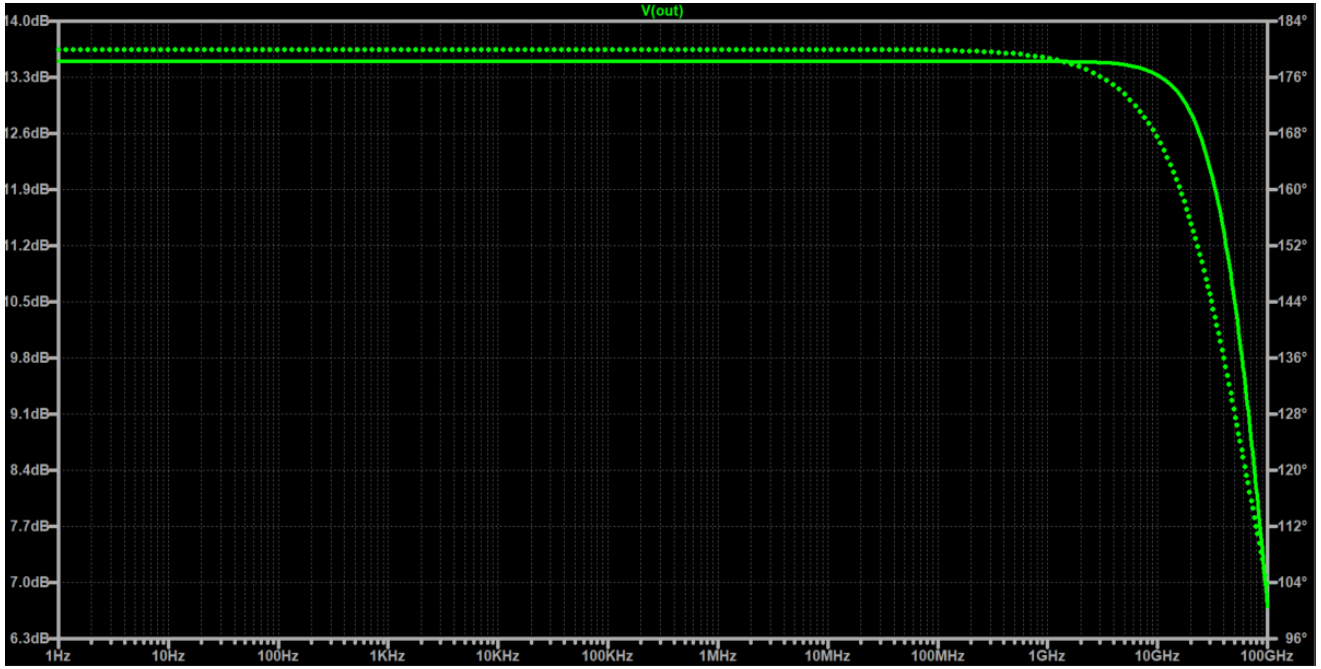
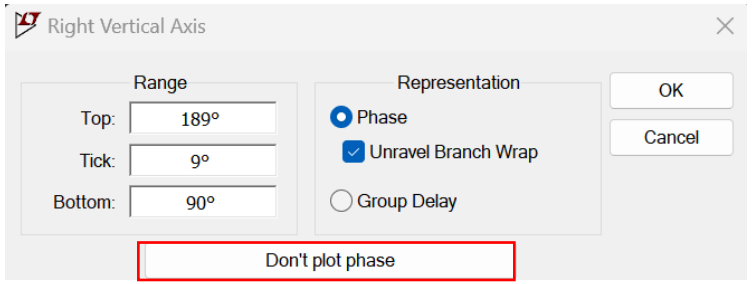
◆ 4. AC Simulation

Magnitude



Phase



7) This moment**,** I just want to see **Magnitude**

so right click on the right axis and click the **'Don't plot phase' button.**

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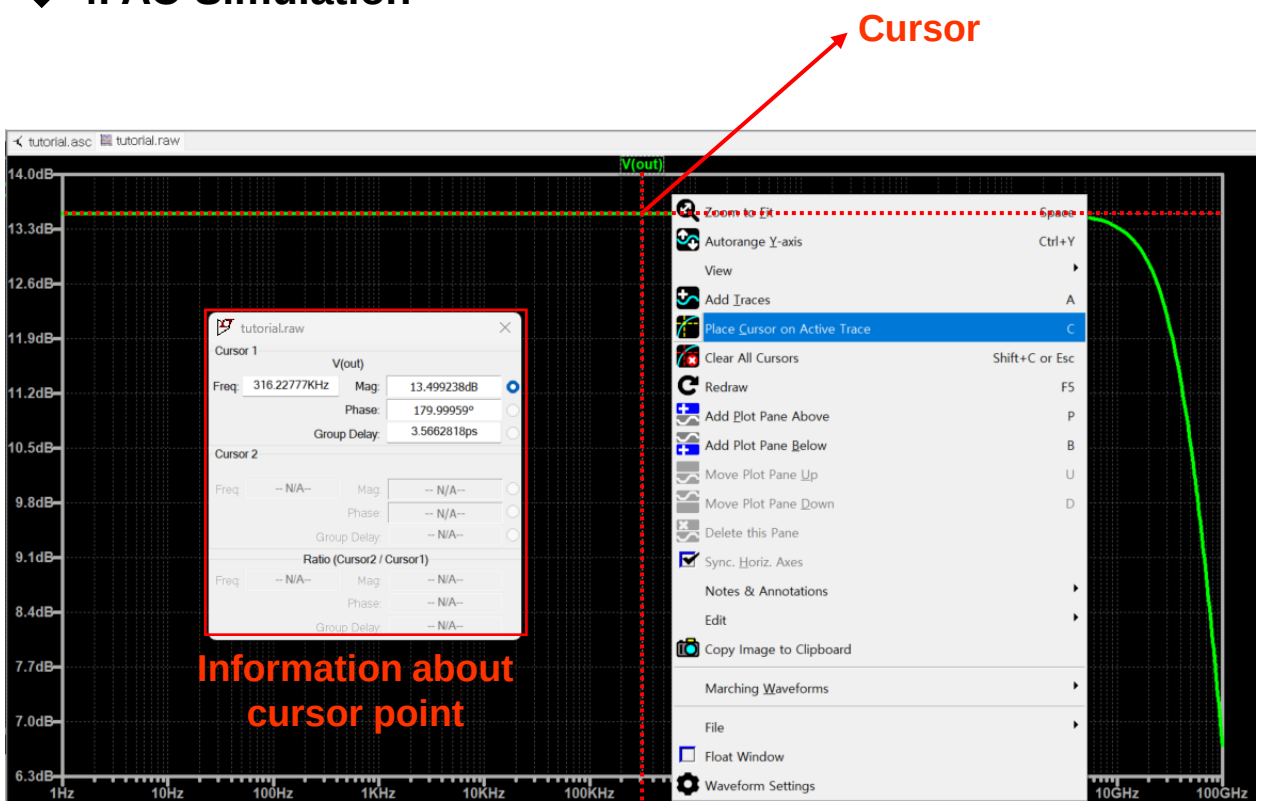
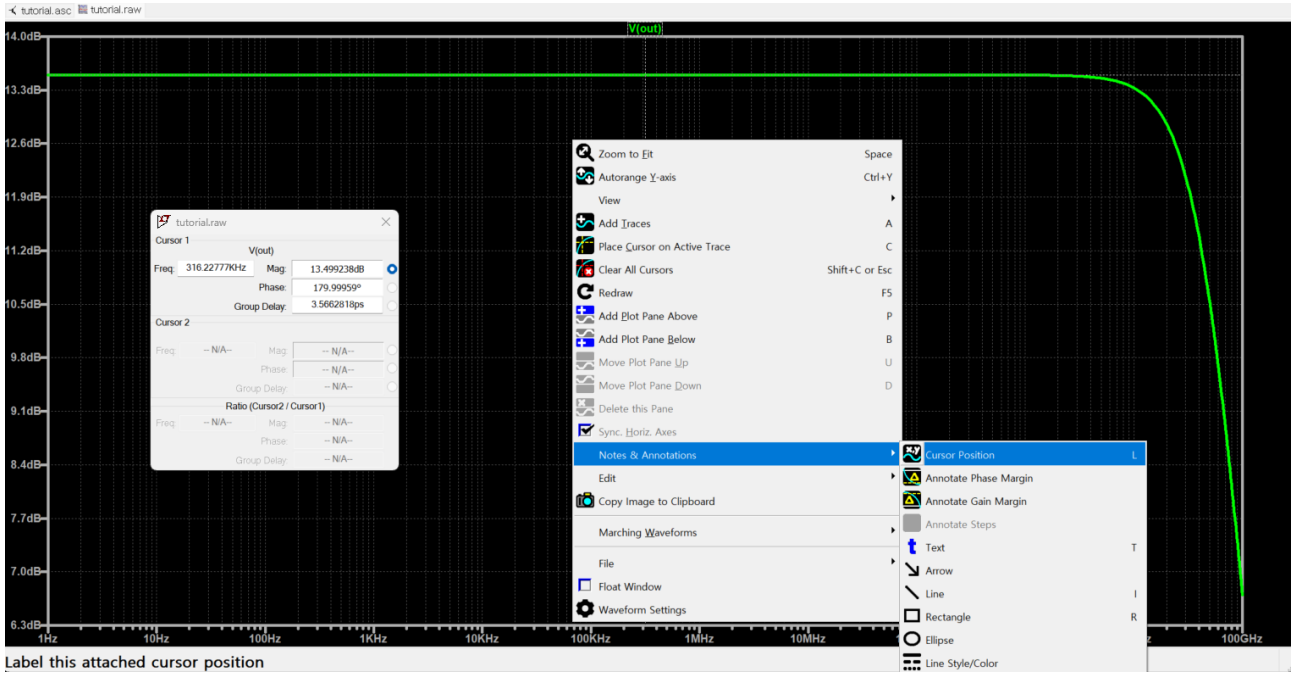
◆ 4. AC Simulation





8) I want to check **Gain and 3dB Bandwidth.**

right click on background and **'Place Cursor on Active Trace' or C**

9) To add the Cursor Position, right click on background and

'Note & Annotations → Cursor Position' or L

Lect. 22: LTspice Tutorial

◆ 4. AC Simulation

For this example : **AC Gain (V/V) = 13.5dB**

3dB Bandwidth = 50.3GHz

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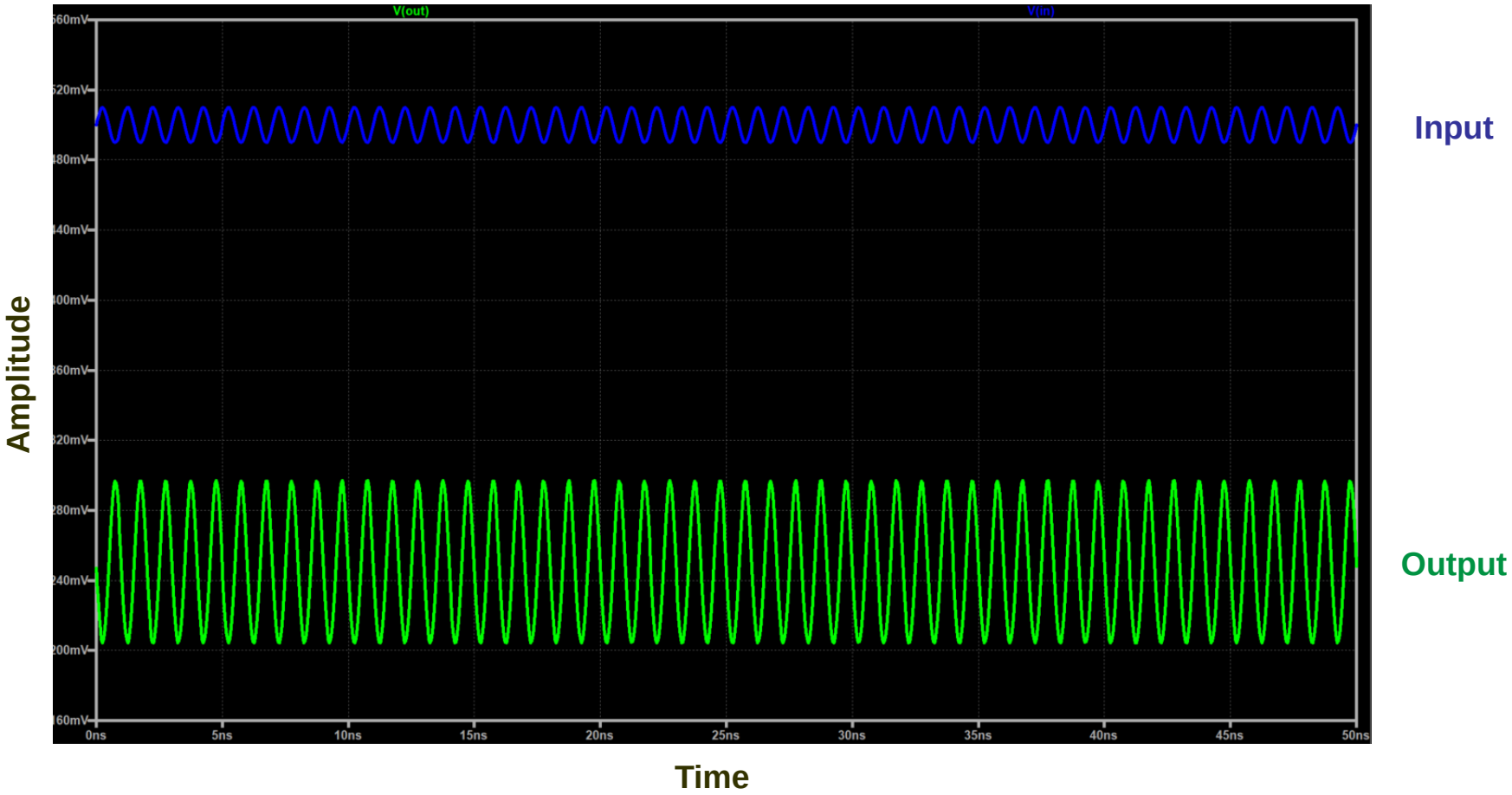
◆ 5. Transient Simulation

Transient simulation is used for **time-domain responses** at a specific node.



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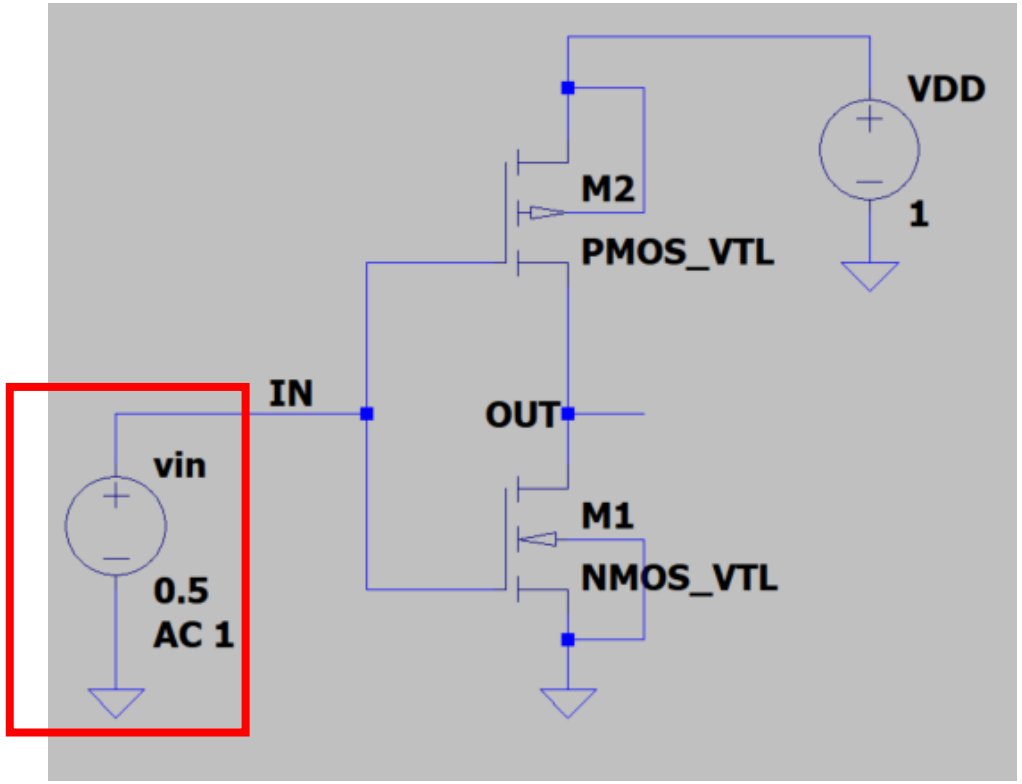
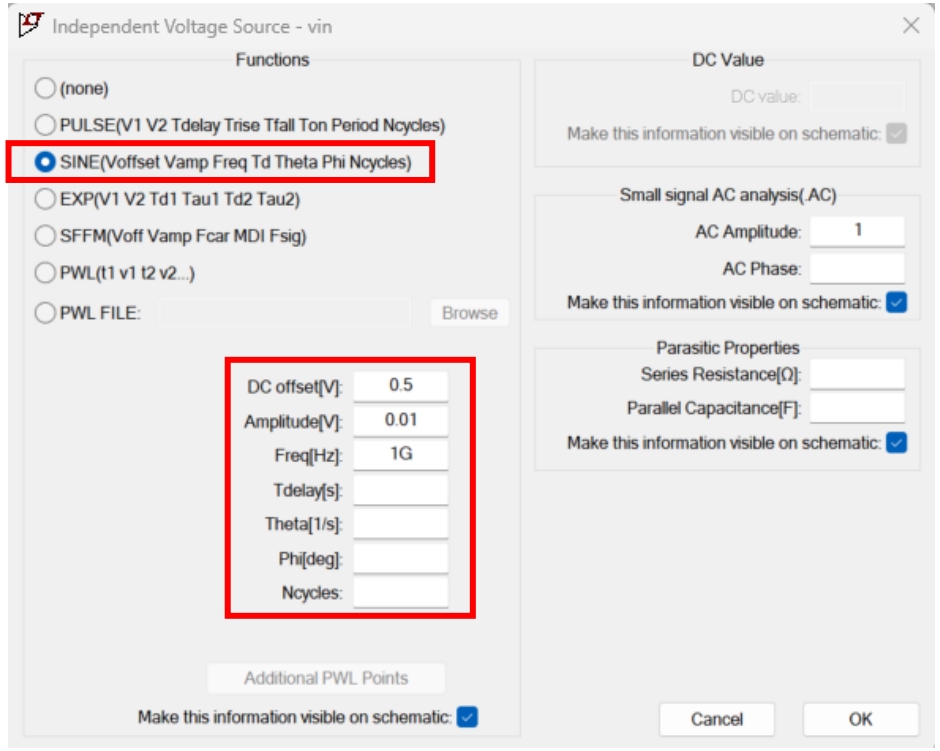
◆ 5. Transient Simulation



1) Right click on voltage source



2) Use any input you want to put in.

If you want to input sine wave, use **SINE Functions**.

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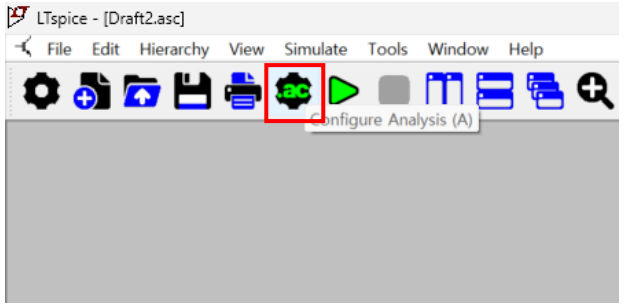
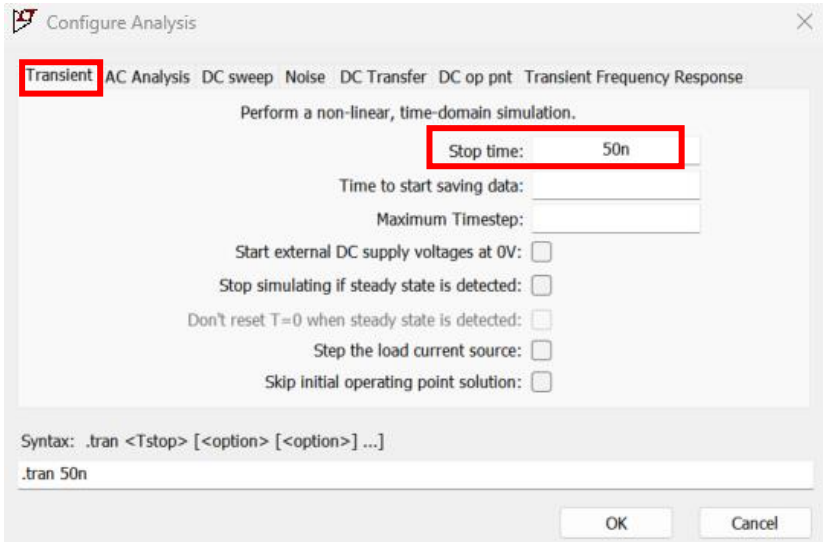
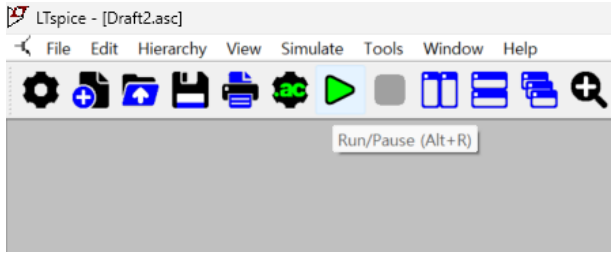
◆ 5. Transient Simulation



3) Click the **Configure Analysis (A)**



4) **Select Transient** and **setup stop time** you want to see



5) Click the **Run/Pause (Alt + R)**

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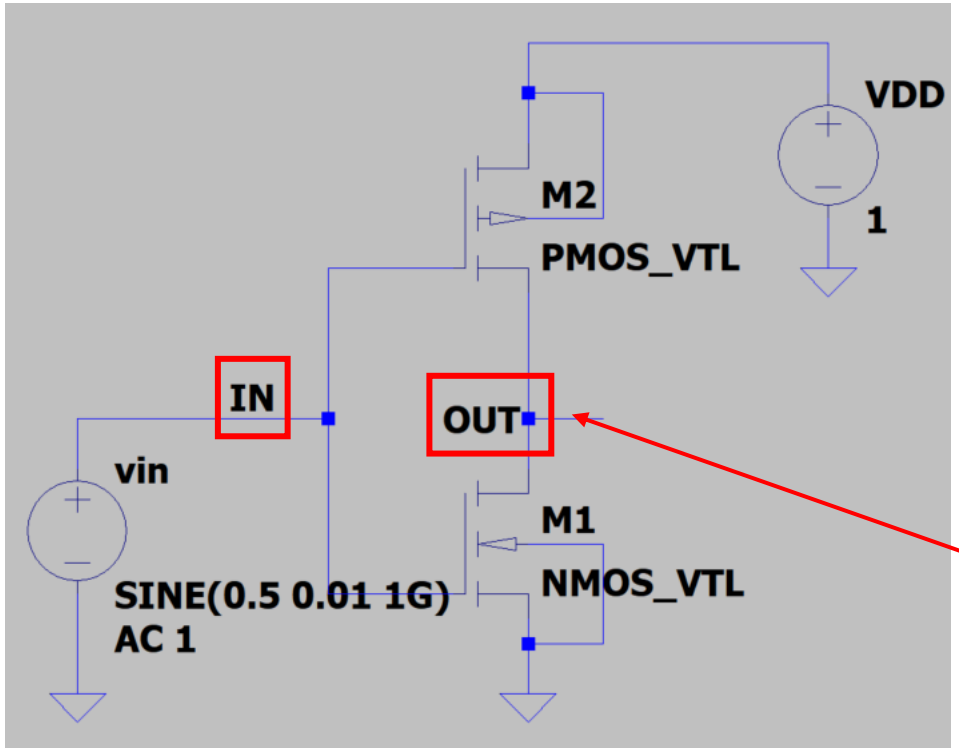
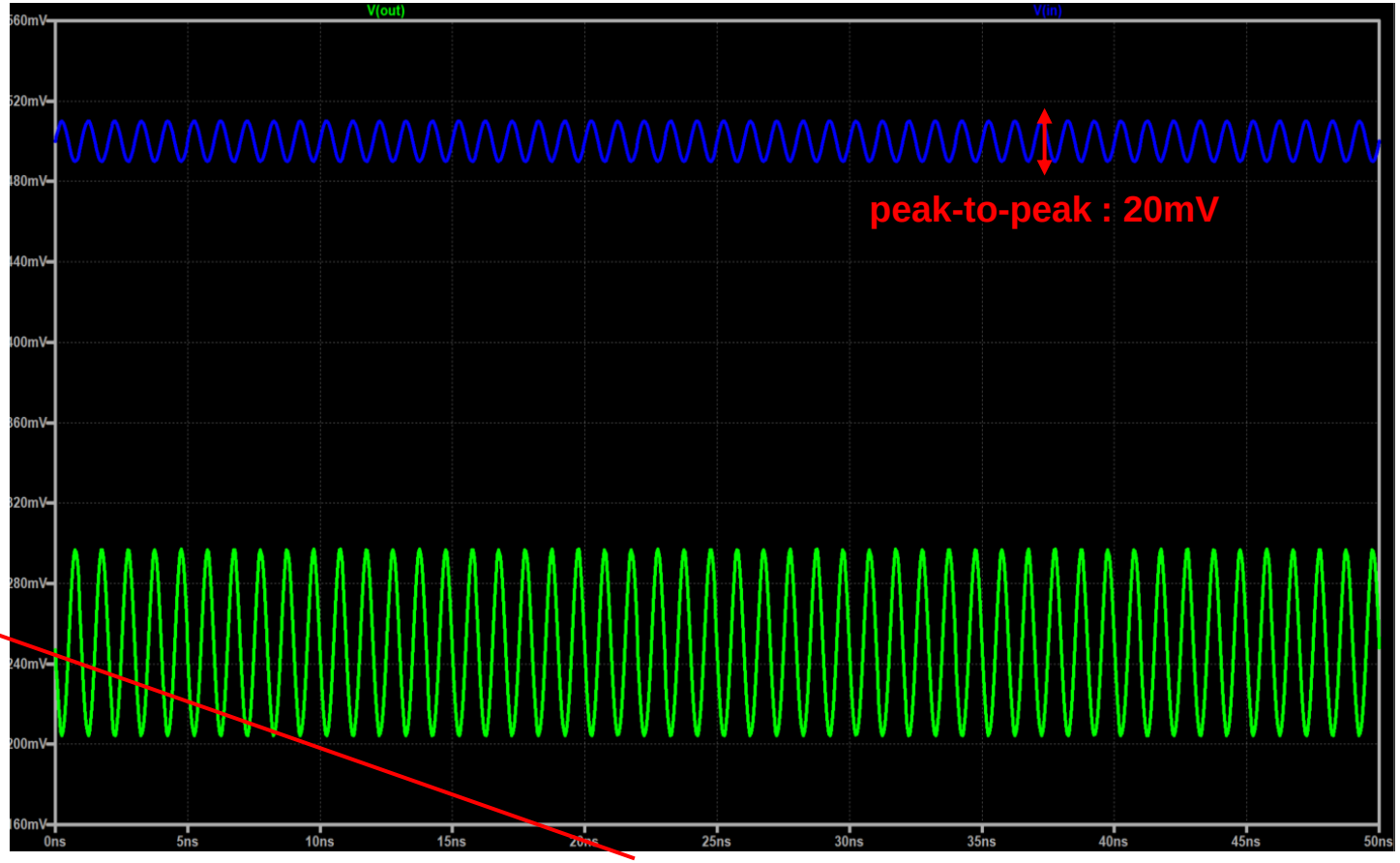
◆ 5. Transient Simulation



Schematic



6) If you want to see **voltage, click on the node(IN, OUT)** in schematic

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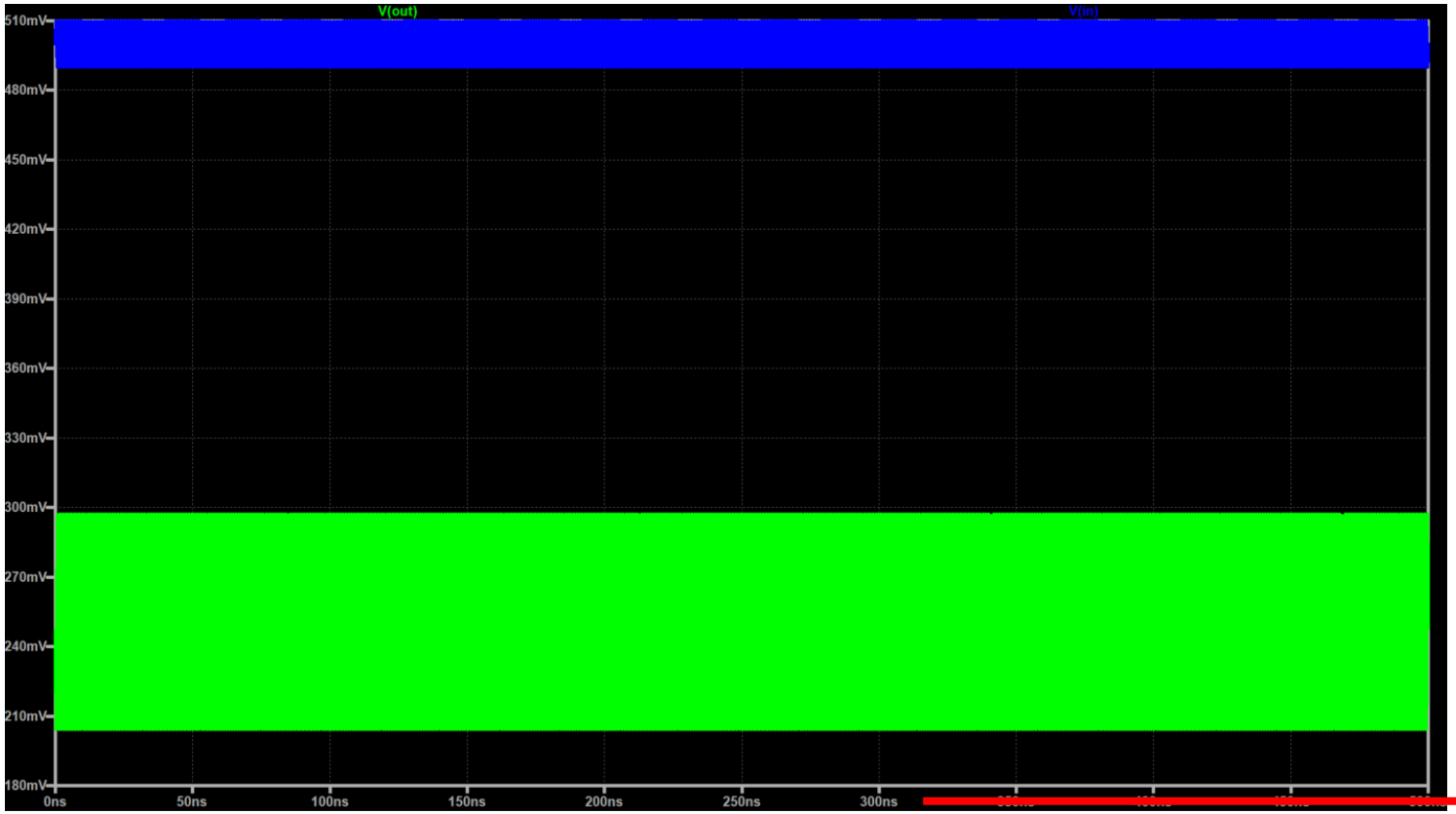
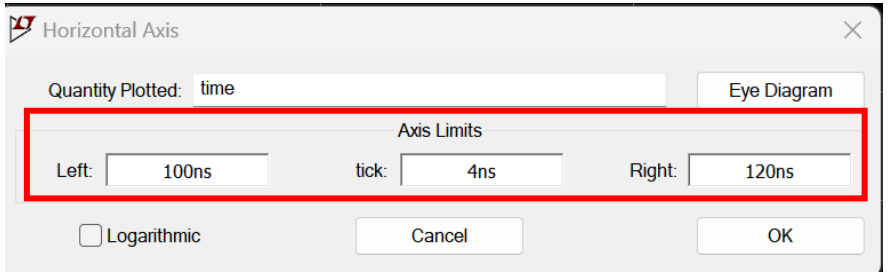
◆ 5. Transient Simulation



If you run too much time, signal can not be seen well.



Right click on x-axis to set up time-range

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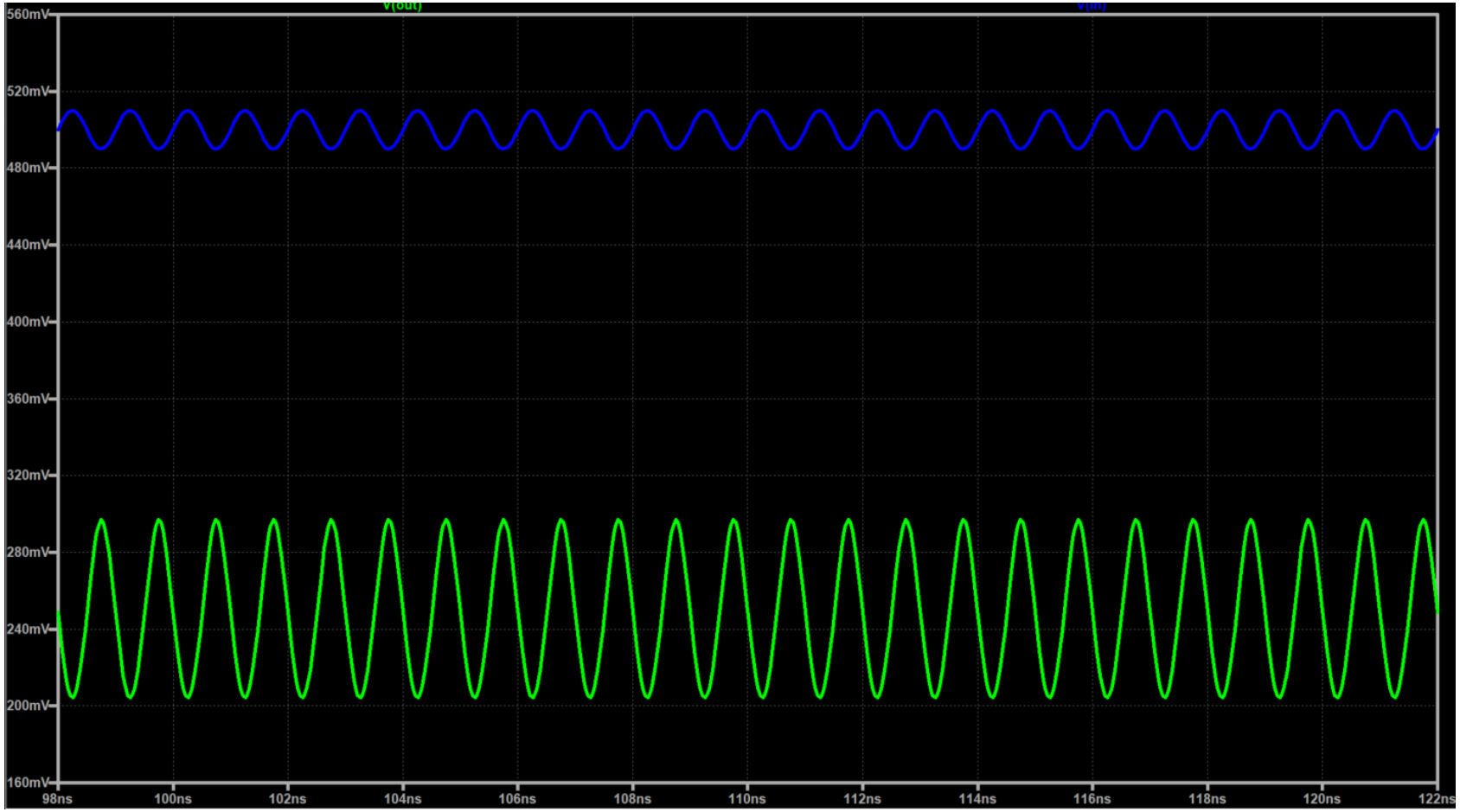
◆ **5. Transient Simulation**

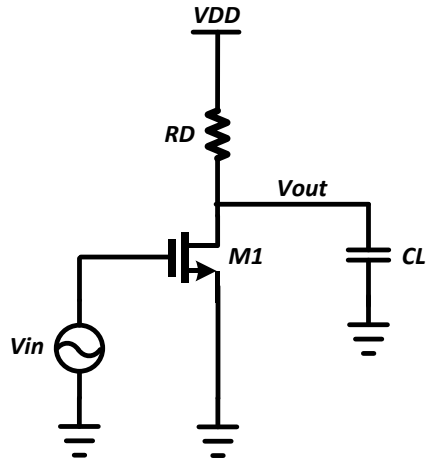


Lect. 22: LTspice Tutorial

Homework

- Design condition

$V_{DD} = 1.2V, V_{SS} = 0V, R_D = 1.4k\Omega, M1\ length = 180nm, M1\ width = 4.5\mu m, C_L = 100fF,$
Vin DC offset voltage $= 0.6V$, Amplitude $= 0.05V$, Frequency $= 300MHz$



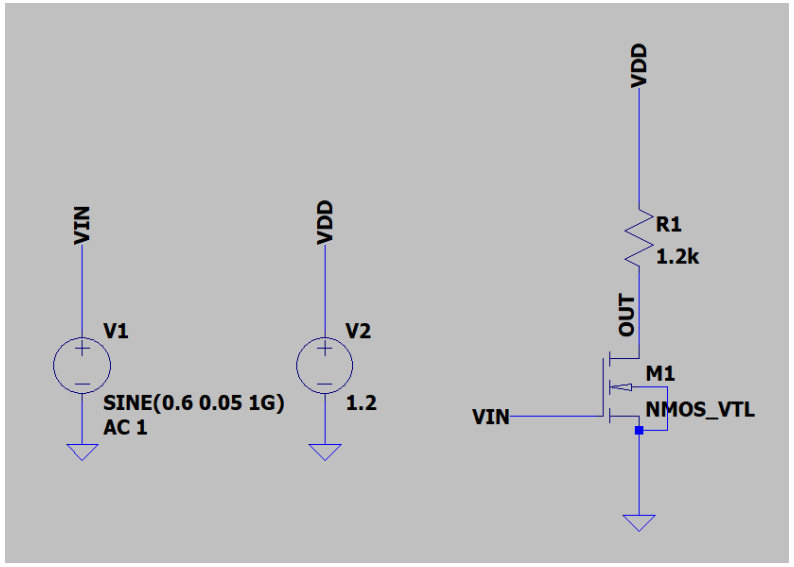
CS Amp

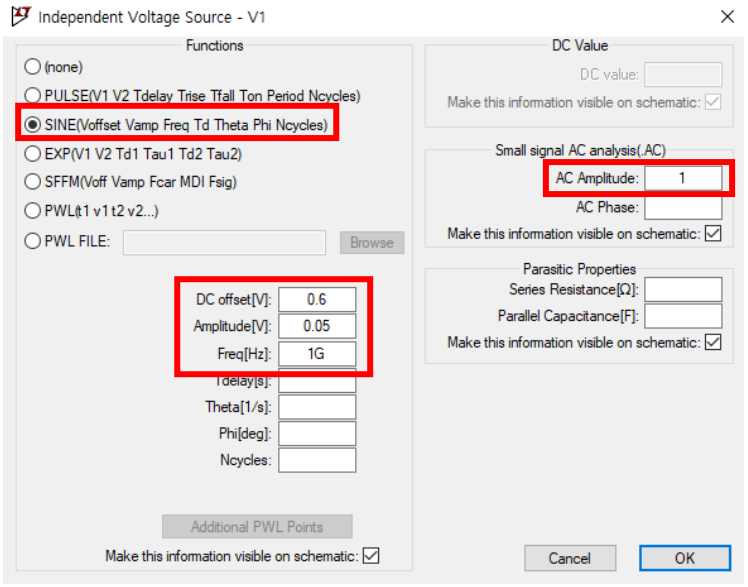
1) Determine Vth by plotting Id-Vgs curve (Sweep Vgs from 0V to 0.6V)
2) Plot gm(transconductance) by using DC sweep simulation. (Sweep Vgs form 0V to 1.2V)
3) Determine ro for the transistor at Vgs=0.6V
4) Run transient simulation and AC analysis simulation. Find DC gain and 3dB-bandwidth.

Lect. 22: LTspice Tutorial

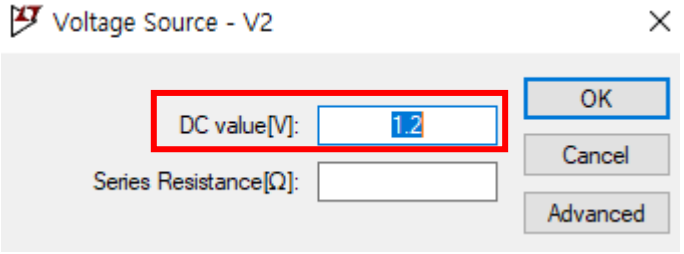
1. Follow the instructions

1-1) Draw CS Amp schematic





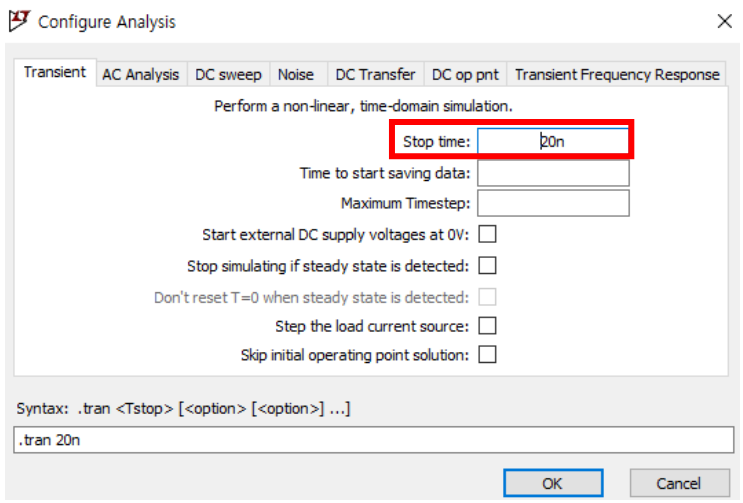
VIN(V1) voltage source setting



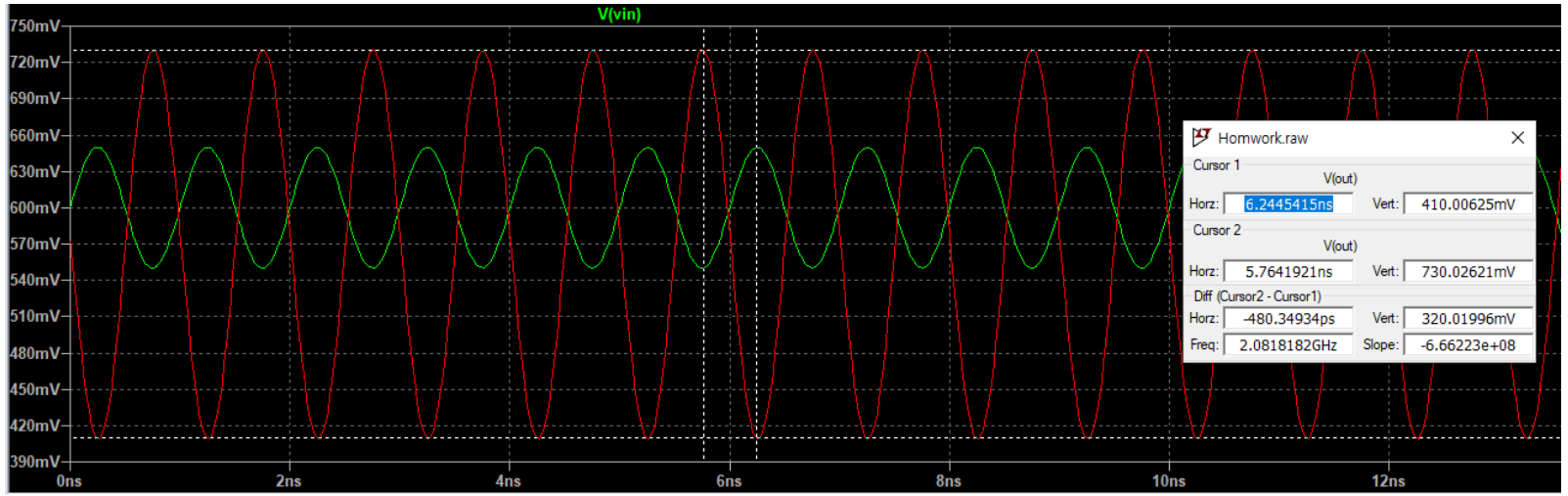
VDD(V2) voltage source setting

Lect. 22: LTspice Tutorial

1-2) Run Transient and AC analysis simulation



Transient simulation

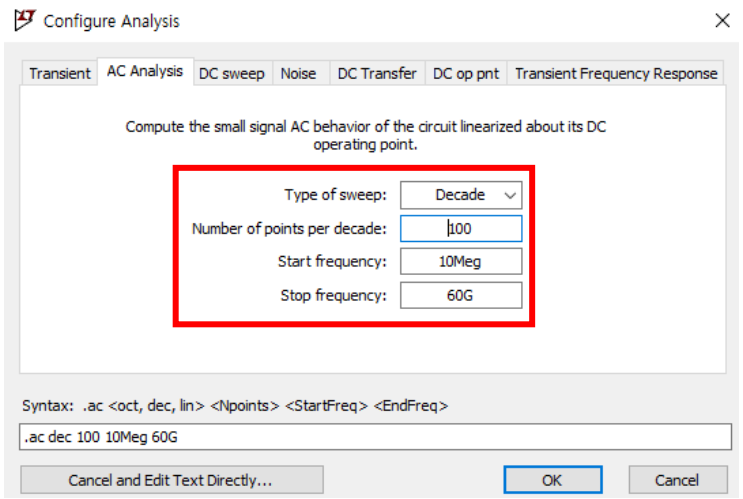


Simulation result

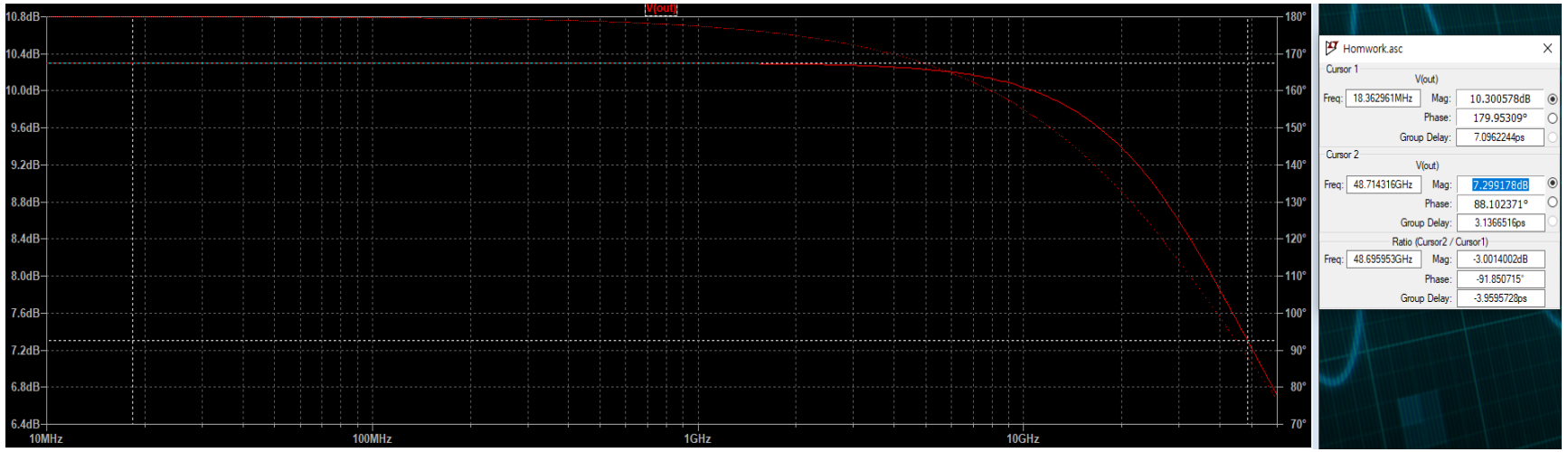
Check input & output amplitude and CS Amp gain

Lect. 22: LTspice Tutorial

1-2) Run Transient and AC analysis simulation



AC analysis simulation

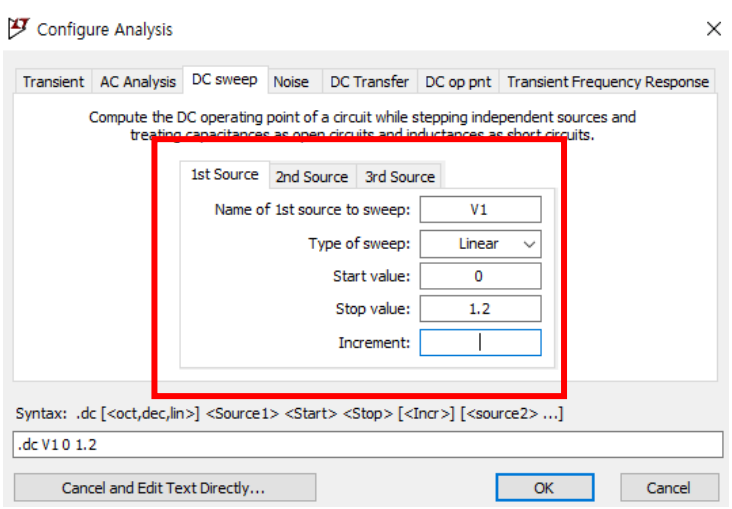


Simulation result

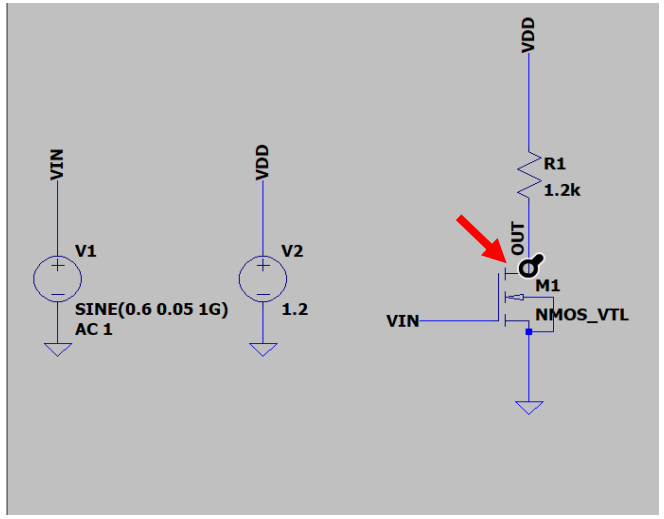
Check DC gain & 3dB Bandwidth

Lect. 22: LTspice Tutorial

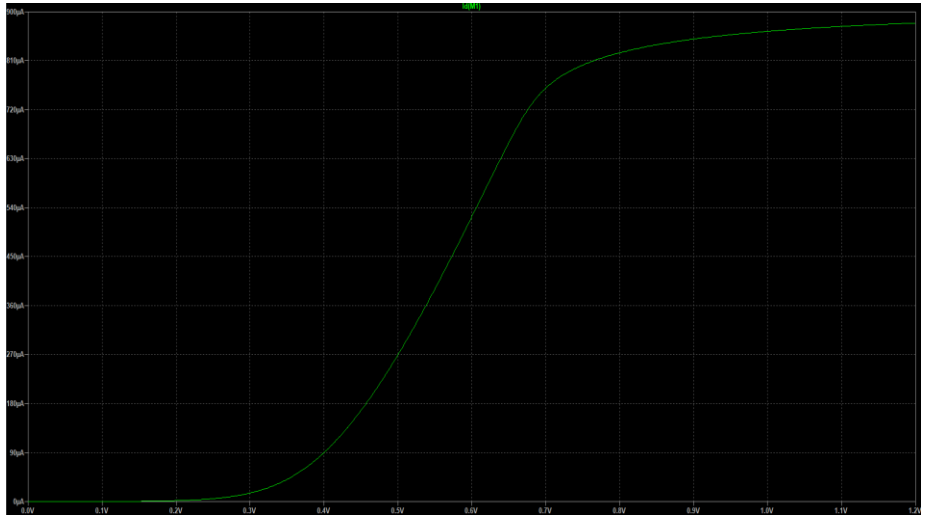
1-3) Find gm(transconductance) using DC sweep simulation



DC sweep simulation



Click Nmos drain terminal

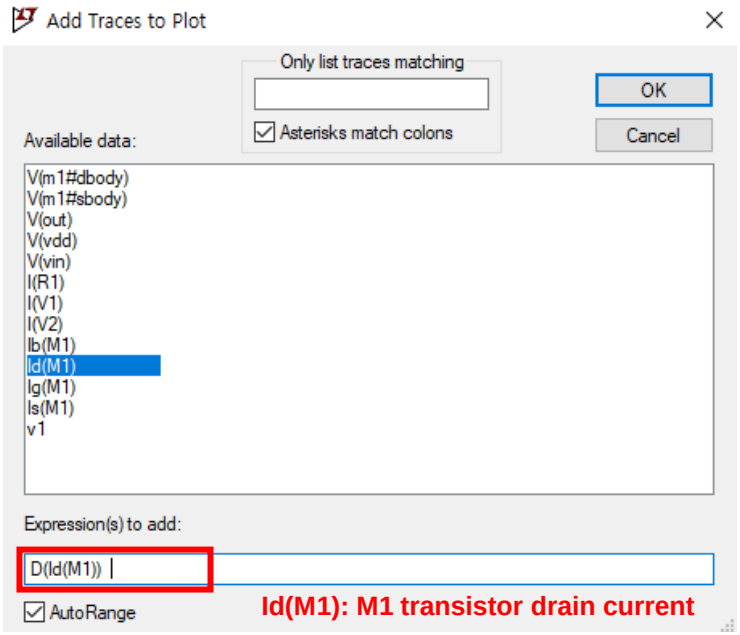


Drain current depending on V_{GS}

Lect. 22: LTspice Tutorial

1-3) Find gm(transconductance) using DC sweep simulation

toolbar → Plot Setting → Add Trace → Expression to add function (D(Id(M1)))



Id(M1): M1 transistor drain current

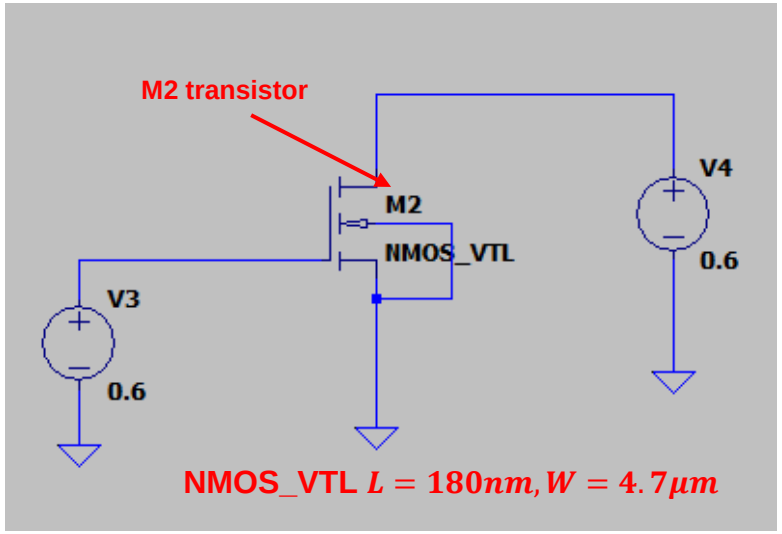
Add Trace

gm and Drain current depending on V_{GS}

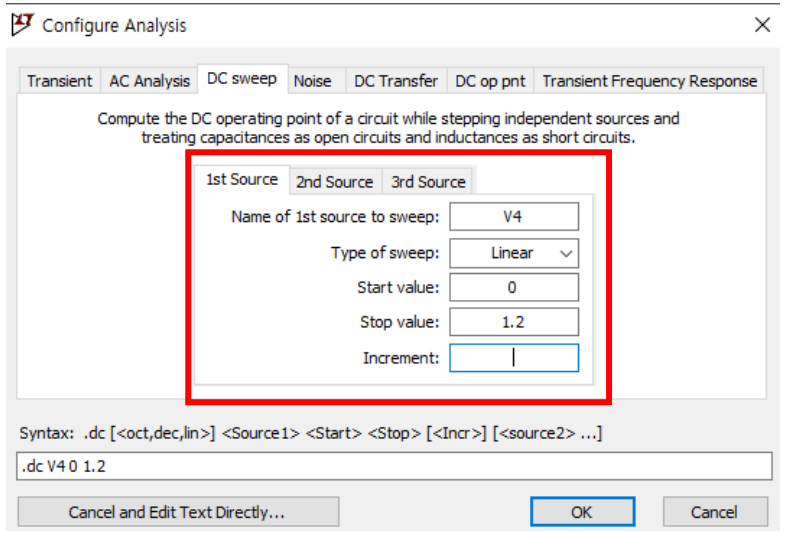
D function calculates derivative of y in terms of x-axis' variable

Lect. 22: LTspice Tutorial

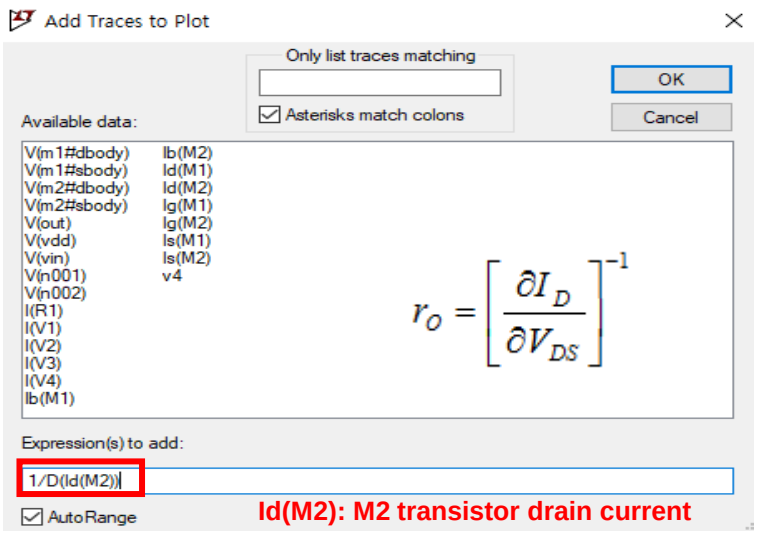
1-4) Find ro for transistor at $V_{GS} = 0.6V$ using DC sweep simulation



Testbench schematic



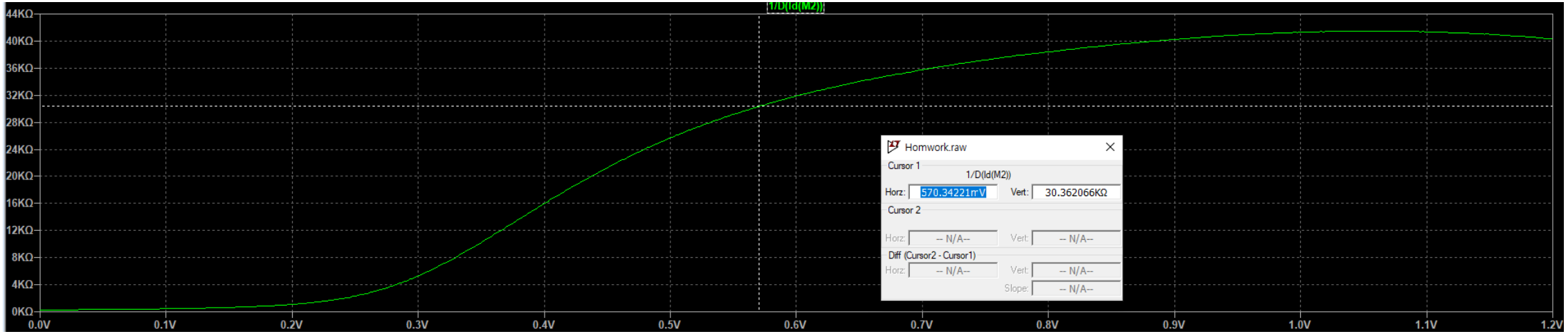
DC sweep simulation



Add trace for ro

Lect. 22: LTspice Tutorial

1-4) Find ro for transistor at $V_{GS} = 0.6V$ using DC sweep simulation



ro depending on V_{DS}