19-2268; Rev 1; 5/02

Dual 1.25Gbps Transceiver

General Description

The MAX3782 is a dual 1.25Gbps data retiming and clock recovery transceiver. It interfaces 1.25Gbps LVDS data and clock to a 1.25Gbps serial interface compatible with 1000Base-SX/LX (IEEE 802.3z-2000) standards, GBIC, and small form-factor pluggable (SFP) module interface recommendations. The serial differential transmitter and receiver are PECL compatible using an AC-coupled CML interface with on-chip termination/bias resistors for superior forward and back terminations. The transmit path converts the LVDS signaling to CML and retimes the serial data to a low-jitter reference clock. The transmitter section contains LVDS buffers, FIFO, clock multiplier, and CML output buffers. The transmitter accepts a single 1.25Gbps serial-data channel and a 625MHz double-data-rate (DDR) clock that are compatible with IEEE Std 1596-1996 DC specifications. Serial LVDS data is clocked into the FIFO on both edges of the 625MHz source-synchronous TCLK. Data is clocked out of the FIFO using an internal 1.25GHz clock derived from a low-jitter 125MHz reference. Serial data is then clocked out as differential CML.

The receive path converts the CML signaling to LVDS and locks on to the data stream to recover the source-synchronous clock (RCLK). The receive section contains a CML input buffer, clock recovery circuit, and LVDS output buffers. The receiver accepts a CML serial data stream. The clock recovery phase-locked loop (PLL) locks on to the incoming serial data stream and generates a 625MHz LVDS DDR clock. RCLK edges are at the center of the "eye" of RDAT data.

Applications

1000Base-SX/LX Optical Links

GBIC Modules

SFP Fiber Transceiver Modules

Typical Application Circuit appears at end of data sheet.

Features

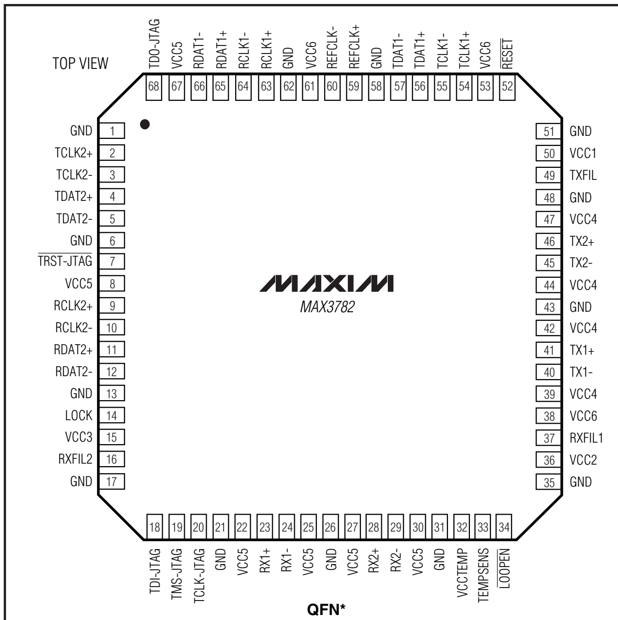
- ♦ **1000Base-SX/LX, GBIC, or SFP Serial Data Conversion to/from 1.25Gbps LVDS Serial Data and DDR Clock**
- ♦ **CML Interface Exceeds all PECL AC Specifications for 1000Base-SX/LX, GBIC, or SFP Serial Data**
- ♦ **Tx Data Retiming with <0.1UI Total Output Jitter as per IEEE802.3z**
- ♦ **Rx Data and Clock Recovery with 0.75UI Jitter Tolerance as per IEEE802.3z**
- ♦ **On-Chip Forward and Back Termination Using CML I/O and Integrated Termination/Bias Resistors**
- ♦ **PLL Lock Status Indicator**
- ♦ **System Loopback**
- ♦ **JTAG I/O Scan for Board-Level Testing**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3782UGK	-5°C to +85°C	68 QFN-EP*

*EP = exposed pad.

Pin Configuration



QFN*

* THE EXPOSED PAD OF THE QFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL AND ELECTRICAL OPERATION OF THE MAX3782.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Dual 1.25Gbps Transceiver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC1, VCC2, VCC3, VCC4, VCC5, VCC6, VCCTEMP) ....-0.5V to +4.0V
LVDS Input and Output Voltage.................-0.5V to (V_{CC} + 0.5V)
LVTTL Input or Output Voltage...................-0.5V to (V_{CC} + 0.5V)
CML Input Voltage......................................-0.5V to (V_{CC} + 0.5V)
Continuous CML Output Current ....-10mA to +25mA
Momentary CML Output Voltage (duration <1min, +25°C)...............................0 to (V_{CC} + 0.5V)
TEMPSENS, RXFIL1, RXFIL2, TXFIL Voltage ....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
68-Pin QFN (derate 38.5mW/°C above +85°C) 2.5W
Operating Ambient Temperature Range ....-5°C to +85°C
Operating Junction Temperature Range.............-5°C to +150°C
Storage Ambient Temperature Range..............-55°C to +150°C
ESD Human Body Model (any pin) 2000V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, LVDS differential load = 100Ω ±1%, CML differential load = 100Ω ±1%, T_A = -5°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current				440	620	mA
Power Dissipation				1.45	2.23	W
Supply Noise Tolerance		DC-500kHz, single-ended REFCLK (Note 1)		50		mV_{P-P}
LVTTL INPUTS AND OUTPUTS (except REFCLK±)						
Input High Voltage			2.0			V
Input Low Voltage					0.8	V
Input High Current					-250	µA
Input Low Current					-500	µA
Output High Voltage		(Note 2)	2.4			V
Output Low Voltage		(Note 2)			0.4	V
Output Three-State Current		Three-state enabled, 0.4V ≤ V_{OUT} ≤ V_{CC}	-100		+100	µA
		Three-state enabled, GND ≤ V_{OUT} < 0.4V			400	
REFCLK INPUTS						
Differential Input Amplitude		REFCLK± AC-coupled	200		2000	mV_{P-P}
Single-Ended Input High Voltage		REFCLK- connected through 0.01µF to GND	2.0			V
Single-Ended Input Low Voltage		REFCLK- connected through 0.01µF to GND			0.8	V
REFCLK Input High Current		2.0V ≤ V_{IN} ≤ V_{CC}			440	µA
REFCLK Input Low Current		GND ≤ V_{IN} ≤ 0.8V			-227	µA
CML INPUTS (Note 3)						
Differential Input Voltage Range		802.3z and GBIC compatible	370		2000	mV_{P-P}
Common-Mode Voltage		Inputs open or AC-coupled		V_{CC} - 0.3		V
Input Impedance		(Note 4)	85	100	115	Ω
CML OUTPUTS (Note 3)						
Differential Output Voltage			1100		2000	mV_{P-P}
Output Common-Mode Voltage				V_{CC} - 0.4		V
Differential Output Impedance		(Note 4)	85	100	115	Ω

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, LVDS differential load = 100Ω ±1%, CML differential load = 100Ω ±1%, T_A = -5°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS INPUTS						
Input Voltage Range	V_I	$\lvert V_{GPD} \rvert$ < 925mV	0		2000	mV
Differential Input Voltage	$\lvert V_{ID} \rvert$	$\lvert V_{GPD} \rvert$ < 925mV	150		500	mV
Differential Input Impedance	R_{IN}		85	100	115	Ω
Input Common-Mode Current		V_{OS} = 1.2V, inputs tied together		270	400	µA
LVDS OUTPUTS						
Differential Output Voltage	$\lvert V_{OD} \rvert$		250		400	mV
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Change in Magnitude of Differential Output Voltage for Complementary States	$\Delta\lvert V_{OD} \rvert$				25	mV
Output Offset Voltage	V_{OS}		1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta\lvert V_{OS} \rvert$				25	mV
Differential Output Impedance	R_{OD}		80	100	120	Ω
Short-Circuit Current		Short to supply or ground			40	mA

Note 1: Supply noise tolerance is the amount of noise allowable on the power supply. The intent of this is to specify the conditions whereby the CML I/O jitter performance remains compliant with IEEE802.3z jitter specifications.
Note 2: The LOCK output is open collector and requires a 10kΩ pullup to V_{CC}. TDO output load ≥ 11kΩ to V_{CC} or to GND.
Note 3: CML differential signal amplitudes are specified as the total signal across the load (V+ - V-). CML inputs and outputs are designed to be AC-coupled.
Note 4: 100Ω is standard for SFP, nonstandard for IEEE802.3z and GBIC.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, LVDS differential load = 100Ω ±1%, CML differential load = 100Ω ±1%, REFCLK = 125MHz, T_A = -5°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JTAG PARAMETERS						
Clock Frequency					15	MHz
Setup Time		Data input to clock positive edge	15	7		ns
Hold Time		Clock positive edge to data input	13	5		ns
Propagation Delay		Clock negative edge to data output (C ≤ 20pF)	2		30	ns
TDO Output Rise Time		C ≤ 20pF, measured 20% to 80%	2		20	ns
TDO Output Fall Time		C ≤ 20pF, measured 20% to 80%	1		20	ns
TDO Output Three-State to Active Time		C ≤ 20pF, measured as rise or fall time	1		30	ns

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, LVDS differential load = 100Ω ±1%, CML differential load = 100Ω ±1%, REFCLK = 125MHz, T_A = -5°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOCK DETECT PARAMETERS						
Assert Time		To assert, the Tx and Rx PLL internal lock indicators must be high (lock achieved) for this period.		394		µs
Deassert Time		To deassert, the Tx or Rx PLL internal lock indicators must be low for this period		1053		µs
TRANSMITTER PARAMETERS						
TCLK Frequency				625		MHz
REFCLK Input Rise/Fall Time		Single ended, 20% to 80%			2	ns
Transmitter Latency		From TDAT to Tx		5		ns
LVDS INPUTS						
Accumulated Phase Error at TCLK1 or TCLK2		Relative to REFCLK		±1		ns
Setup Time	t_{SU}	Figure 1	100	42		ps
Hold Time	t_H	Figure 1	100	42		ps
CML OUTPUTS						
Differential Skew					25	ps
Tx Output Jitter, Total		(Notes 6, 8)		32	73	ps_{P-P}
Tx Output Jitter, Deterministic		(Notes 6, 8)		9	20	ps_{P-P}
Tx Output Jitter, Random		(Notes 6, 8)		23	53	ps_{P-P}
RECEIVER PARAMETERS (Notes 7, 8)						
Input Data Rate				1.25		Gbps
PLL Lock Time		K28.5 pattern applied to Rx inputs, REFCLK must be applied and stable		1		ms
Input Jitter Tolerance (Note 9)		Pattern = 2^7 - 1, differential skew = 0, $0.45UI_{P-P}$ of data-dependent jitter		0.938		ps_{P-P}
		Pattern = CRPAT, differential skew = 0ps, $0.45UI_{P-P}$ of data-dependent jitter		0.885		
		Pattern = CRPAT, differential skew = 218ps, $0.45UI_{P-P}$ of data-dependent jitter	0.776	0.838		
		Pattern = CJTPAT, differential skew = 218ps, $0.248UI_{P-P}$ of pulse-width distortion (Note 10)	0.595	0.694		
Differential Skew Tolerance		802.3z and GBIC compliant	205			ps
Jitter Generation				20	100	ps_{P-P}
Receiver Latency		From Rx to RDAT		5		ns

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, LVDS differential load = 100Ω ±1%, CML differential load = 100Ω ±1%, REFCLK = 125MHz, T_A = -5°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS OUTPUTS						
Clock Duty-Cycle Distortion		Variation of 50% crossing from ideal time	-32		+32	ps
Deterministic Jitter		Measured with K28.5 pattern at RDAT_ outputs		8	50	ps_{P-P}
Edge Speed	t_r, t_f	20% to 80%		200	250	ps
Clock-to-Data Delay	τ_{CLK-Q}	Figure 2	268	400	532	ps
REFERENCE CLOCK REQUIREMENTS						
REFCLK Frequency				125		MHz
REFCLK Frequency Tolerance			-100		+100	ppm
REFCLK Duty Cycle			40		60	%
REFCLK Jitter		f < 5kHz, jitter assumed Gaussian			210	ps_{P-P}
					15	ps_{RMS}
		f > 5kHz, jitter is assumed deterministic, caused by power-supply noise and buffer jitter			20	ps_{P-P}

Note 5: AC characteristics are guaranteed by design and characterization.

Note 6: Tx output jitter, total, is the sum of both deterministic (20ps_{P-P} max) and random (53ps_{P-P} max at BER = 10^{-12}), as per IEEE802.3z. Measured with K28.5 pattern and one-pole 637kHz highpass filter weighting.

Note 7: JITTER TEST METHODS: These are described in the draft technical report by ANSI T11.2/Project 1230, document FC-MJS, "Fibre Channel - Methodologies for Jitter Specification." The maximum BER used to specify both Fibre Channel links, as well as IEEE802.3z links is 10^{-12}.

Note 8: JITTER TEST CONDITIONS: The difference between the MAX3782 jitter specifications and the IEEE802.3z standards (see Table 1) represents the margin that must absorb all impairments such as jitter transfer from REFCLK, power-supply noise, and oscillator pulling (due to different Tx and Rx frequencies).

Note 9: Input jitter tolerance is the total amount of high-frequency jitter at the inputs. Total jitter = deterministic jitter (DJ) + random jitter (RJ) + 5MHz sinusoidal jitter (SJ). Random jitter = 2ps_{RMS} (35mUI_{RMS}).

Note 10: CJTPAT is a unique pattern, which toggles between high transition-density sections to low transition-density sections at a rate within the loop bandwidth of a CDR. Passing this signal through a band-limited channel results in data-dependent jitter (DDJ) that has instantaneous phase jumps occurring at the rate of transition-density change. The phase vs. time looks like a low-frequency square wave. A 0.5UI_{P-P} low-frequency square wave of jitter is the maximum that can be tolerated by an ideal CDR. In other words, 0.5UI_{P-P} low-frequency square-wave jitter produces an equivalent stress as 1.0UI_{P-P} high-frequency square-wave jitter.

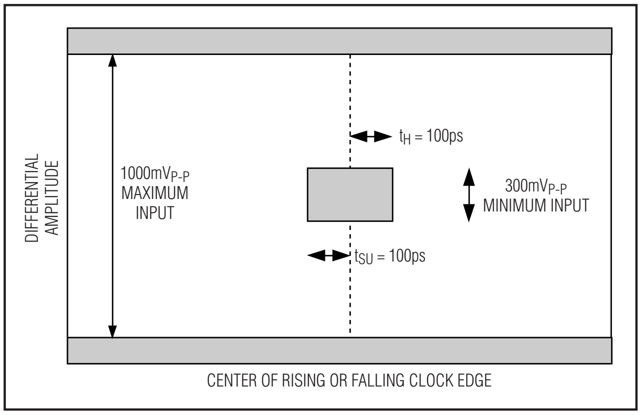


Figure 1. LVDS Receiver Input Eye Mask

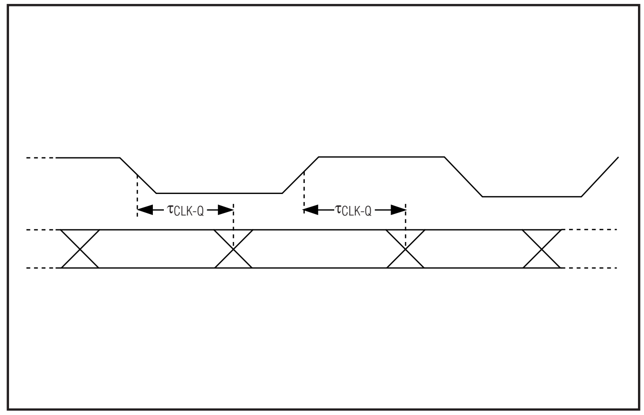
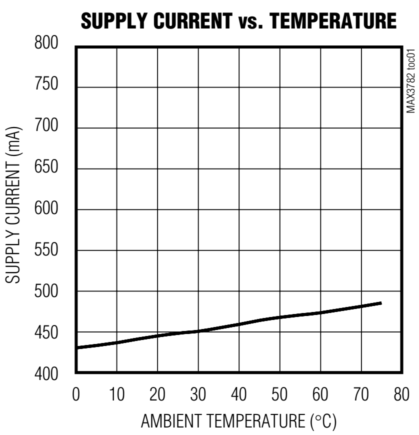
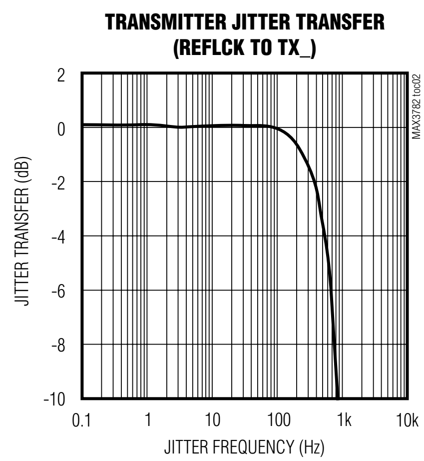


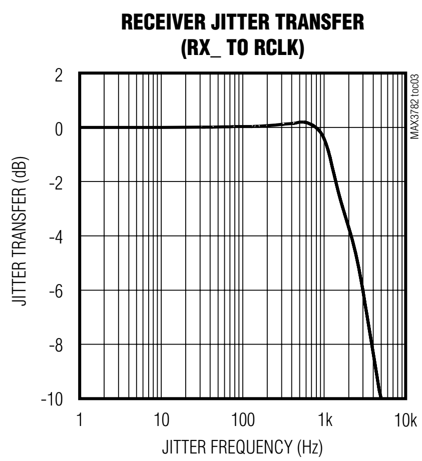
Figure 2. Definition of Clock-to-Data Delay

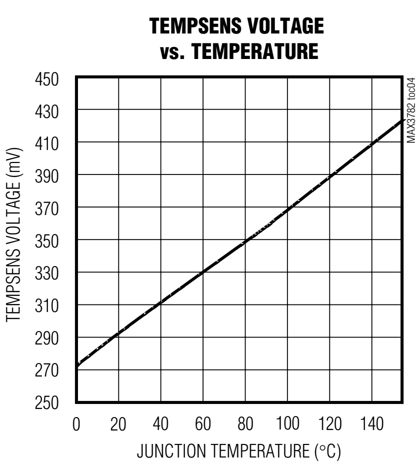
Typical Operating Characteristics

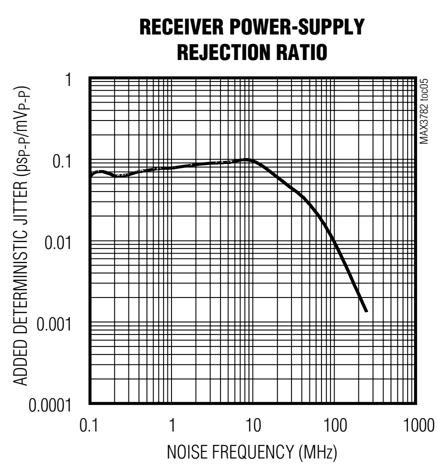
(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

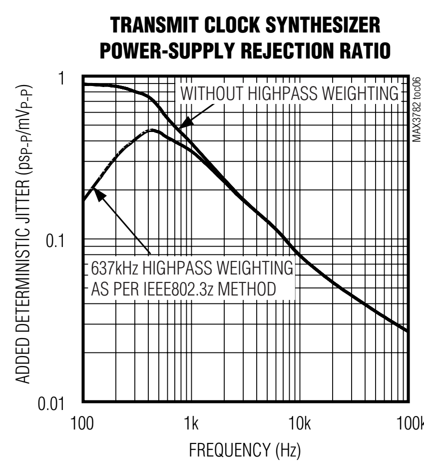








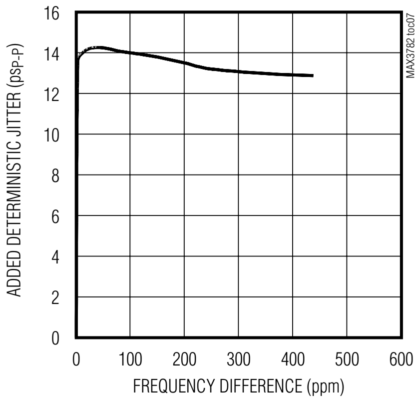




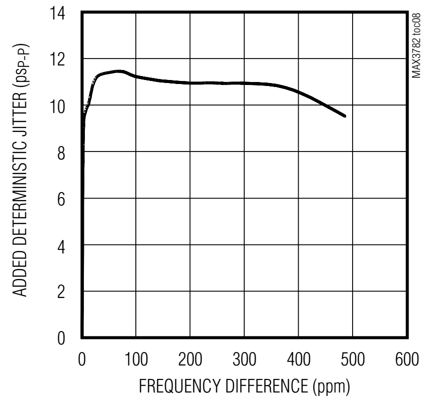
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

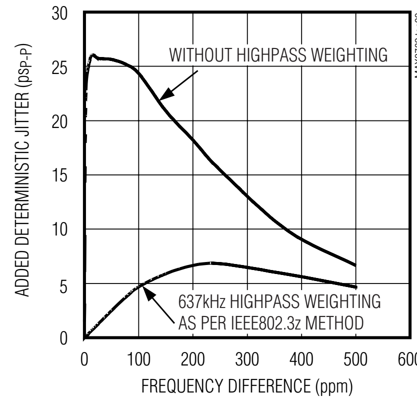
VCO$_{TX}$ AND VCO$_{RX2}$ PULLING TO VCO$_{RX1}$



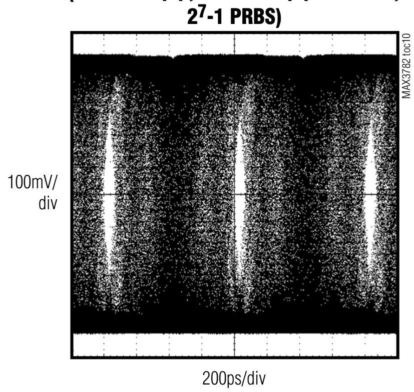
VCO$_{TX}$ AND VCO$_{RX1}$ PULLING TO VCO$_{RX2}$



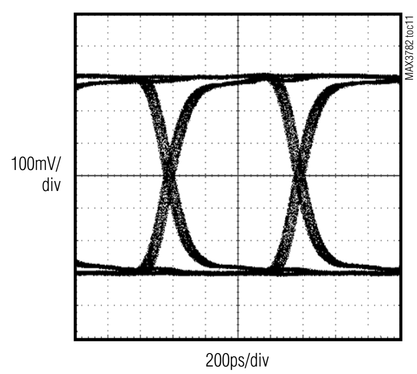
VCO$_{RX1}$ AND VCO$_{RX2}$ PULLING TO VCO$_{TX}$



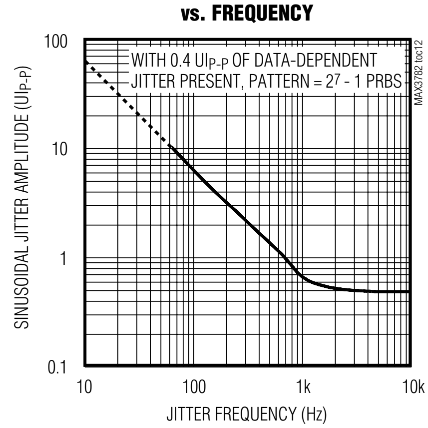
INPUT EYE (DJ = 0.4UI$_{P-P}$, SJ = 0.5UI$_{P-P}$ AT 5MHz, 2^7-1 PRBS)



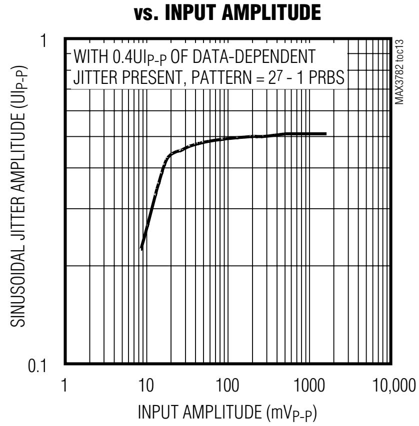
RECOVERED EYE



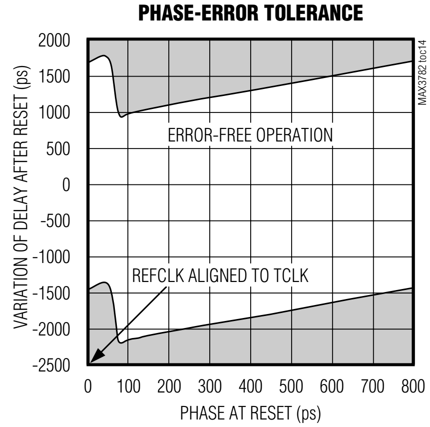
SINUSOIDAL JITTER TOLERANCE vs. FREQUENCY



5MHz JITTER TOLERANCE vs. INPUT AMPLITUDE



REFCLK TO TCLK ACCUMULATED PHASE-ERROR TOLERANCE



Pin Description

PIN	NAME	FUNCTION
1, 6, 13, 17, 21, 26, 31, 35, 43, 48, 51, 58, 62	GND	Supply Ground
2	TCLK2+	Transmitter Positive Clock Input 2, LVDS. Input data is clocked on both the rising and falling edges of the 625MHz clock.
3	TCLK2-	Transmitter Negative Clock Input 2, LVDS. Input data is clocked on both the rising and falling edges of the 625MHz clock.
4	TDAT2+	Transmitter Positive Data Input 2, LVDS
5	TDAT2-	Transmitter Negative Data Input 2, LVDS
7	$\overline{\text{TRST-JTAG}}$	JTAG Test Reset Input, LVTTL. Momentarily connect $\overline{\text{TRST}}$ to GND to reset JTAG test circuitry. Internally pulled high through 15kΩ resistor.
8, 22, 25, 27, 30, 67	VCC5	3.3V Supply for Receiver Digital Functions and JTAG Circuitry
9	RCLK2+	Receiver Positive Clock Output 2, LVDS. Output data is clocked on both the rising and falling edges of the 625MHz clock.
10	RCLK2-	Receiver Negative Clock Output 2, LVDS. Output data is clocked on both the rising and falling edges of the 625MHz clock.
11	RDAT2+	Receiver Positive Data Output 2, LVDS
12	RDAT2-	Receiver Negative Data Output 2, LVDS
14	LOCK	Lock Status Indicator Output, LVTTL. This output goes high when the transmit PLL and receiver PLLs are in lock. Because this output is open-collector TTL, the LOCK pins from multiple MAX3782s can be connected in parallel to form a single LOCK signal.
15	VCC3	3.3V Supply for RX2 Receiver VCO, Analog Receiver Functions, and External Loop-Filter Connection
16	RXFIL2	RX2 Receiver Loop-Filter Connection. Connect a 0.1µF capacitor between RXFIL2 and VCC3.
18	TDI-JTAG	JTAG Test Data Input, LVTTL. Internally pulled high through 15kΩ resistor.
19	TMS-JTAG	JTAG Test Mode Select Input, LVTTL. Internally pulled high through 15kΩ resistor.
20	TCLK-JTAG	JTAG Test Clock Input, LVTTL. Internally pulled high through 15kΩ resistor.
23	RX1+	Receiver Positive Input 1, CML
24	RX1-	Receiver Negative Input 1, CML
28	RX2+	Receiver Positive Input 2, CML
29	RX2-	Receiver Negative Input 2, CML
32	VCCTEMP	3.3V Supply for TEMPSENS. Connect to ground to disable the temperature-sensing function.
33	TEMPSENS	Junction Temperature Sensor Output, Analog. TEMPSENS corresponds to the junction temperature of the die. Leave open for normal use.
34	$\overline{\text{LOOPEN}}$	Loopback Enable Input, LVTTL. Force low to enable system loopback. Internally pulled high through 15kΩ.
36	VCC2	3.3V Supply for RX1 Receiver VCO, Analog Receiver Functions, and External Loop-Filter Connection
37	RXFIL1	RX1 Receiver Loop-Filter Connection. Connect a 0.1µF capacitor between RXFIL1 and VCC2.
38, 53, 61	VCC6	3.3V Supply for Transmitter Digital Functions
39, 42, 44, 47	VCC4	3.3V Supply for CML Outputs

Pin Description (continued)

PIN	NAME	FUNCTION
40	TX1-	Transmitter Negative Output 1, CML
41	TX1+	Transmitter Positive Output 1, CML
45	TX2-	Transmitter Negative Output 2, CML
46	TX2+	Transmitter Positive Output 2, CML
49	TXFIL	Transmitter Loop-Filter Connection. Connect a 0.1µF capacitor between TXFIL and VCC1.
50	VCC1	3.3V Supply for Transmitter VCO, Analog Transmitter Functions, and External Loop-Filter Connection
52	$\overline{\text{RESET}}$	Reset Input, LVTTL. Connect low for >80ns to reset FIFO and receiver components. Internally pulled high through 15kΩ.
54	TCLK1+	Transmitter Positive Clock Input 1, LVDS. Input data is clocked on both the rising and falling edges of the 625MHz clock.
55	TCLK1-	Transmitter Negative Clock Input 1, LVDS. Input data is clocked on both the rising and falling edges of the 625MHz clock.
56	TDAT1+	Transmitter Positive Data Input 1, LVDS
57	TDAT1-	Transmitter Negative Data Input 1, LVDS
59	REFCLK+	Reference Clock Positive Input. See specification table for differential or single-ended use.
60	REFCLK-	Reference Clock Negative Input. See specification table for differential or single-ended use.
63	RCLK1+	Receiver Positive Clock Output 1, LVDS. Output data is clocked on both the rising and falling edges of the 625MHz clock.
64	RCLK1-	Receiver Negative Clock Output 1, LVDS. Output data is clocked on both the rising and falling edges of the 625MHz clock.
65	RDAT1+	Receiver Positive Data Input 1, LVDS
66	RDAT1-	Receiver Negative Data Input 1, LVDS
68	TDO-JTAG	JTAG Test Data Output, Three-State LVTTL
EP	Exposed Pad	Supply Ground. The exposed pad must be soldered to the circuit board ground for proper thermal and electrical performance. See *Exposed-Pad Package*.
EPR	Exposed Pad Ring	Supply Ground. The ground ring must be soldered to ground. See *Exposed-Pad Package.*

Dual 1.25Gbps Transceiver

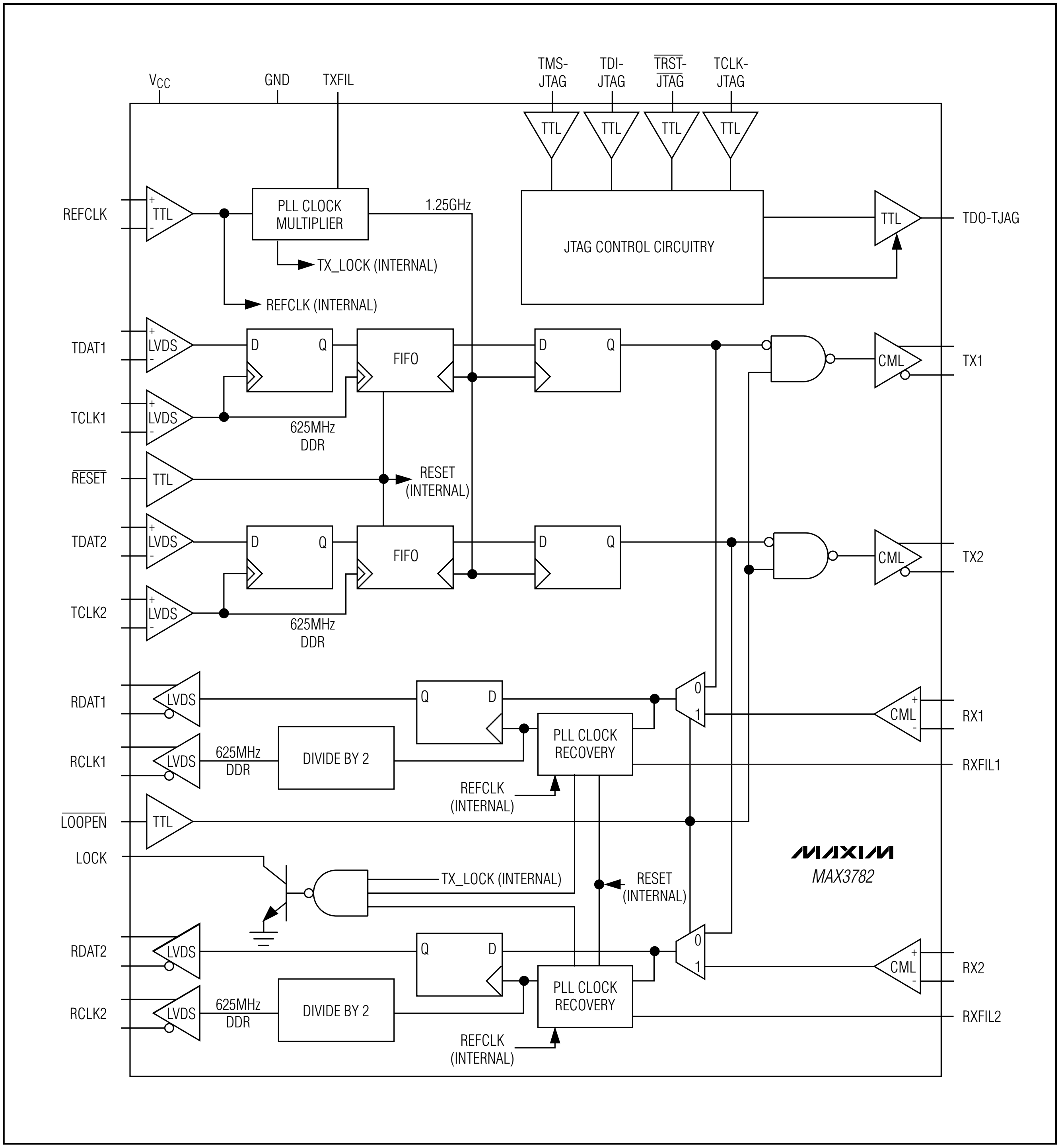


Figure 3. Functional Diagram

Detailed Description

The MAX3782 dual 1.25Gbps transceiver is a data retimer and clock recovery device for 1000Base-SX/LX, GBIC, and SFP applications. In the transmitter, an integrated clock synthesizer generates a clean 1.25GHz clock. This clock is used with a FIFO to retime the data before transmission. CML output buffers provide excellent performance with minimal external components.

The receiver has two separate PLL clock recovery circuits, allowing independent recovery of each received data signal. The receiver has CML inputs, easing system design and decreasing component count.

JTAG functionality is included to help with board-level testing. A LOCK pin indicates the status of the internal PLLs. System loopback may be asserted with the $\overline{\text{LOOPEN}}$ input.

LVDS Inputs and Outputs

The MAX3782 LVDS interface includes two differential data inputs at 1.25Gbps, two half-rate differential clock inputs at 625MHz, two differential data outputs at 1.25Gbps, and two half-rate differential clock outputs at 625MHz. The MAX3782 LVDS-compatible interface is designed to work with the user's ASICs, minimize power dissipation, speed transition time, and improve noise immunity. The LVDS outputs also have short-circuit protection in case of shorts to VCC or GND. The LVDS inputs must be DC-coupled for proper biasing. AC-coupling these inputs results in unreliable operation. The LVDS outputs are designed to drive 100Ω differential loads and are not designed to drive 50Ω to ground.

PLL Clock Multiplier

The PLL clock multiplier uses the 125MHz reference clock to synthesize the 1.25GHz clock that synchronizes the transmitter functions. The reference clock also aids frequency acquisition in the receiver. To achieve proper jitter performance and BER benchmarks, using a high-quality, low-jitter reference clock is critical. REFCLK inputs can be driven differentially or single ended. Differential operation is recommended for its superior jitter performance and noise immunity.

PLL Clock Recovery

Both receive channels (RX1 and RX2) use PLLs to recover synchronous clocks from the incoming serial data. The recovered clocks are then used to retime the serial data. The typical loop bandwidth of the PLL clock recovery circuits is 1.5MHz.

CML Inputs and Outputs

The CML inputs and outputs of the MAX3782 offer low power dissipation, excellent performance, and integrated termination resistors. AC-coupling capacitors should be used for PECL and IEEE802.3z compatibility. Figure 4 shows interface examples. The CML output structure is shown in Figure 5, and the CML input structure is shown in Figure 6. For more information, refer to

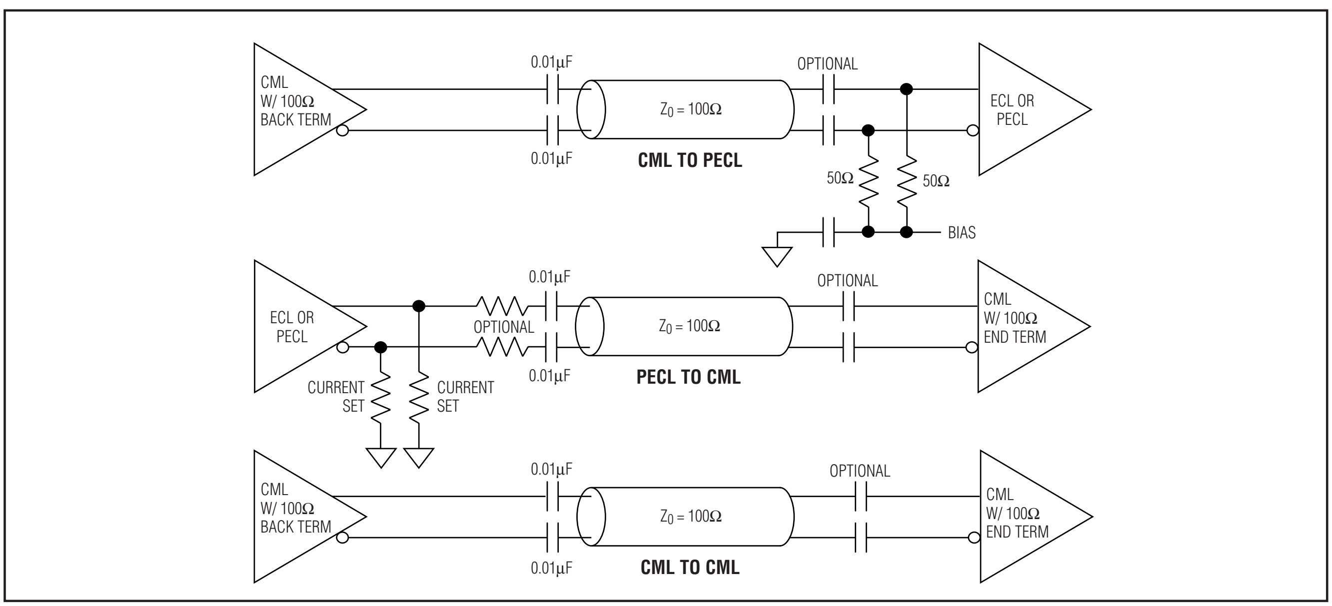


Figure 4. CML I/O Interconnect Examples

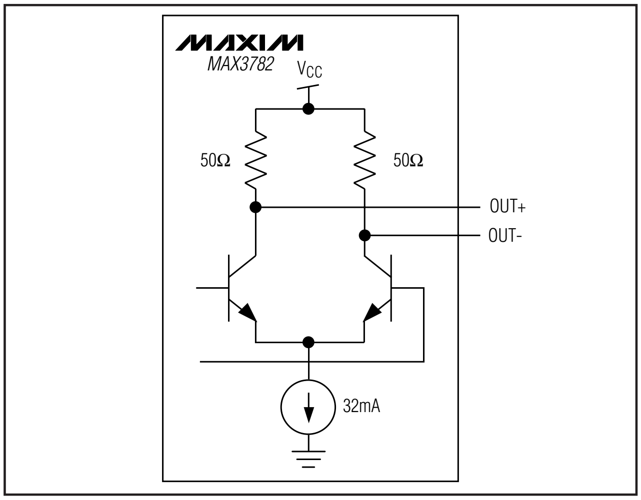


Figure 5. CML Output Structure

the applications note HFAN-01.0, *Introduction to LVDS, PECL, and CML*.

Lock Detection

The LOCK output indicates the state of the transmitter and receiver PLLs. For lock detect to be asserted high, the transmitter and receiver internal lock indicators must be high for 394μs. The internal lock signals go high once frequency lock has been achieved. For lock detect to be asserted low, either the transmitter or receiver internal lock indicators must be low for a minimum of 1053μs. Lock detect also is asserted low when the external reset pin is forced low. LOCK stays low for a minimum of 394μs. For the lock detector to function properly, there must be data transitions at the RX1 and RX2 inputs and a valid reference clock input. **Note:** The LOCK output is not an accurate indicator of signal presence at the receiver inputs. With no data input, the LOCK output can be high, low, or toggling. The output structure of the LOCK pin is shown in Figure 7.

$\overline{\text{RESET}}$ Input

$\overline{\text{RESET}}$ must be held low for a minimum of four reference clock cycles for it to be properly asserted. Approximately 10ms or longer after power up, the $\overline{\text{RESET}}$ input should be asserted low. $\overline{\text{RESET}}$ resets the LOCK state and FIFO clock logic.

Temperature Sensor

To help evaluate thermal performance, a temperature sensor is incorporated into the MAX3782. The temperature sensor may be powered on or off regardless of the state of the rest of the chip. The VCCTEMP pin provides supply voltage for the temperature sensor circuit. The TEMPSENS output is designed to output a voltage proportional to the die junction temperature (1mV per Kelvin). The temperature of the die can be calculated as:

$$T(°C) \approx V_{TEMPSENS}(mV) \times \frac{1°C}{mV} - 273°C$$

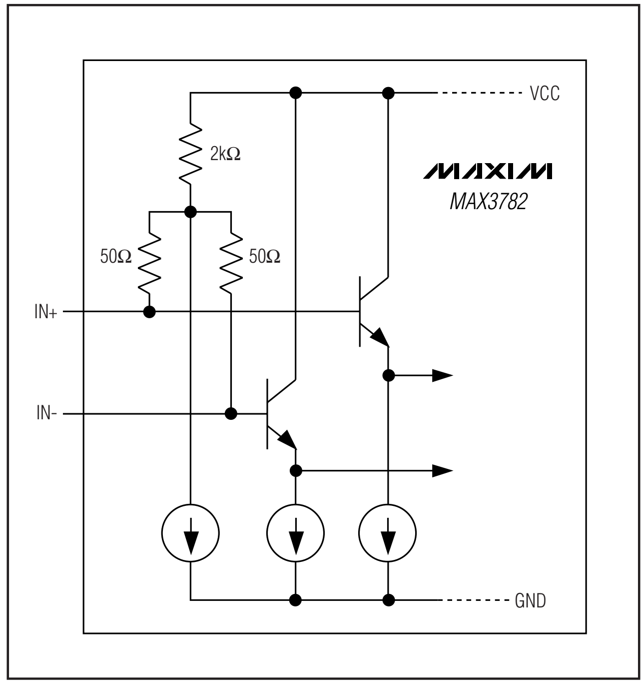


Figure 6. CML Input Structure

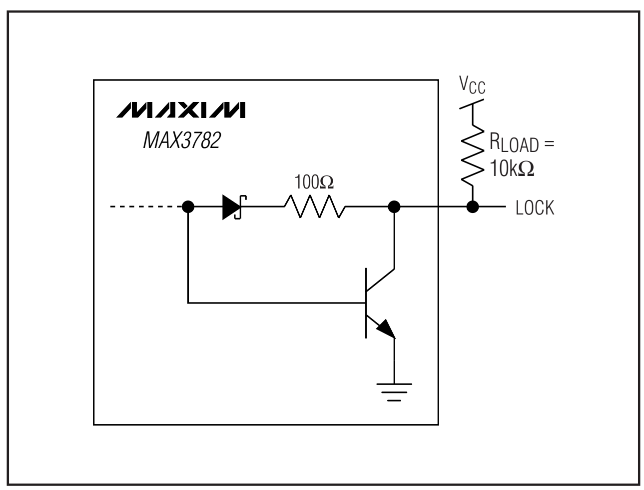


Figure 7. LOCK Output Structure

Applications Information

Jitter Budget Example for Optical Link

The MAX3782 outperforms IEEE802.3z jitter specifications. See Figure 8 and Table 1.

JTAG

JTAG functionality is compliant with IEEE1149.1 specifications. The BSDL file is available on request. Table 2 provides JTAG pin assignments.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies, keep ground connections short, and use multiple vias where possible. Use controlled-impedance 50Ω transmission lines to interface with the MAX3782 high-speed inputs and outputs.

Place power-supply decoupling capacitors as close to V_{CC} as possible. To reduce feedthrough, isolate the input signals from the output signals.

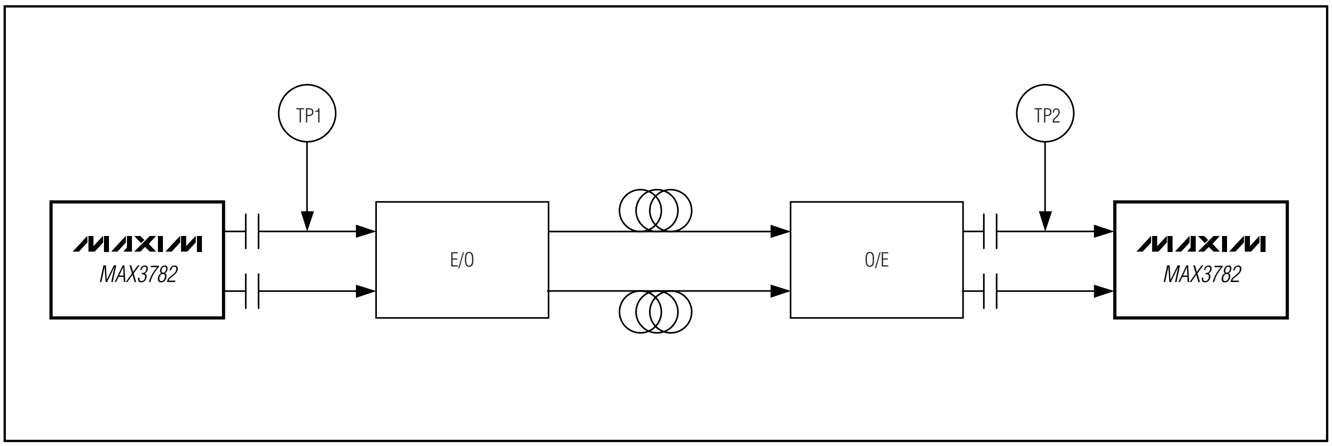


Figure 8. Optical Link

Table 1. Comparison of IEEE802.3z and MAX3782 Jitter Budget

COMPLIANCE POINT	TOTAL JITTER (ps_{P-P})		DETERMINISTIC JITTER (ps_{P-P})	
	IEEE802.3z SPECIFICATION	MAX3782 SPECIFICATION	IEEE802.3z SPECIFICATION	MAX3782 SPECIFICATION
TP1	192	73 (max)	100	20 (max)
		32 (typ)		9 (typ)
COMPLIANCE POINT	TOTAL JITTER TOLERANCE (ps_{P-P})		—	
	IEEE802.3z SPECIFICATION	MAX3782 SPECIFICATION		
TP2	600	620 (min, CRPAT)		
		670 (typ, CRPAT)		

Table 2. JTAG Pin Assignments

MAX3782 PIN NAME	BOUNDARY SCAN PORT NAME	I/O TYPE	CELL TYPE	ROUTING	
				IN	OUT
LOCK	lock	Open Collector Output	Observe and Control		1
RX2+	rx2p	CML Input	Observe	2	
RX2-	rx2n	CML Input	Observe	2	
RX1+	rx1p	CML Input	Observe	3	
RX1-	rx1n	CML Input	Observe	3	
$\overline{\text{LOOPEN}}$	loopen_bar	LVTTL Input	Observe	4	
TDAT2+	tdat2p	LVDS Input	Observe	5	
TDAT2-	tdat2n	LVDS Input	Observe	5	
TCLK2+	tck2p	LVDS Input	Observe	6	
TCLK2-	tck2n	LVDS Input	Observe	6	
TDAT1+	tdat1p	LVDS Input	Observe	7	
TDAT1-	tdat1n	LVDS Input	Observe	7	
TCLK1+	tck1p	LVDS Input	Observe	8	
TCLK1-	tck1n	LVDS Input	Observe	8	
TX1+	tx1p	CML Output	Observe and Control		9
TX1-	tx1n	CML Output	Observe and Control		9
TX2+	tx2p	CML Output	Observe and Control		10
TX2-	tx2n	CML Output	Observe and Control		10
$\overline{\text{RESET}}$	reset_bar	LVTTL Input	Observe	11	
REFCLK+	refckp	LVTTL Input	Observe	12	
REFCLK-	refckn	LVTTL Input	Observe	12	
RCLK1+	rck1p	LVDS Output	Observe and Control		13
RCLK1-	rck1n	LVDS Output	Observe and Control		13
RDAT1+	rdat1p	LVDS Output	Observe and Control		14
RDAT1-	rdat1n	LVDS Output	Observe and Control		14
RCLK2+	rck2p	LVDS Output	Observe and Control		15
RCLK2-	rck2n	LVDS Output	Observe and Control		15
RDAT2+	rdat2p	LVDS Output	Observe and Control		16
RDAT2-	rdat2n	LVDS Output	Observe and Control		16
JTAG CONTROL PINS					
TCLK-JTAG	tck	LVTTL Input			
TDI-JTAG	tdi	LVTTL Input			
TDO-JTAG	tdo	LVTTL Output			
TMS-JTAG	tms	LVTTL Input			
$\overline{\text{TRST-JTAG}}$	trst_bar	LVTTL Input			

Table 3. JTAG Instructions

INSTRUCTION	JTAG OPCODE	ACTION
EXTEST	000 b	External boundary test mode
SAMPLE/PRELOAD	001 b	Initialization for boundary test mode
BYPASS	111 b	Connects bypass register between TDI and TDO
IDCODE	010 b	32-bit device ID register selected (see Table 4)

Table 4. Device Identification Code

CODE	VERSION	PART NO.	MANUFACTURER = MAXIM	LSB
Binary	0001 b	0000 1110 1100 0110 b [= 3782 $_{base10}$]	00011001011 b [ref: JEDEC JEP106-I]	1 b

Exposed-Pad Package

The exposed-pad, 68-pin QFN-EP incorporates features that provide a very low thermal-resistance path for heat removal from the IC. The EP and EP ring are electrical ground on the MAX3782 and must be soldered to the circuit board for proper thermal and electrical performance. Refer to HFAN 08.10, *Thermal Considerations of QFN and Other Exposed-Pad Packages,* for more information.

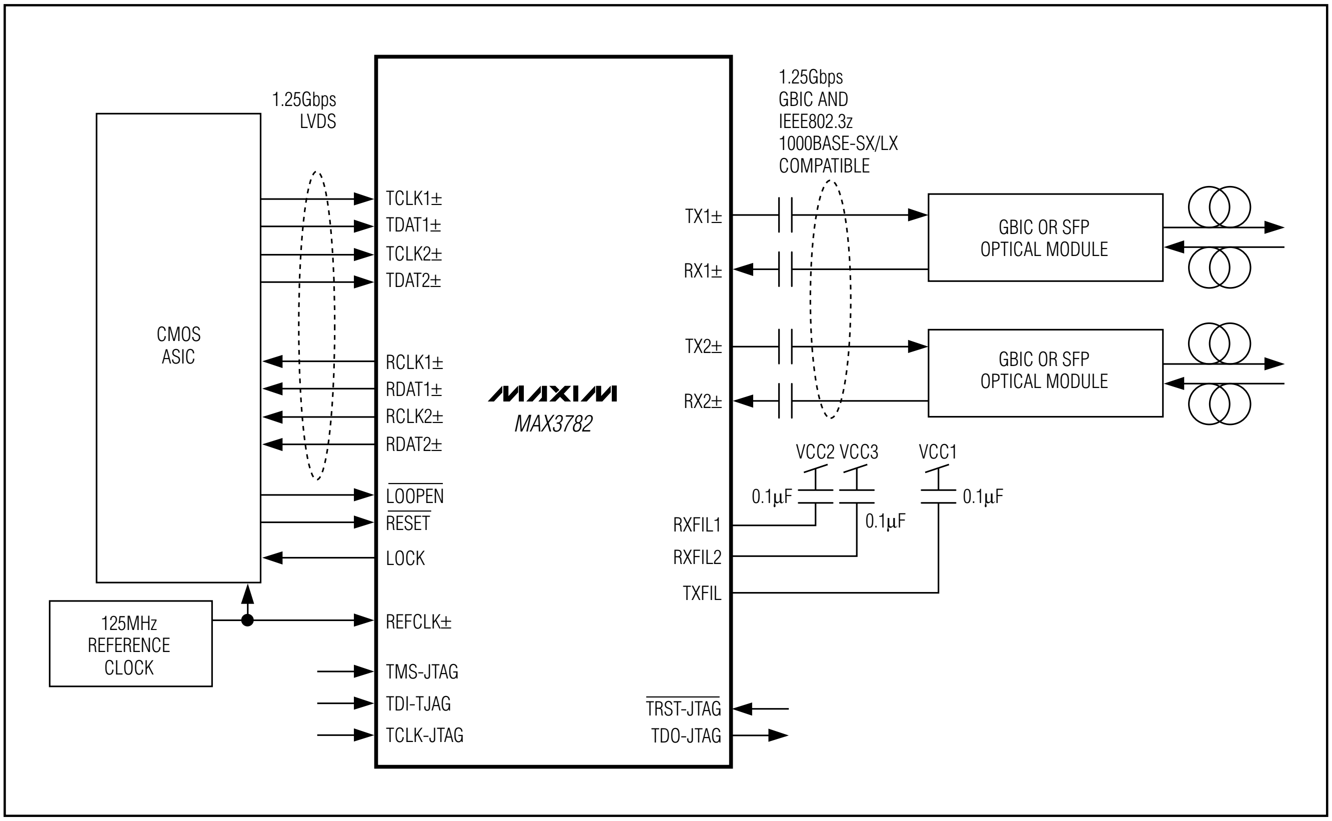
Chip Information

TRANSISTOR COUNT: 14329

PROCESS: Silicon bipolar

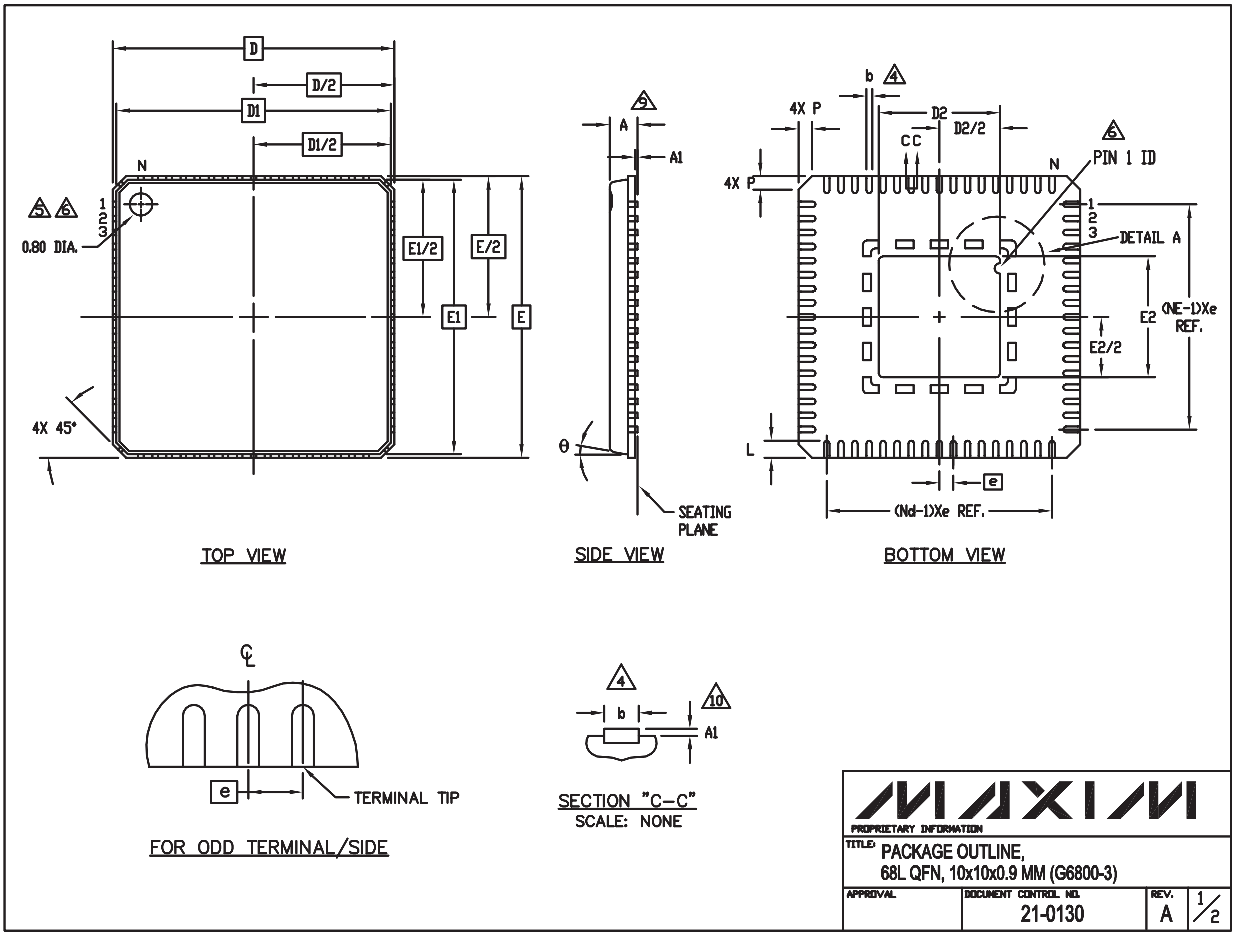
Dual 1.25Gbps Transceiver

Typical Application Circuit



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



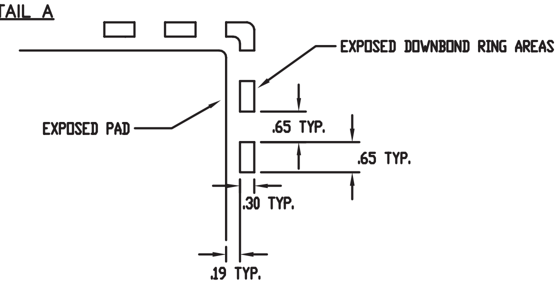
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	–	0.90	1.00	
A1	0.00	0.01	0.05	11
b	0.18	0.23	0.30	4
D		10.00 BSC		
D1		9.75 BSC		
e		0.50 BSC		
E		10.00 BSC		
E1		9.75 BSC		
L	0.50	0.60	0.75	
N		68		3
Nd		17		3
Ne		17		3
θ	0		12°	
P	0	0.42	0.60	
D2	4.40	4.55	4.70	
E2	4.40	4.55	4.70	

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.10mm.
9. APPLIES TO EXPOSED SURFACE OF PADS AND TERMINALS.
10. APPLIES ONLY TO TERMINALS.

DETAIL A



MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 68L QFN, 10x10x0.9 MM (G6800-3)
APPROVAL | DOCUMENT CONTROL NO. 21-0130 | REV. A | 2/2