INA849 Ultra-Low-Noise (1 nV/√Hz), High-Bandwidth, Instrumentation Amplifier

1 Features

- Ultra-low noise: 1-nV/√Hz input voltage noise (typical)
- Precision super-beta input performance:
  - Low offset voltage: 35 µV (maximum)
  - Low offset voltage drift: 0.4 µV/°C (maximum)
  - Low input bias current: 20 nA (maximum)
  - Low gain drift: 5 ppm/°C for G = 1 (maximum)
- Bandwidth: 28 MHz (G = 1), 8 MHz (G = 100)
- Slew rate: 35 V/µs
- Common-mode rejection: 120 dB (minimum) for maximum gain
- Supply range:
  - Single supply: 8 V to 36 V
  - Dual supply: ±4 V to ±18 V
- Specified temperature range: –40°C to +125°C
- Package: 8-pin SOIC

2 Applications

- Analog input module
- Microphone preamplifier
- Flow transmitter
- Battery test
- LCD test
- Electrocardiogram (ECG)
- Surgical equipment
- Process analytics (pH, gas, concentration, force and humidity)

3 Description

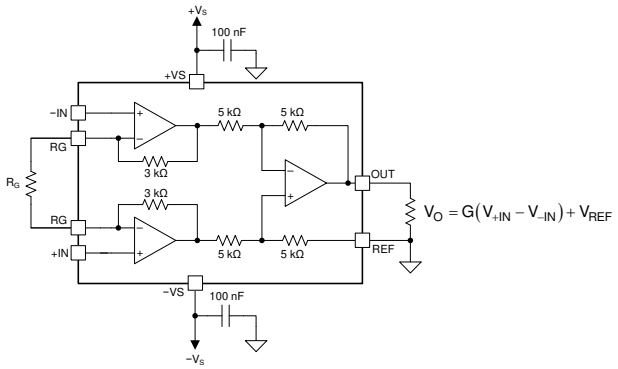
The INA849 is an ultra-low noise instrumentation amplifier optimized for maximum accuracy in high-resolution systems and operation over a wide single-supply or dual-supply range. The device offers significantly lower input bias current than competitors as a result of Super-beta input transistors. A state-of-the-art manufacturing process provides exceptionally low voltage noise, input offset voltage, and offset voltage drift.

Precisely matched integrated resistors provide a high, 92-dB (G = 1) common-mode rejection across the full input common-mode range. A single external resistor sets any gain from 1 to 10,000. The current-feedback topology of the INA849 provides wide bandwidth at higher gains for very-small, fast-moving signals. For example, the device provides 8 MHz of bandwidth at G = 100, and 28 MHz at a G = 1, with a fast 0.4-µs settling time (0.01%) for directly driving high-resolution, analog-to-digital converters (ADCs).

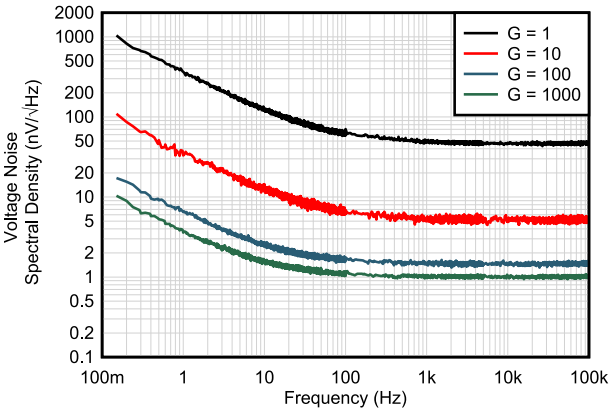
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
INA849	SOIC (8)	4.90 mm × 3.91 mm
	MSOP (8) (Preview)	3.00 mm x 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



INA849 Simplified Internal Schematic



Input-Referred Voltage Noise Spectral Density vs Frequency

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4 Revision History

Changes from Revision * (November 2020) to Revision A (December 2020)	Page
• Changed INA849 device from advanced information (preview) to production data (active)	1
• Added preview DGK package and associated content	1

5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA159	G = 0.2 V differential amplifier for ±10-V to 3-V and 5-V conversion	G = 0.2 V/V	N/A
INA819	35-µV offset, 0.4-µV/°C V_{OS} drift, 8-nV/√Hz noise, low-power, precision instrumentation amplifier	G = 1 + 50 kΩ / RG	2, 3
INA818	35-µV offset, 0.4-µV/°C V_{OS} drift, 8-nV/√Hz noise, low-power, precision instrumentation amplifier	G = 1 + 50 kΩ / RG	1, 8
INA821	35-µV offset, 0.4-µV/°C V_{OS} drift, 7-nV/√Hz noise, high-bandwidth, precision instrumentation amplifier	G = 1 + 49.4 kΩ / RG	2, 3
INA828	50-µV offset, 0.5-µV/°C V_{OS} drift, 7-nV/√Hz noise, low-power, precision instrumentation amplifier	G = 1 + 50 kΩ / RG	1, 8
INA333	25-µV V_{OS}, 0.1-µV/°C V_{OS} drift, 1.8-V to 5-V, RRO, 50-µA I_Q, chopper-stabilized INA	G = 1 + 100 kΩ / RG	1, 8
INA848	Ultra-low-noise (1.5-nV/√Hz), high-bandwidth instrumentation amplifier with fixed gain of 2000	G = 2000 V/V	N/A
PGA280	Zero-drift, high-voltage programmable gain instrumentation amplifier with signal integrity test capability (overload detection, input switch matrix, wire break test, SPI with checksum, GPIO ports)	Digitally programmable	N/A
PGA112	Precision programmable gain op amp with SPI	Digitally programmable	N/A

6 Pin Configuration and Functions

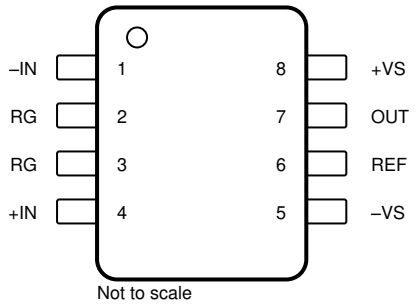


Figure 6-1. D Package (8-Pin SOIC) and DGK Package (8-Pin MSOP, Preview), Top View

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	1	I	Negative (inverting) input
+IN	4	I	Positive (noninverting) input
OUT	7	O	Output
RG	2, 3	—	Gain setting pin. Place a gain resistor between pin 2 and pin 3.
REF	6	I	Reference input. This pin must be driven by a low impedance source.
–VS	5	—	Negative supply
+VS	8	—	Positive supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply, $V_S = (+V_S)$		40	V
		Dual supply, $V_S = (+V_S) – (–V_S)$		±20	
V_I	Signal input pins	Voltage	$(–V_S) – 0.5$	$(+V_S) + 0.5$	V
		Current	–10	+10	mA
	Signal differential input voltage	Gain ≤ 4	$–V_S$	$+V_S$	V
		4 < Gain < 50	$(–V_S)$ / Gain	$(+V_S)$ / Gain	
		Gain > 50	–1 V	+1 V	
V_{REF}	Reference input voltage		$(–V_S) – 0.5$	$(+V_S) + 0.5$	V
V_O	Signal output voltage		$(–V_S) – 0.5$	$(+V_S) + 0.5$	V
I_S	Output short-circuit(2)		Continuous		
T_A	Operating temperature(3)		–40	125	°C
T_J	Junction temperature(3)		–40	175	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2.
(3) As a result of the quiescent current, the supply voltage and load-dependent self-heating of the device must be considered.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply, $V_S = (+V_S)$	8	36	V
		Dual supply, $V_S = (+V_S) – (–V_S)$	±4	±18	
T_A	Specified temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		INA849 D (SOIC) 8 PINS	INA849 DGK (MSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.6	168.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	61.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.9	90.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.5	8.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.4	88.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, connected to ground, V_{REF} = 0 V, V_{CM} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{OSI}	Input stage offset voltage[1] [3]			10	35	µV
		T_A = –40°C to +125°C[2]			75	
	Input stage offset voltage drift	T_A = –40°C to +125°C		0.1	0.4	µV/°C
V_{OSO}	Output stage offset voltage[1] [3]			50	500	µV
		T_A = –40°C to +125°C[2]			2000	
	Output stage offset voltage drift	T_A = –40°C to +125°C[2]			15	µV/°C
PSRR	Power-supply rejection ratio	G = 1, RTI	106	120		dB
		G = 10, RTI	114	130		
		G = 100, RTI	124	131		
		G = 1000, RTI	125	131		
Z_{in}	Input impedance			1 || 7		GΩ || pF
	RFI filter, –3-dB frequency			220		MHz
V_{CM}	Operating input range[4]		(–V_S) + 2.5		(+V_S) – 2.5	V
		V_S = ±4 V to ±18 V	See Figure 8-2 and Figure 8-3			
CMRR	Common-mode rejection ratio	At dc to 60 Hz, RTI, V_{CM} = (V–) + 2.5 V to (V+) – 2.5 V, G = 1	92	110		dB
		At dc to 60 Hz, RTI, V_{CM} = (V–) + 2.5 V to (V+) – 2.5 V, G = 10	112	125		
		At dc to 60 Hz, RTI, V_{CM} = (V–) + 2.5 V to (V+) – 2.5 V, G = 100	120	127		
		At dc to 60 Hz, RTI, V_{CM} = (V–) + 2.5 V to (V+) – 2.5 V, G = 1000	120	127		
BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2			20	nA
	Input bias current drift	T_A = –40°C to +125°C		10	80	pA/°C
I_{OS}	Input offset current	V_{CM} = V_S / 2			6	nA
	Input offset current drift	T_A = –40°C to +125°C		5		pA/°C

7.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, connected to ground, V_{REF} = 0 V, V_{CM} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NOISE VOLTAGE						
e_{NI}	Input stage voltage noise(8)	f = 1 kHz, G = 1000, R_S = 0 Ω		1		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 1000, R_S = 0 Ω		0.06		μV_{PP}
e_{NO}	Output stage voltage noise(8)	f = 1 kHz, R_S = 0 Ω		45		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, R_S = 0 Ω		5		μV_{PP}
I_n	Current noise	f = 1 kHz		1.6		pA/√Hz
		f_B = 0.1 Hz to 10 Hz		100		pA_{PP}
GAIN						
G	Gain equation			1 + (6 kΩ / R_G)		V/V
	Gain		1		10000	V/V
GE	Gain error (7)	G = 1, V_O = ±10 V		±0.005	±0.025	%
		G = 10, V_O = ±10 V		±0.025	±0.1	
		G = 100, V_O = ±10 V		±0.025	±0.1	
		G = 1000, V_O = ±10 V		±0.05		
	Gain drift(5)	G = 1, T_A = –40°C to +125°C			±5	ppm/°C
		G > 1, T_A = –40°C to +125°C			±35	
	Gain nonlinearity	G = 1, V_O = –10 V to +10 V		3		ppm
		G = 10(6), V_O = –10 V to +10 V		10		
THD	Total harmonic distortion	f = 1 kHz, V_O = 10 V_{PP}		127		dBc
HD2	Second-order harmonic distortion	f = 1 kHz, V_O = 10 V_{PP}		127		dBc
HD3	Third-order harmonic distortion	f = 1 kHz, V_O = 10 V_{PP}		157		dBc
THD	Total harmonic distortion	f = 10 kHz, V_O = 10 V_{PP}		119		dBc
HD2	Second-order harmonic distortion	f = 10 kHz, V_O = 10 V_{PP}		130		dBc
HD3	Third-order harmonic distortion	f = 10 kHz, V_O = 10 V_{PP}		120		dBc
OUTPUT						
	Voltage swing	R_L = 10 kΩ	(V–) + 0.15		(V+) – 0.15	V
	Load capacitance stability			200		pF
Z_O	Closed-loop output impedance	f = 1 MHz		1.5		Ω
I_{SC}	Short-circuit current	Continuous to V_S / 2		±34		mA
FREQUENCY RESPONSE						
BW	Bandwidth, –3 dB	G = 1		28		MHz
		G = 10		13		
		G = 100		8		
		G = 1000		1.25		
SR	Slew rate	G = 1, V_{STEP} = 10 V		35		V/µs
t_S	Settling time	0.01%, G = 1 to 100, V_{STEP} = 10 V		0.4		µs
		0.01%, G = 1000, V_{STEP} = 10 V		0.4		
		0.001%, G = 1 to 100, V_{STEP} = 10 V		0.6		
		0.001%, G = 1000, V_{STEP} = 10 V		1.5		

7.5 Electrical Characteristics (continued)

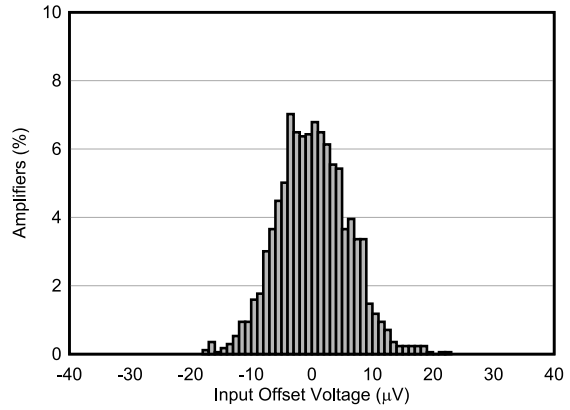
at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, connected to ground, V_{REF} = 0 V, V_{CM} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE INPUT						
R_{IN}	Input impedance			10		kΩ
	Input current			80		µA
	Reference input voltage		(V–)		(V+)	V
	Gain to output			1		V/V
	Reference gain error	V_O = ±10 V, inside the voltage swing range		0.01	0.05	%
POWER SUPPLY						
I_Q	Quiescent current (7)	V_{IN} = 0 V		6.2	6.6	mA
		T_A = –40°C to +125°C			8.9	

(1) Total offset, referred-to-input (RTI): $V_{OS} = (V_{OSI}) + (V_{OSO} / G)$.
(2) Specified by characterization. Not tested in production.
(3) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}^2 + (\Delta V_{OSO} / G)^2]}$.
(4) Input voltage range of the input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage; see Figure 7-12.
(5) The values specified for G > 1 do not include the effects of the external gain resistor, R_G.
(6) Thermal effects can degrade input stage nonlinearity and thus can scale with gain; See Figure 9-5.
(7) This parameter is tested in a high speed automatic test environment and does not measure the thermal effects with a longer a time constant. The thermal effect depends on supply voltage, layout, heat sinking and air flow conditions.
(8) Total RTI voltage noise is equal to: $e_{N(RTI)} = \sqrt{[e_{NI}^2 + (e_{NO} / G)^2]}$.

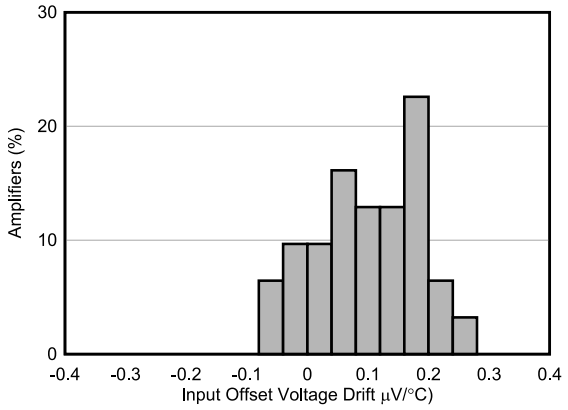
7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, V_{CM} at mid-supply, VR_L = 10 kΩ, connected to ground, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



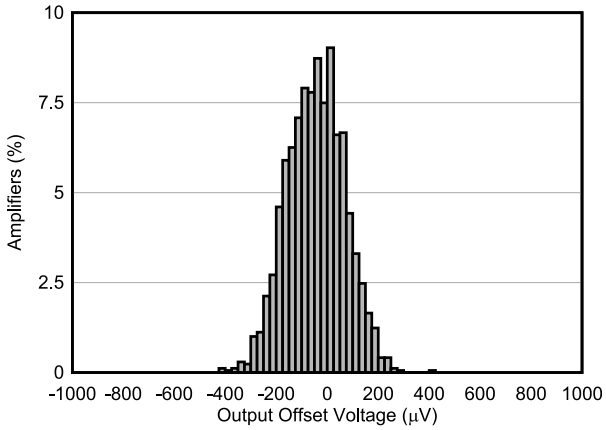
N = 1695, mean = 0.26 µV, std dev = 5.85 µV

Figure 7-1. Typical Distribution of Input Offset Voltage



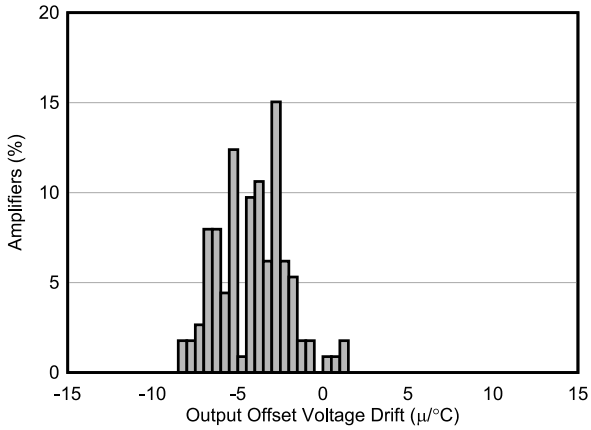
N = 30, mean = 0.10 µV/°C, std dev = 0.08 µV/°C

Figure 7-2. Typical Distribution of Input Offset Voltage Drift



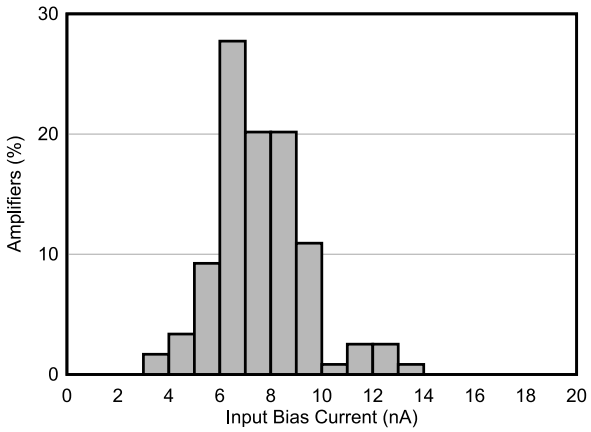
N = 1695, mean = -43.83 µV, std dev = 111.74 µV

Figure 7-3. Typical Distribution of Output Offset Voltage



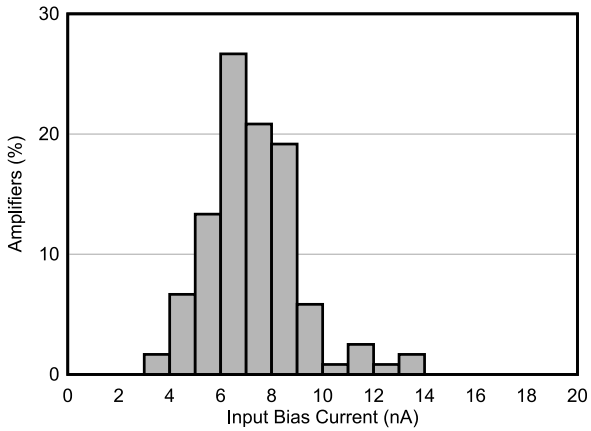
N = 120, mean = -4.14 µV/°C, std dev = 2.00 µV/°C

Figure 7-4. Typical Distribution of Output Offset Voltage Drift



N = 120, mean = 7.58 nA, std dev = 1.84 nA

Figure 7-5. Typical Distribution of Input Bias Current

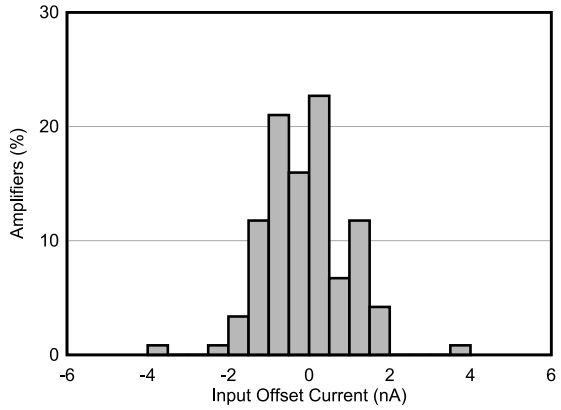


N = 120, mean = 7.24 nA, std dev = 1.80 nA

Figure 7-6. Typical Distribution of Input Bias Current at 85°C

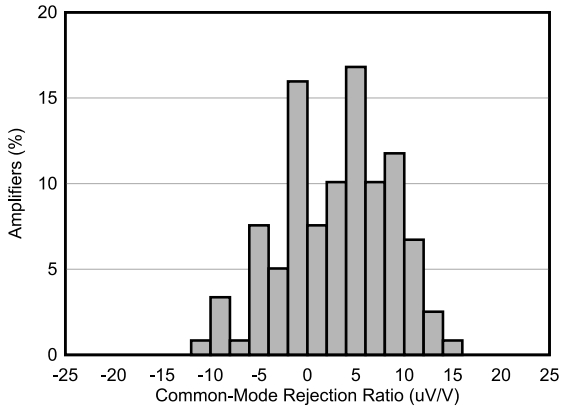
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} at mid-supply, VR_L = 10 kΩ, connected to ground, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



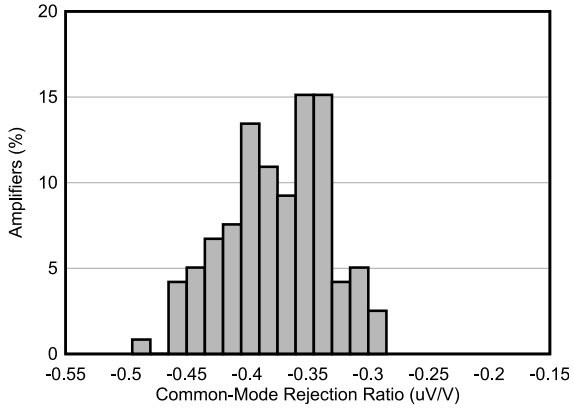
N = 120, mean = -0.11 nA, std dev = 1.01 nA

Figure 7-7. Typical Distribution of Input Offset Current



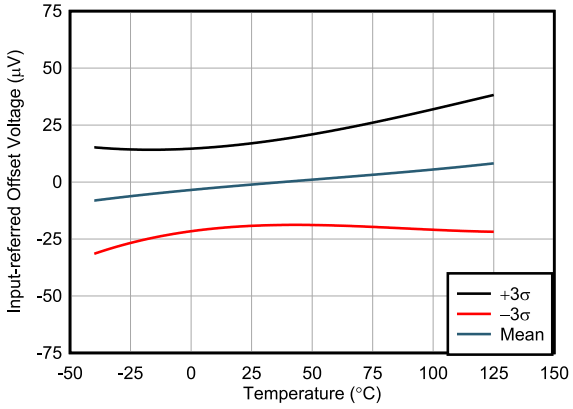
N = 120, mean = 3.08 µV/V, std dev = 5.57 µV/V

Figure 7-8. Typical CMRR Distribution G = 1



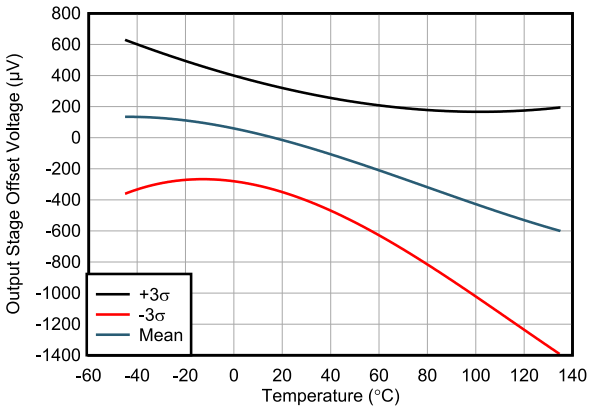
N = 120, mean = -0.375 µV/V, std dev = 0.043 µV/V

Figure 7-9. Typical CMRR Distribution G = 100



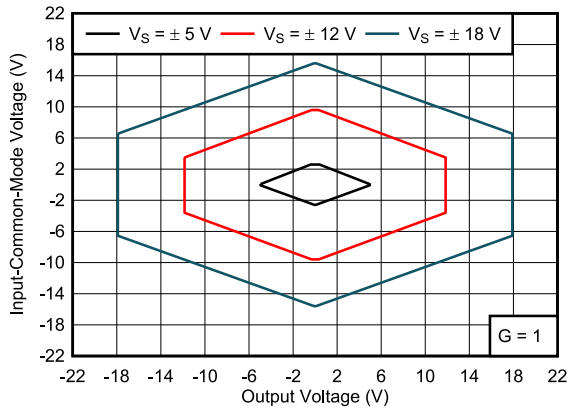
N = 120

Figure 7-10. Input Stage Offset Voltage vs Temperature



N = 120

Figure 7-11. Output Stage Offset Voltage vs Temperature



VREF = 0 V

Figure 7-12. Boundary Plot - Input Common-Mode Voltage vs Output Voltage

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} at mid-supply, VR_L = 10 kΩ, connected to ground, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

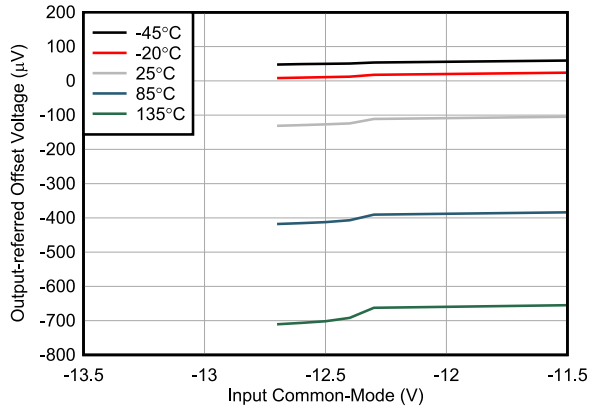


Figure 7-13. Output-referred Offset Voltage vs Negative Input Common-Mode Voltage

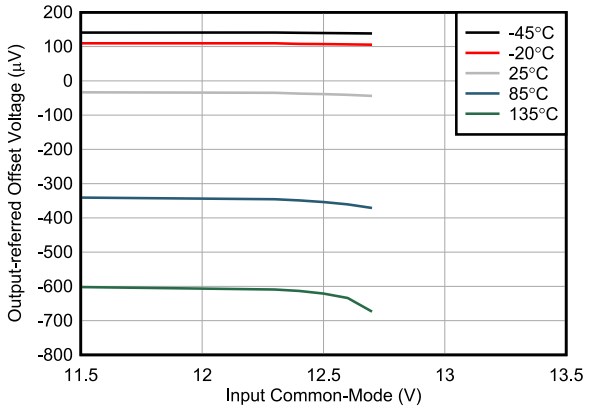


Figure 7-14. Output-referred Offset Voltage vs Positive Input Common-Mode Voltage

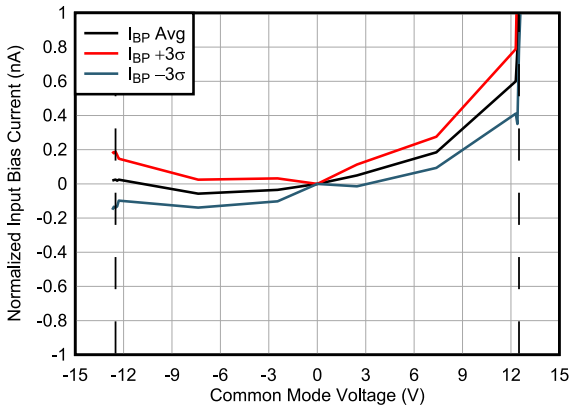


Figure 7-15. Positive Input Bias Current vs Input Common-Mode Voltage

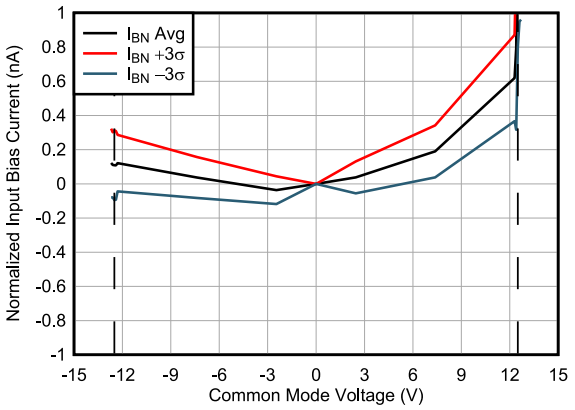


Figure 7-16. Negative Input Bias Current vs Input Common-Mode Voltage

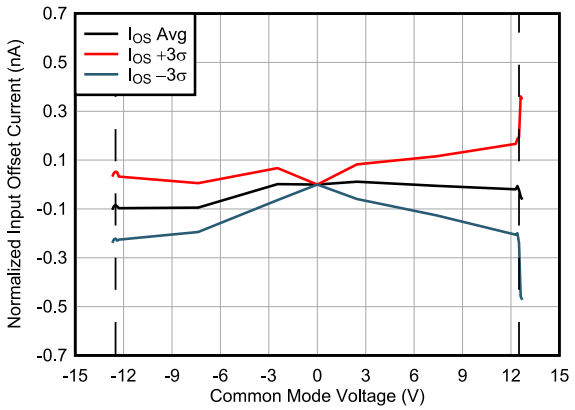


Figure 7-17. Input Offset Current vs Input Common-Mode Voltage

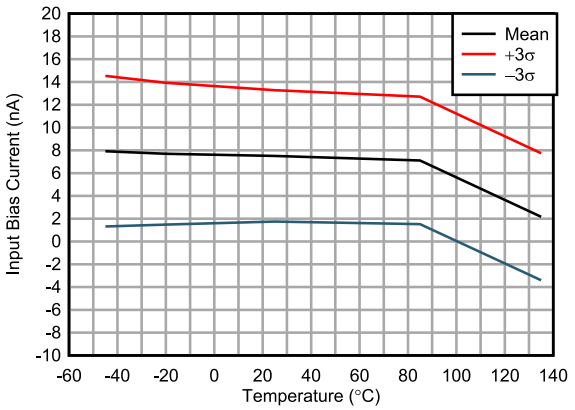


Figure 7-18. Input Bias Current vs Temperature

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} at mid-supply, VR_L = 10 kΩ, connected to ground, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

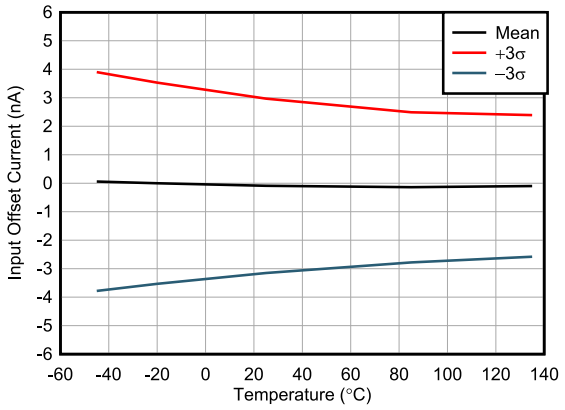


Figure 7-19. Input Offset Current vs Temperature

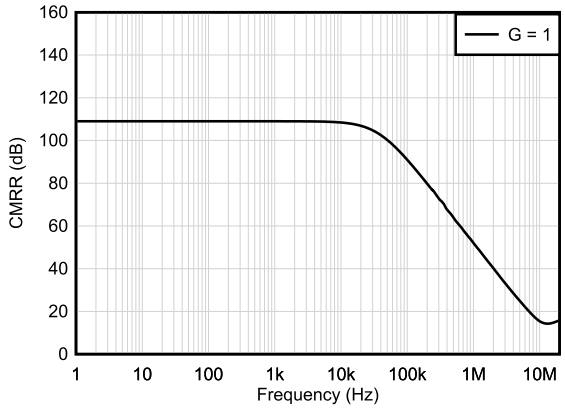


Figure 7-20. CMRR vs Frequency (RTI)

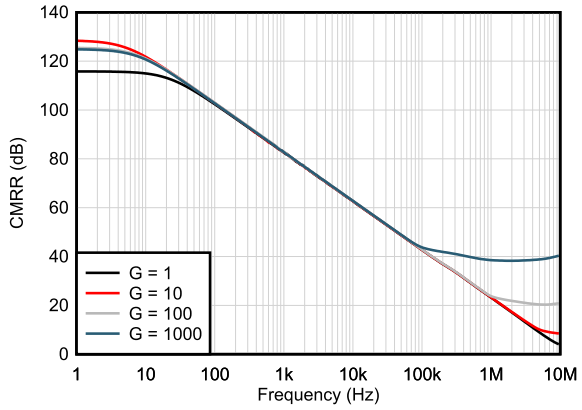


Figure 7-21. CMRR vs Frequency (1-kΩ source imbalance)

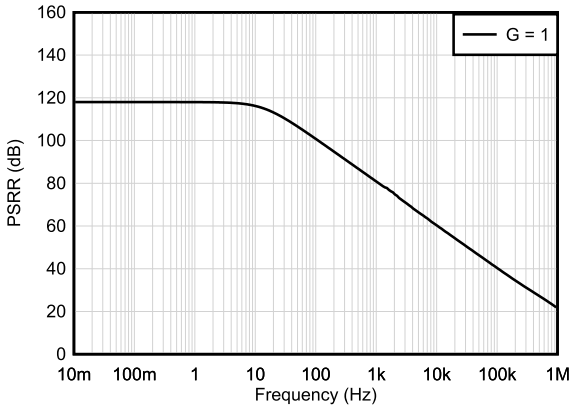


Figure 7-22. Positive PSRR vs Frequency (RTI)

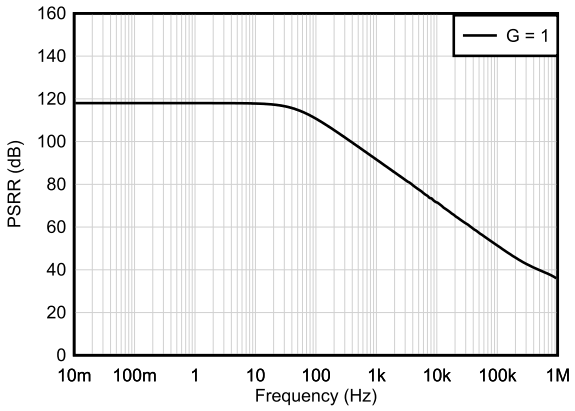


Figure 7-23. Negative PSRR vs Frequency (RTI)

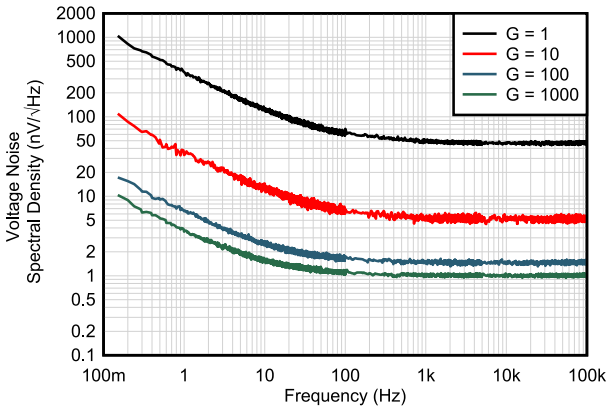


Figure 7-24. Voltage Noise Spectral Density vs Frequency (RTI)

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} at mid-supply, VR_L = 10 kΩ, connected to ground, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

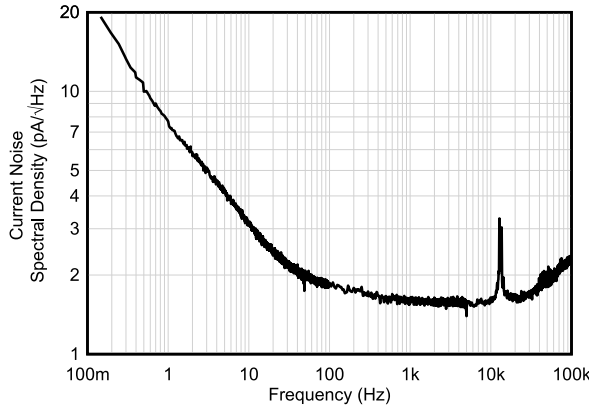


Figure 7-25. Current Noise Spectral Density vs Frequency (RTI)

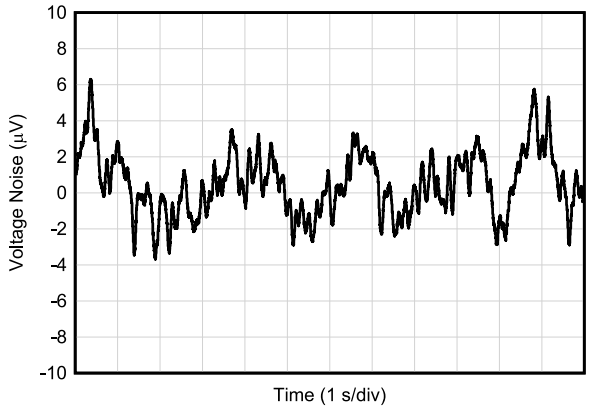


Figure 7-26. 0.1-Hz to 10-Hz RTI Voltage Noise

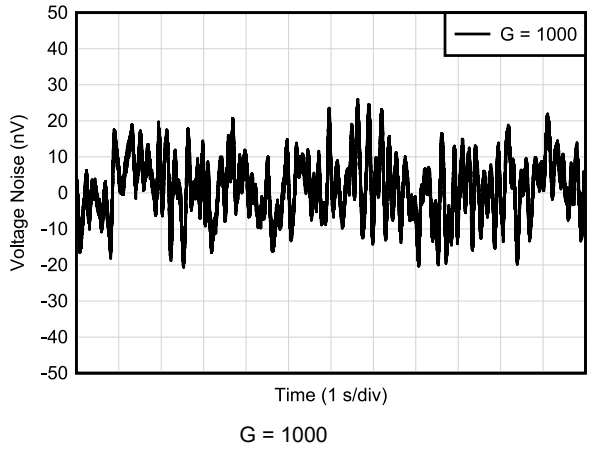


Figure 7-27. 0.1-Hz to 10-Hz RTI Voltage Noise

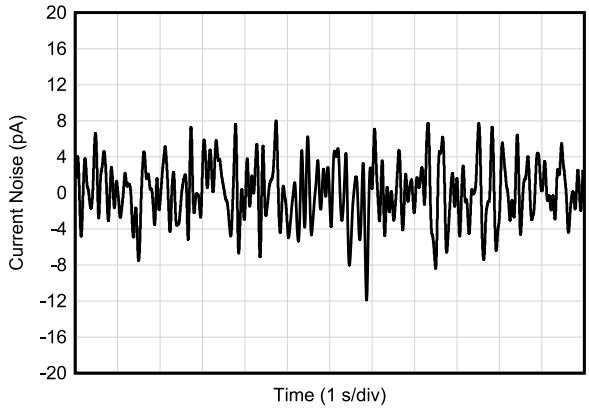


Figure 7-28. 0.1-Hz to 10-Hz RTI Current Noise

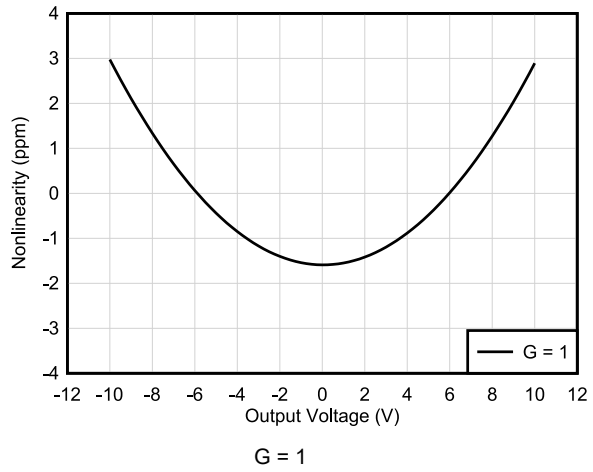


Figure 7-29. Gain Nonlinearity vs Output Voltage

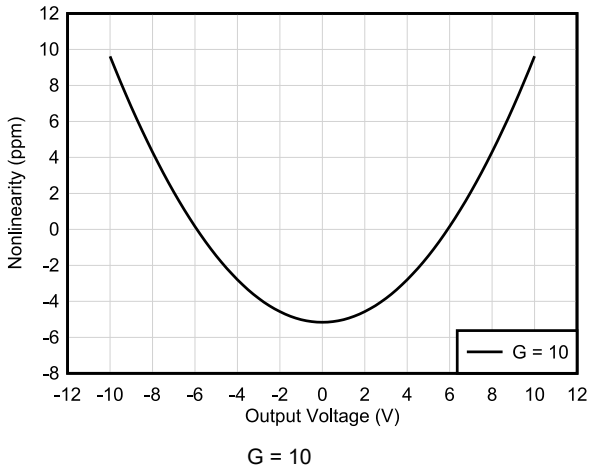


Figure 7-30. Gain Nonlinearity vs Output Voltage

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} at mid-supply, VR_L = 10 kΩ, connected to ground, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

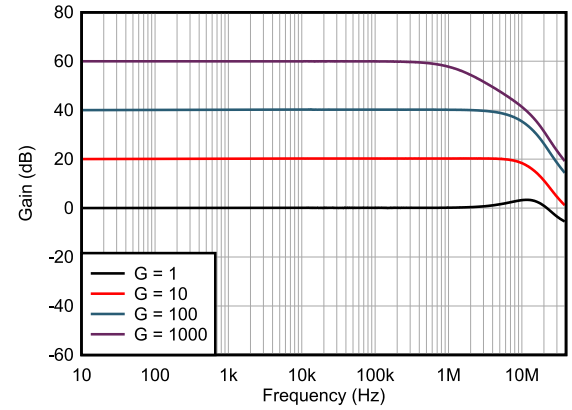


Figure 7-31. Closed-Loop Gain vs Frequency

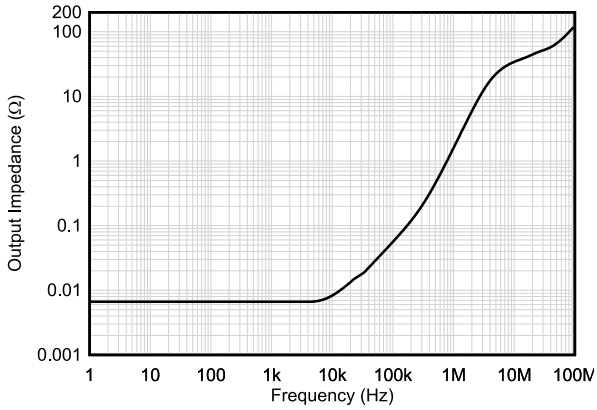


Figure 7-32. Closed-Loop Output Impedance vs Frequency

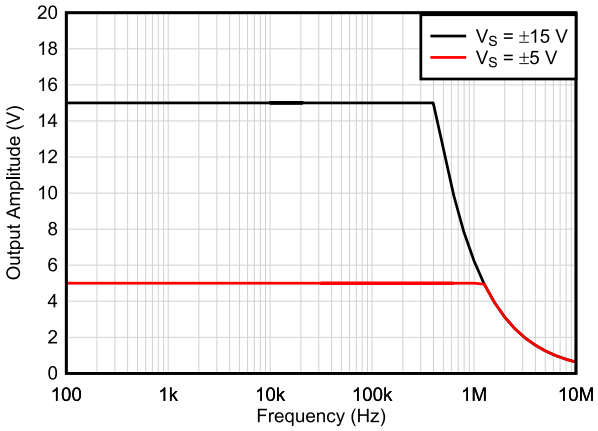


Figure 7-33. Large-Signal Frequency Response

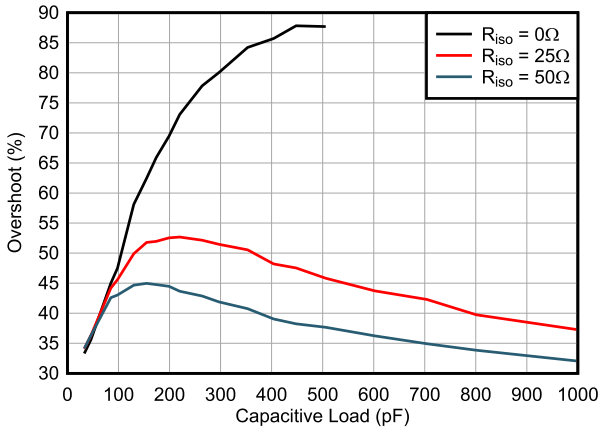
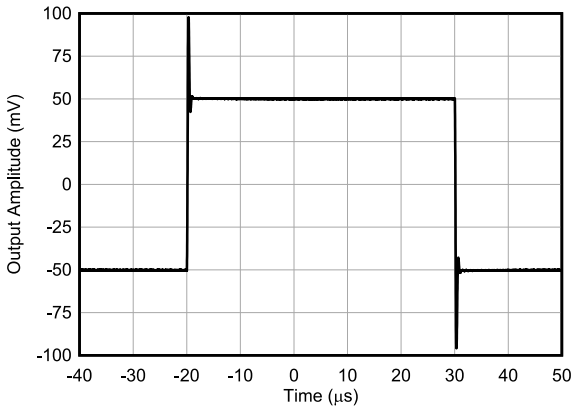
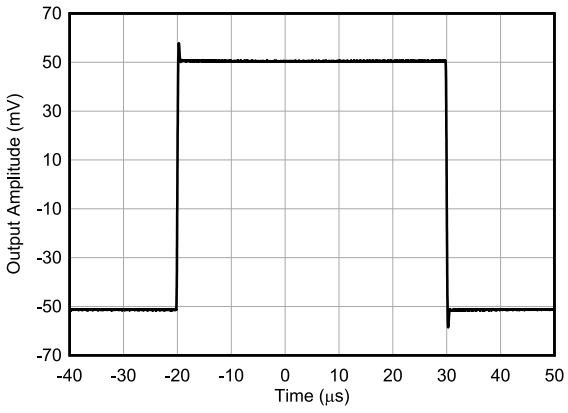


Figure 7-34. Overshoot vs Capacitive Loads



G = 1, C_L = 100 pF

Figure 7-35. Small-Signal Step Response at G = 1

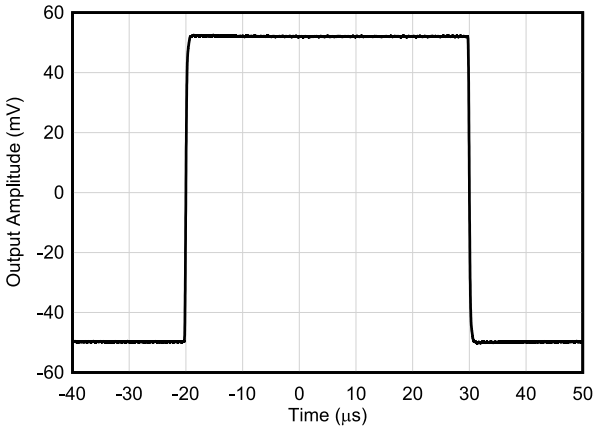


G = 10, C_L = 100 pF

Figure 7-36. Small-Signal Step Response at G = 10

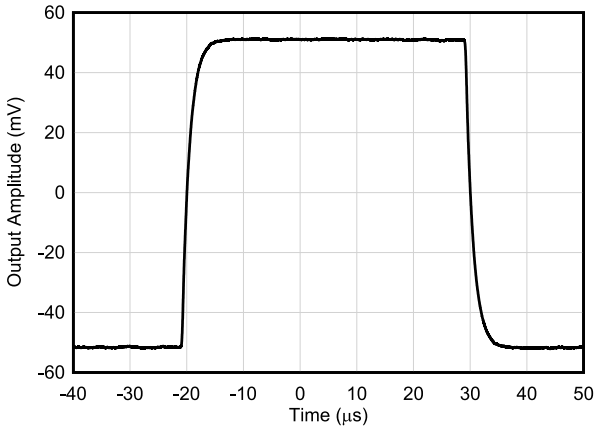
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} at mid-supply, VR_L = 10 kΩ, connected to ground, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



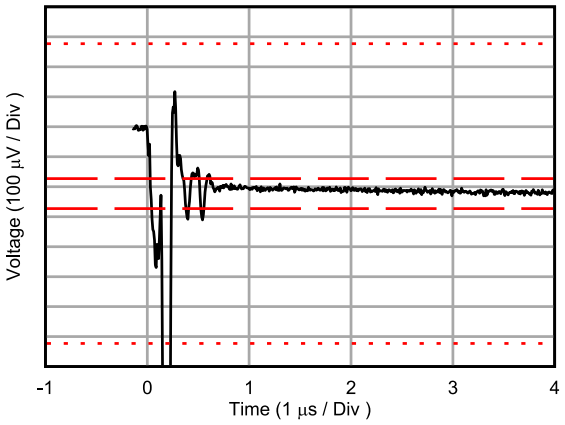
G = 100, C_L = 100 pF

Figure 7-37. Small-Signal Step Response at G = 100



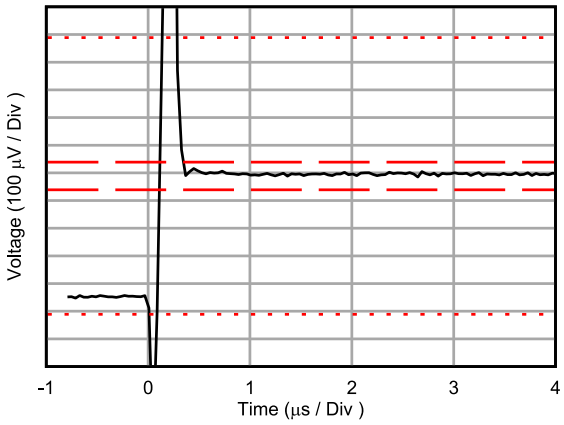
G = 1000, C_L = 100 pF

Figure 7-38. Small-Signal Step Response at G = 1000



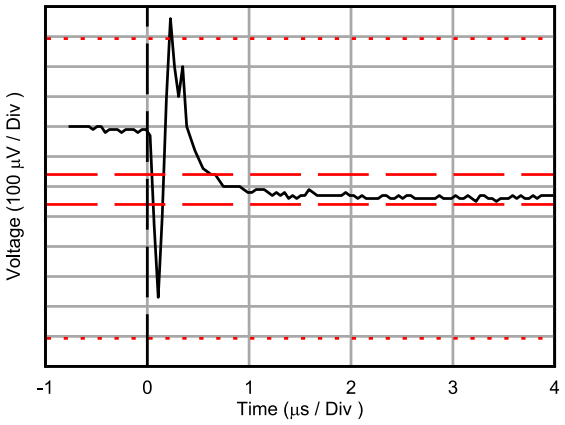
G = 1 V_{STEP} = 10 V

Figure 7-39. Settling Time for G = 1



G = 100 V_{STEP} = 10 V

Figure 7-40. Settling Time for G = 100



G = 1000 V_{STEP} = 10 V

Figure 7-41. Settling Time for G = 1000

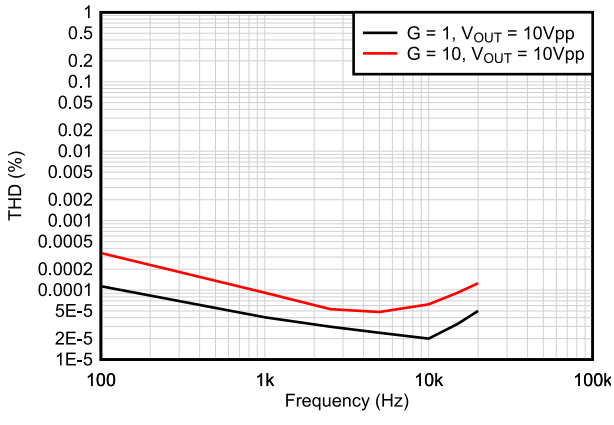


Figure 7-42. Total Harmonic Distortion vs Frequency

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} at mid-supply, VR_L = 10 kΩ, connected to ground, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

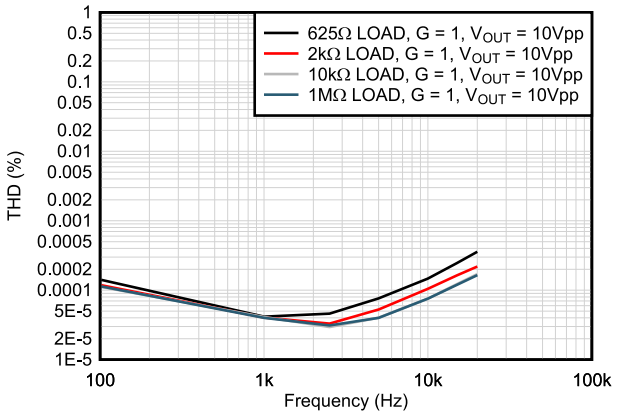


Figure 7-43. Total Harmonic Distortion vs Frequency at different Loads

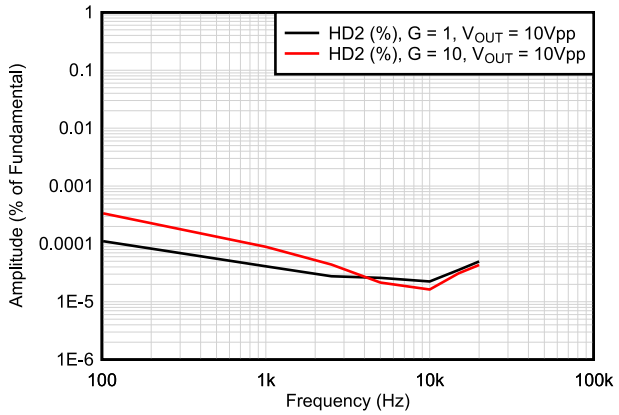


Figure 7-44. Second Harmonic Distortion vs Frequency

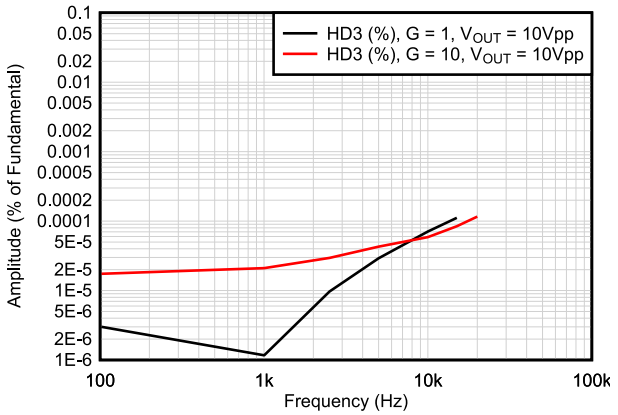


Figure 7-45. Third Harmonic Distortion vs Frequency

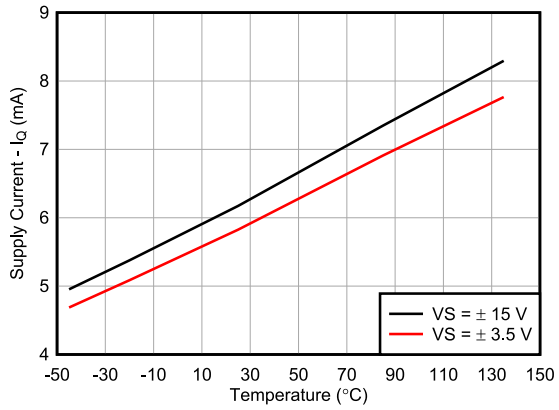


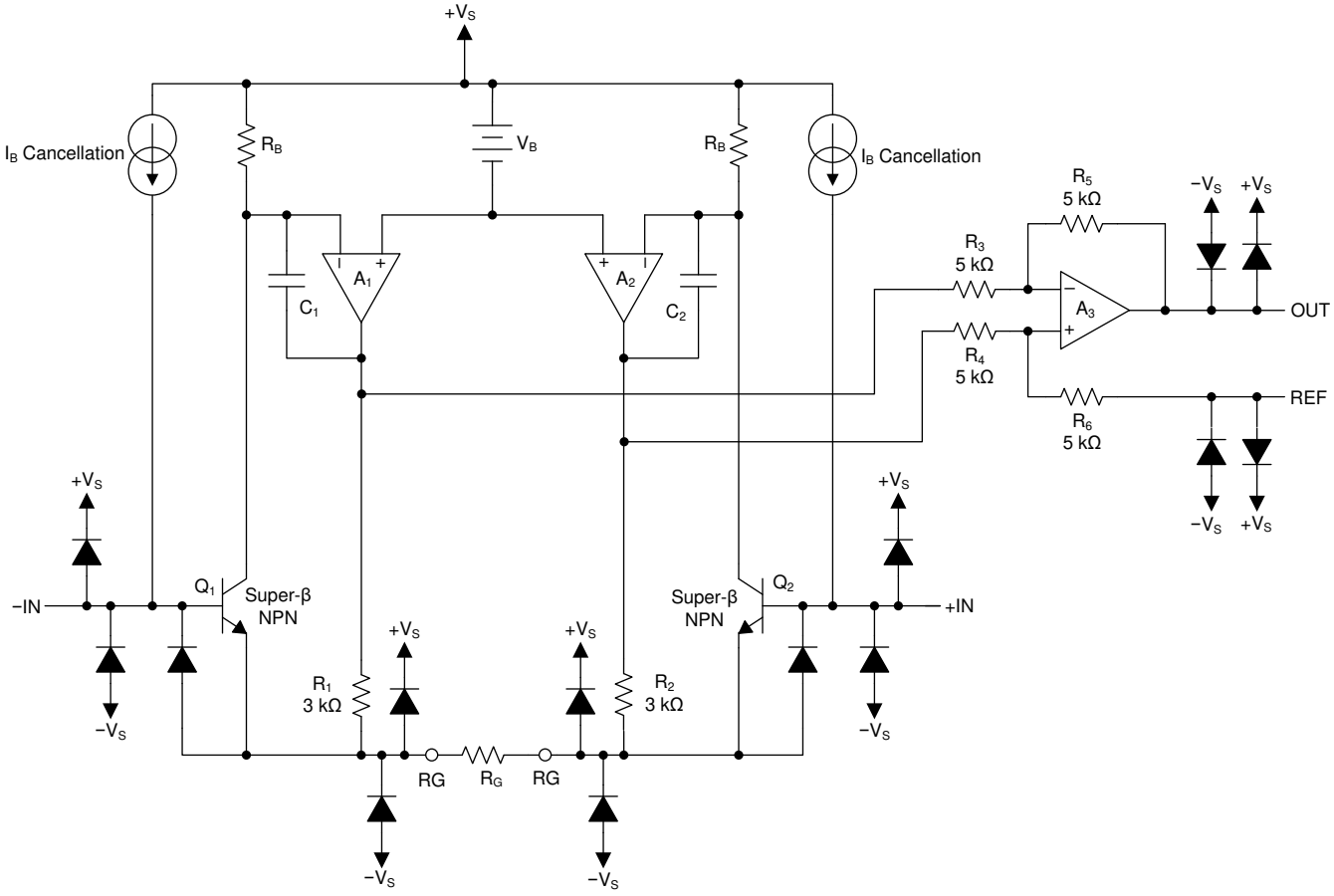
Figure 7-46. Supply Current vs Temperature

8 Detailed Description

8.1 Overview

The INA849 is a monolithic, precision, instrumentation amplifier that incorporates a current-feedback input stage and a four-resistor difference amplifier output stage. The functional block diagram in the next section shows how the differential input voltage is buffered by Q_1 and Q_2, and is forced across R_G, which causes a signal current to flow through R_G, R_1, and R_2. The output difference amplifier, A_3, removes the common-mode component of the input signal and refers the output signal to the REF pin. The V_{BE} and voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 0.8 V lower than the input voltages.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adjustable Gain Setting

Figure 8-1 shows that the gain of the INA849 is set by a single external resistor (R_G) connected between the RG pins (pins 2 and 3).

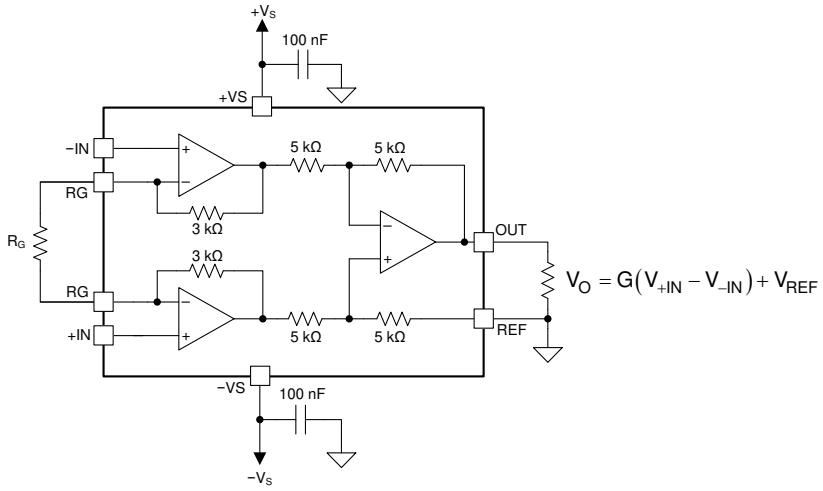


Figure 8-1. Simplified Diagram of the INA849 with Output Equation

The value of R_G is selected according to the following equation:

$$G = 1 + \frac{6\ k\Omega}{R_G} \quad (1)$$

Table 8-1 lists several commonly used gains and resistor values. The 6-kΩ term in Equation 1 is a result of the sum of the two internal 3-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate, absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA849.

Table 8-1. Commonly Used Gains and Resistor Values

DESIRED GAIN (V/V)	STANDARD 1% R_G (Ω)	CALCULATED GAIN (V/V)	CALCULATED GAIN ERROR (%)
1	Not connected	N/A	N/A
2	6.04 k	1.9933	0.33
5	1.50 k	5	0
10	665	10.022	–0.23
20	316	19.987	0.06
50	121	50.586	–1.17
100	60.4	100.337	–0.34
200	30.1	200.335	–0.17
500	12.1	496.867	0.63
1000	6.04	994.377	0.56

The 5-kΩ feedback resistors in the output stage are ratiometrically matched to achieve unity-gain stability. These resistors may shift up to 15% depending on production.

As shown in Figure 8-1 and explained in more detail in Figure 11-1, make sure to connect low-ESR, 0.1-µF, ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible.

8.3.2 Gain Drift

The stability and temperature drift of external gain setting resistor R_G also affects gain. The contribution of R_G to gain accuracy and drift is determined from Equation 1.

The best gain drift of 5 ppm/°C (maximum) is achieved when the INA849 uses G = 1 without R_G connected. In this case, gain drift is limited by the mismatch of the temperature coefficient of the integrated 5-kΩ resistors in differential amplifier A_3. At gains greater than 1, gain drift increases as a result of the individual drift of the 3-kΩ resistors in the feedback of A_1 and A_2, relative to the drift of external gain resistor R_G.

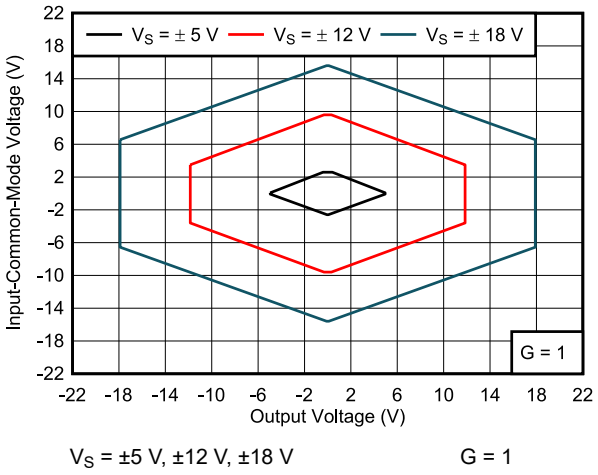
The low temperature coefficient of the internal feedback resistors improves the overall temperature stability of applications using gains greater than 1 V/V over alternate solutions.

The low resistor values required for high gain make wiring resistance an important consideration. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater.

To maintain stability, avoid parasitic capacitance of more than a few picofarads at R_G connections. Careful matching of any parasitics on the R_G pins maintains optimal CMRR over frequency.

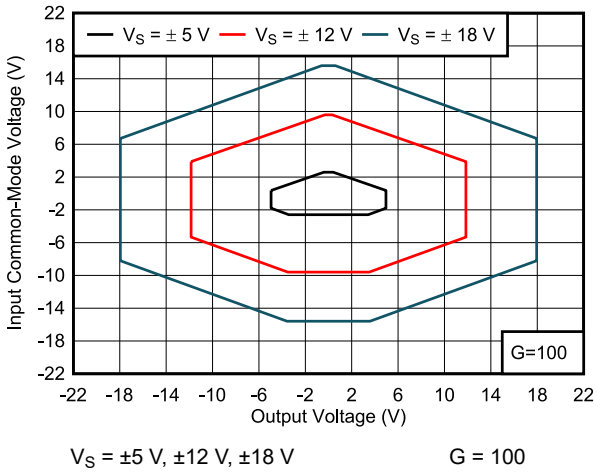
8.3.3 Wide Input Common-Mode Range

The linear input voltage range of the INA849 input circuitry extends within 2.5 V (maximum) of both power supplies, and maintains excellent common-mode rejection throughout this range. The common-mode range for the most common operating conditions are shown in Figure 8-2 and Figure 8-3. The common-mode range for other operating conditions is best calculated using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers*.



V_S = ±5 V, ±12 V, ±18 V G = 1

Figure 8-2. Input Common-Mode Voltage vs Output Voltage



V_S = ±5 V, ±12 V, ±18 V G = 100

Figure 8-3. Input Common-Mode Voltage vs Output Voltage

8.4 Device Functional Modes

The INA849 has a single functional mode and is operational when the power-supply voltage is greater than 8 V (±4 V). The maximum power-supply voltage for the INA849 is 36 V (±18 V).

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Reference Pin

The output voltage of the INA849 is developed with respect to the voltage on reference pin REF.

Use the REF pin to offset the output signal to a precise midsupply level. Typically, this offset is 2.5 V in a 5-V supply environment. To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA849 drives a single-supply analog-to-digital converter (ADC).

For dual-supply operation, the reference pin is typically connected to the low-impedance system ground.

The voltage source applied to the reference pin must have a low output impedance. As shown in Figure 9-1, any resistance at the reference pin (shown as R_{REF}) is in series with an internal 5-kΩ resistor that creates an imbalance in the four resistors of the internal difference amplifier.

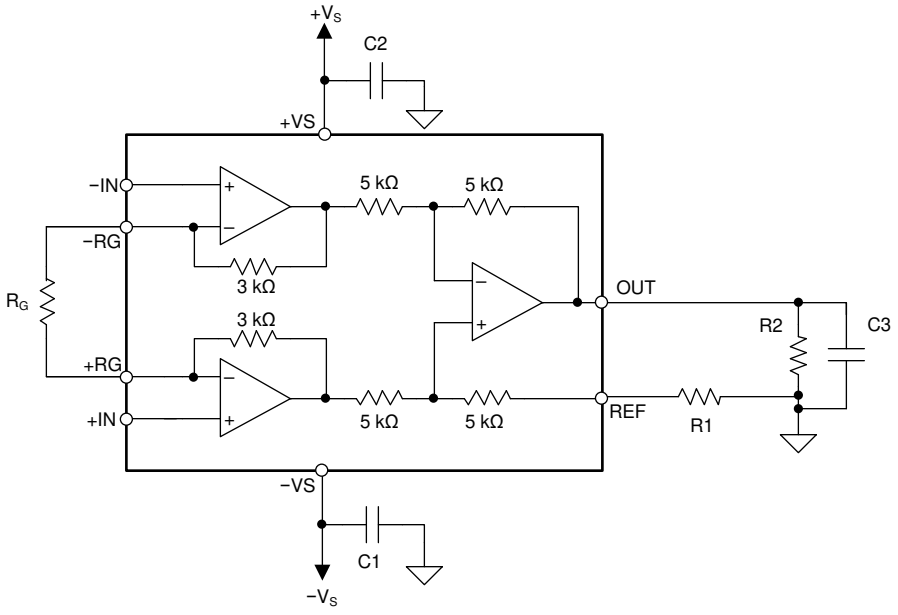


Figure 9-1. Parasitic Resistance Shown at the Reference Pin

This imbalance results in a degraded common-mode rejection ratio (CMRR). Figure 9-2 shows how the common-mode rejection ratio degrades depending on the source resistance on the reference pin. For best performance, keep the dc CMRR greater than 100 dB, by keeping the source impedance (represented as R1) to the REF pin to less than 0.1 Ω.

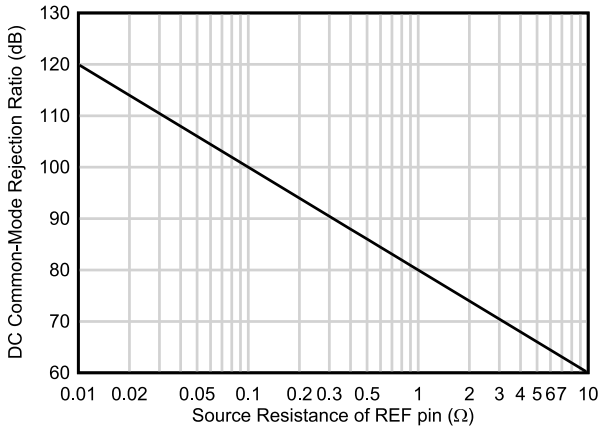


Figure 9-2. Effect of Parasitic Resistance at the Reference Pin

Voltage-reference devices are an excellent option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider generates a reference voltage, the divider must be buffered by an op amp (as Figure 9-3 shows) to avoid CMRR degradation.

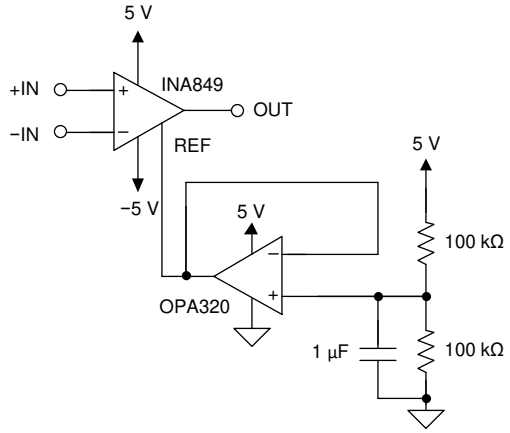
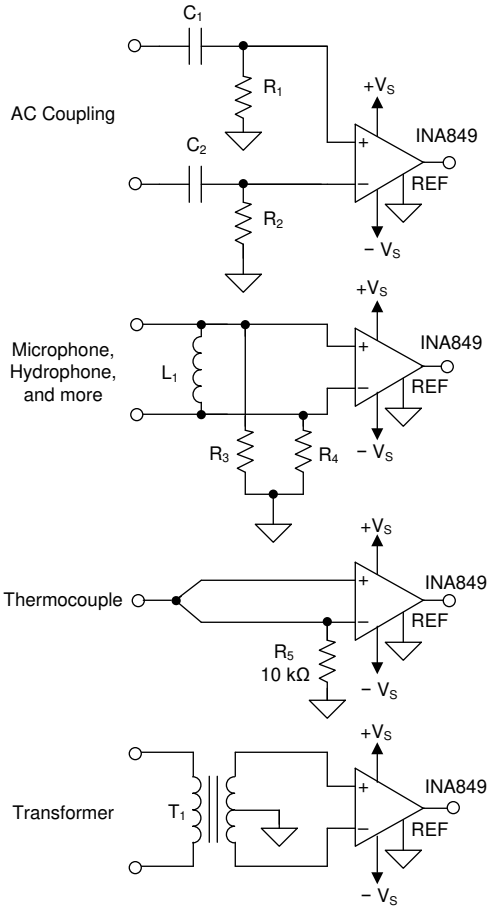


Figure 9-3. Using an Op Amp to Buffer Reference Voltages

9.1.2 Input Bias Current Return Path

The input impedance of the INA849 is extremely high (approximately 100 GΩ). However, a path must be provided for the input bias current of both inputs. This input bias current is typically 6 nA. High input impedance means that this input bias current changes little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 9-4 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA849, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path connects to one input (as shown in the thermocouple example). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current, and better high-frequency common-mode rejection.



NOTE: Center tap in the transformer provides bias current return.

Figure 9-4. Providing an Input Common-Mode Current Path

9.1.3 Thermal Effects due to Power Dissipation

The INA849 dissipates about 200 mW of power under quiescent conditions at a ±15-V supply voltage. The internal resistor network and output load drive causes an additional power dissipation that depends on the input signal. The small silicon area of the INA849 causes the internal circuitry to experience temperature gradients that might adversely affect the electrical performance.

Precision parameters, such as offset voltage, linearity, common-mode rejection ratio, and total harmonic distortion, can be impacted as a result of these thermal effects in the silicon. The thermal gradient particularly affects the performance of low-frequency input signals with higher gains (> 10) and large output voltage variation. As shown in the measurement Figure 9-5, the thermal effect can be minimized by lowering the supply voltage, if the application permits.

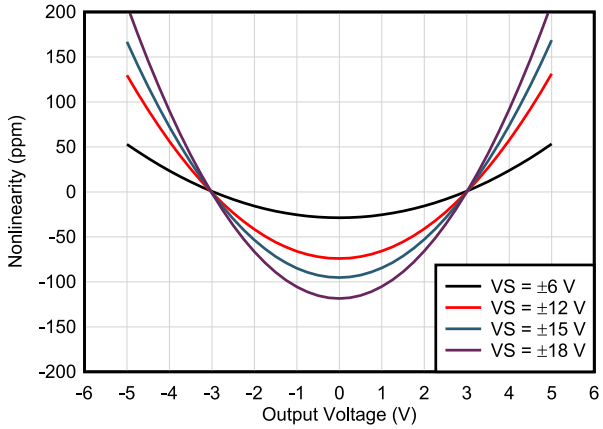


Figure 9-5. Linearity vs Supply Voltage for G=1000

9.2 Typical Application

9.2.1 Sensor Conditioning Circuit

Figure 9-6 shows a typical application for the INA849.

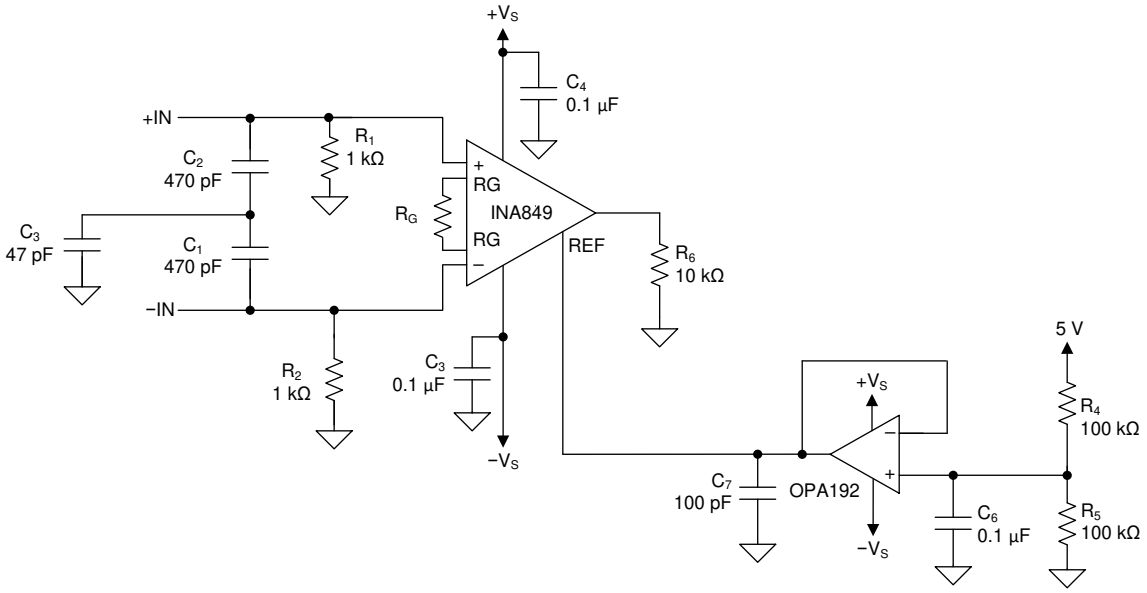


Figure 9-6. Sensor Conditioning Circuit

9.2.1.1 Design Requirements

For the typical application, the design requirements are:

- Power-supply voltage of V_S = ± 15 V
- AC-coupled input signal
  - Capacitor tolerance of 5%
- Reference voltage buffered to V_{REF} = 2.5 V
- Output range within 0 V to 5 V
- First-order filter stage with –3-dB frequency of 27 kHz

9.2.1.2 Detailed Design Procedure

If the instrumentation amplifier is used to drive ac-coupled input signals, an input bias current path must be provided as described in Section 9.1.2, represented with resistors R_1 and R_2 in Figure 9-6. For the selection of the resistor value, a trade-off must be made between input current noise that increases at lower values and input voltage noise that increases at higher values.

Section 9.1.1 states that the reference pin must be connected to a low-impedance reference, as shown in the application circuit example of the Sensor Conditioning Circuit. The reference pin must be connected to a 2.5-V reference voltage established through a high-resistive divider. The OPA192 helps to buffer the reference voltage. The effective output impedance of the OPA192 is derived as follows. The dc open-loop impedance of the OPA192 amplifier is approximately 3 kΩ. In a buffer configuration (A_V = 1), the output impedance of an amplifier degrades by the open-loop voltage gain. The OPA192 specifies a typical A_{OL} of 126 dB, thereby resulting in an output impedance of R_{OUT} = 1.5 mΩ.

9.2.2 Phantom Power in Microphone Preamplifier Circuit

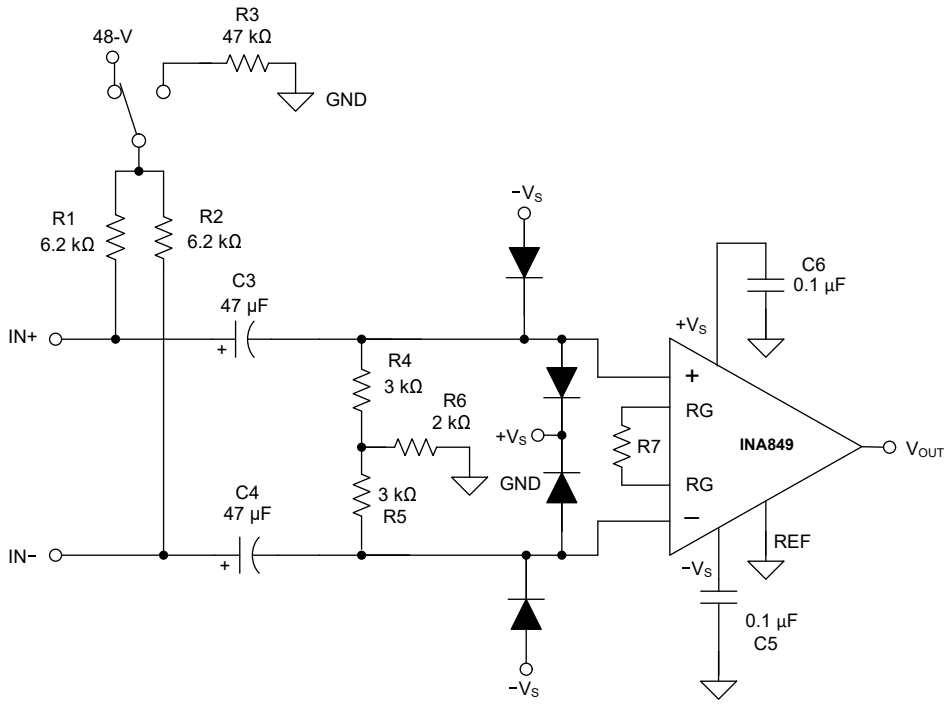


Figure 9-7. Phantom Power in Microphone Preamplifier Circuit

Figure 9-7 shows a typical application circuit for a microphone input amplifier used to generate phantom power. Phantom power is a technique to provide power and the audio signal using the same signal path.

R1 and R2 connected to the 48-V supply define the current path in the case when the microphone needs to be powered. C3 and C4 are therefore used as blocking capacitors to protect the INA849. In a fault scenario when the input connections are shorted a large surge current discharges the dc blocking capacitor through the shottky diodes. In case of a 48-V phantom power the surge current exceed 4 A for a short duration of time. It is recommended to use shottky diodes that are specified for at least 10 A surge current. Additional series resistance with the dc blocking capacitor limits the surge current but needs to be traded off as these add noise to the circuit.

One of the key criteria for high-performance microphones is to enable an optimum source impedance throughout the audible frequency range. The exceptional ultra-low noise performance of the INA849 permits direct input without the need for a transformer.

R4 and R5 in parallel with R1 and R2 provide the bias current path for the INA849. The input bias current (maximum of 20 nA) provides a dc differential input voltage that reflects as an voltage error on the output. To make sure that the thermal noise of these resistors does not dominate, use the lowest possible value resistors.

The mismatch of the input ac-coupling capacitors, C3 and C4, can reduce the common-mode rejection ratio significantly at low frequencies. An additional resistor R6 connected to both of the bias resistors R4 and R5 can mitigate this effect.

Use the TINA TI™ simulation software for a detailed analysis.

10 Power Supply Recommendations

The nominal performance of the INA849 is specified with a supply voltage of ±15 V and midsupply reference voltage. The device also operates using power supplies from ±4 V (8 V) to ±18 V (36 V) and non-midsupply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are shown in Section 7.6.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- To avoid converting common-mode signals into differential signals and thermal electromotive forces (EMFs), make sure that both input paths are symmetrical and well-matched for source impedance and capacitance.
- Place the external gain resistor close to the RG pins to keep the loop inductance as low as possible and to avoid a potential parasitic coupling path, but also so that capacitance mismatch between the RG pins is minimized.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF, ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device.
  - A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Keep traces as short as possible.
- Minimize the number of thermal junctions. Ideally, the signal path is routed within a single layer without vias.
- Keep sufficient distance from major thermal energy sources (circuits with high power dissipation). If not possible, place the device such that it matches the thermal energy source on the differential signal path.

11.2 Layout Example

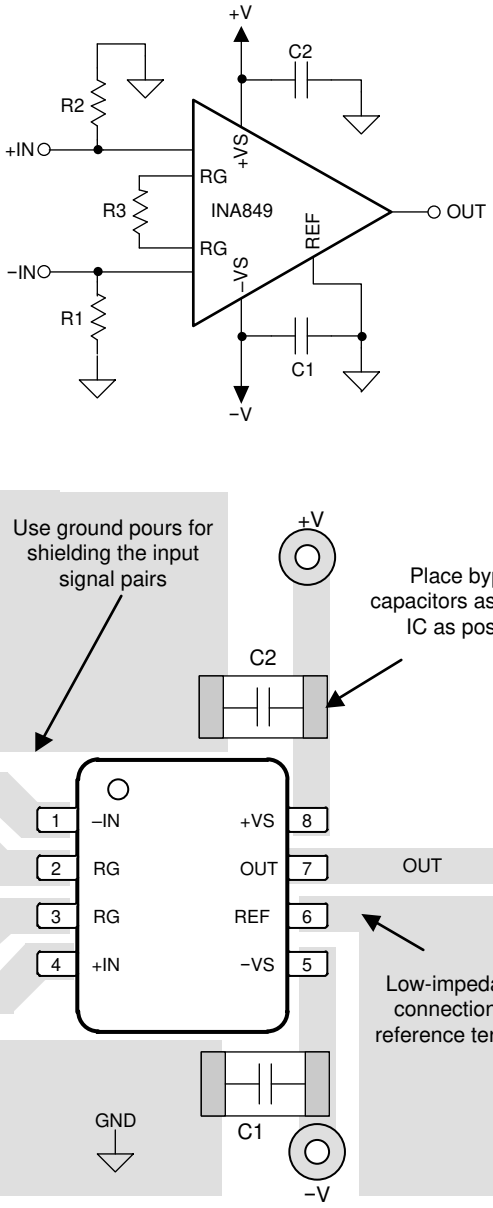


Figure 11-1. Example Schematic and Associated PCB Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Comprehensive Error Calculation for Instrumentation Amplifiers* application note

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA849DGKR	PREVIEW	VSSOP	DGK	8	2500	RoHS (In work) & Green (In work)	Call TI	Call TI	-40 to 125		
INA849DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA849	Samples
XINA849DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS (In work) & Green (In work)	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

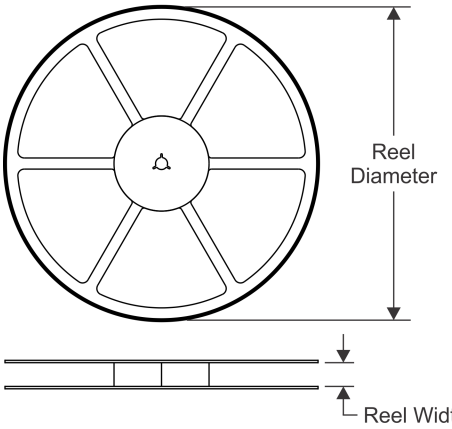
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

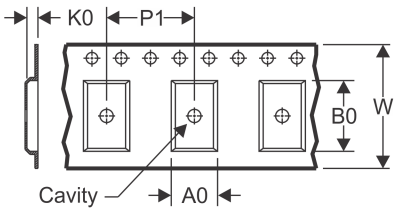
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

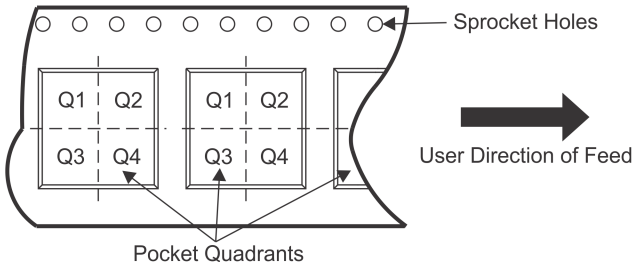


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

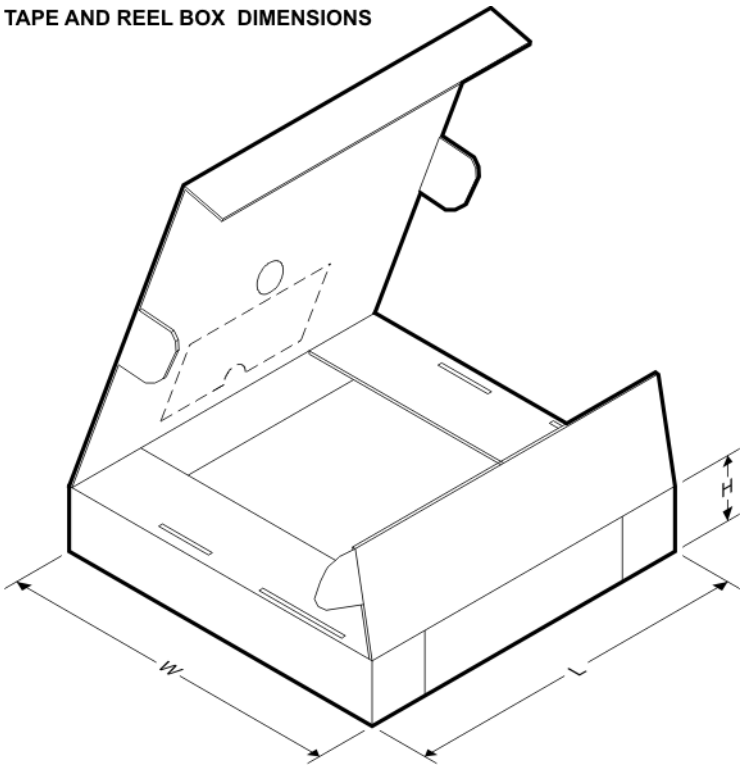
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

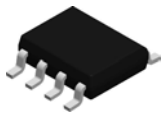
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA849DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA849DR	SOIC	D	8	2500	853.0	449.0	35.0

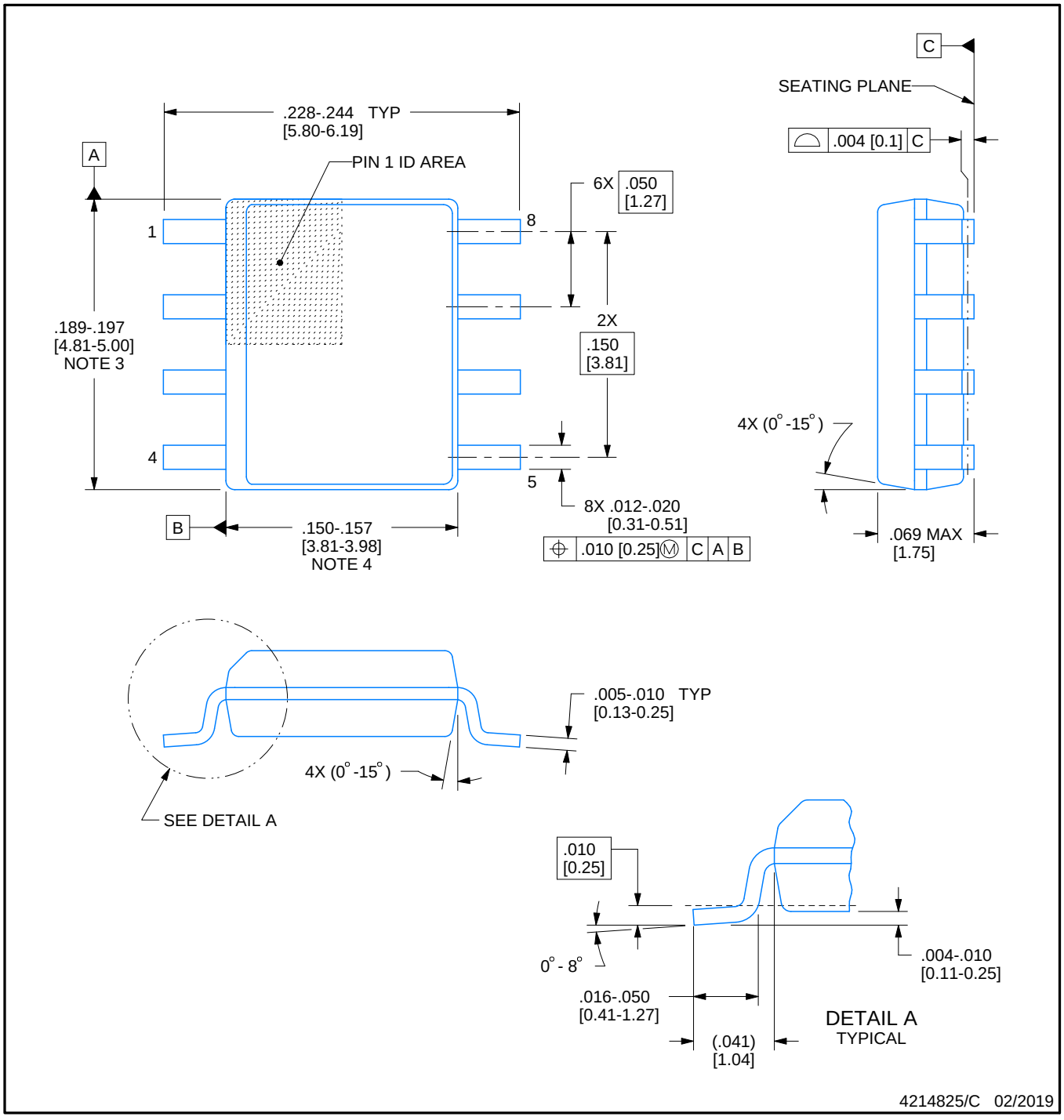


PACKAGE OUTLINE

D0008A

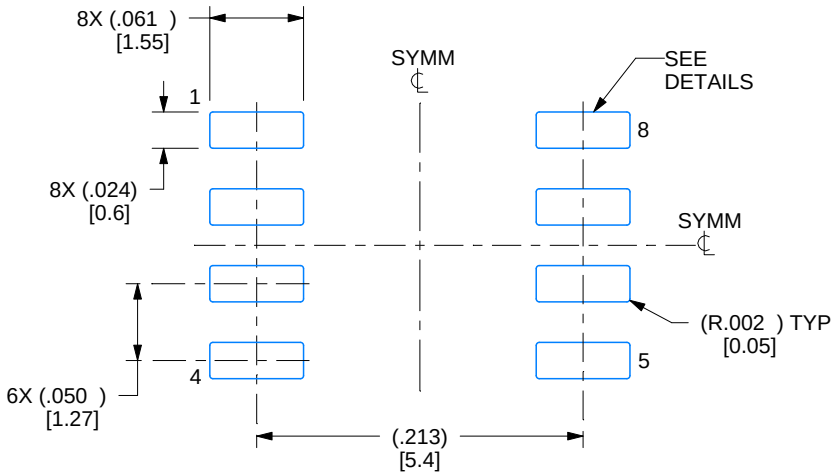
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

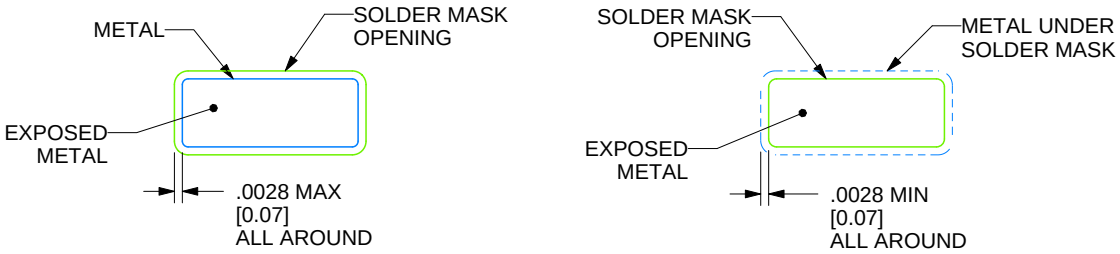


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

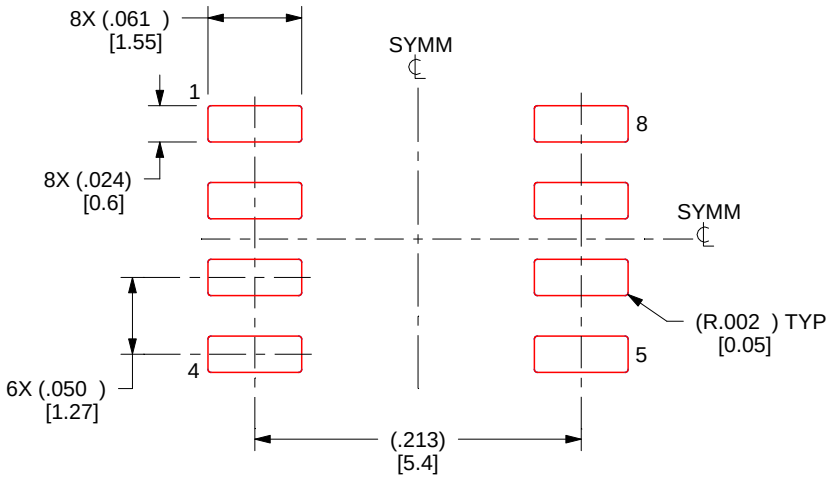
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



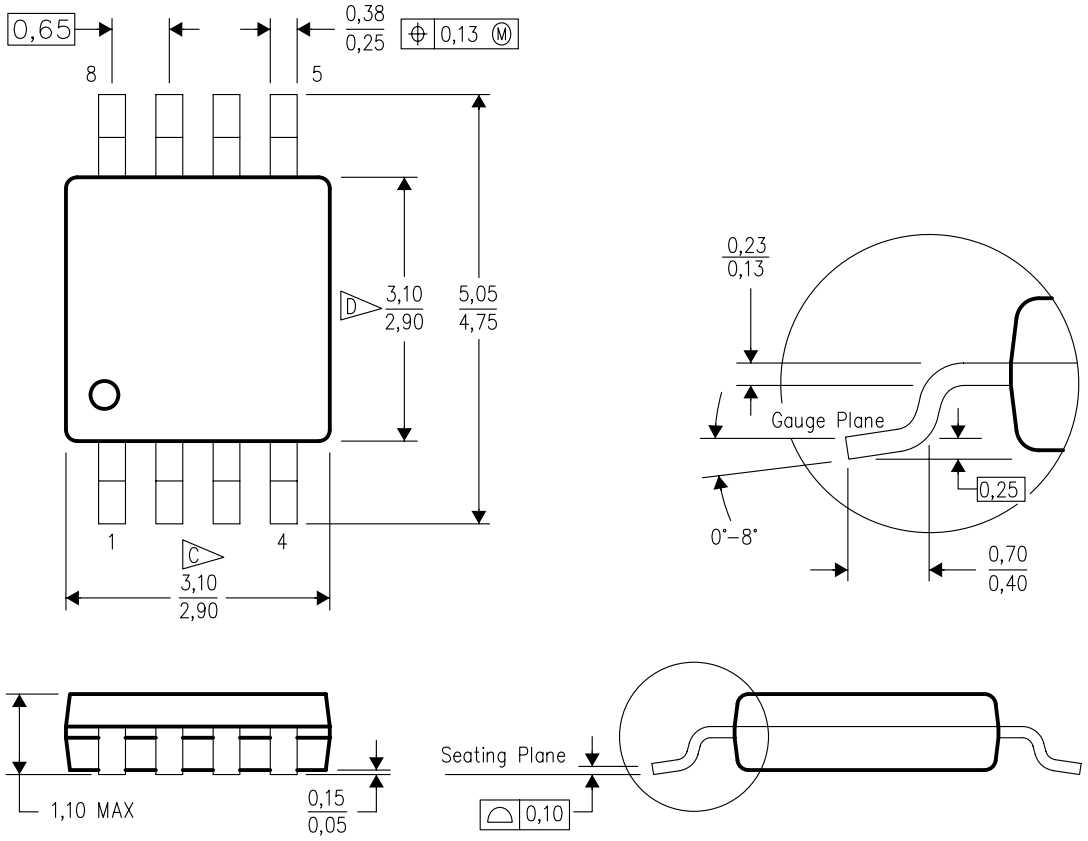
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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