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MAX22506E

50Mbps Half-Duplex RS-485/RS-422 Transceiver with High EFT Immunity

General Description

The MAX22506E ESD-protected RS-485/RS-422 transceiver is optimized for high-speed communication up to 50Mbps. This transceiver features integrated hot-swap protection and a fail-safe receiver, ensuring a logic-high on the receiver output when input signals are shorted or open for longer than 10µs (typ). Additionally, a large receiver hysteresis improves noise rejection and signal integrity.

The MAX22506E is designed to operate in harsh industrial environments and is optimized for robust communication in environments with high levels of electromagnetic interference (EMI).

The MAX22506E is available in an 8-pin SOIC and an 8-pin µMAX package. The transceiver operates over the -40°C to +125°C temperature range.

Applications

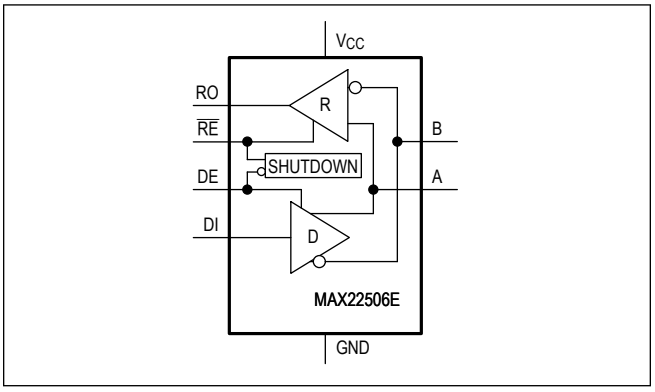
- Motion Control
- Encoder Interfaces
- Field Bus Networks
- Industrial Control Systems
- Backplane Busses

Benefits and Features

- High-Speed Operation over Long Distances
  - Up to 50Mbps Data Rate
  - High Receiver Sensitivity
  - Wide Receiver Bandwidth
  - Symmetrical Receiver Thresholds
- Integrated Protection Increases Robustness
  - -15V to +15V Common-Mode Range
  - ±15kV ESD Protection (Human Body Model)
  - ±7kV IEC 61000-4-2 Air-Gap ESD Protection
  - ±6kV IEC 61000-4-2 Contact Discharge ESD Protection
  - Withstands Over ±4kV EFT
  - Driver Outputs are Short-Circuit Protected
- Flexibility for Many Different Applications
  - 3V to 5.5V Supply Range
  - Low 5µA (max) Shutdown Current
  - Available in 8-pin SOIC and µMAX Packages
  - -40°C to +125°C Operating Temperature Range

***Ordering Information* appears at end of data sheet.**

Simplified Block Diagram



19-100995; Rev 1; 5/21

maxim integrated™

Absolute Maximum Ratings

V_{CC} ..... -0.3V to +6V
RE, DE, DI ..... -0.3V to +6V
RO ..... -0.3V to (V_{CC} + 0.3V)
A, B ..... -15V to +15V
Short-Circuit Duration (RO, A, B) to GND ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.8mW/°C above +70°C)..... 387.8mW
8-Pin SOIC (derate 7.4mW/°C above +70°C) 588.2mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering 10s) .....+300°C
Reflow Temperature .....+270ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

µMAX8

Package Code	U8+1
Outline Number	21-0036
Land Pattern Number	90-0092
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	206.3°C/W
Junction to Case (θ_{JC})	42°C/W

SOIC8

Package Code	S8+2C
Outline Number	21-0041
Land Pattern Number	90-0096
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	136°C/W
Junction to Case (θ_{JC})	38°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{CC} = 3V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / POWER							
Supply Voltage	V_{CC}			3.0		5.5	V
Supply Current	I_{CC}	DE = high, $\overline{RE}$ = low, no load			4	5.6	mA
Shutdown Supply Current	I_{SHDN}	DE = low, $\overline{RE}$ = high				5	µA
DC ELECTRICAL CHARACTERISTICS / DRIVER							
Differential Driver Output	V_{OD}	Figure 1	R_L = 54Ω	1.5			V
			R_L = 100Ω	2.0			
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	R_L = 54Ω, Figure 1 (Note 3)				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 54Ω, Figure 1			V_{CC} / 2	3	V
Change in Magnitude of Common-Mode Voltage	ΔV_{OC}	R_L = 100Ω or 54Ω, Figure 1 (Note 3)				0.2	V
Single-Ended Driver Output High	V_{OH}	A or B output, I_{OUT} = -20mA		2.2			V
Single-Ended Driver Output Low	V_{OL}	A or B output, I_{OUT} = +20mA				0.8	V
Differential Output Capacitance	C_{OD}	DE = high, f = 4MHz			50		pF
Driver Short-Circuit Output Current	$\|I_{OST}\|$	-15V ≤ V_{OUT} ≤ +15V				250	mA
DC ELECTRICAL CHARACTERISTICS / RECEIVER							
Input Current (A and B)	$I_{A,B}$	DE = low, V_{CC} = 0V or 3V ≤ V_{CC} ≤ 5.5V	V_{IN} = +12V			+390	µA
			V_{IN} = -7V	-360			
Differential Input Capacitance	$C_{A,B}$	Between A and B, f = 2MHz			50		pF
Common-Mode Voltage Range	V_{CM}			-15		+15	V
Receiver Differential-Threshold High	V_{TH_H}	-15V ≤ V_{CM} ≤ +15V		+50	+122	+200	mV
Receiver Differential-Threshold Low	V_{TH_L}	-15V ≤ V_{CM} ≤ +15V		-200	-122	-50	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V, time from last transition is < t_{D_FS}			250		mV
Differential Input Fail-Safe Level	V_{TH_FS}	-15V ≤ V_{CM} ≤ +15V, time from last transition > t_{F_DS}		-50		+50	mV
DC ELECTRICAL CHARACTERISTICS / LOGIC INTERFACE ($\overline{RE}$, RO, DE, DI)							
Input-Voltage High	V_{IH}	DE, DI, $\overline{RE}$	3V ≤ V_{CC} ≤ 5.5V	2/3 x V_{CC}			V
			V_{CC} = 5.25V	2.85			
Input-Voltage Low	V_{IL}	DE, DI, $\overline{RE}$				1/3 x V_{CC}	V

Electrical Characteristics (continued)

(V_{CC} = 3V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current	I_{IN}	DE, DI, $\overline{RE}$ (after first transition)	-2		+2	µA
Input Impedance on First Transition	R_{IN_FT}	DE, $\overline{RE}$			10	kΩ
RO Output-High Voltage	V_{OH}	$\overline{RE}$ = low, (V_A - V_B) > 200mV, I_{OUT} = -1mA	V_{CC} – 0.4			V
RO Output-Low Voltage	V_{OL}	$\overline{RE}$ = low, (V_A–V_B) < -200mV, I_{OUT} = +1mA			0.4	V
Three-State Output Current at Receiver	I_{OZR}	$\overline{RE}$ = high, 0 ≤ V_{RO} ≤ V_{CC}	-1		+1	µA
PROTECTION						
Thermal-Shutdown Threshold	T_{SH}	Temperature rising		+160		°C
Thermal-Shutdown Hysteresis	T_{SH_HYS}			10		°C
ESD Protection (A and B Pins)		Human Body Model		±15		kV
		IEC61000-4-2 Air Gap Discharge to GND		±7		
		IEC61000-4-2 Contact Discharge to GND		±6		
ESD Protection (All Other Pins)		Human Body Model		±2		kV
AC ELECTRICAL CHARACTERISTICS / DRIVER (Note 4)						
Driver Propagation Delay	t_{DPLH}	R_L = 54Ω, C_L = 50pF, Figure 2, Figure 3			32	ns
	t_{DPHL}	R_L = 54Ω, C_L = 50pF, Figure 2, Figure 3			32	
Differential-Driver Output Skew	t_{DSKEW}	$\lvert t_{DPLH} - t_{DPHL} \rvert$, R_L = 54Ω, C_L = 50pF, Figure 2, Figure 3 (Note 5)			1.2	ns
Driver Differential-Output Rise and Fall Time	t_{HL}, t_{LH}	R_L = 54Ω, C_L = 50pF, Figure 3 (Note 5)			3	ns
Maximum Data Rate	DR		50			Mbps
Driver Enable to Output High	t_{DZH}	R_L = 500Ω, C_L = 50pF, Figure 4			32	ns
Driver Enable to Output Low	t_{DZL}	R_L = 500Ω, C_L = 50pF, Figure 5			32	ns
Driver Disable Time from High	t_{DHZ}	R_L = 500Ω, C_L = 50pF, Figure 4			32	ns
Driver Disable Time from Low	t_{DLZ}	R_L = 500Ω, C_L = 50pF, Figure 5			32	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 4			100	µs
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 5			100	µs
Time to Shutdown	t_{SHDN}	(Notes 6, 7)	50		800	ns

Electrical Characteristics (continued)

(V_{CC} = 3V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS / RECEIVER (Note 4)						
Delay to Fail-Safe Operation	t_{D_FS}			10		µs
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 15pF, *Figures 6*, 7			40	ns
Receiver Output Skew	t_{RSKEW}	$\lvert t_{RPHL} - t_{RPLH} \rvert$, C_L= 15pF, *Figures 6*, 7 (Note 5)			2.5	ns
Maximum Data Rate	DR		50			Mbps
Receiver Enable to Output High	t_{RZH}	R_L = 1kΩ, C_L = 15pF, Figure 8			32	ns
Receiver Enable to Output Low	t_{RZL}	R_L = 1kΩ, C_L = 15pF, Figure 8			32	ns
Receiver Disable Time from Low	t_{RLZ}	R_L = 1kΩ, C_L = 15pF, Figure 8			32	ns
Receiver Disable Time from High	t_{RHZ}	R_L = 1kΩ, C_L = 15pF, Figure 8			32	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 8			100	µs
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 8			100	µs
Time to Shutdown	t_{SHDN}	(Notes 6, 7)	50		800	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications for all temperature limits are guaranteed by design.

Note 2: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to the device ground, unless otherwise noted.

Note 3: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.

Note 4: Capacitive load includes test probe and fixture capacitance.

Note 5: Not production tested. Guaranteed by design.

Note 6: Shutdown is enabled by driving $\overline{RE}$ high and DE low. The device is guaranteed to have entered shutdown after t_{SHDN} has elapsed.

Note 7: Time to shutdown refers to the driver or receiver enable delay when the device has exited the initial hot-swap protect state and is in normal operating mode.

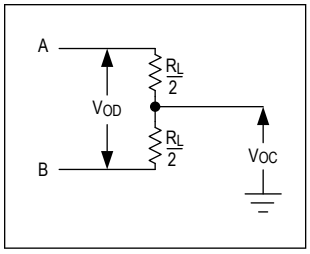


Figure 1. Driver DC Test Load

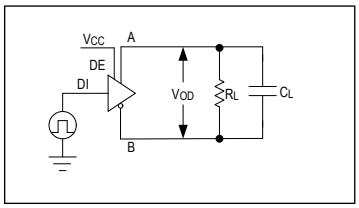


Figure 2. Driver Timing Test Circuit

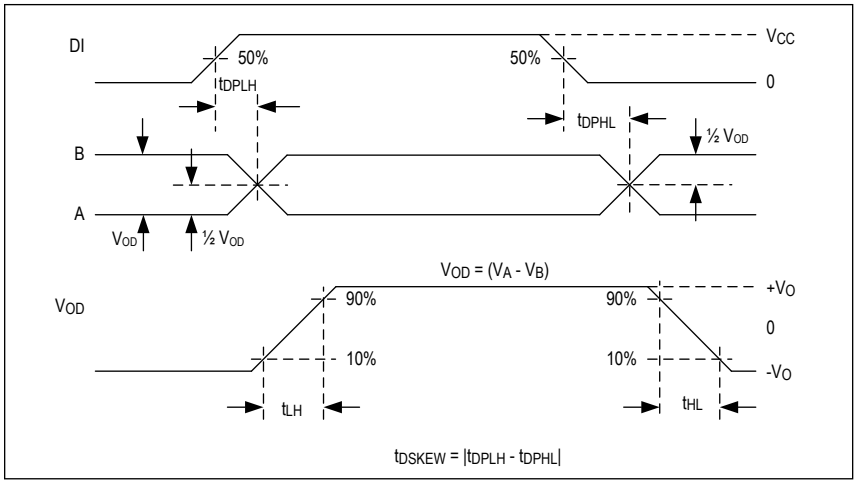


Figure 3. Driver Propagation Delays

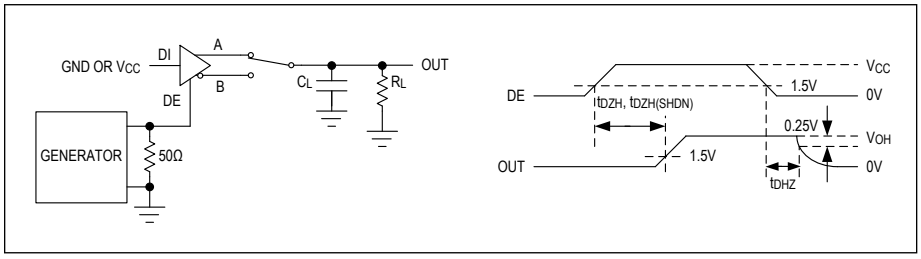


Figure 4. Driver Enable and Disable Times (t_{DZH}, t_{DHZ})

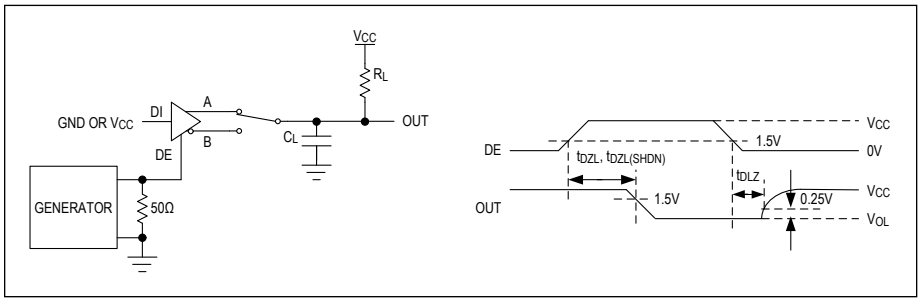


Figure 5. Driver Enable and Disable Times (t_{DZL}, t_{DLZ})

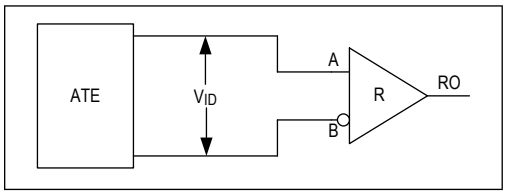


Figure 6. Receiver Propagation Delay Test Circuit

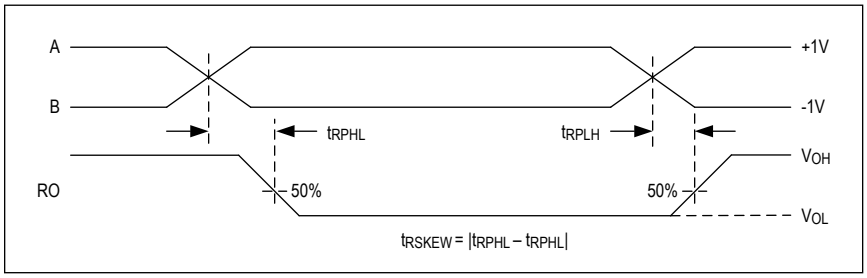


Figure 7. Receiver Propagation Delays

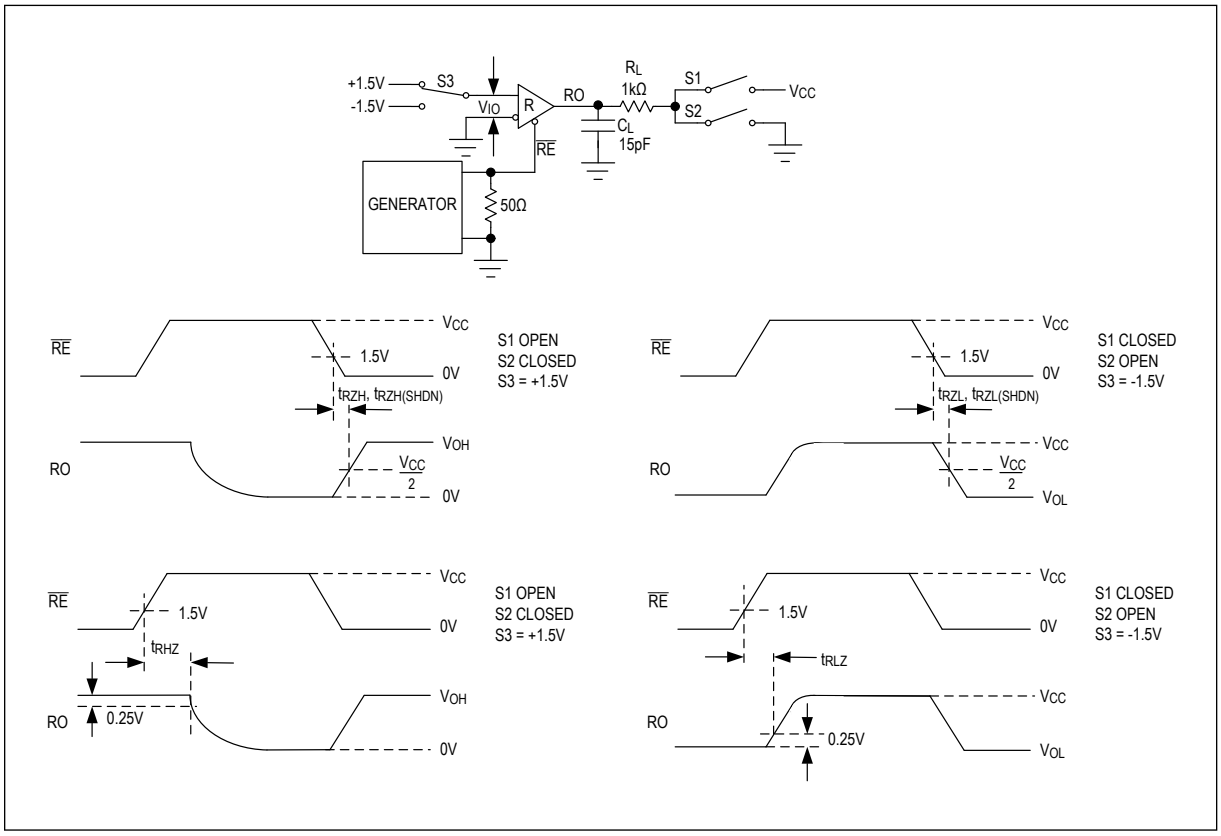
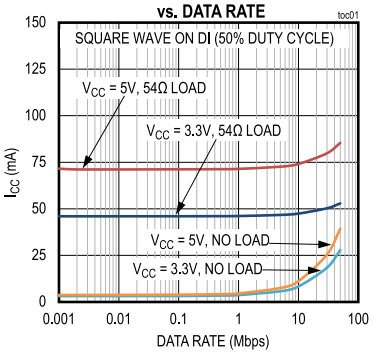


Figure 8. Receiver Enable and Disable Times

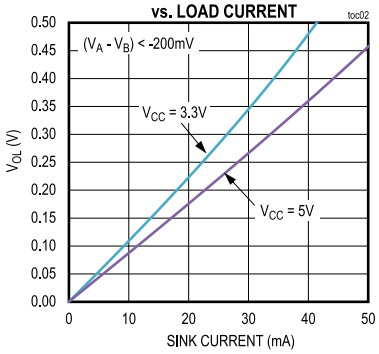
Typical Operating Characteristics

(V_{CC} = 5V, 60Ω termination between the driver outputs, T_A = 25°C, unless otherwise noted.)

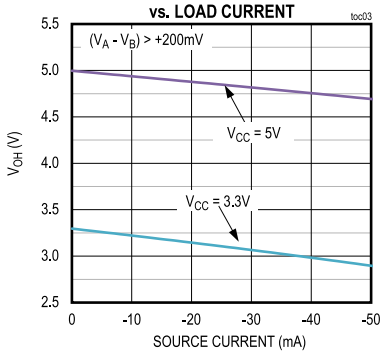
SUPPLY CURRENT vs. DATA RATE



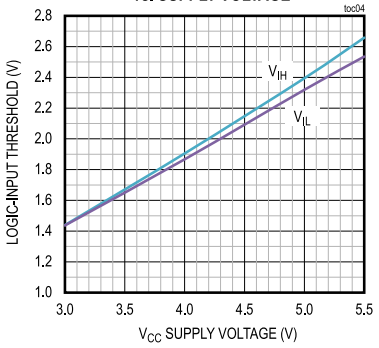
RO OUTPUT-VOLTAGE LOW vs. LOAD CURRENT



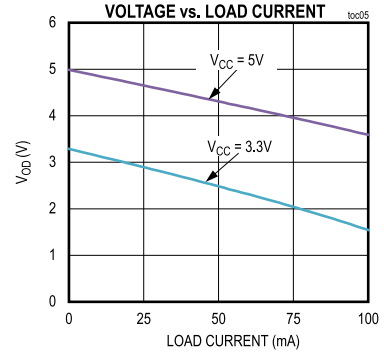
RO OUTPUT-VOLTAGE HIGH vs. LOAD CURRENT



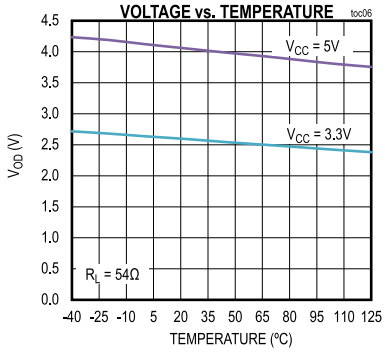
INPUT-LOGIC THRESHOLDS vs. SUPPLY VOLTAGE



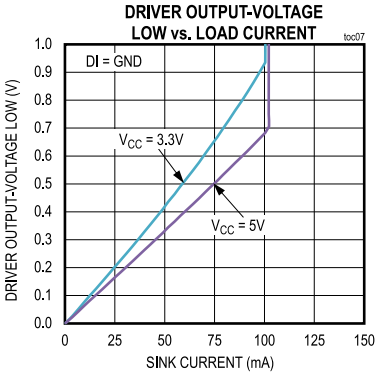
DIFFERENTIAL DRIVER OUTPUT VOLTAGE vs. LOAD CURRENT



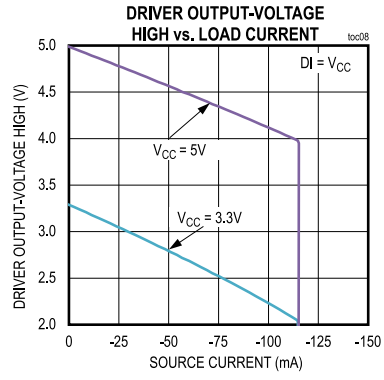
DIFFERENTIAL DRIVER OUTPUT VOLTAGE vs. TEMPERATURE



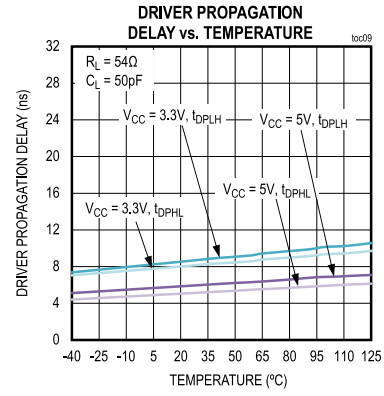
DRIVER OUTPUT-VOLTAGE LOW vs. LOAD CURRENT



DRIVER OUTPUT-VOLTAGE HIGH vs. LOAD CURRENT

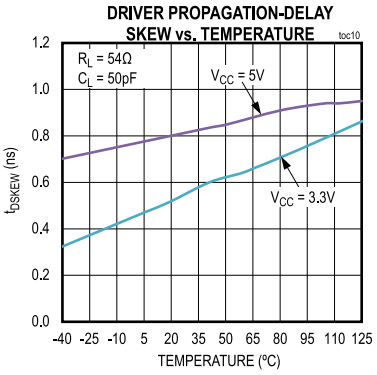


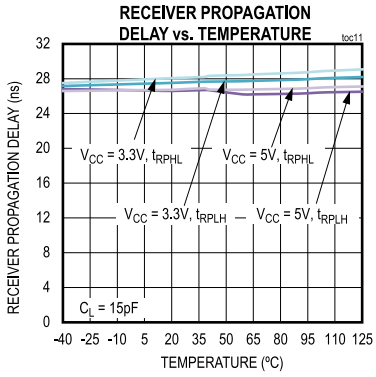
DRIVER PROPAGATION DELAY vs. TEMPERATURE

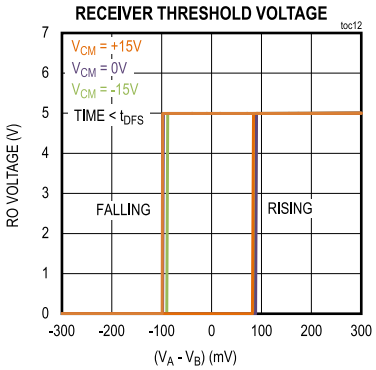


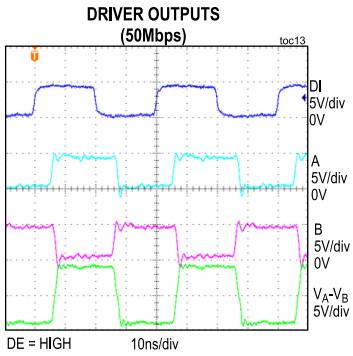
Typical Operating Characteristics (continued)

(V_{CC} = 5V, 60Ω termination between the driver outputs, T_A = 25°C, unless otherwise noted.)



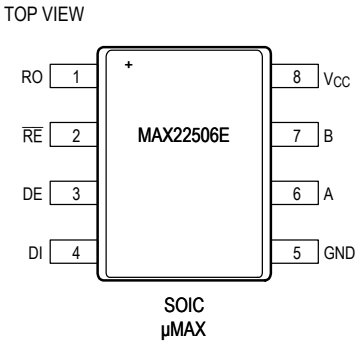






Pin Configuration

MAX22506E



Pin Description

PIN	NAME	FUNCTION
1	RO	Receiver Output. See the *Receiving Table* for more information.
2	$\overline{RE}$	Receiver Enable. Pull $\overline{RE}$ high to disable the receiver and three-state RO. The device is in low-power shutdown when $\overline{RE}$ = high and DE = low.
3	DE	Driver Output Enable. Force DE high to enable the driver. The device is in low-power shutdown when $\overline{RE}$ = high and DE = low.
4	DI	Driver Input. See the *Transmitting Table* for more information.
5	GND	Ground
6	A	Noninverting Driver Output/Receiver Input
7	B	Inverting Driver Output/Receiver Input
8	V_{CC}	Supply Input. Bypass V_{CC} to ground with a 0.1µF ceramic capacitor as close to the device as possible.

Function Tables

Transmitting Table

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	A	B
X	1	1	1	0
X	1	0	0	1
0	0	X	High Impedance	High Impedance
1	0	X	Shutdown. Driver outputs are high impedance	

X = Don't care

Receiving Table

INPUTS				OUTPUTS
$\overline{RE}$	DE	$(V_A - V_B)$	Time from Last A-B Transition	RO
0	X	≥ +200mV	Always	1
0	X	-200mV < $(V_A - V_B)$ < +200mV	< t_{D_FS}	Indeterminate RO is latched to previous value
0	X	-50mV < $(V_A - V_B)$ < +50mV	> t_{D_FS}	1
0	X	≤ -200mV	Always	0
0	X	Open/Shorted	> t_{D_FS}	1
1	1	X	X	High Impedance
1	0	X	X	Shutdown. RO is high impedance

Detailed Description

The MAX22506E ESD-protected RS-485/RS-422 transceiver is optimized for high-speed communications up to 50Mbps. This transceiver features integrated hot-swap functionality to eliminate false transitions on the driver during power-up or during a hot-plug event. This transceiver also feature fail-safe receiver inputs, guaranteeing a logic-high on the receiver output when inputs are shorted or open for longer than 10µs (typ).

Receiver Threshold Voltages

The device receiver features a large threshold hysteresis of 250mV (typ) for increased differential noise rejection. Additionally, the receiver features symmetrical threshold voltages. Symmetric thresholds have the advantage that recovered data at the RO output does not have duty-cycle distortion. Typically, fail-safe receivers, which have unipolar (non-symmetric) thresholds, show some duty-cycle distortion at high signal attenuation due to long cable lengths.

Fail-Safe Functionality

The MAX22506E features fail-safe receiver inputs, guaranteeing a logic-high on the receiver output (RO) when the receiver inputs are shorted or open for longer than 10µs (typ). When the differential receiver input voltage is between ±50mV, or -50mV ≤ (V_A - V_B) ≤ +50mV, for more than 10µs (typ), RO is logic-high. For example, in the case of a terminated bus with all transmitters disabled, the receiver differential input voltage is pulled to 0V by the termination resistor, so -50mV ≤ (V_A - V_B) = 0V ≤ +50mV and RO is guaranteed to be a logic high after 10µs (typ).

Driver Single-Ended Operation

The driver outputs of the MAX22506E can be used in the standard differential operating mode or as single-ended outputs. Because the driver outputs swing rail-to-rail, they can also be used as individual standard TTL or CMOS logic outputs.

Hot-Swap Capability

The DE and $\overline{RE}$ enable inputs feature hot-swap functionality. At each input there are two nMOS devices, M1 and M2 (Figure 9). When V_{CC} ramps from zero, an internal 10µs timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2 (a 500µA current sink) and M1 (a 100µA current sink) pull DE to GND through a 5kΩ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After 10µs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

Note: Figure 9 shows a complementary circuit for $\overline{RE}$ that uses two pMOS devices to pull $\overline{RE}$ to V_{CC}.

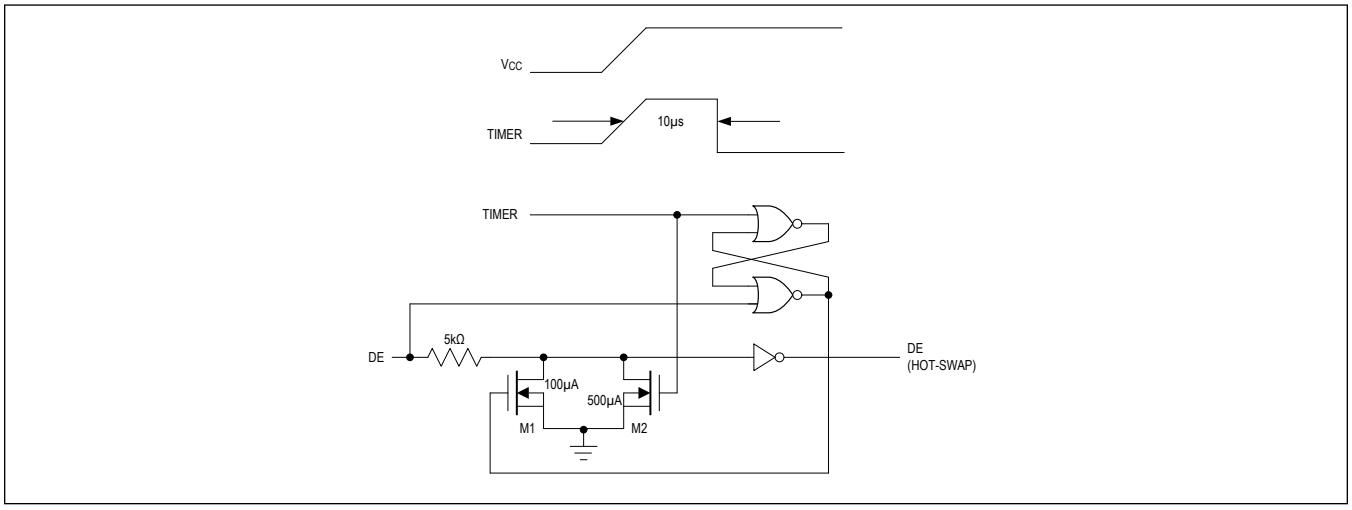


Figure 9. Simplified Structure of the Driver Enabled (DE) Pin

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a current limit on the output stage, provides immediate protection against short-circuits over the whole common-mode voltage range. The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

Low-Power Shutdown Mode

The MAX22506E features a low-power shutdown mode to reduce supply current when the transceiver is not needed. Pull the $\overline{RE}$ input high and the DE input low to put the device in low-power shutdown mode. If the inputs are in this state for at least 800ns, the parts are guaranteed to enter shutdown. The MAX22506E draws 5µA (max) of supply current when the device is in shutdown.

The $\overline{RE}$ and DE inputs can be driven simultaneously. The MAX22506E is guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns.

Integrated ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the MAX22506E have extra protection against static electricity. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX22506E is able to keep working without latch-up or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX22506E are characterized for protection to the following limits:

- ±15kV HBM
- ±7kV using the Air-Gap Discharge method specified in IEC 61000-4-2
- ±6kV using the Contact Discharge method specified in IEC 61000-4-2

Human Body Model (HBM)

Figure 10 shows the HBM test model, and Figure 11 shows the current waveform it generates when discharged into a low-impedance state. This models consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into a test device through a 1.5kΩ resistor.

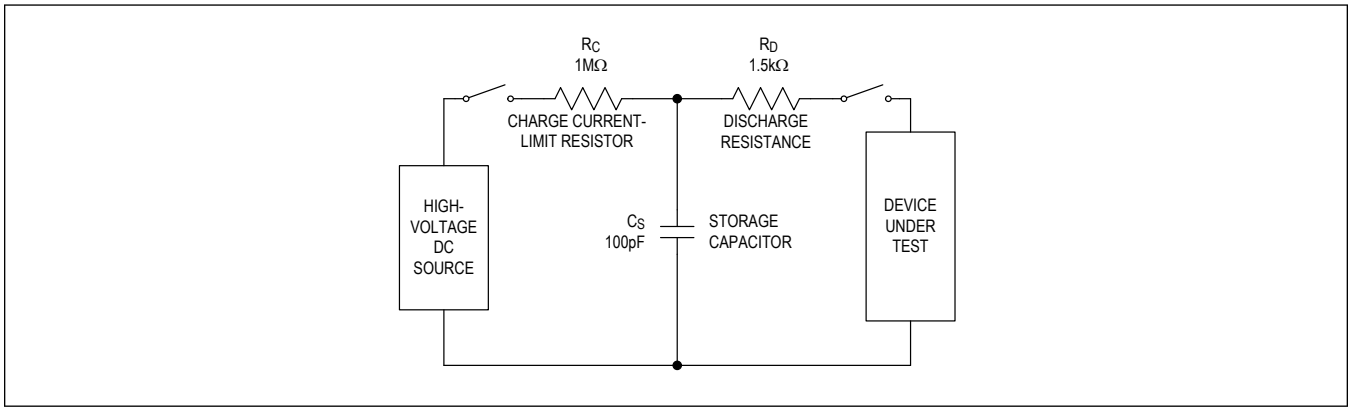


Figure 10. Human Body ESD Test Model

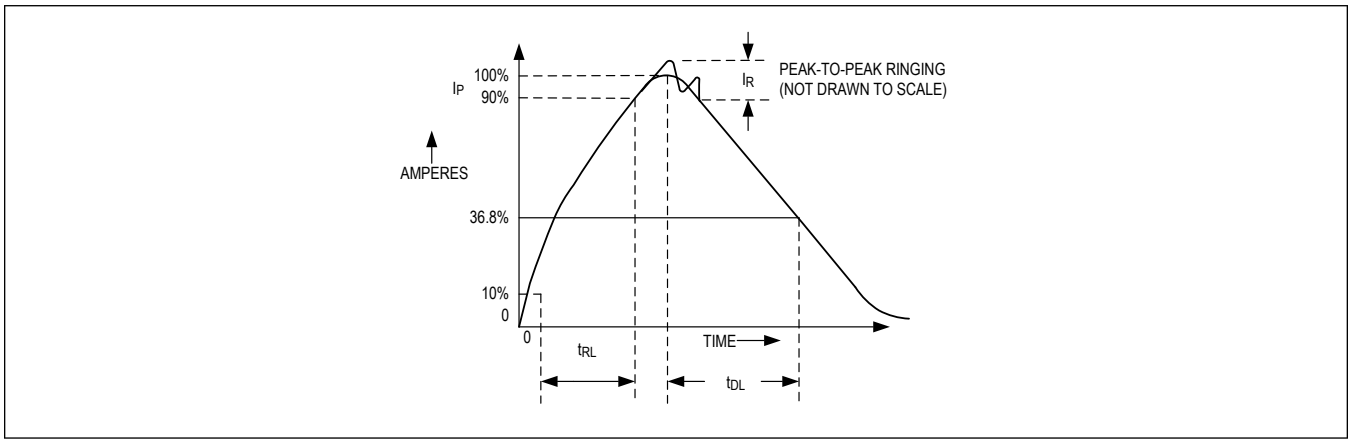


Figure 11. Human Body Current Waveform

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The integrated ESD protection circuitry in the transceiver helps in designing equipment to meet IEC 61000-4-2.

The major difference between tests done using the HBM and IEC 61000-4-2 models is the higher peak current in IEC 61000-4-2. This is due to the lower series resistance in the IEC 61000-4-2 model and typically results in the withstand voltage measured to IEC 61000-4-2 being generally lower than that measured using the HBM.

Figure 12 shows the IEC 61000-4-2 model and Figure 13 shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

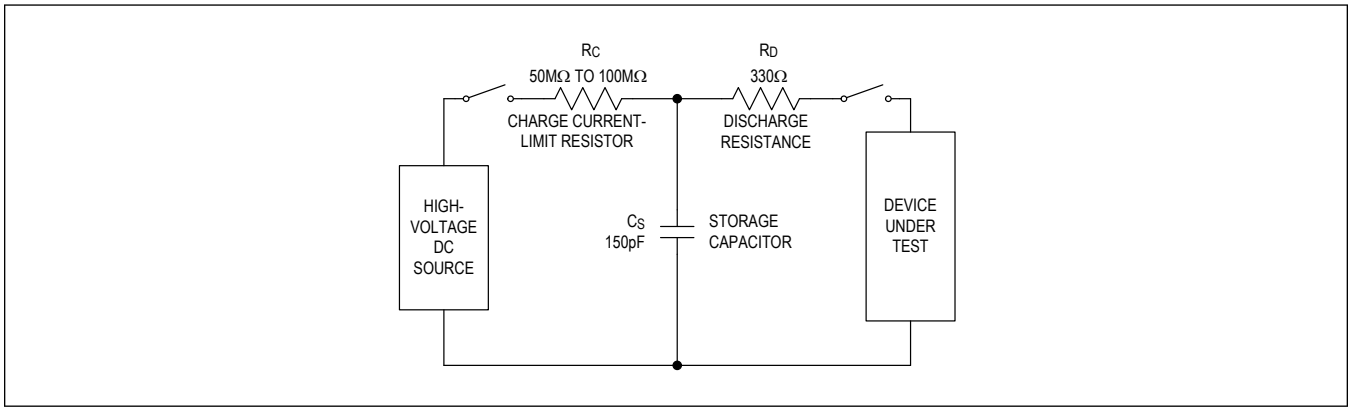


Figure 12. IEC 61000-4-2 ESD Test Model

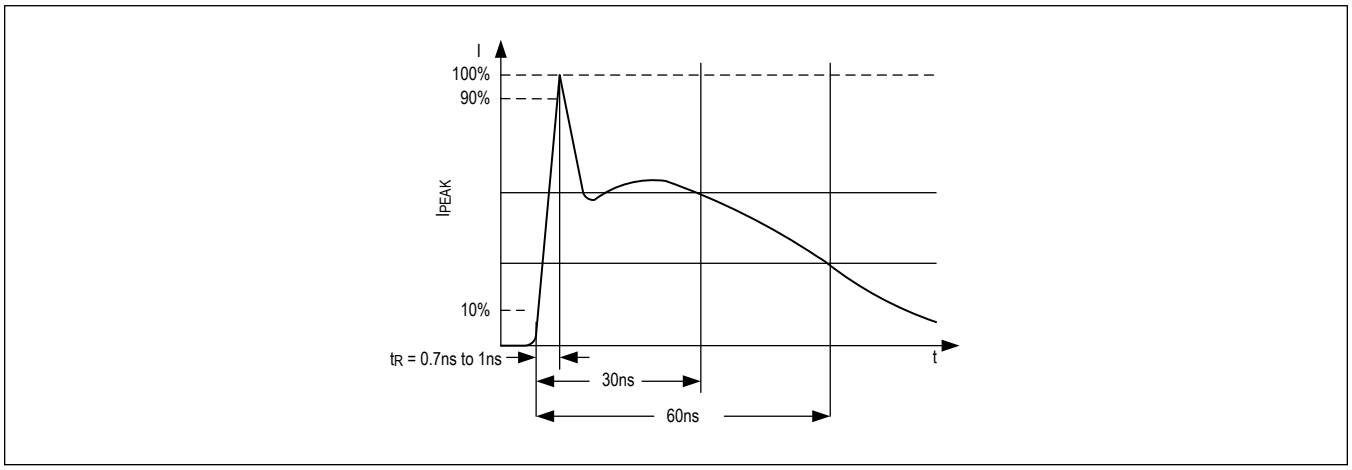


Figure 13. IEC 61000-4-2 ESD Generator Current Waveform

Applications Information

Transceivers on the Bus

The A and B receiver inputs have an input current of 390µA (max) at 12V and -360µA (min) at -7V, respectively. According to the RS-485 standard, the relative receiver input resistance can be calculated as 360µA/800µA = 0.45 unit load (UL). Assuming a line terminated at both ends, up to 71 (= 32UL/0.45UL) MAX22506E transceivers can be used on a multi-drop network. Note that this maximum number of nodes is calculated based on DC criteria only and does not take into consideration signal integrity and transmission line effects at high data rates.

Transient Protection

Transient events that can occur in industrial environments include electrostatic discharge (ESD), surge events (e.g., lightning strikes), and electrical fast transient (EFT) or burst events. Surge pulses typically have a longer duration and higher power-withstand requirements than EFT and ESD strikes. Test requirements and limits for ESD, surge, and burst conditions are included in the IEC 61000-4-2, IEC 61000-4-4, and IEC 6100-4-5 standards.

External ESD Protection

The MAX22506E is internally protected against electrostatic discharge (ESD) events for the levels shown in the Protection section of the *Electrical Characteristics* table. While this internal protection increases the robustness of the device, additional external protection might be required to meet higher ESD limits or to protect against other high-voltage transients in the final application.

Electrical Fast Transient (EFT) Events

The IEC 61000-4-4 standard outlines the voltage levels and duration of an electrical fast transient (EFT) or burst event. EFT is typically a high-frequency, high-voltage burst that is coupled on to the RS-485 cable from external high-voltage switching signals. For example, switching from nearby relays or motors can generate EFT on a RS-485 data line. Relative to surge transient events, EFT bursts generate a small amount of power, but can corrupt data along the line.

To minimize the impact of EFT on signal lines, always use bypass capacitors soldered as close to the IC as possible. Additionally, common-mode chokes and TVS diodes can help to clamp high-voltage transients. Capacitive or resistor-capacitor filters can also be added on the signal lines. Shielded cables, if available, also help to reduce interference from EFT.

Surge Protection

Surge transient events can occur during lightning strikes, for example, and are characterized by the IEC 61000-4-5 standard. Surge events generate high energy, with high voltage peaks and large currents being driven to the driver outputs and receiver inputs.

Per the IEC 61000-4-5 standard, surge pulses must be referenced to protective earth (PE). Isolate PE from the field ground and connect a high-voltage capacitor and a high-voltage resistor between the field ground and PE. Figure 14 shows the current flow through the transceiver and PCB during a surge event. The MAX22506E survived 8/20µs surge testing up to ±2kV/42Ω with a 1000pF high-voltage capacitor without the need for external TVS protection.

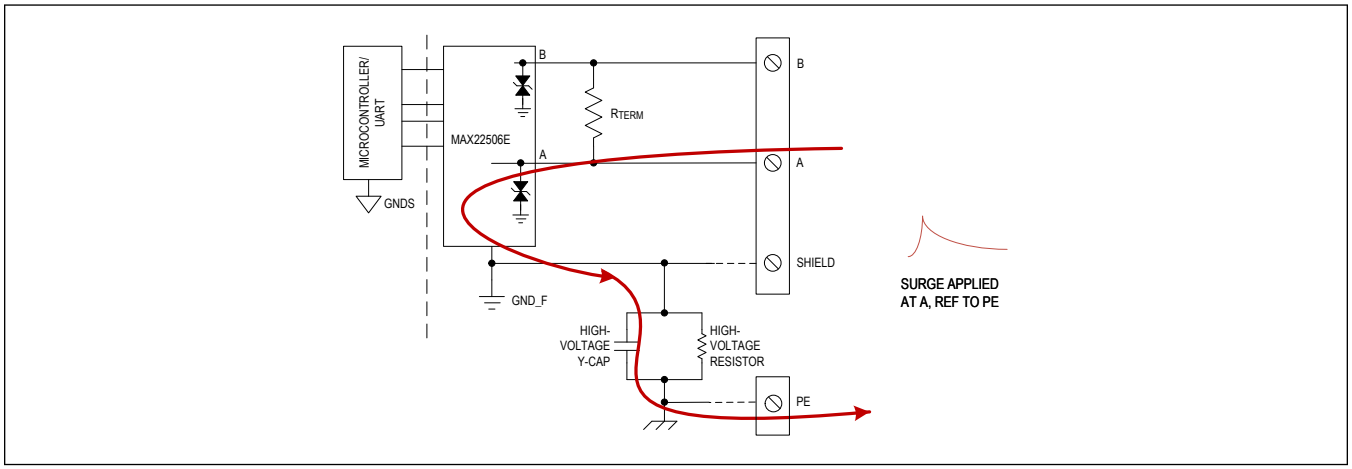


Figure 14. Surge Protection

Layout Guidelines

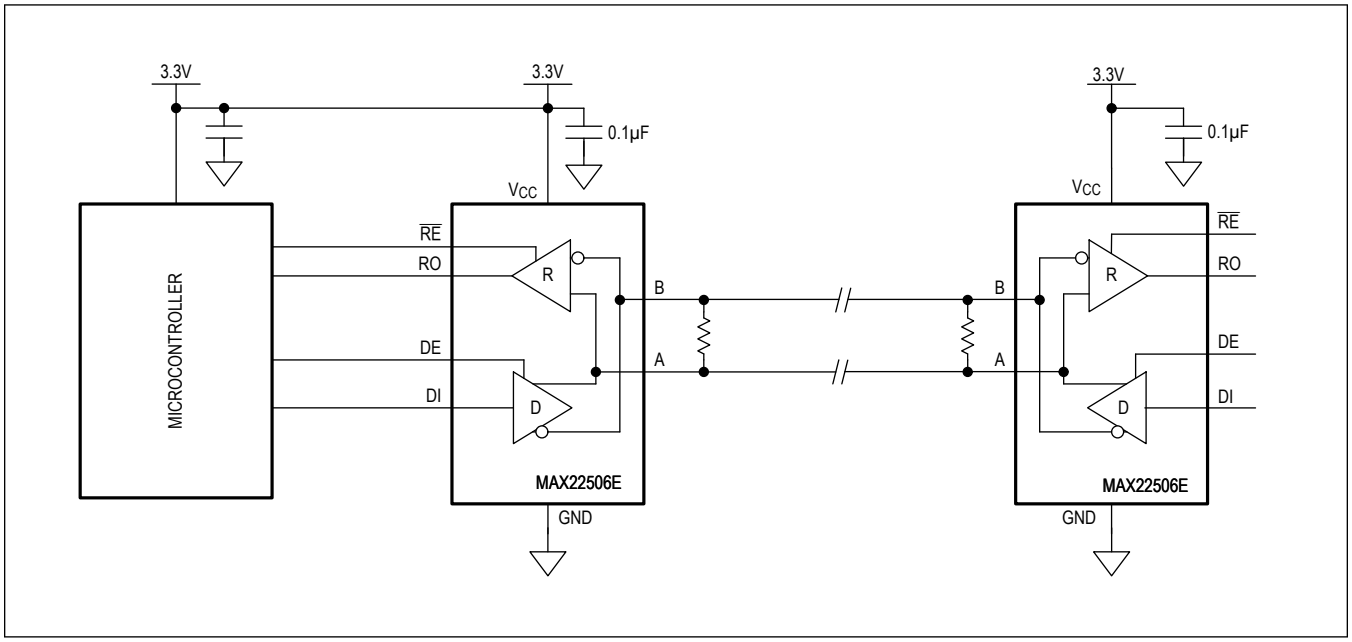
The MAX22506E is designed for robust communication in harsh industrial environments. Use the following guidelines for layout to ensure optimum performance:

- Place the bypass capacitor as close to the V_{CC} pin as possible
- Use supply and ground planes to reduce trace inductance.
- Place external protection (resistors, capacitors, diodes) as close to the device as possible.
- Design protection components directly in the path of the driver output and receiver input signals.

Additionally, pull ground planes away from the RS-485/RS-422 data lines when operating at high data rates to reduce capacitive coupling that can slow edge rates.

Typical Application Circuits

Half Duplex Point-to-Point Network



Ordering Information

PART	PIN-PACKAGE	PACKAGE CODE
MAX22506EASA+	SOIC8	S8+2C
MAX22506EASA+T	SOIC8	S8+2C
MAX22506EAUA+	µMAX8	U8+1
MAX22506EAUA+T	µMAX8	U8+1

+ Denotes lead (Pb)-free/RoHS compliance.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/21	Release for Market Intro	—
1	5/21	Updated the *General Description,* Figure 3, *Layout Guidelines,* and removed the future product designation from MAX22506EAUA+ and MAX22506EAUA+T in the *Ordering Information* table	1, 6, 17, 18

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