

Optical Receiver IC for CD/DVD/Blue-Laser Application

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Abstract

In this paper an optoelectronic receiver IC for optical data storage applications is presented. The IC was developed in a $0.5\ \mu\text{m}$ BiCMOS technology with integrated PIN-photodiodes. It includes a new architecture of high-speed and low-noise transimpedance amplifiers with a gain range of $130\ \Omega$ to $270\ \text{k}\Omega$ programmable with a serial interface. The bandwidth is $260\ \text{MHz}$ for highest gain which gives a gain-bandwidth-product of $70\ \text{THz}\Omega$ and a sensitivity improvement by a factor of 2 compared to published OEICs. The amplifiers support a special write/clip mode. The output buffers are $130\ \Omega$ impedance matched for optimized data transmission over a flex cable.

1. Introduction

The optical pickup units (OPU) in optical data storage systems like CD, DVD or future applications with blue laser light ("Blue-Ray") needs receiver optoelectronic ICs (OEICs) that convert the reflected light from a storage disc to an electrical output signal. On one hand the data rates in optical storage applications increase rapidly up to $500\ \text{Mb/s}$ and on the other hand the reflected light intensity for read application is decreasing below $1\ \mu\text{W}$. Therefore there is a strong demand on OEICs including integrated photodiodes with high-speed and sensitivity performance combined with high-bandwidth and low-noise transimpedance amplifier circuits. Due to the broad variety of operating conditions (CD, DVD, "Blue-Ray", read, write, single or double layer disc...) the transimpedance amplifiers must be programmable over a wide range of gains. In the presented prototype IC the circuits are implemented in a $0.5\ \mu\text{m}$ BiCMOS technology including an integrated PIN-photodiode with a high speed and light sensitivity for all 3 wavelengths used for optical data storage like CD ($780\ \text{nm}$), DVD ($660\ \text{nm}$) and "Blue-Ray" ($410\ \text{nm}$). The measured photodiode sensitivity is $0.35\ \text{A/W}$ for $780\ \text{nm}$, $0.4\ \text{A/W}$ for $660\ \text{nm}$ and $0.25\ \text{A/W}$ for $410\ \text{nm}$ wavelength. The $3\ \text{dB}$ small-signal-bandwidth of the photodiode is above $700\ \text{MHz}$ without slow diffusion effects of photo generated minority carriers [1]. The

photodetector configuration on the IC is the typical 8-photodiode arrangement used by most of the OPU manufacturers [2]. It consists of 4 central segments (A...D) and 4 satellite segments (E...H) used for data detection as well as for laser beam focussing and tracking. Each segment is connected to a programmable transimpedance amplifier (TIA) stage. Compared to classical solutions for the transimpedance amplifiers [3] we used a new architecture that combines a classical TIA with an input current preamplifier. This architecture allows a very flexible gain programming in combination with high-speed and low-noise performance. The IC has 12 different gain settings for read and write applications and additional 17 gain settings in a special write/clip mode programmable with a serial interface. Another critical issue for an OEIC in OPU is the data transmission over the flex cable to the controller unit. We implemented an impedance matching of the output driver stage to the $130\ \Omega$ cable impedance to avoid signal reflexions.

2. OEIC Architecture and Building Blocks

The IC architecture is shown in Figure 1. The 8 photodiode segments (4 central segments A to D and 4 satellite segments E to H) are located in the center. Left and right to the segments the 8 amplifier channels can be seen. Every single photodiode current is amplified to a single-ended output voltage V_A to V_H . In addition a differential signal RFP and RFM for the RF-data output is implemented which is a summation of the central photodiode signals (A to D). Every amplifier channel consists of a current preamplifier (CA to CH) as input stage, followed by a transimpedance amplifier (TA to TH) and an output buffer (Buf). All stages are programmable with a serial I^2C -interface. A DC output reference voltage between $2\ \text{V}$ and $2.4\ \text{V}$ can be applied to an external pin V_{ref} . To avoid channel crosstalk and stability problems, every channel has its own decoder (Dec) with reference voltage and current generation and a power supply filter network is implemented.

Due to the high range of input signal levels for the different operating conditions as read, write and

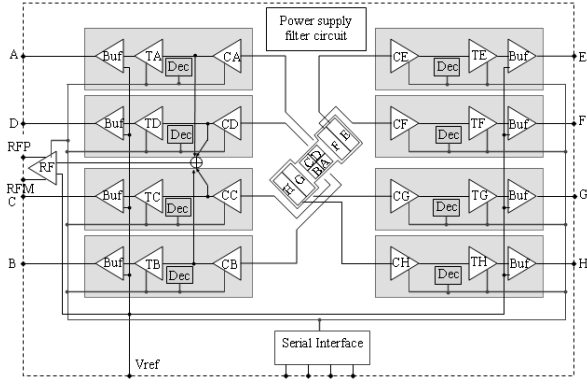


Figure 1. OEIC architecture

write/clip we implemented a large number of different transimpedance gain settings. The gains in read and write operation for the central segments A to D can be programmed between 130Ω and $270k\Omega$ in steps of two. The gain for the satellite segments is even 4 times higher and the differential RF gain is 2/5 of the central segments gain. For the so called write/clip mode additional 17 gains can be programmed. The objective for the write/clip mode is to use a much higher central segments gain as RF-gain compared to the standard write mode. This allows a 'low' level measurement during write with a high central segment gain which is used for tracking calculation. During the write 'high' level a gain clipping circuit for the central segment becomes active. This circuit adaptively reduces the central amplifier gain at the input stage when the input current become too high for maximum central segment output voltage swing. The central segment output voltage swing is reduced to nearly 0 during the 'high' phase. This dramatically decreases the current consumption during write mode.

2.1. Transimpedance Amplifier Architecture

To implement the required number of different gains and operating modes we used a new multistage transimpedance amplifier (TIA) architecture. The TIA for one central segment and the differential RF-amplifier is shown in Figure 2. In difference to a classical TIA solution we used a 2-stage current preamplifier (CA1 and CA2) as input stage followed by a TIA stage and a buffer at the output. The input current $I_{in,c}$ coming from a central segment photodiode is preamplified in the current amplifiers CA1 and CA2 with a gain of $A_{I1,c} * A_{I2,c}$. For the offset compensation of output current $I_{out,c}$ a matched replica of amplifiers CA1 and CA2 are implemented without input current. The output offset current of the replica amplifiers is subtracted from current $I_{out,c}$. The offset compensated current is then feed into a classical TIA with programmable transimpedance $R_{t,c}$. Finally the TIA output voltage is buffered to an output voltage $V_{out,c}$. The output reference voltage V_{ref} is applied to the TIA and buffer amplifier inputs from an external pin.

Also a differential TIA is implemented as shown in Figure 2. The input current of this TIA is the sum of the 4 central segment currents $I_{out,rf}$ coming from a second path in current amplifier CA2. The common-mode output voltage of the differential output buffer is defined by V_{ref} .

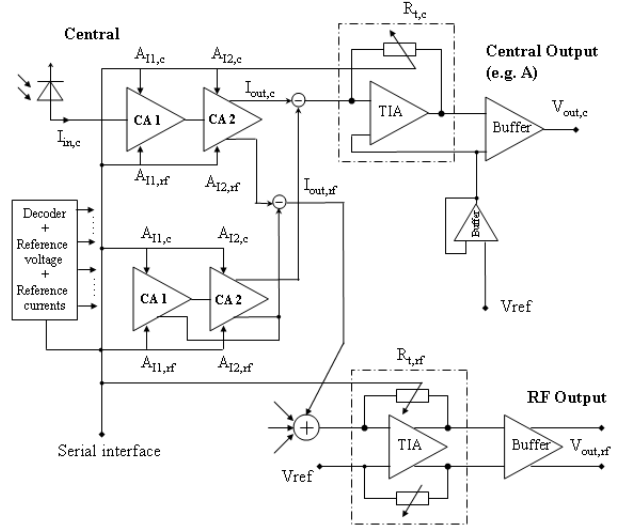


Figure 2. TIA architecture for central and RF channel

All amplifier stages are programmable with the serial interface. The gains of the amplifier stages are shown in Table 1.

Table 1. Gain values of the TIA gain stages

	Central Segments	Satellite Segments
A_{I1}	0.375/1.5/6	0.9/4/16
A_{I2}	0.25/0.5/1/2/4	0.5/1/2/4/8
$A_{I1,rf}$	0.375/1.5/6	
$A_{I2,rf}$	0.25/0.5/1/2/4	
$R_{t,c}$	1.4k Ω /11k Ω	1.4k Ω /11k Ω
$R_{t,rf}$	530 Ω /4k Ω	

2.2. Current Amplifier Circuit

In Figure 3 a simplified schematic of the input current preamplifier stage is shown. The amplifier consists of a programmable regulated current mirror with a capacitive-speed-enhancement circuit (CSE) and a clipping circuit. The current mirror includes 2 bipolar NPN transistors T_1 and T_2 that are regulated with a transconductance amplifier (OTA). The OTA has a high transconductance $g_m = \frac{i_{pm}}{v_{in}}$ which regulates the input node V_{in} to a potential $V_{in,ref}$. Due to this low-impedance input node the pole is shifted to high frequencies even for larger photodiode capacitances. This enables a high amplifier bandwidth which is defined by a dominant pole in node V_{pm} and is quite independent of photodiode size. This current amplifier architecture has the advantage of a simple continuous gain adjustment with a variable voltage source $V_{gain} = V_p - V_m$. Compared to other solutions [4] no

switching in the current signal path is necessary. The current gain G is defined by the Equation(1) with V_T is the thermal voltage of 26mV.

$$G = \frac{I_{out}}{I_{in}} = \exp\left(\frac{V_p - V_m}{V_T}\right). \quad (1)$$

To enable the clipping functionality described in Section 2 an additional clipping circuit block is included. This circuit reduces the amplifier gain in the input stage via voltage source V_{gain} after reaching a defined input current I_{in} level. Therefore the high input currents up to 5mA in write operation are only flowing through the input transistor T_1 and the OTA to ground. This results in a lower current consumption for the write/clip mode compared to the normal write mode.

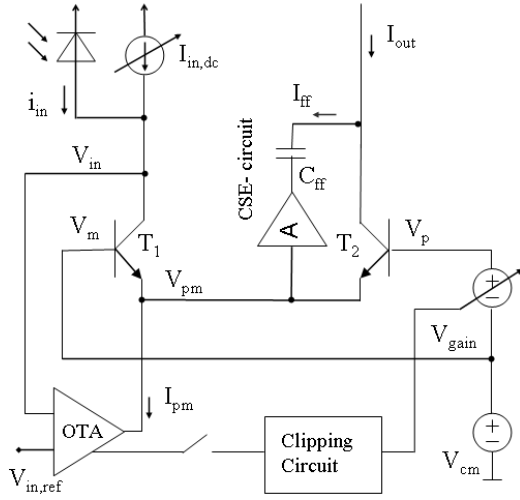


Figure 3. Current amplifier including capacitive-speed enhancement (CSE) and clipping circuit

The noise performance of the circuit is dominated by the shot noise of the transistors T_1 and T_2 . To minimize the input referred noise current, $I_{in,dc}$ must be as low as possible. On the other hand the small-signal-bandwidth of the circuit depends on the transconductance g_m of transistor T_1 and therefore decreases with lower $I_{in,dc}$. To optimize the noise and bandwidth behaviour a capacitive-speed-enhancement circuit (CSE) is included that speeds up the circuit for high gains and low input currents with a capacitive feed-forward path. The circuit consists of a capacitance C_{ff} that adds an additional current I_{ff} to the output current I_{out} according to the relation $I_{ff} = AC_{ff} \frac{dV_{pm}}{dt}$.

2.3. Output Buffer

For RF data transmission over a flex cable an impedance matching is necessary for signal frequencies above 200MHz. Therefore the output buffer stage has a $130 \Omega \pm 15 \Omega$ output impedance matched to the flex cable. The 130Ω impedance is generated with active impedance synthesis. Figure 4 show the circuit concept for a single ended output buffer with a positive feedback path.

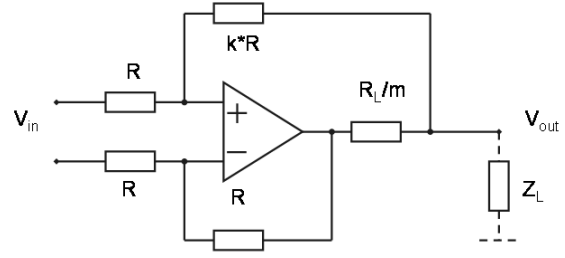


Figure 4. Output buffer

The resistor values for the buffer feedback circuit can be calculated according to Equation(2) with a synthesis factor m and Equation(3) showing the amplifier gain G including load. The factor k defines the relation between m and G . Therefore the integrated output resistor can be m -times smaller than the load resistor R_L matching to the load impedance Z_L . This increases the output voltage dynamic range by a factor of m . In our IC the synthesis factor $m=2$ and gain $G=1.5$. The maximum buffer output voltage swing is 0.8V.

$$m = \frac{k+1}{k-1} \quad (2)$$

$$G = \frac{m+1}{2} \quad (3)$$

3. Measurement Results

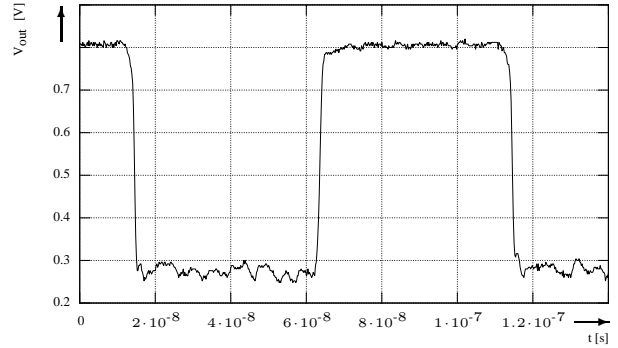


Figure 5. Transient signal of central channel

The IC is mounted in a LGA type package including supply filter caps. For characterization a PCB was developed with external 130Ω load resistor simulating a flex-cable. The measurement setup is fixed on an optical bench. As light source we used laser diodes with a wavelength of 650 nm and 780 nm focused on the chip with optical lenses. The laser diode current is modulated with a pulse generator over a bias-tee circuit. The transient output voltages are measured on the external load resistors with a high impedance probe.

Figure 5 shows a transient pulse of the central segments signal with highest gain value of 270 k Ω . The measured rise/falltime is 1.3 ns. This means a small signal bandwidth of approximately 260 MHz. The eye diagram of the differential RF signal at highest gain is shown in Figure 6. The diagram shows a well opened eye with a 200 Mbit/s pseudo random data signal. Therefore a maximum data rate up to 400 Mbit/s is possible even with the highest transimpedance gain value.

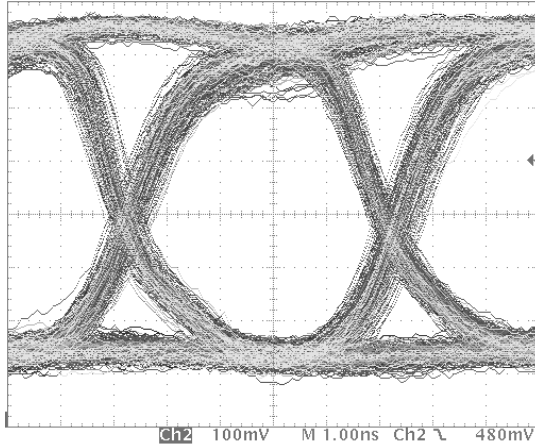


Figure 6. Eyediagram at 200MBit

The write/clip mode behaviour is shown in Figure 7. The diagram includes the input light signal and the clipped central channel output signal. During the 'low' phase of the input signal the output is amplified with a high gain. After input signal is switching to 'high' state the amplifier gain is reduced to a very low value. Therefore the output voltage is decreasing to approximately 0 which decrease the IC current consumption during the write.

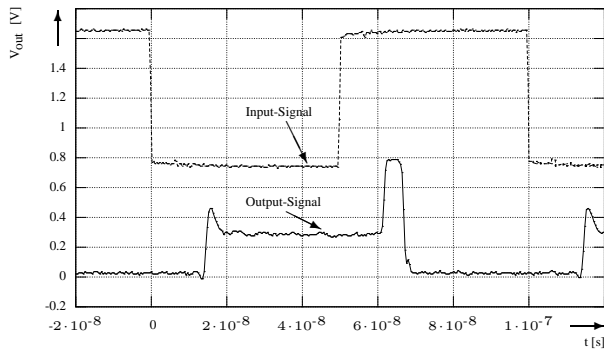


Figure 7. Input signal and clipped output signal

The maximum output voltage swing for the single ended signals and for the differential output signal is 800 mV. The power consumption of the ASIC is 300 mW with a supply voltage of 5 V.

Figure 8 shows a photograph of the ASIC. In the center the 8 photodiodes can be seen. The whole chip except

the photodiodes are covered with a metal plane for light shielding.

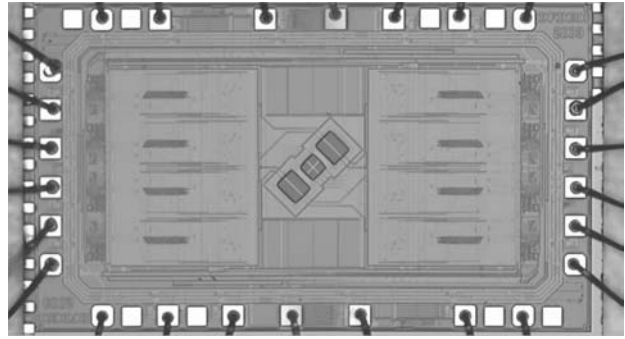


Figure 8. IC photo

4. Conclusion

An optical receiver IC for the data storage applications CD, DVD and "Blue Ray" has been realized. The IC consists of integrated PIN photodiodes connected to programmable transimpedance amplifiers (TIA). The new multistage TIA architecture gives a high flexibility in gain programming for read, write and write/clip operation mode with 29 different gain settings. A special write/clip mode with active gain control in the input stage is implemented. The rise/fall time for the central segments is 1.3 ns which means a small-signal-bandwidth of 260 MHz for the highest gain of 270 k Ω . In combination with the photodiodes this leads to a sensitivity of 100 $\frac{mV}{\mu W}$ which is an improvement by a factor of 2 compared to other publications [4]. For an optimized RF data transmission the amplifier output buffers are matched to the 130 Ω flex cable impedance. To improve the amplifier output dynamic range the impedance is generated by an active impedance synthesis with a synthesis factor of 2.

5. Acknowledgment

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