MOTOROLA

SN74LS295A

4-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

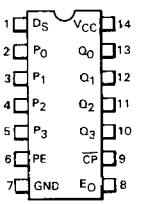
DESCRIPTION — The SN74LS295A is a 4-Bit Shift Register with serial and parallel synchronous operating modes, and independent 3-state output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfers and shifting occur synchronous with the HIGH to LOW clock transition.

The 3-State output buffers are controlled by an active HIGH Output Enable input (EO). Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion.

The LS295A is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **NEGATIVE EDGE-TRIGGERED CLOCK INPUT**
- **PARALLEL ENABLE MODE CONTROL INPUT**
- **3-STATE BUSSABLE OUTPUT BUFFERS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

CONNECTION DIAGRAM
DIP (TOP VIEW)



J Suffix — Case 632-07 (Ceramic)
N Suffix — Case 646-05 (Plastic)

PIN NAMES

		LOADING (Note a) HIGH	LOW
PE	Parallel Enable Input	0.5 U.L.	0.25 U.L.
D_S	Serial Data Input	0.5 U.L.	0.25 U.L.
P_0—P_3	Parallel Data Input	0.5 U.L.	0.25 U.L.
$\overline{E_O}$	Output Enable Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock Pulse (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
Q_0—Q_3	3-State Outputs	10 U.L.	5 U.L.

NOTE:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

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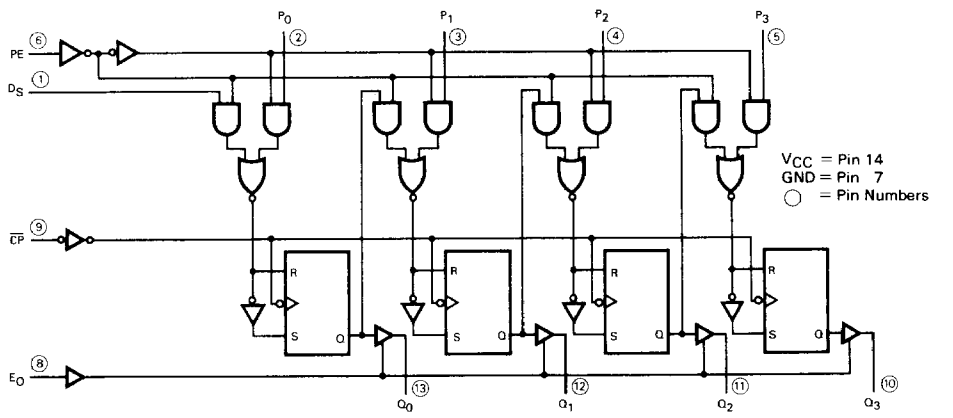
LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The LS295A is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial Data (D_S) and four Parallel Data (P_0–P_3) inputs and four parallel 3-State output buffers (Q_0–Q_3). When the Parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data Inputs (P_0—P_3) into the register synchronous with the HIGH to LOW transition of the Clock ($\overline{CP}$). When the PE is LOW, a HIGH to LOW transition on the clock transfers the serial data on the D_S input to register Q_0, and shifts data from Q_0 to Q_1, Q_1 to Q_2 and Q_2 to Q_3. The input data and parallel enable are fully edge-triggered and must be stable only one set-up time before the HIGH to LOW clock transition.

The 3-State output buffers are controlled by an active HIGH Output Enable input (E_O). When the E_O is HIGH, the four register outputs appear at the Q_0—Q_3 outputs. When E_O is LOW, the outputs are forced to a high impedance "off" state. The 3-State output buffers are completely independent of the register operation,i.e., the input transitions on the E_O input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-State devices whose outputs are tied together are designed so there is no overlap.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS*			
	PE	$\overline{CP}$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift Right	l	⎍	l	X	L	q_0	q_1	q_2
	h	⎍	h	X	H	q_0	q_1	q_2
Parallel Load	h	⎍	X	p_n	p_0	p_1	p_2	p_3

*The indicated data appears at the Q outputs when E_O is HIGH. When E_O is LOW, the indicated data is loaded into the register, but the outputs are all forced to the high impedance "off" state.

L = LOW Voltage Levels
H = HIGH Voltage Levels
X = Don't Care
$p_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.
l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

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GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current — High			−0.4	mA
I_{OL}	Output Current — Low			8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage		−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA
I_{OZH}	Output Off Current HIGH			20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V
I_{OZL}	Output Off Current LOW			−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V
I_{IH}	Input HIGH Current			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current	−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				mA	V_{CC} = MAX, E_O = 4.5 V, $\overline{CP}$ momentary 3.0 V, then GND
	Total, Output HIGH			29		V_{CC} = MAX, E_O = GND, $\overline{CP}$ = GND
	Total, Output LOW			33		

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	30	45		MHz	C_L = 15 pF, V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay Clock to Output		14 19	20 30	ns	
t_{PZH}	Output Enable Time to HIGH LEVEL		18	26	ns	
t_{PZL}	Output Enable Time to LOW Level		20	30	ns	
t_{PLZ}	Output Disable Time from LOW Level		13	20	ns	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level		13	20	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width	16			ns	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_s	Data Setup Time	20			ns	
t_h	Data Hold Time	0			ns	

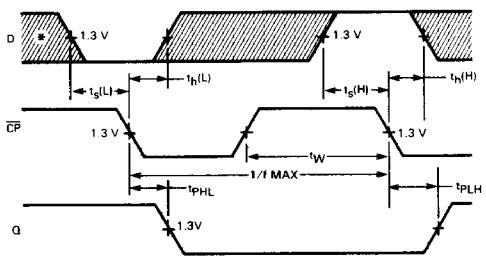
DEFINITION OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

- The shaded areas indicate when the input is permitted to change for predictable output performance.



*The Data Input is D_S for PE = LOW and P_n for PE = HIGH.

Fig. 1

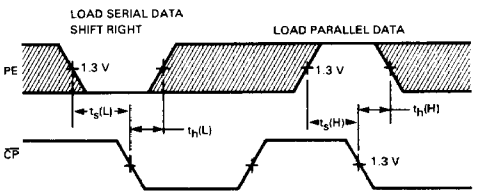


Fig. 2

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