54F/74F547

Octal Decoder/Demultiplexer With Address Latches and Acknowledge

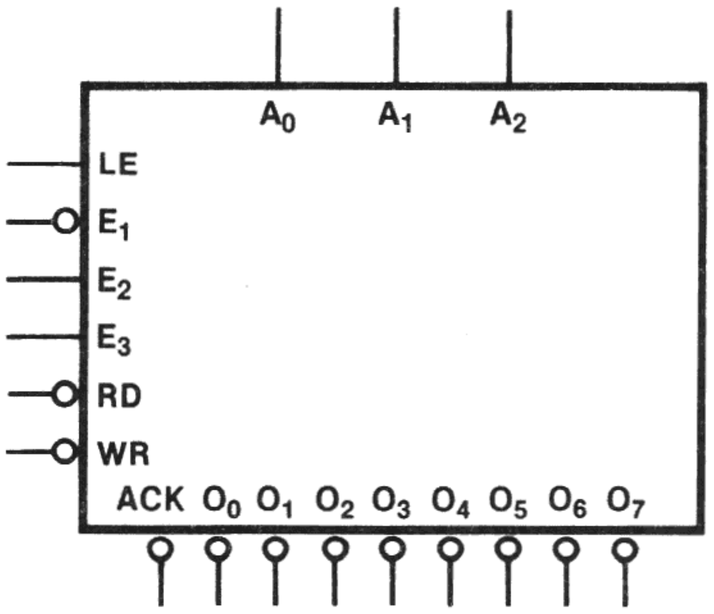
Description

The 'F547 is a 3-to-8 line address decoder with latches for address storage. Designed primarily to simplify multiple chip selection in a microprocessor system, it contains one active LOW and two active HIGH Enables to conserve address space. Also included is an active LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

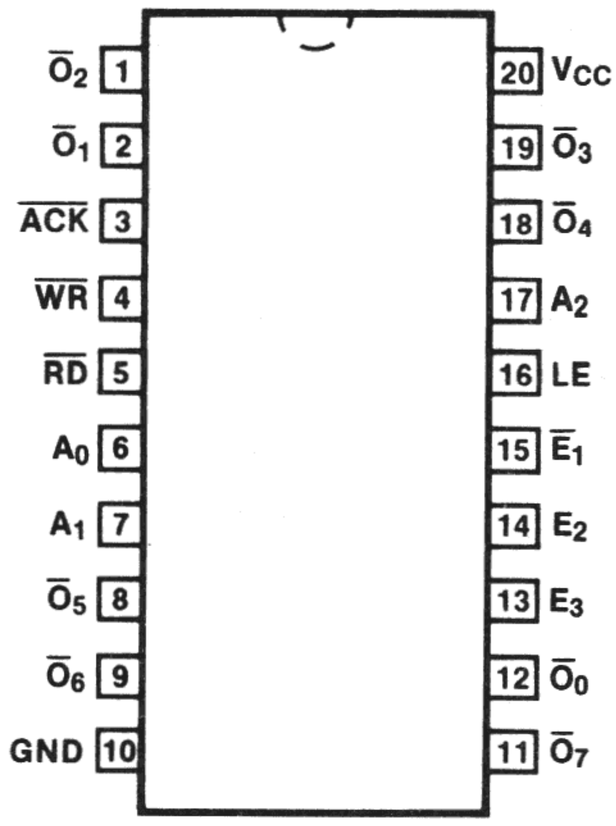
- **3-to-8 Line Address Decoder**
- **Address Storage Latches**
- **Multiple Enables for Address Extension**
- **Open Collector Acknowledge Output**

Ordering Code: See Section 5

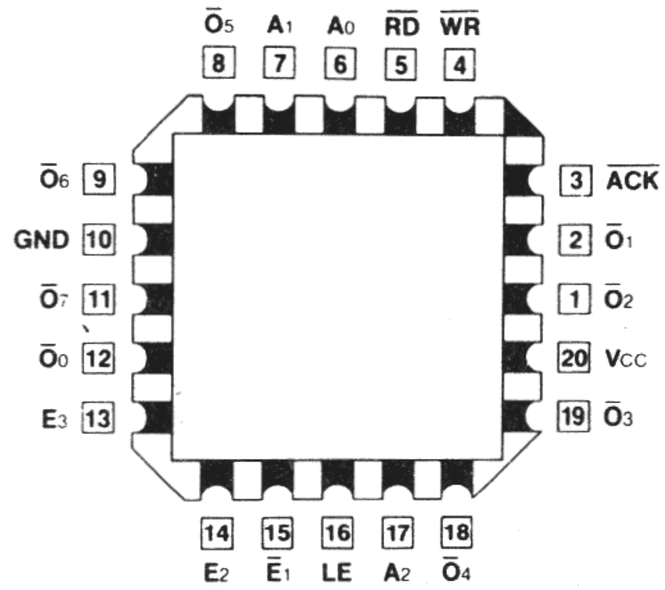
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_2	Output Select Address Inputs	0.5/0.375
$\overline{E}_1$	Chip Enable Input (Active LOW)	0.5/0.375
E_2, E_3	Chip Enable Inputs	0.5/0.375
LE	Latch Enable Input	0.5/0.375
$\overline{RD}$	Read Acknowledge Input (Active LOW)	0.5/0.375
$\overline{WR}$	Write Acknowledge Input (Active LOW)	0.5/0.375
$\overline{ACK}$	Open Collector Acknowledge Output (Active LOW)	OC*/12.5
$\overline{O}_0$-$\overline{O}_7$	Decoded Outputs (Active LOW)	25/12.5

*OC = Open Collector

Functional Description

When enabled, the 'F547 accepts the A_0-A_2 Address inputs and decodes them to select one of eight active LOW, mutually exclusive outputs, as shown in the Decoder Truth Table. With LE HIGH, the Address latches are transparent and the output selection changes each time the A_0-A_2 address changes. When LE is LOW, the latches store the last valid address preceding the HIGH-to-LOW transition of the LE input signal. For applications in which the separation of latch enable and chip enable functions is not required, LE and $\overline{E}_1$ can be tied together, such that when HIGH the outputs are OFF and the latches are transparent, and when LOW the latches are storing and the selected output is enabled.

The open collector Acknowledge ($\overline{ACK}$) output is normally HIGH (i.e. OFF) and goes LOW when $\overline{E}_1$, E_2 and E_3 are all active and either the Read ($\overline{RD}$) or Write ($\overline{WR}$) input is LOW, as indicated in the Acknowledge Truth Table.

Acknowledge Truth Table

Inputs					Output
$\overline{E}_1$	E_2	E_3	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
L	H	H	H	H	H
L	H	H	L	X	L
L	H	H	X	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Latch and Output Status Table

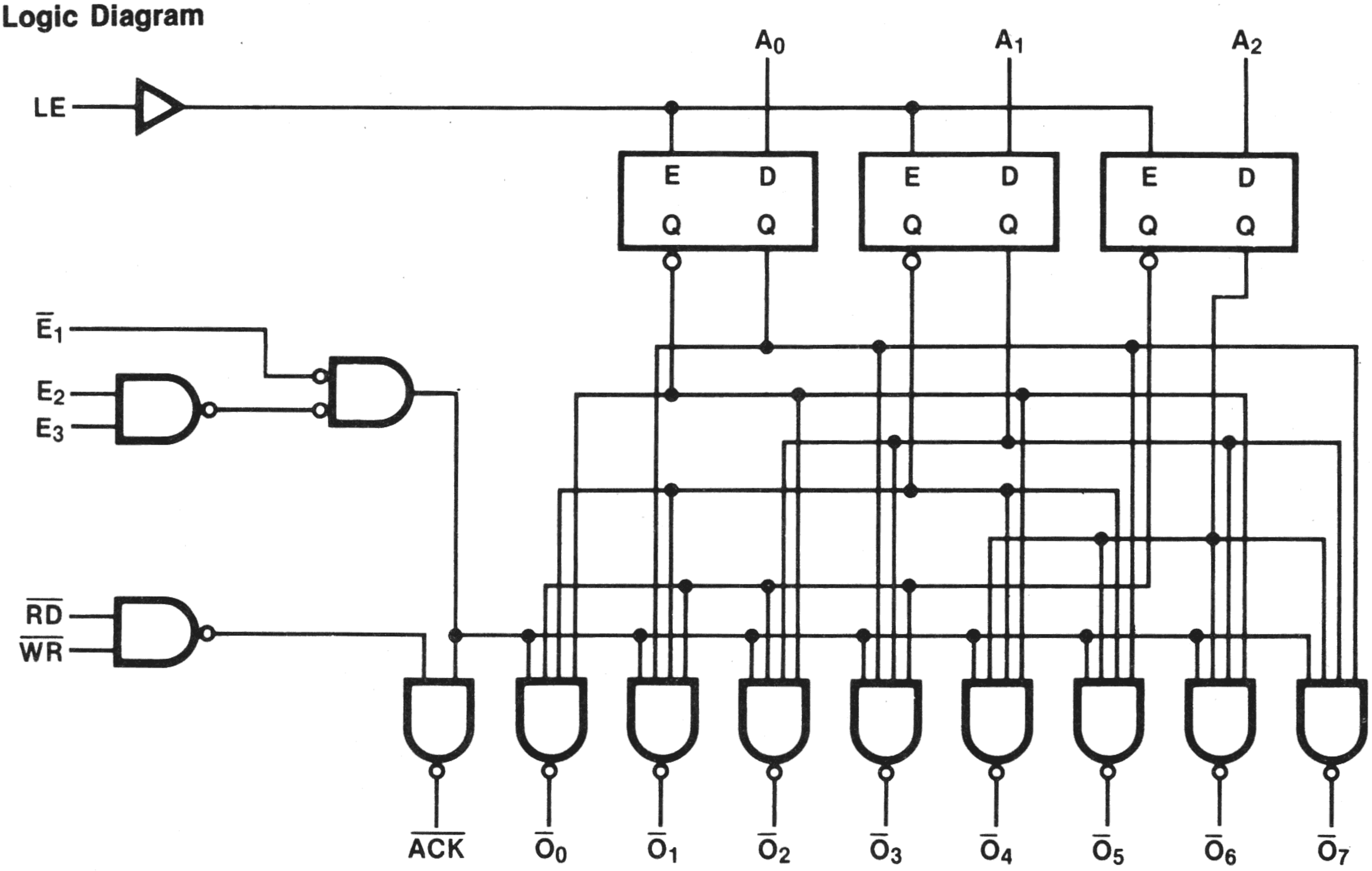
Inputs				Latch	Decoder
$\overline{E}_1$	E_2	E_3	LE	Status	Outputs
L	H	H	H	Transparent	—
L	H	H	L	Storing	Selected Output LOW
H	X	X	X	Storing	All Outputs HIGH
X	L	X	X	Storing	All Outputs HIGH
X	X	L	X	Storing	All Outputs HIGH

Decoder Truth Table*

Inputs			Outputs							
A_2	A_1	A_0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H
L	H	L	H	H	L	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H
H	L	H	H	H	H	H	H	L	H	H
H	H	L	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	L

*Assuming $\overline{E}_1$, LOW; E_2 and E_3, HIGH

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		17	25	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$ $C_L = 50\,pF$			T_A, V_{CC} = Mil $C_L = 50\,pF$		T_A, V_{CC} = Com $C_L = 50\,pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	4.0 5.0	7.0 9.0	9.0 12.0	3.0 5.0	10.5 13.0	4.0 5.0	10.0 13.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ to $\overline{O}_n$	4.0 4.0	6.5 6.5	8.5 8.5	3.0 3.5	10.0 10.0	4.0 4.0	9.5 9.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	4.0 5.0	7.5 14.5	9.5 18.0	4.0 5.0	11.5 20.0	4.0 5.0	10.5 19.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay E_2 or E_3 to $\overline{O}_n$	5.0 5.0	8.5 8.5	11.0 11.0	4.5 4.5	12.5 12.5	5.0 5.0	12.0 12.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{RD}$ or $\overline{WR}$ to $\overline{ACK}$	6.5 4.0	11.0 7.5	14.0 9.5	6.5 3.5	16.0 11.0	6.5 4.0	15.0 10.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay E_2 or E_3 to $\overline{ACK}$	8.0 5.0	13.0 8.5	16.5 11.0	8.0 5.0	18.5 12.5	8.0 5.0	17.5 12.0	ns	3-1 3-3

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to LE	5.0 5.0			5.0 5.0		5.0 5.0		ns	3-15
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to LE	6.0 6.0			6.0 6.0		6.0 6.0			
$t_w(H)$	LE Pulse Width, HIGH	6.0			6.0		6.0		ns	3-7

54F/74F DC Family Characteristics[1]

Symbol	Parameter		Limits[2] Min	Limits[2] Typ[3]	Limits[2] Max	Units	V_{CC}[4]	Conditions[2]
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal over Recommended V_{CC} and T_A Range
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage Std/3-State[6]	Mil	2.5	3.4		V	Min	I_{OH} = -1 mA
		Com[7]	2.7	3.4				
	Output HIGH Voltage 3-State/Line Driver[6]	Mil	2.4	3.3		V	Min	I_{OH} = -3 mA
		Com[7]	2.7	3.3				
	Output HIGH Voltage Line Driver[6]	Mil	2.0	3.2		V	Min	I_{OH} = -12 mA
		Com[7]	2.0	3.1				I_{OH} = -15 mA
V_{OL}	Output LOW Voltage Standard[6]	Mil		0.30	0.5	V	Min	I_{OL} = 20 mA
		Com		0.30	0.5			
	Output LOW Voltage 3-State[6]	Mil		0.30	0.5	V	Min	I_{OL} = 20 mA
		Com		0.35	0.5			I_{OL} = 24 mA
	Output LOW Voltage Line Driver[6]	Mil		0.38	0.55	V	Min	I_{OL} = 48 mA
		Com		0.42	0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current	0.5 U.L.			20	μA	Max	V_{IN} = 2.7 V
		n U.L.			n(40)			I_{IH} = 40 μA Multiplied by Input HIGH U.L. Shown on Data Sheet
	Input HIGH Current Breakdown Test, Std Inputs				100	μA	Max	V_{IN} = 7.0 V
	Input HIGH Current Breakdown Test, Transceivers				1.0	mA	Max	V_{IN} = 5.5 V
I_{IL}	Input LOW Current	0.375 U.L.			-0.6	mA	Max	I_{IL} = -1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet, V_{IN} = 0.5 V
		n U.L.			n(-1.6)			
I_{OZH}	3-State Output OFF Current HIGH				50	μA	Max	V_{OUT} = 2.7 V
I_{OZL}	3-State Output OFF Current LOW				-50	μA	Max	V_{OUT} = 0.5 V
I_{OH}	Open Collector Output Leakage Current				100	μA	Min	$V_{IN} = V_{IH}/V_{IL}$ $V_{OUT} = V_{CC}$
I_{OS}[5]	Output Short-Circuit Current	Std/3-State[6]	-60		-150	mA	Max	V_{OUT} = 0 V
		Line Driver[6]	-100		-225			

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to $T_A = +25°C$ and $V_{CC} = +5.0$ V.
4. Min and Max refer to the values listed in the table of recommended operating conditions.
5. For I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
6. Refers to the type of output pull-up/pulldown circuitry used for the particular device. Standard outputs may be identified by an Output HIGH/LOW fan-out of 25/12.5 U.L.; 3-State outputs may be identified by an Output HIGH/LOW fan-out of 75/15 (12.5) U.L.; Line Driver outputs may be identified by an Output HIGH/LOW fan-out of 75/40 (30) U.L.
7. Refers to ±5% V_{CC} specifications. ±10% V_{CC} Commercial limits are the same as the Military limits.

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Ordering Information/ Package Outlines

The Product Index and Selection Guide in Section 1 lists only the basic device numbers. This basic number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F 402 P C QR

Temperature Range Family
74F = Commercial FAST
54F = Military FAST
29F = Commercial or Military FAST

Device Type

Package Code
P = Plastic DIP
SP = Slim Plastic DIP
D = Ceramic DIP
SD = Slim Ceramic DIP
F = Flatpak
L1 = Ceramic Leadless Chip Carrier (LCC)
Q = Plastic Chip Carriers (PCC)
S = Small Outline Package (SOIC)

Temperature Range
C = Commercial
M = Military

Special Variations
QR = Commercial grade device with burn-in
QB = Military grade device with environmental and burn-in processing

Package	Package Code
Plastic DIP	P
Slim Pastic DIP	SP
Ceramic DIP	D
Slim Ceramic DIP	SD
Flatpak	F
Ceramic Leadless Chip Carrier (LCC)	L1
Plastic Chip Carrier (PCC)	Q
Small Outline, 150 mils (SOIC)	S
Small Outline, 300 mils (SOIC)	V

Temperature Range	Temperature Code
Commercial 0°C to +70°C	C
Military −55°C to +125°C	M

Package Outlines

The package outlines indicated above are shown in the detailed outline drawings in this section.