SLG47004

GreenPAK Programmable Mixed-Signal Matrix
with In-System Programmability and Advanced Analog Features

The SLG47004 provides a small, low power component for commonly used analog signal processing and mixed-signal functions. Individual, tunable, analog components used in conjunction with configurable logic provide a way to solve a wide variety of tasks with minimal costs. The user creates their circuit design by programming the Non-Volatile Memory (NVM) to configure the interconnect logic, the analog and digital macrocell, and the IO Pins of the SLG47004.

Features

- Two Programmable Bandwidth Op Amps
  - 3-Op Amp Instrumentation Amplifier Function (including Additional Internal Op Amp)
  - Rail to Rail Input
  - Low Quiescent Current
  - Low Offset Voltage
  - Analog Comparator Mode
  - Optional V_{REF} Voltage Connection for In put Pins
- Two 1024 Position Digital Rheostats
  - User Defined Auto-Trim Option
  - Manual Control Option
  - I^2C Control Option
  - Potentiometer Mode
- Two Single-Pole/Single-Throw Analog Switches
  - Voltage or Current Source/Sink Mode
- One Low Offset Chopper Comparator
- Two Low Power General Purpose ACMPs
  - ACMP Sampling Mode
  - Hysteresis with Independently-Selectable Thresholds
- Three Voltage References
  - Two ACMP V_{REF} Output Buffers
  - One High Drive Buffer
- Thirteen Combination Function Macrocells
  - Three Selectable DFF/LATCH or 2-bit LUTs
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Seven Selectable DFF/LATCH or 3-bit LUTs
  - One Selectable Pipe Delay or Ripple Counter or 3-bit LUT
  - One Selectable DFF/LATCH or 4-bit LUT
- Seven Multi-Function Macrocells
  - Six Selectable DFF/LATCH or 3-bit LUTs + 8-bit Delay/Counters
  - One Selectable DFF/LATCH or 4-bit LUT + 16-bit Delay/Counter
- Serial Communications
  - I^2C Protocol Interface
- 2-kbit (256 x 8) I^2C-Compatible (2-Wire) Serial EEPROM Emulation with Software Write Protection
- Programmable Delay with Edge Detector Output
- Deglitch Filter or Edge Detector
- Three Oscillators
  - 2.048 kHz Oscillator
  - 2.048 MHz Oscillator
  - 25 MHz Oscillator
- Analog Temperature Sensor
- Power-On-Reset
- In-System Debug
- Multiple Time Programmable Memory in Development
- Wide Range Power Supply
  - 2.5 V (±4 %) to 5 V (±10 %) V_{DD}
- Ambient Operation Temperature Range: -40 °C to 85 °C
- RoHS Compliant/Halogen-Free
- Package Available
  - 24-pin STQFN: 3 mm x 3 mm x 0.55 mm, 0.4 mm pitch

Applications

- Adjust Precision Threshold
- Sensor Offset Trimming/Calibration
- Tunable Analog Filters
- Operational Amplifier Adjustable Gain and Offset
- Adjustable Voltage-to-Current Conversions
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics
- Smartphones and Fitness Bands
- Notebook and Tablet PCs

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1. Block Diagram

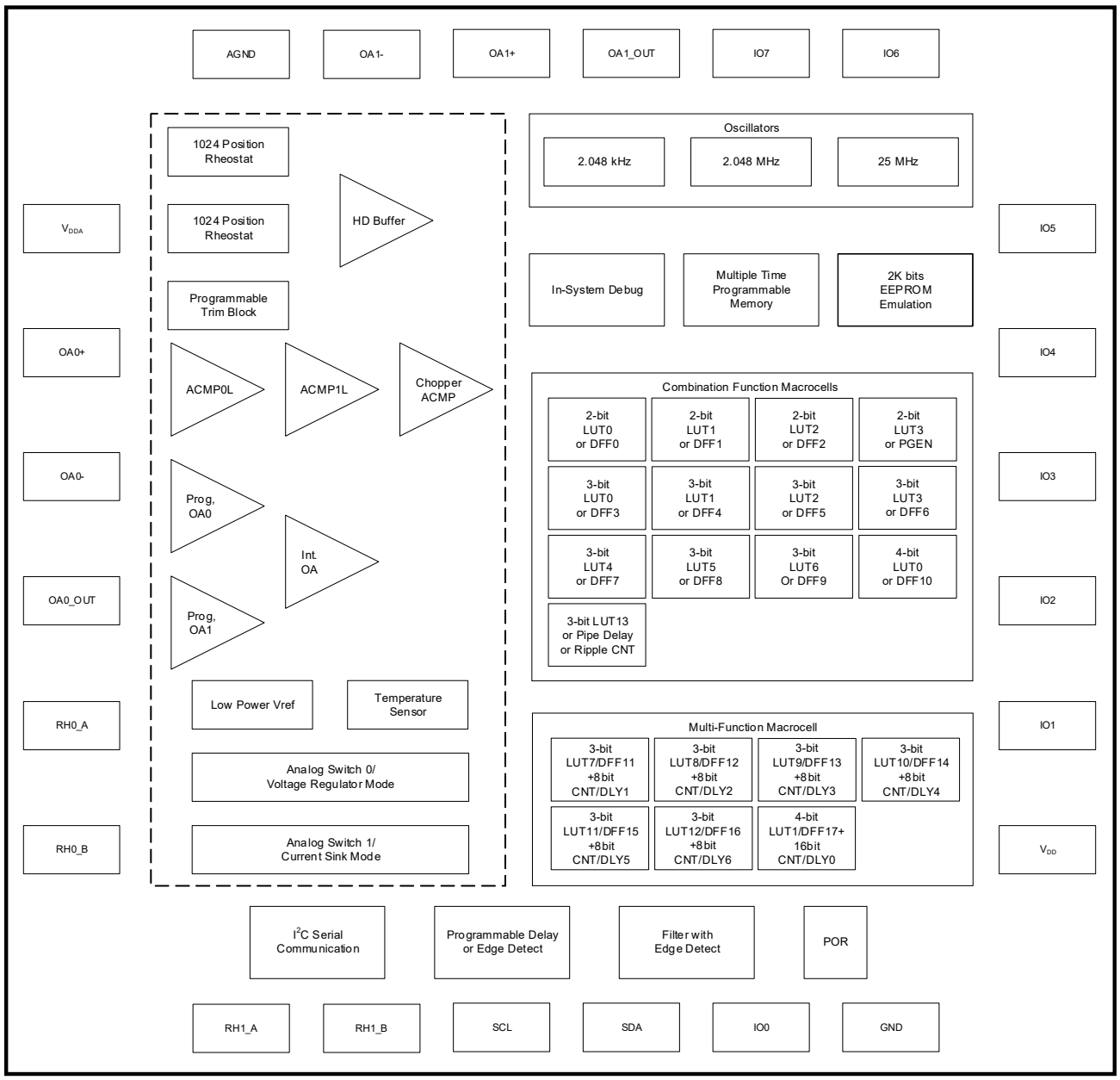


Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignments

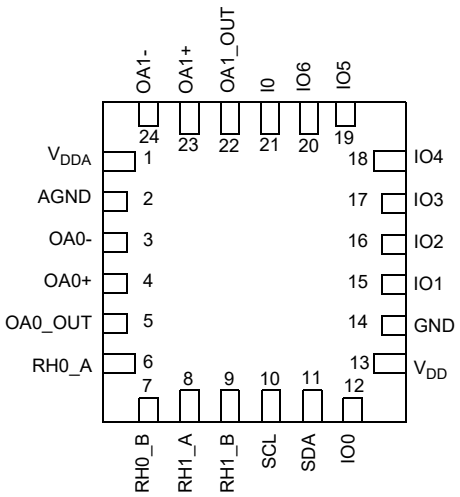


Figure 2. Pin Assignments - STQFN-24 (Top View)

2.2 Pin Descriptions

Table 1. Pin Description

Pin Number	Pin Name	Description
1	V_{DDA}	Analog Power Supply
2	AGND	Analog Ground
3	OA0-	Op Amp0 Inverting Input
4	OA0+	Op Amp0 Non-Inverting Input
5	OA0_OUT	Op Amp0_OUT/ACMP0L+
6	RH0_A	Digital Rheostat 0 Terminal A
7	RH0_B	Digital Rheostat 0 Terminal B
8	RH1_A	Digital Rheostat 1 Terminal A
9	RH1_B	Digital Rheostat 1 Terminal B
10	SCL	I^2C_SCL
11	SDA	I^2C_SDA
12	IO0	GPIO, ACMP0L-, ACMP1L-, EXT_OSC0_IN, V_{REF}0_Out or Temp_Sens_Out
13	V_{DD}	Digital Power Supply
14	GND	Digital Ground
15	IO1	GPIO, Chop_ACMP+, Vref1_OUT or Temp_Sens_Out, EXT_OSC1_IN or SLA_0
16	IO2	GPIO, ACMP0L+, EXT_OSC2_IN, SLA_1
17	IO3	GPIO, AS_1_A, ACMP1L+ or SLA_2
18	IO4	GPIO, AS_1_B, Chop_ACMP-or SLA_3
19	IO5	GPIO, AS_0_B
20	IO6	GPIO, AS_0_A, HD_Buff_Out, In Amp_V_{REF}
21	I0	GPI, In Amp_OUT
22	OA1_OUT	Op Amp1_OUT, ACMP1L+

Table 1. Pin Description (Cont.)

Pin Number	Pin Name	Description
23	OA1+	Op Amp1 Non-inverting Input
24	OA1-	Op Amp1 Inverting Input

Table 2. Functional Pin Description

Pin Number STQFN 24L	Pin Name	Signal Name	Function	Input Options	Output Options
1	V_{DDA}	V_{DDA}	Analog Power Supply	-	-
2	AGND	AGND	Analog Ground	-	-
3	OA0-	OA0-	Op Amp0 Inverting Input	Analog	-
4	OA0+	OA0+	Op Amp0 Non-Inverting Input	Analog	-
5	OA0_OUT	OA0_OUT	Op Amp0 Output	-	Analog
		ACMP0L+	Analog Comparator 0 Positive Input	Analog	-
6	RH0_A	RH0_A	Digital Rheostat 0 Terminal A	-	-
7	RH0_B	RH0_B	Digital Rheostat 0 Terminal B	-	-
8	RH1_A	RH1_A	Digital Rheostat 1 Terminal A	-	-
9	RH1_B	RH1_B	Digital Rheostat 1 Terminal B	-	-
10	SCL	SCL	I^2C Serial Clock	-	-
11	SDA	SDA	I^2C Serial Data	-	-
12	IO0	IO0	General Purpose IO	-	-
		ACMP0L-	Analog Comparator 0 Negative Input	Analog	-
		ACMP1L-	Analog Comparator 1 Negative Input	Analog	-
		EXT_OSC0_IN	External Clock Connection	-	-
		V_{REF}0_Out	Voltage Reference 0 Output	-	Analog
		Temp_Sens_Out	Temperature Sensor Output	-	Analog
13	V_{DD}	V_{DD}	Digital Power Supply	-	-
14	GND	GND	Digital Ground	-	-
15	IO1	IO1	General Purpose IO	-	-
		CHOP_ACMP+	Chopper ACMP Positive Input	Analog	-
		Temp_Sens_Out	Temperature Sensor Output	-	Analog
		EXT_OSC1_IN	External Clock Connection	-	-
		SLA_0	Target Address 0	-	-

Table 2. Functional Pin Description (Cont.)

Pin Number STQFN 24L	Pin Name	Signal Name	Function	Input Options	Output Options
16	IO2	IO2	General Purpose IO	-	-
		ACMP0L+	Analog Comparator 0 Positive Input	Analog	-
		EXT_OSC2_IN	External Clock Connection	-	-
		SLA_1	Target Address 1	-	-
17	IO3	IO3	General Purpose IO	-	-
		AS_1_A	Analog Switch 1 Input A	Analog	Analog
		ACMP1L+	Analog Comparator 1 Positive Input	-	-
		SLA_2	Target Address 2	-	-
18	IO4	IO4	General Purpose IO	-	-
		AS_1_B	Analog Switch 1 Input B	Analog	Analog
		CHOP_ACMP-	Chopper ACMP Negative Input	Analog	-
		SLA_3	Target Address 3	-	-
19	IO5	IO5	General Purpose IO	-	-
		AS_0_B	Analog Switch 0 Input B	Analog	Analog
20	IO6	IO6	General Purpose IO	-	-
		AS_0_A	Analog Switch 0 Input A	Analog	Analog
		HD_Buffer_Out	High Drive Buffer Out put	-	Analog
		In Amp_V_{REF}	Instrumentation Amplifier Voltage Reference	Analog	-
21	I0	I0	General Purpose Input	-	-
		In Amp Out	Instrumentation Amplifier Output	Analog	-
22	OA1_OUT	OA1_OUT	Op Amp1 Output	-	Analog
		ACMP1L+	Analog Comparator 1 Positive Input	Analog	-
23	OA1+	OA1+	Op Amp1 Non-inverting Input	Analog	-
24	OA1-	OA1-	Op Amp1 Inverting Input	Analog	-

Table 3. Pin Type Definitions

Pin type	Definition
V_{DDA}	Analog Power Supply
AGND	Analog Ground
OA-	Op Amp Inverting Input
OA+	Op Amp Non-Inverting Input
OA_OUT	Op Amp Output
RH_A	Digital Rheostat Terminal A

Table 3. Pin Type Definitions

Pin type	Definition
RH_B	Digital Rheostat Terminal B
SCL	I^2C Serial Clock
SDA	I^2C Serial Data
IO	General Purpose Input/Output
V_{DD}	Digital Power Supply
GND	Digital Ground
I	General Purpose Input

3. Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Analog and digital grounds must be connected together on the PCB board. The place of connection depends on users schematic. For application cases with low digital current of SLG47004, both AGND and GND should be connected to analog ground plane.

Parameter		Min	Max	Unit
V_{DD} to GND, V_{DDA} to AGND [1]		-0.3	7	V
Maximum Slew Rate of V_{DDA}		-	2	V/µs
Voltage at Input Pin		GND-0.3	V_{DD}+0.3	V
Current at Input Pin		-1.0	1.0	mA
Maximum Average or DC Current through V_{DDA} or AGND Pin (Per chip side)	T_J = 85 °C	-	110	mA
	T_J = 110 °C	-	50	
Maximum Average or DC Current through V_{DD} or GND Pin (Per chip side)	T_J = 85 °C	-	100	
	T_J = 110 °C	-	50	
Input Leakage (Absolute Value)		-	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		-	150	°C
Thermal Resistance [2]		-	132	°C/W
Moisture Sensitivity Level		1		

1. V_{DDA} must be equal to V_{DD}.
2. Measurements based on Analog Switches.

3.2 Electrostatic Discharge Ratings

Parameter	Value	Unit
ESD protection (human body model)	2000	V
ESD protection (charged device model)	1300	V

3.3 Recommended Operating Conditions

Parameter	Conditions	Min	Max	Unit
Supply Voltage (V_{DDA})	-	2.4	5.5	V
	During NVM Write and Erase Commands	2.5	5.5	V
Operating Ambient Temperature	-	-40	+85	°C
Capacitor Value at V_{DD}	-	0.1	-	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	-0.2	V_{DDA}+0.2	V

3.4 Electrical Specifications

T_A = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-level Input Voltage	V_{IH}	Logic input [1]	0.7x V_{DD}	-	V_{DD}+ 0.3	V
		Logic input with Schmitt trigger	0.8x V_{DD}	-	V_{DD}+ 0.3	V
		Low-level logic input [1]	1.25	-	V_{DD}+ 0.3	V
Low-level Input Voltage	V_{IL}	Logic input [1]	GND-0.3	-	0.3x V_{DD}	V
		Logic Input with Schmitt trigger	GND-0.3	-	0.2x V_{DD}	V
		Low-level logic input [1]	GND-0.3	-	0.5	V
Schmitt Trigger Hysteresis Voltage	V_{HYS}	V_{DD} = 2.5 V +/- 8 %	0.30	0.43	0.58	V
		V_{DD} = 3.3 V +/- 10 %	0.34	0.46	0.60	V
		V_{DD} = 5 V +/- 10 %	0.45	0.58	0.77	V
Maximal Voltage Applied to any PIN in High Impedance State	V_O		-	-	V_{DD}+ 0.3	V
High-level Output Voltage	V_{OH}	Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = 2.4 V	2.282	-	-	V
		Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = 2.5 V	2.387	-	-	V
		Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = 2.7 V	2.597	-	-	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.0 V	2.709	-	-	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V	3.037	-	-	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V	3.359	-	-	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = 4.5 V	4.161	-	-	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = 5.0 V	4.687	-	-	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = 5.5 V	5.213	-	-	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = 2.4 V	2.342	-	-	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = 2.5 V	2.445	-	-	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = 2.7 V	2.649	-	-	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.0 V	2.859	-	-	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V	3.171	-	-	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V	3.481	-	-	V
		Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = 4.5 V	4.333	-	-	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-level Output Voltage	V_{OH}	Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = 5.0 V	4.845	-	-	V
		Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = 5.5 V	5.356	-	-	V
Low-level Output Voltage	V_{OL}	Push-Pull, 1x Drive, I_{OL}= 1 mA, V_{DD} = 2.4 V	-	-	0.085	V
		Push-Pull, 1x Drive, I_{OL}= 1 mA, V_{DD} = 2.5 V	-	-	0.082	V
		Push-Pull, 1x Drive, I_{OL}= 1 mA, V_{DD} = 2.7 V	-	-	0.077	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.0 V	-	-	0.218	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V	-	-	0.202	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V	-	-	0.190	V
		Push-Pull, 1x Drive, I_{OL}= 5 mA, V_{DD} = 4.5 V	-	-	0.277	V
		Push-Pull, 1x Drive, I_{OL}= 5 mA, V_{DD} = 5.0 V	-	-	0.260	V
		Push-Pull, 1x Drive, I_{OL}= 5 mA, V_{DD} = 5.5 V	-	-	0.245	V
		Push-Pull, 2x Drive, I_{OL}= 1 mA, V_{DD} = 2.4 V	-	-	0.043	V
		Push-Pull, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.5 V	-	-	0.042	V
		Push-Pull, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.7 V	-	-	0.039	V
		Push-Pull, 2x Drive, I_{OL}= 3 mA, V_{DD} = 3.0 V	-	-	0.109	V
		Push-Pull, 2x Drive, I_{OL}= 3 mA, V_{DD} = 3.3 V	-	-	0.102	V
		Push-Pull, 2x Drive, I_{OL}= 3 mA, V_{DD} = 3.6 V	-	-	0.096	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = 4.5 V	-	-	0.143	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5.0 V	-	-	0.136	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5.5 V	-	-	0.127	V
		NMOS OD, 1x Drive, I_{OL}= 1 mA, V_{DD} = 2.4 V	-	-	0.035	V
		NMOS OD, 1x Drive, I_{OL} = 1 mA, V_{DD} = 2.5 V	-	-	0.034	V
		NMOS OD, 1x Drive, I_{OL} = 1 mA, V_{DD} = 2.7 V	-	-	0.032	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.0 V	-	-	0.088	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V	-	-	0.082	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V	-	-	0.078	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low-level Output Voltage	V_{OL}	NMOS OD, 1x Drive, I_{OL} = 5 mA, V_{DD} = 4.5 V	-	-	0.114	V
		NMOS OD, 1x Drive, I_{OL} = 5 mA, V_{DD} = 5.0 V	-	-	0.108	V
		NMOS OD, 1x Drive, I_{OL} = 5 mA, V_{DD} = 5.5 V	-	-	0.103	V
		NMOS OD, 2x Drive, I_{OL}= 1 mA, V_{DD} = 2.4 V	-	-	0.019	V
		NMOS OD, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.5 V	-	-	0.019	V
		NMOS OD, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.7 V	-	-	0.018	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.0 V	-	-	0.047	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V	-	-	0.044	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V	-	-	0.042	V
		NMOS OD, 2x Drive, I_{OL} = 5 mA, V_{DD} = 4.5 V	-	-	0.063	V
		NMOS OD, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5.0 V	-	-	0.060	V
		NMOS OD, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5.5 V	-	-	0.057	V
High-level Output Current [2]	I_{OH}	Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.4 V	1.63	-	-	mA
		Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.5 V	1.72	-	-	mA
		Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.7 V	1.88	-	-	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.0 V	5.48	-	-	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V	8.31	-	-	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V	11.11	-	-	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 4.5 V	19.61	-	-	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 5.0 V	24.00	-	-	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 5.5 V	29.24	-	-	mA
		Push-Pull, 2x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.4 V	3.25	-	-	mA
		Push-Pull, 2x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.5 V	3.42	-	-	mA
		Push-Pull, 2x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.7 V	3.73	-	-	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.0 V	10.84	-	-	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V	16.34	-	-	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-level Output Current [2]	I_{OH}	Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V	21.83	-	-	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 4.5 V	38.34	-	-	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 5.0 V	47.07	-	-	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 5.5 V	56.68	-	-	mA
Low-level output current [2]	I_{OL}	Push-Pull, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.4 V	1.67	-	-	mA
		Push-Pull, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.5 V	1.74	-	-	mA
		Push-Pull, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.7 V	1.85	-	-	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.0 V	5.07	-	-	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.3 V	5.48	-	-	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.6 V	5.85	-	-	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 4.5 V	6.81	-	-	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 5.0 V	7.27	-	-	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 5.5 V	7.72	-	-	mA
		Push-Pull, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.4 V	3.27	-	-	mA
		Push-Pull, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.5 V	3.39	-	-	mA
		Push-Pull, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.7 V	3.61	-	-	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.0 V	9.85	-	-	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.3 V	10.63	-	-	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.6 V	11.33	-	-	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 4.5 V	13.06	-	-	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 5.0 V	13.79	-	-	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 5.5 V	14.80	-	-	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.4 V	4.07	-	-	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.5 V	4.22	-	-	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.7 V	4.49	-	-	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.0 V	12.24	-	-	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low-level output current [2]	I_{OL}	NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.3 V	13.20	-	-	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.6 V	14.04	-	-	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 4.5 V	16.24	-	-	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 5.0 V	17.24	-	-	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 5.5 V	18.24	-	-	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.4 V	7.71	-	-	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.5 V	7.97	-	-	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.7 V	8.46	-	-	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.0 V	22.96	-	-	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.3 V	24.63	-	-	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.6 V	26.10	-	-	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 4.5 V	29.82	-	-	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 5.0 V	31.42	-	-	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 5.5 V	33.25	-	-	mA
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR} Slew Rate 1 V/µs	-	1.9	2.7	ms
NVM Page Write Time	T_{WR}	V_{DD} = 2.5 V to 5.5 V	-	-	20	ms
NVM Page Erase Time	T_{ER}	V_{DD} = 2.5 V to 5.5 V	-	-	20	ms
Power-on threshold	PON_{THR}	V_{DD} level required to start up the chip	1.63	-	2.04	V
Power-off threshold	$POFF_{THR}$	V_{DD} level required to switch off the chip	0.96	-	1.54	V
Pull-up or pull-down resistance	R_{PULL}	1 M for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	-	1	-	MΩ
		100 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	-	100	-	kΩ
Pull-up or pull-down resistance	R_{PULL}	10 k For Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	-	9.3	-	kΩ
Input capacitance	C_{IN}	PINs 10, 11	-	2.9	-	pF
		PIN 12	-	3.6	-	pF
		PINs 15, 16	-	3.8	-	pF
		PINs 17, 18, 19	-	10.2	-	pF
		PIN 20	-	27.8	-	pF
		PIN 21	-	5.7	-	pF

1. No hysteresis.
2. DC or average current through any pin should not exceed value given in Absolute maximum conditions.

3.5 I²C Pins Specifications

3.5.1 Electrical Specification for DI Mode

T_A = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V, unless otherwise noted.

Parameter	Symbol	Conditions	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
Low-level input voltage	V_{IL}	-	-0.5	0.3xV_{DD}	-0.5	0.3xV_{DD}	V
High-level input voltage	V_{IH}	-	0.7xV_{DD}	5.5	0.7xV_{DD}	5.5	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	-	0.05xV_{DD}	-	0.05xV_{DD}	-	V
Low-level output voltage 1	V_{OL1}	(Open-Drain) at 3 mA sink current V_{DD} > 2 V	0	0.4	0	0.4	V
Low-level output voltage 2	V_{OL2}	(Open-Drain) at 2 mA sink current V_{DD} ≤ 2 V	0	0.2xV_{DD}	0	0.2xV_{DD}	V
Low-level output current [1]	I_{OL}	V_{OL} = 0.4 V, V_{DD} = 2.4 V	3	-	16.75	-	mA
		V_{OL} = 0.4 V, V_{DD} = 3.0 V	3	-	20	-	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	-	20	-	
		V_{OL}= 0.6 V	6	-	-	-	
Output fall time from V_{IHmin} to V_{ILmax} [1]	t_{OF}	-	14x (V_{DD}/5.5 V)	250	10x (V_{DD}/5.5 V)	120	ns
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	-	0	50	0	50	ns
Input current (each IO pin)	I_i	0.1xV_{DD} < V_I < 0.9xV_{DDmax}	-10	+10	-10	+10	µA
Capacitance (each IO pin)	C_i	-	-	10	-	10	pF

1. Does not meet standard I²C specifications: t_{OF} = 20x(V_{DD}/5.5 V) (min); for Fast-mode Plus I_{OL} = 20 mA (min) at V_{OL} = 0.4 V.
2. For Fast-mode Plus SDA pin must be configured as NMOS 2x Open-Drain, see reg [1155] in section 21. Register Definitions.

3.5.2 Electrical Specification for DILV Mode

T_A = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V, unless otherwise noted.

Parameter	Symbol	Conditions	Fast-Mode		Unit
			Min	Max	
Low-level input voltage	V_{IL}	-	-	0.562	V
High-level input voltage	V_{IH}	-	1.154	-	V
Low-level output voltage 1	V_{OL1}	(Open-Drain) at 3 mA sink current V_{DD} > 2 V	0	0.4	V
Low-level output voltage 2	V_{OL2}	(Open-Drain) at 2 mA sink current V_{DD} ≤ 2 V	0	0.2xV_{DD}	V
Low-level output current	I_{OL}	V_{OL} = 0.4 V, V_{DD} = 2.4 V	3	-	mA
		V_{OL} = 0.4 V, V_{DD} = 3.0 V	3	-	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	-	mA
		V_{OL}= 0.6 V	6	-	mA
Output fall time from V_{IHmin} to V_{ILmax} [1]	t_{OF}		14x (V_{DD}/5.5 V)	250	ns
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	50	ns

Parameter	Symbol	Conditions	Fast-Mode		Unit
			Min	Max	
Input current (each IO pin)	I_i	$0.1xV_{DD} < V_I < 0.9xV_{DDmax}$	-10	+10	µA
Capacitance (each IO pin)	C_i		-	10	pF

1. Does not meet standard I²C specifications: $t_{OF} = 20x(V_{DD}/5.5\ V)$ (min).
2. For Fast-mode Plus SDA pin must be configured as NMOS 2x Open-Drain, see reg [1155] in section 21. Register Definitions

3.5.3 Timing Specifications

T_A = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V, unless otherwise noted.

Parameter	Symbol	Conditions	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}		-	400	-	1000	kHz
SCL Clock, Low Period	t_{LOW}		1300	-	500	-	ns
SCL Clock, High Period	t_{HIGH}		600	-	260	-	ns
Data Valid Time	t_{VD_DAT}		-	900	-	450	ns
Data Valid Acknowledge Time	t_{VD_ACK}		-	900	-	450	ns
Bus Free Time between STOP and START Conditions	t_{BUF}		1300	-	500	-	ns
Hold Time for Repeated START Condition	t_{HD_STA}		600	-	260	-	ns
Set-Up Time for Repeated STOP Condition	t_{SU_STA}		600	-	260	-	ns
Data Hold Time	t_{HD_DAT}		0	-	0	-	ns
		Low-voltage Logic Input Mode [1]	185	-	N/A	N/A	ns
Data Set-up Time	t_{SU_DAT}		100	-	50	-	ns
		Low-voltage Logic Input Mode [1]	335	-	N/A	N/A	ns
SCL, SDA Rise Time	t_R		-	300	-	120	ns
SCL, SDA Fall Time	t_F		-	300	-	120	ns
Set-up Time for STOP Condition	t_{SU_STO}		600	-	260	-	ns

1. Does not meet standard I²C specifications.
2. Timing diagram can be found in Figure 239.

3.6 Macrocells Current Consumption

Typical values are at T_A = 25 °C, unless otherwise noted.

Parameter	Symbol	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Current	I_{DD}	Chip Quiescent, BG disabled	0.06	0.08	0.13	µA
		Chip Quiescent, BG enabled	0.36	0.39	0.47	µA
		OSC2 25 MHz, pre-divider = 1	40.78	49.64	70.54	µA
		OSC2 25 MHz, pre-divider = 4	31.75	37.46	51.41	µA
		OSC2 25 MHz, pre-divider = 8	29.96	35.06	47.62	µA
		OSC1 2.048 MHz, pre-divider = 1	19.19	19.98	21.73	µA
		OSC1 2.048 MHz, pre-divider = 4	18.50	19.05	20.26	µA
		OSC1 2.048 MHz, pre-divider = 8	18.36	18.87	19.97	µA
		OS00 2.048 kHz, pre-divider = 1	0.33	0.36	0.44	µA
		OSC0 2.048 kHz, pre-divider = 4	0.33	0.36	0.44	µA

Parameter	Symbol	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Current	I_{DD}	OSC0 2.048 kHz, pre-divider = 8	0.33	0.36	0.44	µA
		Push-Pull 1x + 4 pF @ 2.048 kHz	0.38	0.44	0.55	µA
		Push-Pull 1x + 4 pF @ 2.048 MHz	66.8	82.6	116.0	µA
		Temperature Sensor, range 1	10.9	10.9	11.2	µA
		Temperature Sensor, range 2	11.0	11.1	11.4	µA
		One ACMPx_L (includes internal V_{REF})	6.1	6.2	6.4	µA
		Two ACMPx_L (includes internal V_{REF})	8.4	8.5	8.8	µA
		Op AmpX Quiescent Current (128 kHz bandwidth)	32.2	32.8	33.8	µA
		Op AmpX Quiescent Current (8.192 MHz bandwidth)	607	611	613	µA
		In Amp Quiescent Current (three Op Amps are ON, Rf1 = Rf2 = 50 kΩ, Rg =1 kΩ, 128 kHz bandwidth, Charge Pump - Disabled)	98	101	104	µA
		In Amp Quiescent Current (three Op Amps are ON, Rf1 = Rf2 = 50 kΩ, Rg =1 kΩ, 128 kHz bandwidth, Charge Pump - Enabled)	75.2	77.5	80.8	µA
		In Amp Quiescent Current (three Op Amps are ON, Rf1 = Rf2 = 50 kΩ, Rg =1 kΩ, 8.192 MHz bandwidth, Charge Pump - Disabled)	1819	1834	1844	µA
		In Amp Quiescent Current (three Op Amps are ON, Rf1 = Rf2 = 50 kΩ, Rg =1 kΩ, 8.192 MHz bandwidth, Charge Pump - Enabled)	1225	1235	1245	µA
		Chopper ACMP (with 2.048 kHz clock)	31.4	33.6	38.4	µA

3.7 Timing Specifications

3.7.1 Typical Delay Estimated for Each Macrocell

Typical values are at T_A = +25 °C, unless otherwise noted

Parameter	Symbol	Conditions	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
Delay	tpd	Digital Input to PP 1x	26	27	18	20	13	15	ns
Delay	tpd	Digital Input with Schmitt Trigger to PP 1x	27	28	19	21	15	15	ns
Delay	tpd	Digital Input to PP 2x	24	25	17	18	12	14	ns
Delay	tpd	Low Voltage Digital input to PP 1x	28	246	20	163	15	95	ns
Delay	tpd	Digital input to NMOS output	-	24	-	18	-	13	ns
Delay	tpd	Output enable from Pin, OE Hi-Z to 1	26	-	19	-	13	-	ns
Delay	tpd	Output enable from Pin, OE Hi-Z to 0	-	26	-	19	-	14	ns
Delay	tpd	Digital input to 1x3-State (Z to 1)	26	-	19	-	13	-	ns
Delay	tpd	Digital input to x3-State (Z to 0)	-	26	-	17	-	14	ns
Delay	tpd	Digital input to 2x3-State (Z to 1)	24	-	17	-	13	-	ns
Delay	tpd	Digital input to 2x3-State (Z to 0)	-	24	-	19	-	12	ns
Delay	tpd	2-bit LUT	17	17	12	12	8	8	ns
Delay	tpd	3-bit LUT	19	20	13	14	9	10	ns

Delay	tpd	4-bit LUT	20	21	15	14	9	10	ns
Delay	tpd	LATCH	25	25	17	18	12	12	ns
Delay	tpd	DFF	24	25	16	18	11	12	ns
Delay	tpd	CNT/DLY	107	107	77	74	48	70	ns
Width	tw	Edge detect	206	205	161	160	116	116	ns
Delay	tpd	Edge detect	19	20	13	13	8	8	ns
Delay	tpd	Edge detect Delayed	241	241	175	175	125	125	ns
Delay	tpd	Ripple Counter	45	60	32	44	22	31	ns
Delay	tpd	PGen	20	20	14	14	9	10	ns
Delay	tpd	Filter	177	177	121	121	77	78	ns
Delay	tpd	Inverter Filter	115	115	83	83	57	57	ns
Delay	tpd	Pipe Delay	36	37	25	26	17	18	ns

3.7.2 Programmable Delay Expected Typical Delays and Widths

Typical values are at T_A = +25 °C, unless otherwise noted.

Parameter	Symbol	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Pulse width, 1 cell	tw	mode: (any) edge detect, edge detect output	223	163	118	ns
Pulse width, 2 cell	tw	mode: (any) edge detect, edge detect output	444	324	233	ns
Pulse width, 3 cell	tw	mode: (any) edge detect, edge detect output	663	484	347	ns
Pulse width, 4 cell	tw	mode: (any) edge detect, edge detect output	882	643	461	ns
Delay, 1 cell	time1	mode: (any) edge detect, edge detect output	18	12	8	ns
Delay, 2 cell	time1	mode: (any) edge detect, edge detect output	18	12	8	ns
Delay, 3 cell	time1	mode: (any) edge detect, edge detect output	18	12	8	ns
Delay, 4 cell	time1	mode: (any) edge detect, edge detect output	18	12	8	ns
Delay, 1 cell	time2	mode: both edge delay, edge detect output	243	176	126	ns
Delay, 2 cell	time2	mode: both edge delay, edge detect output	464	337	241	ns
Delay, 3 cell	time2	mode: both edge delay, edge detect output	683	497	356	ns
Delay, 4 cell	time2	mode: both edge delay, edge detect output	902	655	470	ns

3.7.3 Typical Filter Rejection Pulse Width

Typical values are at T_A = +25 °C, unless otherwise noted.

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered pulse width	< 131	< 89	< 59	ns

3.7.4 Counter/Delay Specifications

Typical values are at T_A = +25 °C, unless otherwise noted.

Parameter	OSC Freq	OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Power-on time	25 MHz	auto	0.046	0.032	0.022	µs
Power-on time	2.048 MHz	auto	0.511	0.458	0.414	µs
Power-on time	2.048 kHz	auto	657	563	477	µs
Frequency settling time	25 MHz	auto	0.314	0.378	0.455	µs
Frequency settling time	2.048 MHz	auto	1.344	1.597	2.063	µs
Frequency settling time	2.048 kHz	auto	657	1066	476	µs
Variable (CLK period)	25 MHz	forced	0.039 - 0.042	0.040 - 0.041	0.038 - 0.042	µs
Variable (CLK period)	2.048 MHz	forced	0.480 - 0.500	0.490 - 0.491	0.480 - 0.495	µs

Parameter	OSC Freq	OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Variable (CLK period)	2.048 kHz	forced	477 - 500	478 - 499	478 - 498	µs
Typical Propagation Delay (non-delayed edge)	25 MHz/ 2.048 kHz	either	35	14	10	ns

3.8 Oscillator Specifications

3.8.1 Oscillators Frequency Limits

V_{DD} = 2.4 V to 5.5 V.

OSC	Temperature Range					
	+25 °C			-40 °C to +85 °C		
	Minimum Value, kHz	Maximum Value, kHz	Error, %	Minimum Value, kHz	Maximum Value, kHz	Error, %
2.048 kHz OSC0	2.029	2.065	+0.83	1.935	2.075	+1.32
			-0.93			-5.52
2.048 MHz OSC1	2023	2071	+1.12	2007	2073	+1.22
			-1.22			-2.00
25 MHz OSC2	24676	25323	+1.29	24144	25323	+1.29
			-1.30			-3.42

3.8.2 Oscillators Power-On Delay

T_A = 25 °C, OSC Power Setting: "Auto Power-On" .

Power Supply Range (V_{DD}) V	OSC0 2.048 kHz		OSC1 2.048 MHz		OSC2 25 MHz		OSC2 25 MHz Start with Delay	
	Typical value, µs	Maximum value, µs	Typical value, ns	Maximum value, ns	Typical value, ns	Maximum value, ns	Typical value, ns	Maximum value, ns
2.50	492	559	491	500	46	53	145	153
3.30	490	525	489	501	32	37	140	148
4.00	489	509	489	509	26	31	139	146
5.00	488	495	488	530	22	26	138	146
5.50	488	499	487	532	20	24	138	145

3.9 ACMP Specifications

T_A = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V, unless otherwise noted

Parameter	Symbol	Conditions	Note	Min	Typ	Max	Unit
ACMP Input Voltage Range	V_{ACMP}	Positive Input	-	0	-	V_{DD}	V
		Negative Input		0	-	V_{DD}	V
ACMP input offset	V_{offset}	ACMPxL, Vhys = 0 mV, Gain = 1, V_{REF} = 32 mV to 2048 mV	T_A = -40 °C to +85 °C	-6.27	-	3.67	mV
			T_A = 25 °C	-5.76	-0.98	3.39	mV
Chopper ACMP Input Offset	V_{offset}	ACMPxL, Vhys = 0 mV, Gain = 1, V_{REF} = 32 mV to 2048 mV	T_A = -40 °C to +85 °C	-0.24	-	0.49	mV
			T_A = 25 °C	-0.12	0.11	0.39	mV
ACMP Startup Time when BG ON	t_{start}	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxL	T_A = -40 °C to +85 °C	-	51.0	99.6	µs
ACMP Startup Time when BG OFF				-	1729	2822	µs

Parameter	Symbol	Conditions	Note	Min	Typ	Max	Unit
Series input resistance	R_{sin}	Gain = 1x	-	-	10	-	GΩ
		Gain = 0.5x		-	1.6	-	MΩ
		Gain = 0.33x		-	1.6	-	MΩ
		Gain = 0.25x		-	1.6	-	MΩ
Propagation Delay, Response time	PROP	ACMPxL, V_{REF} =1.024 V, Gain = 1, Overdrive = 100 mV	Low to High	-	2.59	3.66	µs
			High to Low	-	2.80	5.21	µs
		ACMPxL, V_{REF} = 32 mV to 2048 mV, Gain = 1, Overdrive = 100 mV	Low to High	-	2.83	5.16	µs
			High to Low	-	2.96	7.63	µs
		ACMPxL, V_{REF} =1.024 V, Gain = 1, Overdrive = 10 mV	Low to High	-	8.18	12.57	µs
			High to Low	-	9.14	18.54	µs
		ACMPxL, V_{REF} = 32 mV to 2048 mV, Gain = 1, Overdrive = 10 mV	Low to High	-	9.16	21.41	µs
			High to Low	-	10.01	32.37	µs
Gain error	G	G = 1	-	1	1	1	
		G = 0.5		0.496	0.500	0.504	
		G = 0.33		0.331	0.330	0.336	
		G = 0.25		0.248	0.250	0.253	

3.10 Internal V_{REF} Specifications

V_{DD} = 2.4 V to 5.5 V.

Parameter	Symbol	Conditions	Note	Min	Typ	Max	Unit
Internal V_{REF} Accuracy at V_{REF} > 1216 mV	V_{REF} Accuracy and Loading	No loading	T_A = +25 °C	-0.30	-	0.18	%
			T_A = -40 °C to +85 °C	-0.73	-	0.19	%
V_{REF} Divider Accuracy	$V_{REF\_ACCURACY}$	V_{REF} from (16/64) to (64/64)	T_A = -40 °C to +85 °C	-0.38	0.04	0.37	%
		V_{REF} from (1/64) to (64/64)	T_A = -40 °C to +85 °C	-1.94	0.02	1.31	%
V_{REF} Divider Offset	V_{REF_OFFSET}	V_{REF} from (16/64) to (64/64)	T_A = -40 °C to +85 °C	-5.58	0.83	7.84	mV
		V_{REF} from (1/64) to (64/64)	T_A = -40 °C to +85 °C	-5.58	0.62	7.84	mV

3.11 HD Buffer Specifications

T_A = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Offset						
Input Offset Voltage	V_{OFFSET}	V_{DDA} = 5 V, V_{OUT} = 0.5 V to 4 V, T_A = 25 °C	-	0.25	8.0	mV
Input Offset Voltage	V_{OFFSET}	V_{DDA} = 5 V, V_{OUT} = 0.5 V to 4 V	-	-	9.0	mV
Offset Drift with Ambient Temperature	dV_{OFFSET}/dt	V_{OUT} = $V_{DDA}/2$	-	0.75	13.5	µV/C
Output						

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Load Regulation	$\Delta V_{OUT}(I)$	V_{DDA} = 5 V, V_{OUT} = 2.048 V, I_{LOAD} = 0.5 mA to 2 mA, T_A = 25 °C	-	0.2	1.2	mV
		V_{DDA} = 5 V, V_{OUT} = 2.048 V, I_{LOAD} = 0.5 mA to 5 mA, T_A = 25 °C		0.4	1.9	mV
Line Regulation	$\Delta V_{OUT}(U)$	V_{DDA} = 2.5 V to 5 V, V_{OUT} = 2.048 V, T_A = 25 °C	-	0.9	5.0	mV
Short Circuit Current	I_{SC}	V_{DDA} = 2.4 V to 5.5 V	-	67.8	-	mA
Shutdown Characteristics						
Buffer Turn-On Time	t_{on}	R_{LOAD} = 5 kΩ, T_A = 25 °C	-	-	50	µs
Buffer Turn-Off Time	t_{off}	R_{LOAD} = 5 kΩ, T_A = 25 °C	-	0.071	-	µs

3.12 V_{REF} Output Buffer Specifications

T_A = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V, unless otherwise noted.

Parameter	Symbol	Conditions	Note	Min	Typ	Max	Unit
Load Regulation	$\Delta V_{OUT}(I)$	V_{DDA} = 5 V, V_{OUT} = 2.048 V, I_{LOAD} = 0.5 mA to 2 mA, T_A = 25 °C	-	-0.99	-	1.21	mV
		V_{DDA} = 5 V, V_{OUT} = 2.048 V, I_{LOAD} = 0.5 mA to 5 mA, T_A = 25 °C	-	-0.99	-	1.39	mV
Line Regulation	$\Delta V_{OUT}(U)$	V_{DDA} = 2.5 V to 5 V, V_{OUT} = 2.048 V, T_A = 25 °C	-	-2.97	-	5.13	mV
V_{REF} Output Buffer Offset	V_{REF} Buffer Accuracy and Loading	V_{REF} < 1024 mV, V_{DDA} = 2.4 V to 5.5V, No Loading	T_A = 25 °C	-11.2	-	10.0	mV
				-12.2	-	10.6	mV
		V_{REF} =1024 mV to 1600 mV, V_{DDA} = 2.4 V to 5.5V, No Loading	T_A = 25 °C	-6.8	-	6.2	mV
				-7.3	-	6.9	mV
		V_{REF} >1600 mV, V_{DDA} = 2.4 V to 5.5V, No Loading	T_A = 25 °C	-11.1	-	11.6	mV
				-12.0	-	12.9	mV
V_{REF} Output Buffer Offset	V_{REF} Buffer Accuracy and Loading	V_{REF} =1024 mV to 2048 mV, V_{DDA} = 3.3 V, No Loading	T_A = 25 °C	-6.8	-	5.8	mV
				-7.2	-	6.4	mV
V_{REF}0 Buffer Output Capacitance Loading	V_{REF} Buffer Accuracy and Loading		Load Resistance = 1 MΩ	-	-	5	pF
			Load Resistance = 560 kΩ	-	-	10	pF
			Load Resistance = 100 kΩ	-	-	40	pF
			Load Resistance = 10 kΩ	-	-	80	pF
			Load Resistance = 2 kΩ	-	-	120	pF
			Load Resistance = 1 kΩ, V_{REF} = 32 mV to 1024 mV	-	-	150	pF

3.13 Analog Temperature Sensor Specifications

3.13.1 Output Range 1

T, °C	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V	
	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %
-40	991	±0.41	989	±0.38	989	±0.33
-30	968	±0.35	967	±0.32	966	±0.33
-20	945	±0.33	944	±0.31	943	±0.34
-10	922	±0.37	921	±0.35	920	±0.38
0	899	±0.39	898	±0.38	897	±0.42
10	876	±0.41	875	±0.39	874	±0.43
20	853	±0.41	852	±0.39	851	±0.44
30	830	±0.45	828	±0.44	828	±0.48
40	806	±0.52	805	±0.51	804	±0.55
50	782	±0.56	781	±0.55	780	±0.60
60	758	±0.62	756	±0.61	756	±0.65
70	733	±0.70	732	±0.69	731	±0.73
80	709	±0.77	707	±0.76	707	±0.80
85	696	±0.81	695	±0.80	694	±0.84

3.13.2 Output Range 2

T, °C	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V	
	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %
-40	1195	±0.39	1194	±0.34	1193	±0.34
-30	1168	±0.37	1166	±0.35	1165	±0.36
-20	1141	±0.37	1139	±0.35	1138	±0.36
-10	1113	±0.40	1111	±0.39	1110	±0.41
0	1085	±0.43	1084	±0.42	1083	±0.44
10	1057	±0.44	1056	±0.43	1055	±0.45
20	1029	±0.45	1028	±0.44	1027	±0.45
30	1001	±0.48	999	±0.47	999	±0.50
40	972	±0.54	971	±0.53	970	±0.56
50	943	±0.58	942	±0.57	941	±0.60
60	914	±0.64	913	±0.63	912	±0.66
70	885	±0.72	883	±0.71	882	±0.74
80	855	±0.79	854	±0.77	853	±0.81
85	840	±0.83	839	±0.81	838	±0.84

3.14 Programmable Operational Amplifier Specifications

V_{DDA} = 2.4 V to 5.5 V, V_{CM}= V_{DDA}/2, V_{OUT} = V_{DDA}/2, R_L = 100 kΩ to V_{DDA}/2, C_L = 50 pF, T_A = 25 °C.

Parameter	Symbol	Conditions [1]	Min	Typ	Max	Unit
Input Voltage Offset (without Customers Trimming, Included Factory Block Offset Trim)						
Input Offset Voltage	V_{OFFSET}	BW = 128 kHz	-	69	500	µV
		BW = 128 kHz, T_A = -40 °C to +85 °C	-	69	930	µV
		BW = 512 kHz	-	56	500	µV
		BW = 512 kHz, T_A = -40 °C to +85 °C	-	56	1230	µV
		BW = 2 MHz	-	47	500	µV

Parameter	Symbol	Conditions [1]	Min	Typ	Max	Unit
Input Offset Voltage	V_{OFFSET}	BW = 2 MHz, T_A = -40 °C to +85 °C	-	47	1030	µV
		BW = 8 MHz	-	35	243	µV
		BW = 8 MHz, T_A = -40 °C to +85 °C	-	35	643	µV
Offset Drift with Ambient Temperature	dV_{OFFSET}/dT	$V_{CM} = V_{DD}/2$, T_A = -40 °C to +85 °C	-	0.6	13.0	µV/°C
		V_{CM} = GND, T_A = -40 °C to +85 °C	-	0.5	12.6	µV/°C
Long-Term Offset Voltage Drift	dV_{OFFSET} over Time	$V_{CM} = V_{DD}/2$	0	-	985	µV
Trimmed Input Offset (Customer Perspective after Using Digital Rheostats with Gain = 200x) [2]						
Input Offset Voltage	V_{OFFSET}		-	-	5	µV
Input Voltage Range						
Input Common-Mode Voltage Range	V_{CMR}	T_A = -40 °C to +85 °C	-0.2	-	V_{DD} + 0.2	V
Common-Mode Rejection Ratio	CMRR	All Op Amps GND + 0.8 V < V_{CM} < V_{DD} - 0.8 V, T_A = -40 °C to +85 °C	73.5	102	-	dB
		All Op Amps GND < V_{CM}< GND + 0.8 V or V_{DD} - 0.8 V < V_{CM} < V_{DD}	69.7	101	-	dB
		All Op Amps GND + 0.8 V < V_{CM} < V_{DD} - 0.8 V, T_A = -40 °C to +85 °C	73.5	103	-	dB
		All Op Amps GND < V_{CM}< GND + 0.8 V or V_{DD} - 0.8 V < V_{CM} < V_{DD}	69.7	102	-	dB
		Internal Op Amp, GND + 0.8 V < V_{CM} < V_{DD} - 0.8 V, T = -40 °C to +85 °C	77.6	100	-	dB
Common-Mode Rejection Ratio	CMRR	Internal Op Amp, GND < V_{CM}< GND+ 0.8 V or V_{DD} - 0.8 V < V_{CM} < V_{DD}	69.7	100	-	dB
Power Supply Rejection Ratio	PSRR	T_A = -40 °C to +85 °C	80	101	-	dB
		V_{CM} = GND, T_A = -40 °C to +85 °C	83	102	-	dB
Channel Separation	CS	V_{DD} = 5 V, f = 10 Hz	-	119	-	dB
		V_{DD} = 5 V, f = 1 kHz	-	112	-	dB
Input Current and Impedance						
Input Bias Current	I_B		-	1.9	±9	pA
		T_A = -40 °C to +85 °C	-	1.9	±258	pA
Input Offset Current	I_{OFFSET}		-	-	3.2	pA
		T_A = +85 °C	-		210	pA
Common-Mode Input Resistance	R_{CM}		-	$3*10^{12}$	-	Ω
Differential Input Resistance	R_{DIFF}		-	10^{13}	-	Ω
Input Capacitance Common-Mode	C_{CM}		-	5	7	pF
Input Capacitance Differential	C_{DIFF}		-	1.98	2.27	pF

Parameter	Symbol	Conditions [1]		Min	Typ	Max	Unit
Open-Loop Gain							
DC Open Loop Gain	A_{OL}	R_{LOAD} = 1 MΩ, GND + 0.1 V < V_{OUT} < V_{DD} - 0.1 V, T_A = -40 °C to +85 °C		103.3	125	-	dB
		R_{LOAD} = 50 kΩ, GND + 0.5 V < V_{OUT} < V_{DD} - 0.5 V T_A = -40 °C to +85 °C		103.4	125	-	dB
Output							
Maximum Voltage Swing	V_{OH}	R_{LOAD} = 50 kΩ, T_A = -40 °C to +85 °C		V_{DD} - 5.73	-	-	mV
		BW = 8.192 MHz, R_{LOAD} = 600 Ω, T_A = -40 °C to +85 °C		V_{DD} - 135	-	-	mV
	V_{OL}	R_{LOAD} = 50 kΩ, T_A = -40 °C to +85 °C		-	-	GND + 3.122	mV
		BW = 8.192 MHz, R_{LOAD} = 600 Ω, T_A = -40 °C to +85 °C		-	-	GND + 101	mV
Linear Output Swing Range	V_{OSR}	V_{OVR} from Rail R_{LOAD} = 1 MΩ		GND + 100	-	V_{DD} - 100	mV
Short Circuit Current	I_{SC}	I_{SC} to GND	BW = 128 kHz, T_A = -40 °C to +85 °C	-	10.8	-	mA
			BW = 512 kHz, T_A = -40 °C to +85 °C	-	14.4	-	mA
Short Circuit Current	I_{SC}	I_{SC} to GND	BW = 2.048 MHz, T_A = -40 °C to +85 °C	-	22.5	-	mA
			BW = 8.192 MHz, T_A = -40 °C to +85 °C	-	52.0	-	mA
		I_{SC} to V_{DD}	BW = 128 kHz, T_A = -40 °C to +85 °C		20.6	-	mA
			BW = 512 kHz, T_A = -40 °C to +85 °C		27.0	-	mA
			BW = 2.048 MHz, T_A = -40 °C to +85 °C		41.1	-	mA
			BW = 8.192 MHz, T_A = -40 °C to +85 °C		92.1	-	mA
Capacitive Load Drive	C_{LOAD}			See section 10.3 Op Amps Typical Performance (Small Signal Overshoot vs. Capacitive Load plots)			
Power Supply							
Supply Voltage	V_{DD}	Guaranteed by PSRR Test		2.4	-	5.5	V
Quiescent Current per Amplifier, BW = 128 kHz	I_Q (including charge pump current consumption)	V_{DDA} = 2.5 V to 5.5 V		-	33.3	47	µA
		T_A = -40 °C to +85 °C, V_{DDA} = 2.5 V to 5.5 V		-	34.1	59	µA
Quiescent Current per Amplifier, BW = 512 kHz		V_{DDA} = 2.5 V to 5.5 V		-	89.8	101	µA
		T_A = -40 °C to +85 °C, V_{DDA} = 2.5 V to 5.5 V		-	91.1	124	µA
Quiescent Current per Amplifier, BW = 2.048 MHz		V_{DDA} = 2.5 V to 5.5 V		-	238.7	255	µA
		T_A = -40 °C to +85 °C, V_{DDA} = 2.5 V to 5.5 V		-	238.9	274	µA

Parameter	Symbol	Conditions [1]		Min	Typ	Max	Unit
Quiescent Current per Amplifier, BW = 8.192 MHz	I_Q (including charge pump current consumption)	T_A = 25 °C, V_{DDA} = 2.5 V to 5.5 V		-	611.5	652	µA
		T_A = -40 °C to +85 °C, V_{DDA} = 2.5 V to 5.5 V		-	611.6	701	µA
Full Shutdown				-	105.8	-	nA
Partial Shutdown [3], All Supporting Blocks are ON, BW = 128 kHz				-	7.3	-	µA
Partial Shutdown [3], All Supporting Blocks are ON, BW = 8.192 MHz				-	21.3	-	µA
Frequency Response							
Gain Bandwidth Product	GBW	R_{LOAD} = 10 kΩ, C_{LOAD} = 20 pF, G = +1 V/V, T_A = -40 °C to +85 °C	BW = 128 kHz	-	124	-	kHz
			BW = 512 kHz	-	542	-	kHz
			BW = 2.048 MHz	-	2569	-	kHz
			BW = 8.192 MHz	-	9594	-	kHz
Phase Margin	PM	G = +1 V/V, BW = 128 kHz → 8.192 MHz; R_{LOAD} = 10 kΩ, C_{LOAD} = 20 pF, T_A = -40 °C to +85 °C		43	71	-	°
Slew Rate	SR	R_{LOAD} = 50 kΩ, C_{LOAD} = 85 pF	BW = 128 kHz, T_A = -40 °C to +85 °C	-	0.09	-	V/µs
			BW = 512 kHz, T_A = -40 °C to +85 °C	-	0.38	-	V/µs
			BW = 2.048 MHz, T_A = -40 °C to +85 °C	-	1.85	-	V/µs
			BW = 8.192 MHz, T_A = -40 °C to +85 °C	-	6.48	-	V/µs
Overload Recovery Time	t_{OR}	T_A = -40 °C to +85 °C R_{LOAD} = 50 kΩ		-	12.68	-	µs
Noise							
Total Harmonic Distortion	THD	AV = 1, R_{LOAD} = 50 kΩ, $V_{OUT(PP)}$ = V_{DD}/2	f = 1 kHz, BW = 128 kHz	-	0.171	-	%
			f = 1 kHz, BW = 512 kHz	-	0.073	-	%
			f = 1 kHz, BW = 2.048 MHz	-	0.033	-	%
			f = 1 kHz, BW = 8.192 MHz	-	0.02	-	%
Input Voltage Noise	e_n	f = 0.1 to 10 Hz		-	24.78	-	µVpp
Input Voltage Noise Density	Vn	f = 1 kHz	BW = 128 kHz	-	92	-	nV/$\sqrt{Hz}$
			BW = 512 kHz	-	86	-	
			BW = 2.048 MHz	-	74	-	
			BW = 8.192 MHz	-	51	-	
Input Current Noise Density	In	f = 1 kHz		-	1	-	fA/$\sqrt{Hz}$
Shutdown Characteristics							

Parameter	Symbol	Conditions [1]		Min	Typ	Max	Unit
Amplifier Turn-On Time	t_{on}	BW = 8.192 MHz, T_A = -40 °C to +85 °C	$V_{CM} = V_{DDA}/2$, R_L = 50 kΩ	-	2.143	6.095	µs
			$V_{DDA} > V_{CM} > (V_{DDA} - 1.3)$ R_L = 50 kΩ	-	2.166	6.070	µs
		BW = 128 kHz, T_A = -40 °C to +85 °C	$V_{CM} = V_{DDA}/2$, R_L = 50 kΩ	-	25.177	43.158	µs
			$V_{DDA} > V_{CM} > (V_{DDA} - 1.3)$ R_L = 50 kΩ	-	34.769	70.602	µs
Amplifier Turn-Off Time	t_{off}	T_A = -40 °C to +85 °C R_L = 50 kΩ		-	0.653	1.015	µs
Comparator Mode							
Propagation Delay Output High to Low	t_{PHL}	V_{REF} = 2.048 mV, Overdrive = 100 mV, Charge Pump is always On	BW = 128 kHz	-	23.6	39.4	µs
			BW = 512 kHz	-	10.8	17.9	µs
			BW = 2.048 MHz	-	6.8	11.5	µs
			BW = 8.192 MHz	-	5.6	10.0	µs
Propagation Delay Output Low to High	t_{PLH}		BW = 128 kHz	-	24.6	40.1	µs
			BW = 512 kHz	-	10.6	17.2	µs
			BW = 2.048 MHz	-	6.5	10.8	µs
			BW = 8.192 MHz	-	5.4	9.0	µs

1. AGND = GND, unless otherwise noted.
2. Equivalent offset voltage of the amplifier after user's trim using digital rheostat. Gain of the amplifier is G = 200 and the zero output voltage level Vzero = $V_{DD}/2$ (See section 10.2.1 Operational Amplifier Mode).
3. Op Amps analog supporting blocks are always turned on.

3.15 100K Digital Rheostat Specifications

$V_A = V_{DD}$, V_B = GND, T_A = -40°C to +85°C, V_{DD} = 2.4 V to 5.5 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Rheostat Pin Voltage Range	V_{DR}	Voltage between any (A or B) pins and AGND	AGND	-	V_{DDA}	V
Digital Rheostat Resistance	R_{DR}	Full resistance with all switches open [1]	94.426	101.582	113.741	kΩ
Minimal Rheostat Resistance	R_{DR_MIN}	Code = 0x00	43.679	-	84.779	Ω
Mismatch between rheostats	R_{MATCH}	Code = 0x3FF, T_A = 25 °C	-	0.084	-	%
	Number of taps		-	-	1024	
Digital Rheostat Bandwidth	$BWDT_{DR}$	Frequency applied on one side of resistor chain and -3 dB frequency measured at the other side with full 100 kΩ, assume no additional load	-	50	-	kHz
Step Resistance	R_S	V_{DD} = (2.4 V; 3.3 V; 5.5 V) V_{AB} = (1 V; -1 V) T_A = 25 °C	-	99.236	-	Ω
Max current through Rheostat	I_{DR_MAX}	T_A = 25 °C	-	-	2	mA
Resistor Noise Voltage	E_{SW_N}	R_{AB} = 25 kΩ, f = 1 kHz	-	30	-	nV/√Hz
Chopper Comparator Switching Frequency	f_{ChACMP}		-	-	30	kHz

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Chopper comparator offset when Auto-Trim process is active	V_{Ch_offset}		-	100	300	µV
Counter Frequency independent from the Rheostat	f_{DR_CLK}	The counter frequency is determined by user selection	0	-	25	MHz
Rheostat Switch Speed [2]	f_{DR_SWCH}	V_A = 5 V, V_B = 0 V, ±1 LSB error band, Auto-Trim or Fast mode	-	-	100	kHz
		V_A = 5 V, V_B = 0 V, ±1 LSB error band, regular mode	-	-	1	kHz
Settling Time	T_{settle}	Fast mode, I^2C code change from 0 to 1023	-	-	50	µs
		Fast mode, Rheostat 1 bit code change	-	-	10	µs
Maximum Capacitance of A, B pins Measured to AGND	C_{DR}	All switches are ON, f = 200 kHz	-	33.152	-	pF
Leakage Current	I_{LKG}	Including active charge pump current consumption	-	-	1000	nA
Zero-Scale Error	Error ZScale	Code = 0x00	-	-	0.776	LSB
Integral Non-linearity	INL		-	-	±2	LSB
Differential Non-linearity	DNL		-	-	±1	LSB
Bandwidth -3 dB (Load = 30 pF)	$BWDT_{CAP}$	$R_{RHEOSTAT}$ < 12.5 kΩ	-	240	-	kHz
		$R_{RHEOSTAT}$ = 12.5 kΩ to 25 kΩ	-	120	-	kHz
		$R_{RHEOSTAT}$ = 25 kΩ to 50 kΩ	-	60	-	kHz
		$R_{RHEOSTAT}$ = 50 kΩ to 100 kΩ	-	30	-	kHz
Resistance Temperature Coefficient	αR(T)	V_{AB} = const	-119.69	0	163.84	ppm/ °C

1. User can calculate actual Digital Rheostat value using calibration data from NVM (see section 12.2 Calculating Actual Resistance).
2. Includes internal timing. External circuit should be counted separately.

3.16 Analog Switches Specifications

3.16.1 Analog Switch0/Voltage Regulator

T_A = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Voltage at Pins	V_{AS}	Voltage between any Analog Switch pin to AGND	0	-	V_{DD} + 0.3	V
Maximum Switching Frequency	f_{MAX}	Pull Up	2.5	-	-	MHz
		Pull Up, V_{DD} = 2.4 V	3.9	-	-	MHz
		Pull Down	363	-	-	kHz
		Pull Down, V_{DD} = 2.4 V	363	-	-	kHz
ON Resistance	R_{ON}	V_{DD} = 3.3 V, V_{IN} < 1.2 V, N-ch FET, T_A = 25 °C	-	30	53	Ω
		V_{DD} = 3.3 V, V_{IN} > V_{DD} - 1.2, P-ch FET, T_A = 25 °C	-	2	3	Ω

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OFF Leakage Current	I_{PWROFF}	Switch OFF; from IN to OUT $V_A = V_{DD}$ or $V_B = V_{DD}$	-	-	17	nA
Maximum ON-state Switch Current	I_{SW_MAX}	$V_A = V_{DD}$, load connected to ground, V_{AB}= 0.4 V	-	-	300	mA
Maximum Pulse Current Through Switch	I_{SW_PULSE}	Pulse duration = 1 ms, Duty cycle < 5 %	-	-	500	mA

3.16.2 Analog Switch1/Current Sink

T_A = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Voltage at Pins	V_{AS}	Voltage between any Analog Switch pin to AGND	0	-	V_{DD} + 0.3	V
Maximum Switching Frequency	f_{MAX}	Pull Up	1.6	-	-	MHz
		Pull Up, V_{DD} = 2.4 V	1.6	-	-	MHz
		Pull Down	5	-	-	MHz
		Pull Down, V_{DD} = 2.4 V	5	-	-	MHz
ON Resistance	R_{ON}	V_{DD} = 3.3 V, V_{IN} < 1.2 V, N-ch FET, T_A = 25 °C	-	0.8	1.5	Ω
		V_{DD} = 3.3 V, $V_{IN} > V_{DD}$ - 1.2, P-ch FET, T_A = 25 °C	-	53.4	204	Ω
OFF Leakage Current	I_{PWROFF}	Switch OFF; from IN to OUT, $V_A = V_{DD}$ or $V_B = V_{DD}$	-	-	34	nA
Maximum ON-state Switch Current	I_{SW_MAX}	$V_A = V_{DD}$, load connected to ground, V_{AB}= 0.4 V	-	-	300	mA
Maximum Pulse Current Through Switch	I_{SW_PULSE}	Pulse duration = 1 ms, Duty cycle < 5 %	-	-	500	mA

4. User Programmability

The SLG47004 is a user programmable device with One-Time-Programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.aap file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

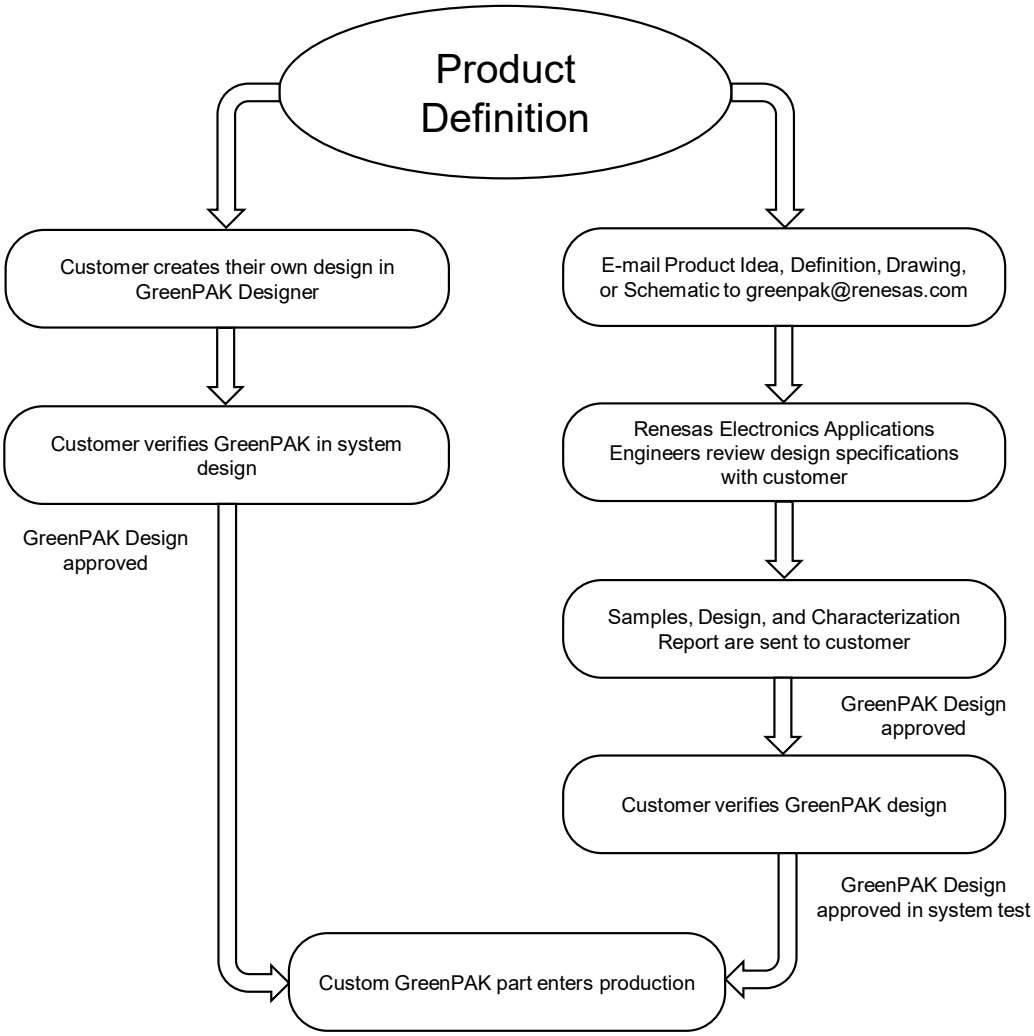


Figure 3. Steps to Create a Custom GreenPAK Device

5. IO Pins

The SLG47004 has a total of 7 GPIO Pins which can function as either a user-defined input or output, as well as serve as a special function (such as outputting the voltage reference) and 1 GPI Pin.

5.1 GPIO Pins

IO0, IO1, IO2, IO3, IO4, IO5, and IO6 serve as general purpose IO pins.

5.2 GPI Pin

I0 serves as general purpose input pin. It is strongly recommended to connect I0 (Pin21) to the ground if it is not used in the project.

5.3 Pull-Up/Down Resistors

All IO pins have the option of user-selectable resistors that can be connected to the pin structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. The internal resistors can be configured as either pull-up or pull-downs.

5.4 Fast Pull-Up/Down During Power-Up

During power-up, IO pull-up/down resistance will switch to 2.6 kΩ initially and then it will switch to normal setting value. This function is enabled by reg [1207].

5.5 Mode IO Structure

5.5.1 I²C Mode Structure (for SCL and SDA)

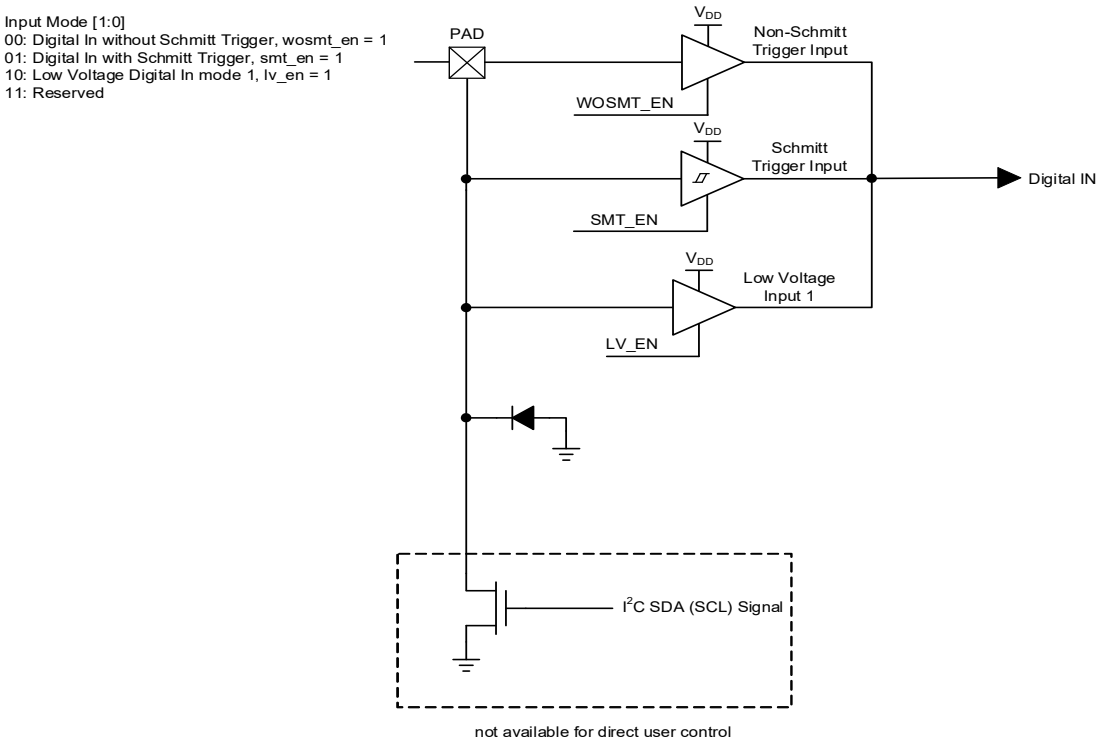


Figure 4. IO with I²C Mode IO Structure Diagram

5.6 Matrix OE IO Structure

Input Mode registers [1153:1152]
00: Digital In without Schmitt Trigger, wosmt_en = 1
01: Digital In with Schmitt Trigger, smt_en = 1
10: Low Voltage Digital In mode, lv_en = 1
11: analog IO mode

Output Mode [1:0]
00: Push-Pull 1x mode, pp1x_en = 1
01: Push-Pull 2x mode, pp2x_en = 1, pp1x_en = 1
10: NMOS 1x Open-Drain mode, od1x_en = 1
11: NMOS 2x Open-Drain mode, od2x_en = 1, od1x_en = 1

Note 1: Digital Out and OE are Matrix Output, Digital In is Matrix Input.
Note 2: Can be varied over PVT, for reference only.

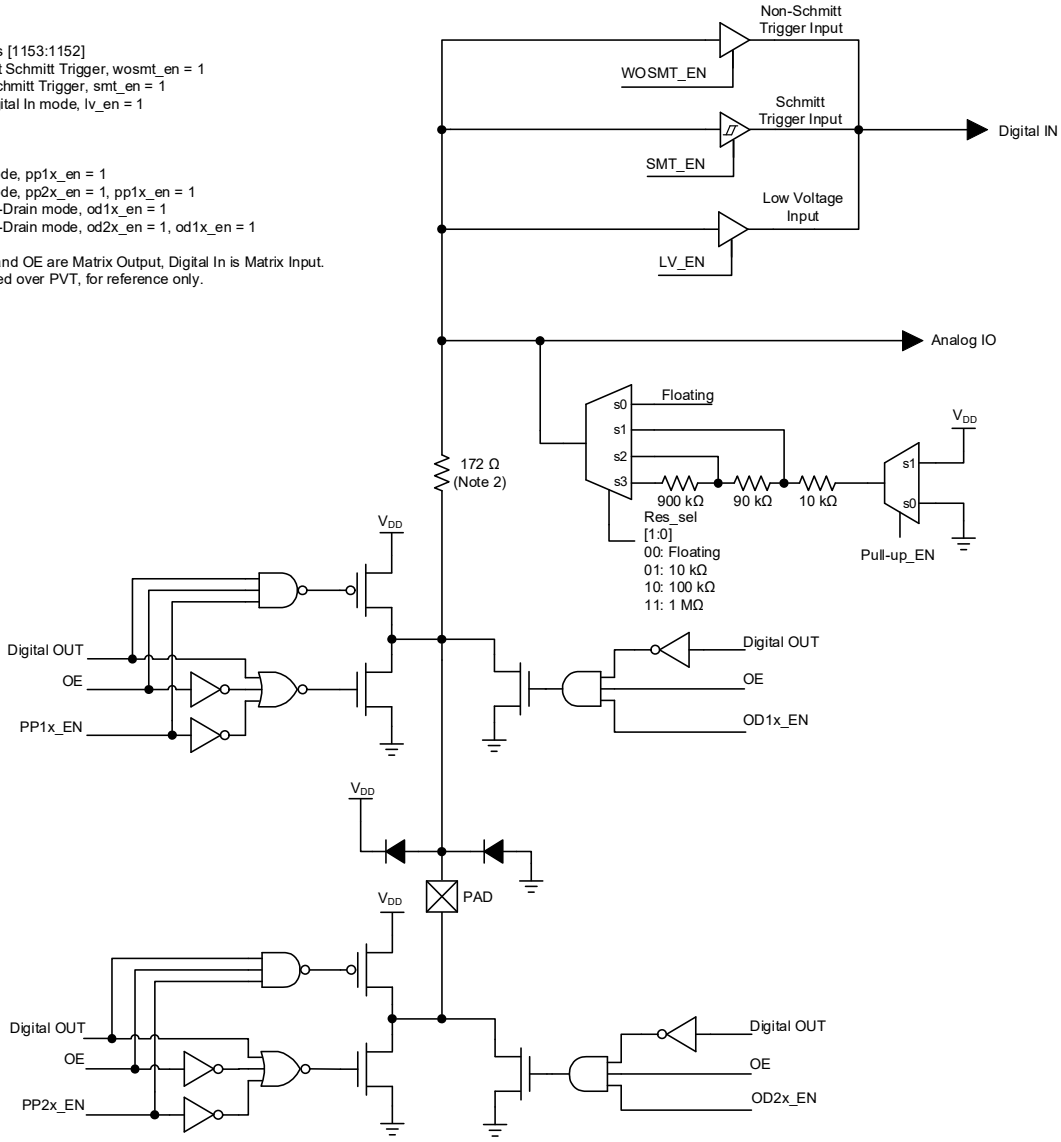


Figure 5. Matrix OE IO Structure Diagram

5.7 GPI Structure

5.7.1 GPI Structure (for I0)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1, OE=0
01: Digital In with Schmitt Trigger, smt_en = 1, OE = 0
10: Low Voltage Digital In mode, lv_en = 1, OE = 0
11: Reserved

Note 1: OE cannot be selected by user.
Note 2: OE is Matrix output, Digital In is Matrix input.

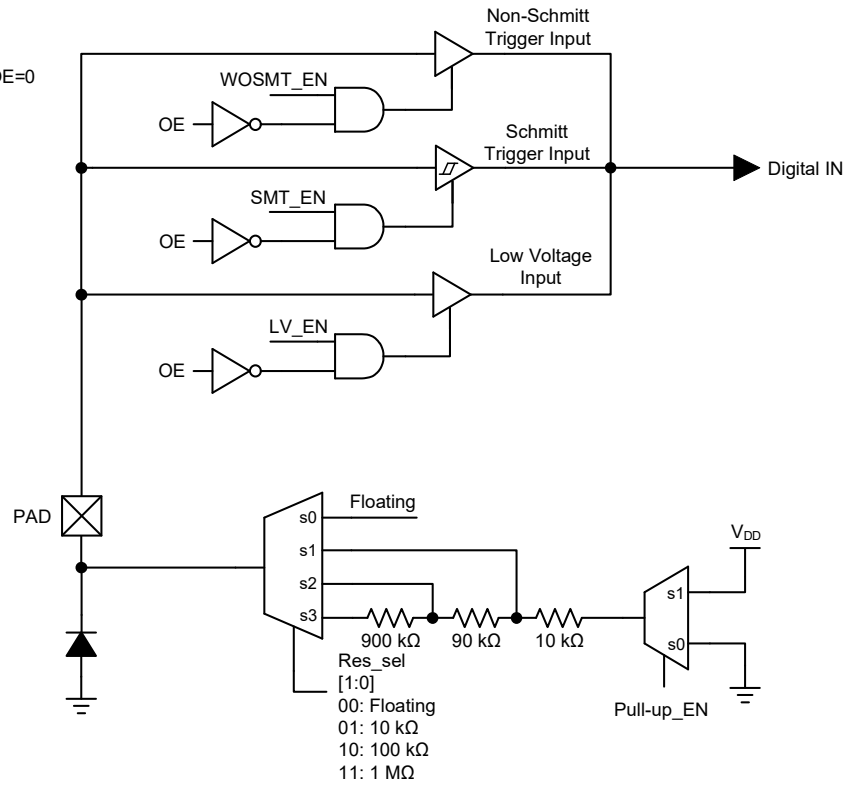


Figure 6. IO0 GPI Structure Diagram

5.8 IO Pins Typical Performance

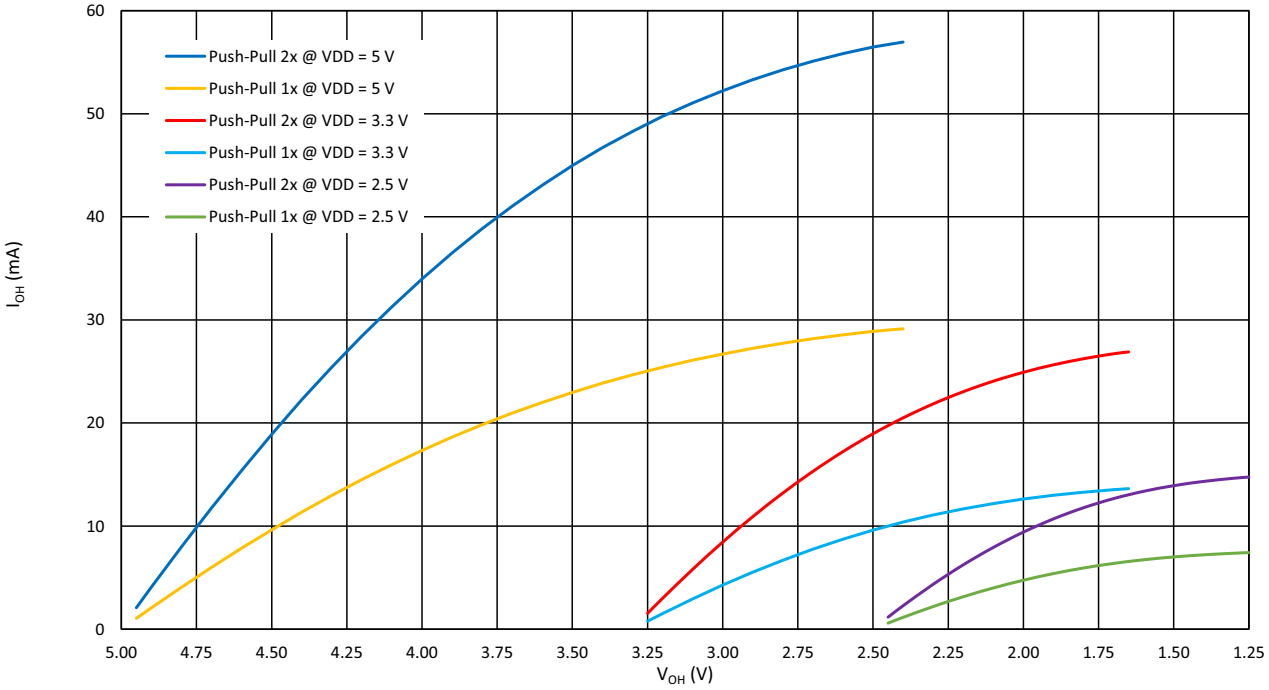


Figure 7. Typical High Level Output Current vs. High Level Output Voltage at T_A = 25 °C

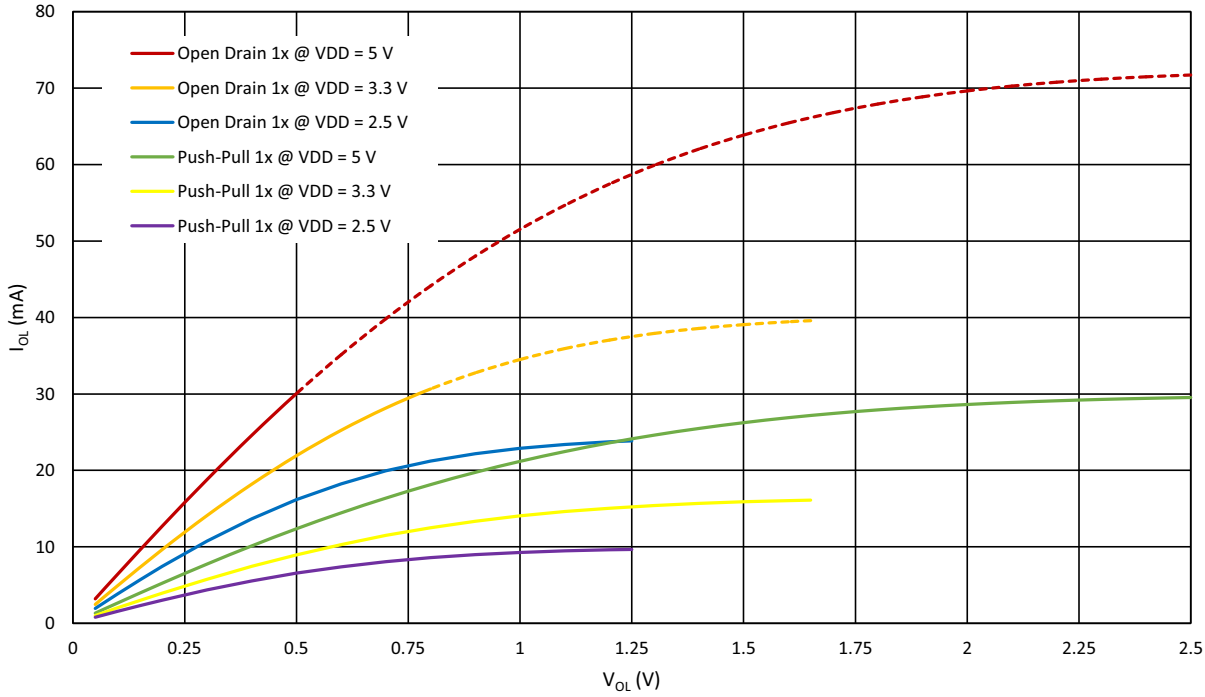


Figure 8. Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T_A = 25 °C, Full Range

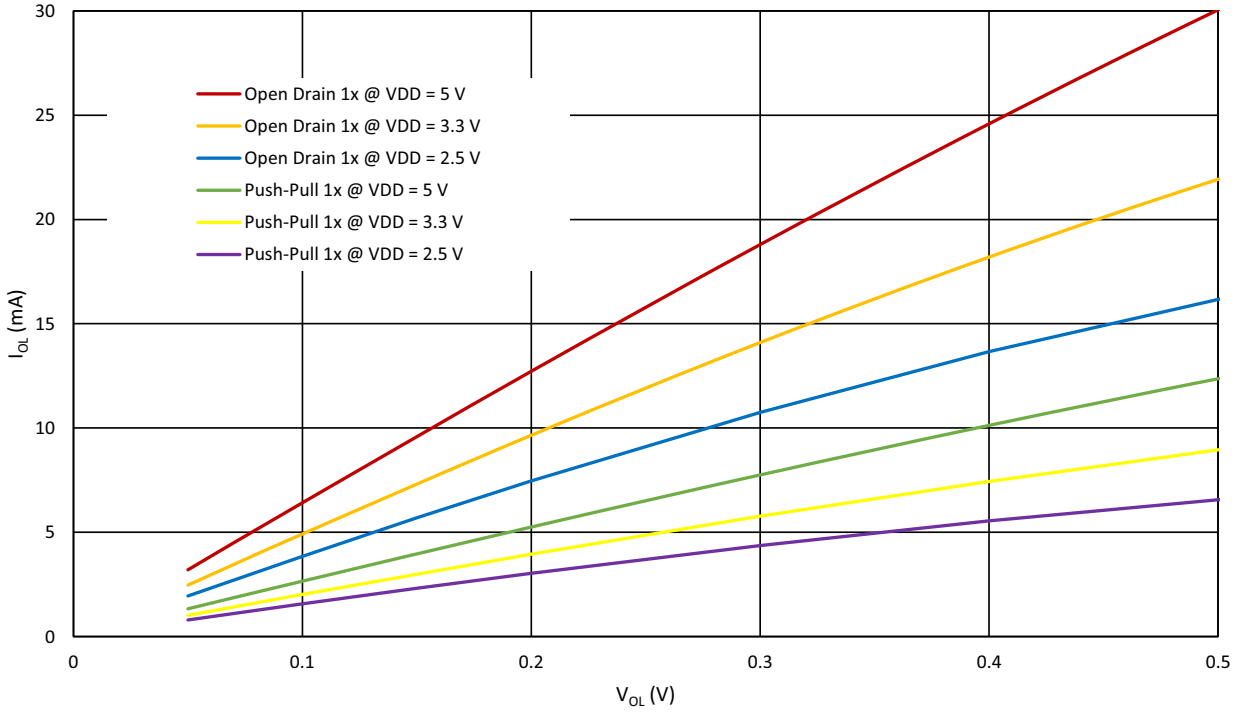


Figure 9. Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T_A = 25 °C

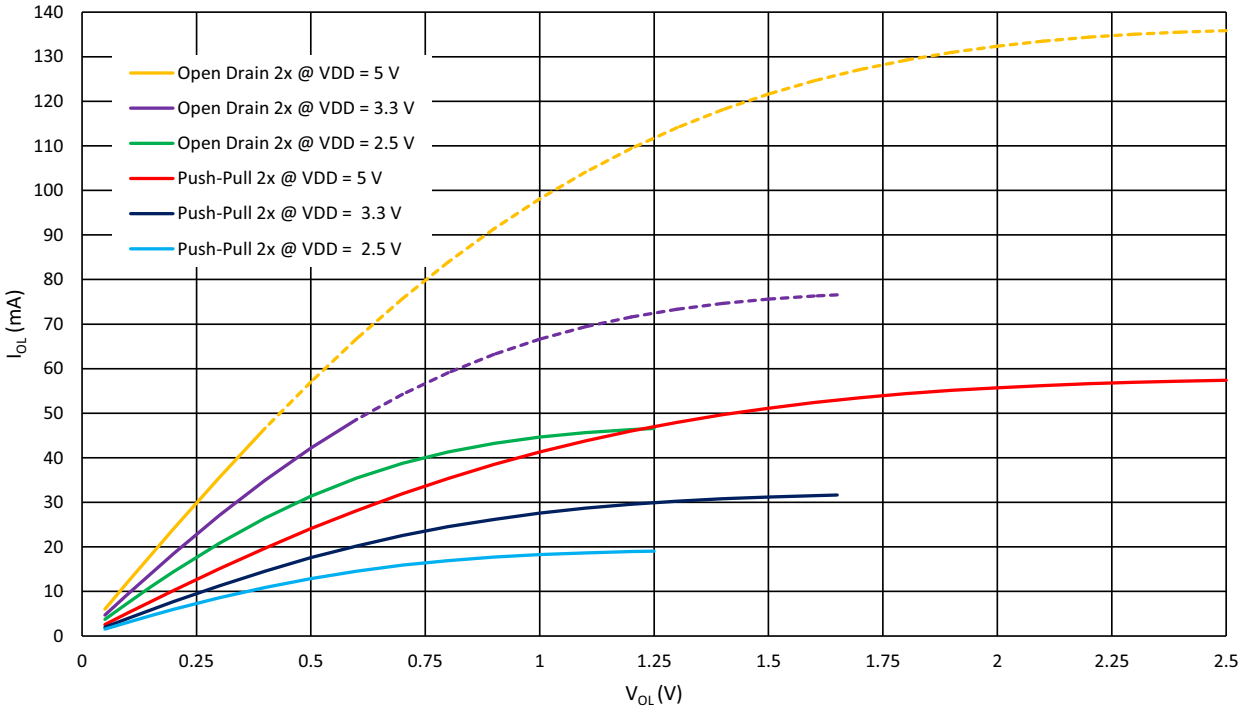


Figure 10. Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T_A = 25 °C, Full Range

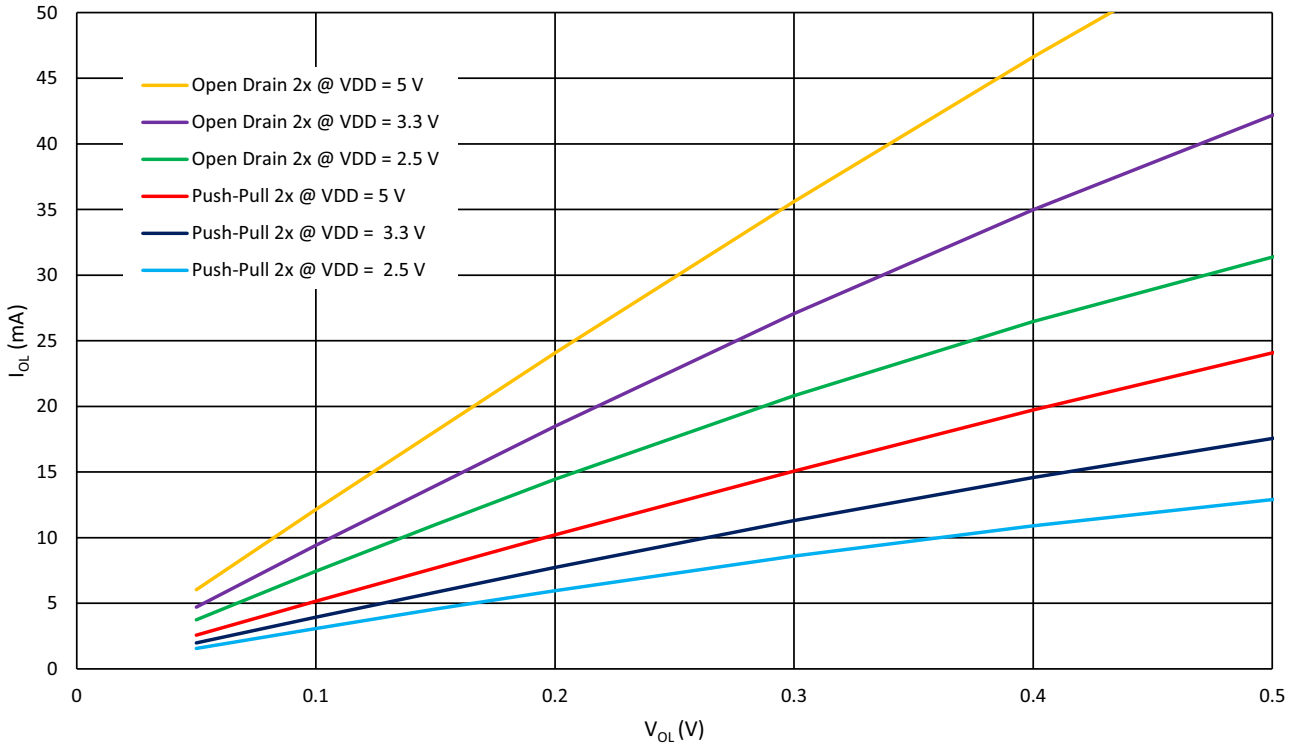


Figure 11. Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T_A = 25 °C

6. Connection Matrix

6.1 Connection Matrix Structure

The Connection Matrix in the SLG47004 is used to create an internal routing for internal functional macrocells of the device once it is programmed. The output of each functional macrocell within the SLG47004 has a specific digital bit code assigned to it, that is either set to active "High" or inactive "Low", based on the design that is created. Once the 2048 register bits within the SLG47004 are programmed, a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 99 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IOs, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG47004's register table, see section 21. Register Definitions.

Matrix Input Signal Functions	N
GND	0
2-bit LUT0/DFF0 output	1
2-bit LUT1/DFF1 output	2
2-bit LUT2/DFF2 output	3
⋮	⋮
V_{DD}	62
V_{DD}	63

Matrix Inputs / Matrix Outputs

N	0	1	2	⋯	99
Registers	registers [5:0]	registers [11:6]	registers [17:12]	⋯	registers [599:594]
Function	Matrix OUT: IN0 of 2-bit LUT0 or Clock Input of DFF0	Matrix OUT: IN1 of 2-bit LUT0 or Data Input of DFF0	Matrix Out: IN0 of 2-bit LUT1 or Clock Input of DFF1	⋯	OP V_{REF} ENABLE

Figure 12. Connection Matrix

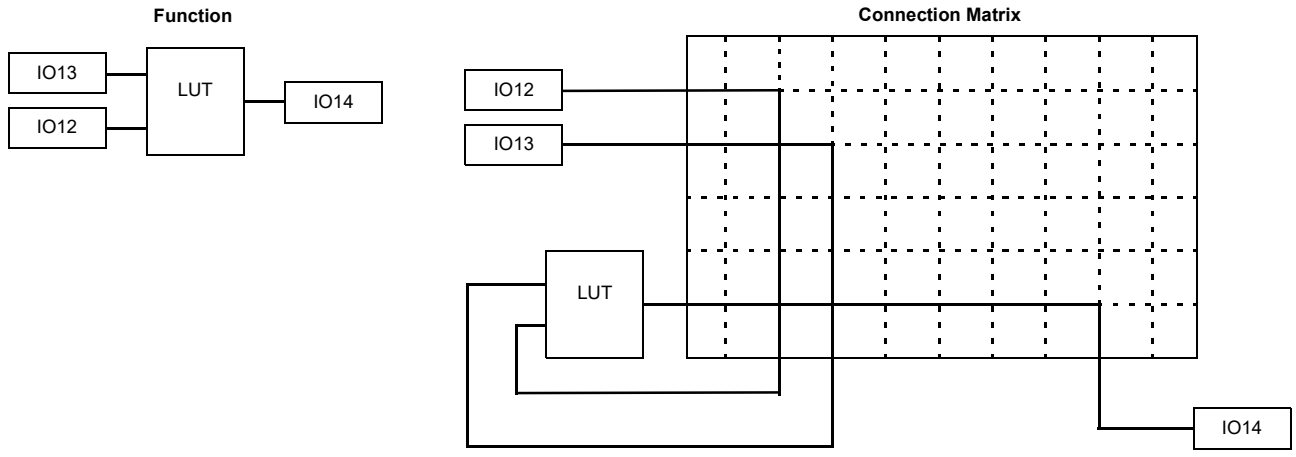


Figure 13. Connection Matrix Example

6.2 Matrix Input Table

Table 4. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	2-bit LUT0/DFF0 output	0	0	0	0	0	1
2	2-bit LUT1/DFF1 output	0	0	0	0	1	0
3	2-bit LUT2/DFF2 output	0	0	0	0	1	1
4	2-bit LUT3/PGen output	0	0	0	1	0	0
5	3-bit LUT0/DFF3 output	0	0	0	1	0	1
6	3-bit LUT1/DFF4 output	0	0	0	1	1	0
7	3-bit LUT2/DFF5 output	0	0	0	1	1	1
8	3-bit LUT3/DFF6 output	0	0	1	0	0	0
9	3-bit LUT4/DFF7 output	0	0	1	0	0	1
10	3-bit LUT5/DFF8 output	0	0	1	0	1	0
11	3-bit LUT6/DFF9 output	0	0	1	0	1	1
12	CNT_DLY0 output	0	0	1	1	0	0
13	MLT0 4-bit LUT1/DFF17_OUT	0	0	1	1	0	1
14	CNT_DLY1 output	0	0	1	1	1	0
15	MLT1 3-bit LUT7/DFF11_OUT	0	0	1	1	1	1
16	CNT_DLY2 output	0	1	0	0	0	0
17	MLT2 3-bit LUT8/DFF12_OUT	0	1	0	0	0	1
18	CNT_DLY3 output	0	1	0	0	1	0
19	MLT3 3-bit LUT9/DFF13_OUT	0	1	0	0	1	1
20	CNT_DLY4 output	0	1	0	1	0	0
21	MLT4 3-bit LUT10/DFF14_OUT	0	1	0	1	0	1
22	CNT_DLY5 output	0	1	0	1	1	0
23	MLT5 3-bit LUT11/DFF15_OUT	0	1	0	1	1	1
24	CNT_DLY6 output	0	1	1	0	0	0
25	MLT6 3-bit LUT12/DFF16_OUT	0	1	1	0	0	1
26	3-bit LUT13/Pipe Delay/RippleCNT_out0	0	1	1	0	1	0
27	Pipe Delay/RippleCNT_out1	0	1	1	0	1	1
28	Pipe Delay/RippleCNT_out2	0	1	1	1	0	0
29	4-bit LUT0/DFF10 output	0	1	1	1	0	1
30	Programmable Delay Edge Detect Output	0	1	1	1	1	0
31	Edge Detect Filter Output	0	1	1	1	1	1
32	I^2C_virtual_0 Input	1	0	0	0	0	0
33	I^2C_virtual_1 Input	1	0	0	0	0	1
34	I^2C_virtual_2 Input	1	0	0	0	1	0
35	I^2C_virtual_3 Input	1	0	0	0	1	1
36	I^2C_virtual_4 Input	1	0	0	1	0	0
37	I^2C_virtual_5 Input	1	0	0	1	0	1
38	I^2C_virtual_6 Input	1	0	0	1	1	0
39	I^2C_virtual_7 Input	1	0	0	1	1	1

Table 4. Matrix Input Table (Cont.)

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
40	RH0 Idle/Active	1	0	1	0	0	0
41	RH1 Idle/Active	1	0	1	0	0	1
42	Output of Op Amp0 in ACMP mode	1	0	1	0	1	0
43	Output of Op Amp1 in ACMP mode	1	0	1	0	1	1
44	IO0 Digital Input	1	0	1	1	0	0
45	IO1 Digital Input	1	0	1	1	0	1
46	IO2 Digital Input	1	0	1	1	1	0
47	IO3 Digital Input	1	0	1	1	1	1
48	IO4 Digital Input	1	1	0	0	0	0
49	IO5 Digital Input	1	1	0	0	0	1
50	IO6 Digital Input	1	1	0	0	1	0
51	I0 Digital Input	1	1	0	0	1	1
52	Oscillator0 output 0	1	1	0	1	0	0
53	Oscillator1 output 0	1	1	0	1	0	1
54	Oscillator2 output	1	1	0	1	1	0
55	Chopper ACMP Out	1	1	0	1	1	1
56	ACMP0 Output (low speed)	1	1	1	0	0	0
57	ACMP1 Output (low speed)	1	1	1	0	0	1
58	Oscillator0 output 1	1	1	1	0	1	0
59	Oscillator1 output 1	1	1	1	0	1	1
60	POR OUT	1	1	1	1	0	0
61	V_{DD}	1	1	1	1	0	1
62	V_{DD}	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

6.3 Matrix Output Table

Table 5. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[5:0]	IN0 of 2-bit LUT0 or Clock Input of DFF0	0
[11:6]	IN1 of 2-bit LUT0 or Data Input of DFF0	1
[17:12]	IN0 of 2-bit LUT1 or Clock Input of DFF1	2
[23:18]	IN1 of 2-bit LUT1 or Data Input of DFF1	3
[29:24]	IN0 of 2-bit LUT2 or Clock Input of DFF2	4
[35:30]	IN1 of 2-bitLUT2 or Data Input of DFF2	5
[41:36]	IN0 of 2-bit LUT3 or Clock Input of PGen	6
[47:42]	IN1 of 2-bit LUT3 or nRST of PGen	7
[53:48]	IN0 of 3-bit LUT0 or CLK Input of DFF3	8
[59:54]	IN1 of 3-bit LUT0 or Data of DFF3	9
[65:60]	IN2 of 3-bit LUT0 or nRST (nSET) of DFF3	10
[71:66]	IN0 of 3-bit LUT1 or CLK Input of DFF4	11
[77:72]	IN1 of 3-bit LUT1 or Data of DFF4	12
[83:78]	IN2 of 3-bit LUT1 or nRST (nSET) of DFF4	13
[89:84]	IN0 of 3-bit LUT2 or CLK Input of DFF5	14
[95:90]	IN1 of 3-bit LUT2 or Data of DFF5	15
[101:96]	IN2 of 3-bit LUT2 or nRST(nSET) of DFF5	16
[107:102]	IN0 of 3-bit LUT3 or CLK Input of DFF6	17
[113:108]	IN1 of 3-bit LUT3 or Data of DFF6	18
[119:114]	IN2 of 3-bit LUT3 or nRST (nSET) of DFF6	19
[125:120]	IN0 of 3-bit LUT4 or CLK Input of DFF7	20
[131:126]	IN1 of 3-bit LUT4 or Data of DFF7	21
[137:132]	IN2 of 3-bit LUT4 or nRST (nSET) of DFF7	22
[143:138]	IN0 of 3-bit LUT5 or CLK Input of DFF8	23
[149:144]	IN1 of 3-bit LUT5 or Data of DFF8	24
[155:150]	IN2 of 3-bit LUT5 or nRST (nSET) of DFF8	25
[161:156]	IN0 of 3-bit LUT6 or CLK Input of DFF9	26
[167:162]	IN1 of 3-bit LUT6 or CLK Input of DFF9	27
[173:168]	IN2 of 3-bit LUT6 or nRST (nSET) of DFF9	28
[179:174]	IN0 of 3-bit LUT7 or CLK Input of DFF11 Delay1 Input (or Counter1 nRST Input)	29
[185:180]	IN1 of 3-bit LUT7 or nRST (nSET) of DFF11 Delay1 Input (or Counter1 nRST Input)	30
[191:186]	IN2 of 3-bit LUT7 or Data of DFF11 Delay1 Input (or Counter1 nRST Input)	31
[197:192]	IN0 of 3-bit LUT8 or CLK Input of DFF12 Delay2 Input (or Counter2 nRST Input)	32
[203:198]	IN1 of 3-bit LUT8 or nRST (nSET) of DFF12 Delay2 Input (or Counter2 nRST Input)	33
[209:204]	IN2 of 3-bit LUT8 or Data of DFF12 Delay2 Input (or Counter2 nRST Input)	34
[215:210]	IN0 of 3-bit LUT9 or CLK Input of DFF13 Delay3 Input (or Counter3 nRST Input)	35

Table 5. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[221:216]	IN1 of 3-bit LUT9 or nRST (nSET) of DFF13 Delay3 Input (or Counter3 nRST Input)	36
[227:222]	IN2 of 3-bit LUT9 or Data of DFF13 Delay3 Input (or Counter3 nRST Input)	37
[233:228]	IN0 of 3-bit LUT10 or CLK Input of DFF14 Delay4 Input (or Counter4 nRST Input)	38
[239:234]	IN1 of 3-bit LUT10 or nRST (nSET) of DFF14 Delay4 Input (or Counter4 nRST Input)	39
[245:240]	IN2 of 3-bit LUT10 or Data of DFF14 Delay4 Input (or Counter4 nRST Input)	40
[251:246]	IN0 of 3-bit LUT11 or CLK Input of DFF15 Delay5 Input (or Counter5 nRST Input)	41
[257:252]	IN1 of 3-bit LUT11 or nRST (nSET) of DFF15 Delay5 Input (or Counter5 nRST Input)	42
[263:258]	IN2 of 3-bit LUT11 or nRST (nSET) of DFF15 Delay5 Input (or Counter5 nRST Input)	43
[269:264]	IN0 of 3-bit LUT12 or CLK Input of DFF16 Delay6 Input (or Counter6 nRST Input)	44
[275:270]	IN1 of 3-bit LUT12 or nRST (nSET) of DFF16 Delay6 Input (or Counter6 nRST Input)	45
[281:276]	IN2 of 3-bit LUT12 or Data of DFF16 Delay6 Input (or Counter6 nRST Input)	46
[287:282]	IN0 of 3-bit LUT13 or Input of Pipe Delay or UP signal of RIPP CNT	47
[293:288]	IN1 of 3-bit LUT13 or nRST of Pipe Delay or nSet of RIPP CNT	48
[299:294]	IN2 of 3-bit LUT13 or CLK of Pipe Delay_RIPP CNT	49
[305:300]	IN0 of 4-bit LUT0 or CLK of DFF10	50
[311:306]	IN1 of 4-bit LUT0 or Data of DFF10	51
[317:312]	IN2 of 4-bit LUT0 or nRST (nSET) of DFF10	52
[323:318]	IN3 of 4-bit LUT0	53
[329:324]	IN0 of 4-bit LUT1 or CLK Input of DFF17 Delay0 Input (or Counter0 nRST Input)	54
[335:330]	IN1 of 4-bit LUT1 or nRST of DFF17 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source	55
[341:336]	IN2 of 4-bit LUT1 or nSet of DFF17 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source KEEP Input of FSM0	56
[347:342]	IN3 of 4-bit LUT1 or Data of DFF17 Delay0 Input (or Counter0 nRST Input) UP Input of FSM0	57
[353:348]	Programmable delay/edge detect input	58
[359:354]	Filter/Edge detect input	59
[365:360]	IO0 DOUT	60
[371:366]	IO0 DOUT OE	61
[377:372]	IO1 DOUT	62
[383:378]	IO1 DOUT OE	63
[389:384]	IO2 DOUT	64
[395:390]	IO2 DOUT OE	65
[401:396]	IO3 DOUT	66

Table 5. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[407:402]	IO3 DOUT OE	67
[413:408]	IO4 DOUT	68
[419:414]	IO4 DOUT OE	69
[425:420]	IO5 DOUT	70
[431:426]	IO5 DOUT OE	71
[437:432]	IO6 DOUT	72
[443:438]	IO6 DOUT OE	73
[449:444]	Set of PT0 block	74
[455:450]	Clock of PT0 block	75
[461:456]	Reload of PT0 block	76
[467:462]	Reserved	77
[473:468]	Up/Down of PT0 block	78
[479:474]	Set of PT1 block	79
[485:480]	Clock of PT1 block	80
[491:486]	Reload of PT1 block	81
[497:492]	Reserved	82
[503:498]	Up/Down of PT1 block	83
[509:504]	FIFO Reset of PT blocks	84
[515:510]	Power Up of Chopper ACMP	85
[521:516]	Rheostats Charge Pump Enable	86
[527:522]	ASW0 enable/Half bridge Enable	87
[533:528]	ASW1 enable/Half bridge data	88
[539:534]	ACMP0 Power Up	89
[545:540]	ACMP1 Power Up	90
[551:546]	Oscillator0 Enable	91
[557:552]	Oscillator1 Enable	92
[563:558]	Oscillator2 Enable	93
[569:564]	$V_{REF}0$, Temp sensor, $V_{REF}0$ Power Up	94
[575:570]	HDBUF Enable	95
[581:576]	Op Amp0 Power Up	96
[587:582]	Op Amp1 Power Up	97
[593:588]	Op Amp2 Power Up	98
[599:594]	Op Amps V_{REF} Enable	99
[1] For each Address, the two most significant bits are unused.		

6.4 Connection Matrix Virtual Inputs

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at 0x7C (124).

An I2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened). See table Table 6.

Table 6. Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
32	I2C_virtual_0 Input	[992]
33	I2C_virtual_1 Input	[993]
34	I2C_virtual_2 Input	[994]
35	I2C_virtual_3 Input	[995]
36	I2C_virtual_4 Input	[996]
37	I2C_virtual_5 Input	[997]
38	I2C_virtual_6 Input	[998]
39	I2C_virtual_7 Input	[999]

6.5 Connection Matrix Virtual Outputs

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I2C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I2C addresses for reading these register values are bytes 0xC4 (196) to 0xCA (202). Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at byte 0x7C (124)).

7. Combination Function Macrocells

The SLG47004 has 13 combination function macrocells that can serve as more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells:

- Three macrocells that can serve as either 2-bit LUT or as D Flip-Flop
- Seven macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay/Ripple Counter
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen)

One macrocell that can serve as either 4-bit LUT or as D Flip-Flop with Set/Reset Input.

Inputs/Outputs for the 13 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of configuration bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user-defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

7.1 2-Bit LUT or D Flip-Flop Macrocells

There is one macrocell that can serve as either 2-bit LUT or as D Flip-Flop. When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

- DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.
- LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

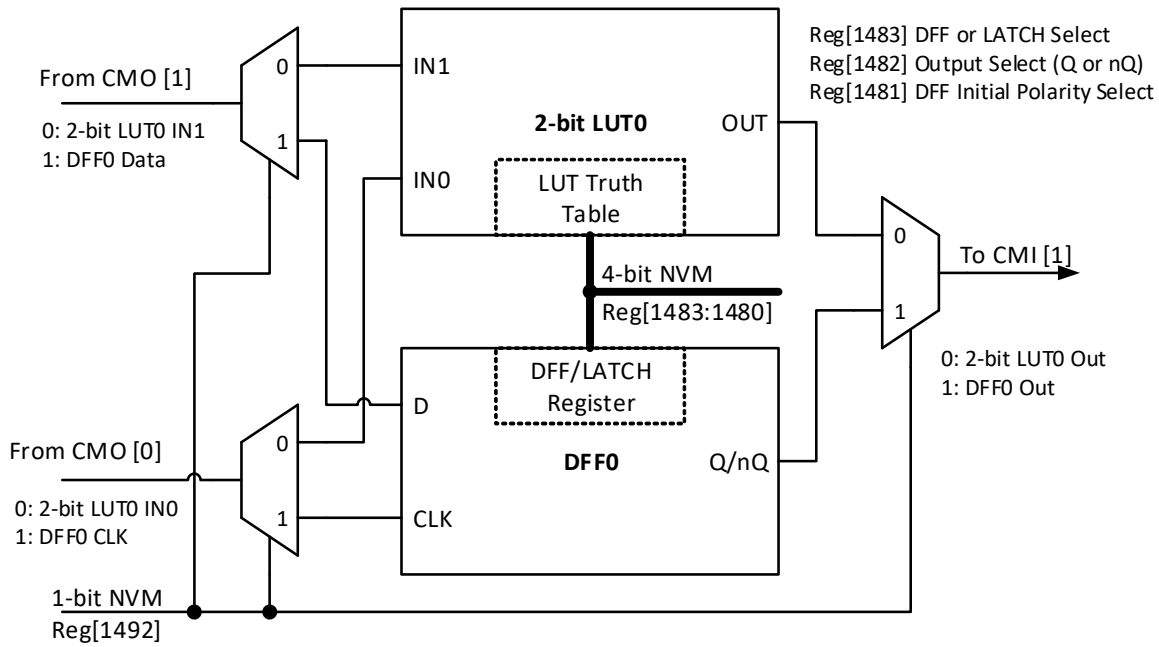


Figure 14. 2-bit LUT0 or DFF0

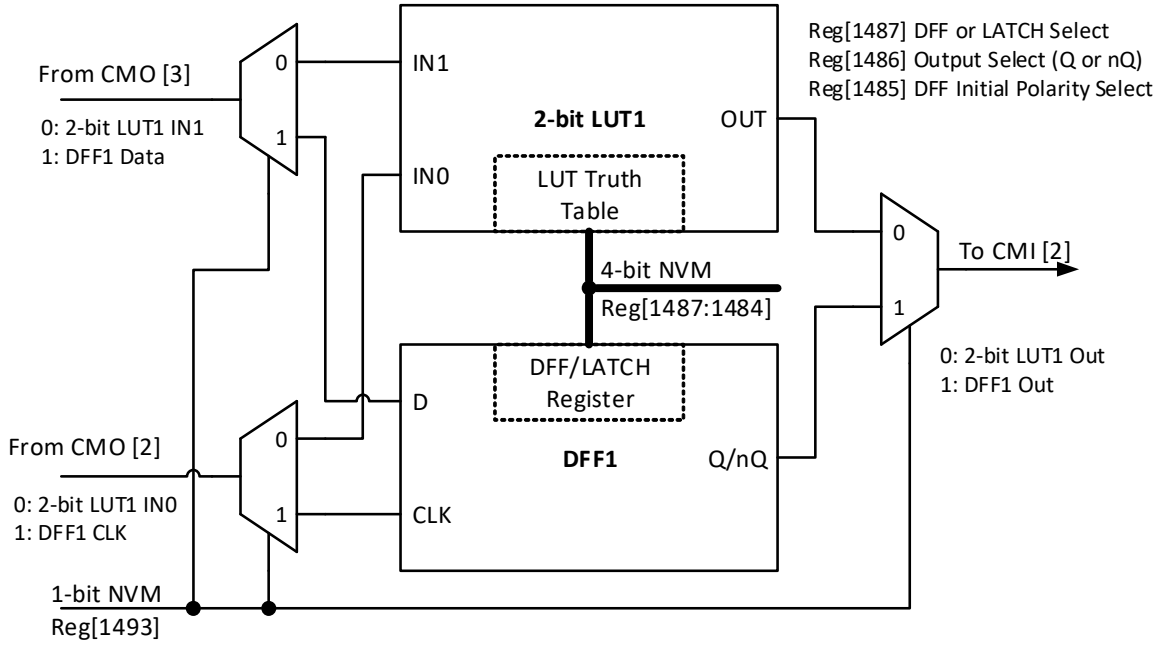


Figure 15. 2-bit LUT1 or DFF1

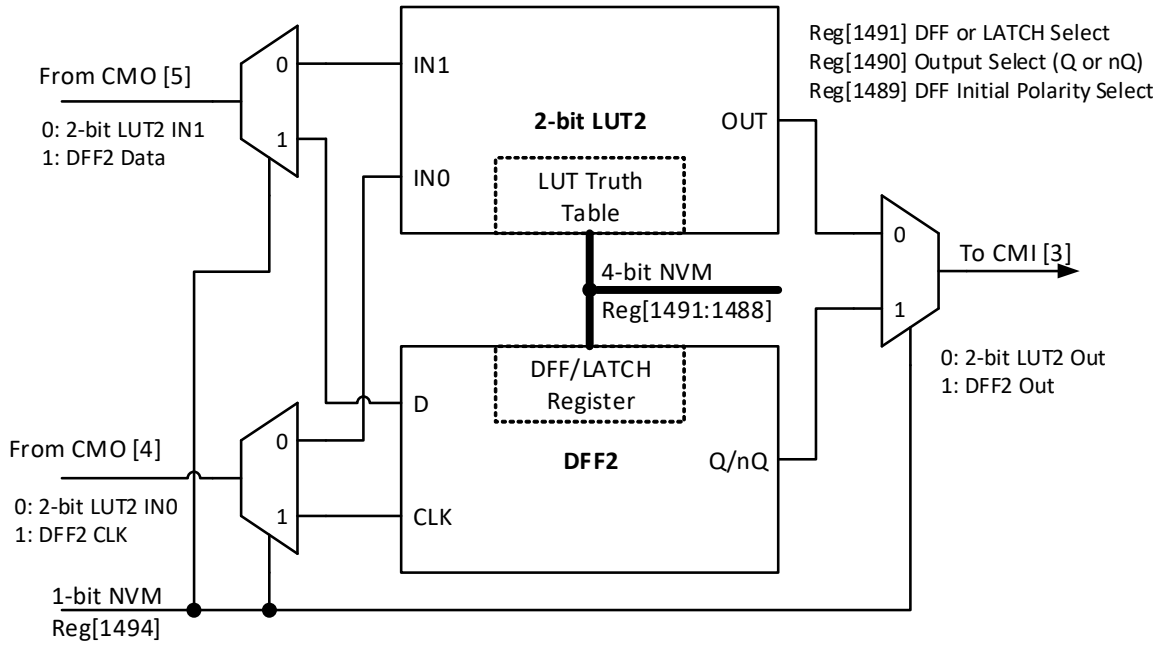


Figure 16. 2-bit LUT2 or DFF2

7.1.1 2-Bit LUT or D Flip-Flop Macrocell Used as 2-Bit LUT

Table 7. 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	reg [1480]	LSB
0	1	reg [1481]	
1	0	reg [1482]	
1	1	reg [1483]	MSB

Table 8. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	reg [1484]	LSB
0	1	reg [1485]	
1	0	reg [1486]	
1	1	reg [1487]	MSB

Table 9. 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	reg [1488]	LSB
0	1	reg [1489]	
1	0	reg [1490]	
1	1	reg [1491]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

- 2-bit LUT0 is defined by reg [1483:1480]
- 2-bit LUT1 is defined by reg [1487:1484]
- 2-bit LUT2 is defined by reg [1491:1488]

Table 10 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 10. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.1.2 Initial Polarity Operations

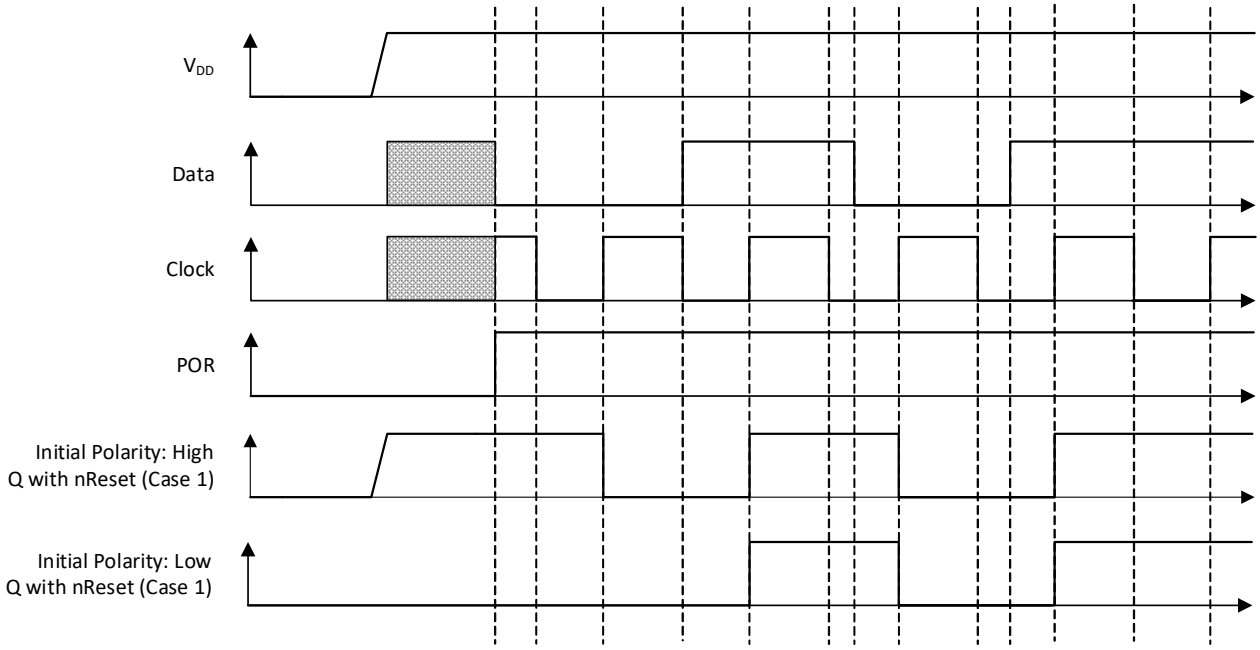


Figure 17. DFF Polarity Operations

7.2 2-bit LUT or Programmable Pattern Generator

The SLG47004 has one combination function macrocell that can serve as a logic or a timing function. This macrocell can serve as a Look Up Table (LUT), or a Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUT can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

It is possible to define the RST level for the PGen macrocell. There are both high level reset (RST) and a low level reset (nRST) options available, which are selected by reg [1517]. When operating as the Programmable Pattern Generator, the output of the macrocell will clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

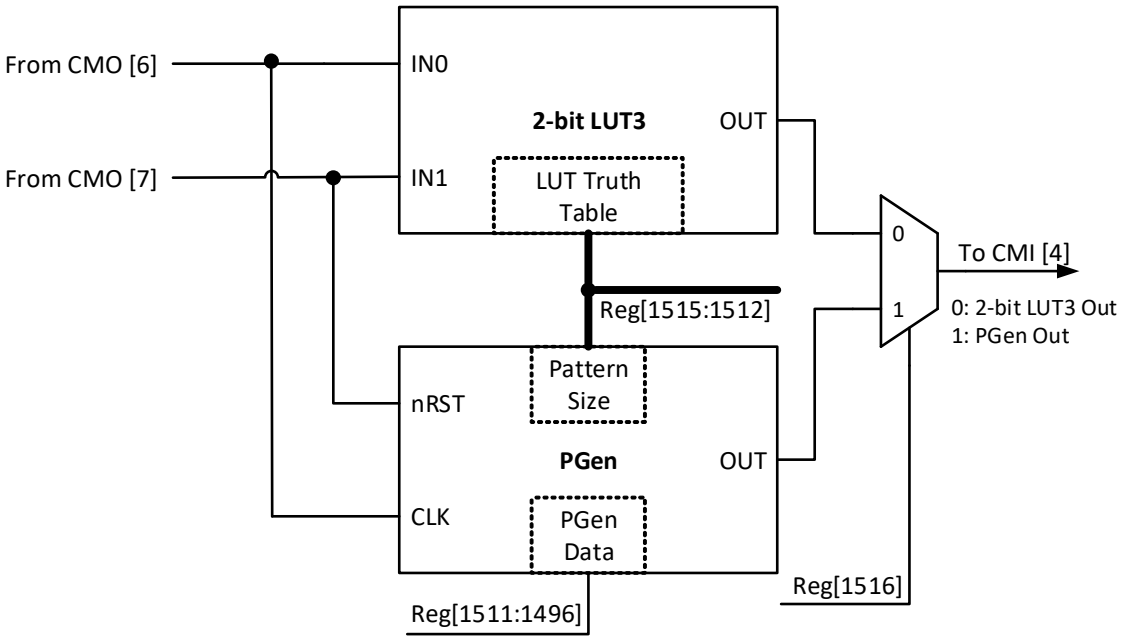


Figure 18. 2-bit LUT3 or PGen

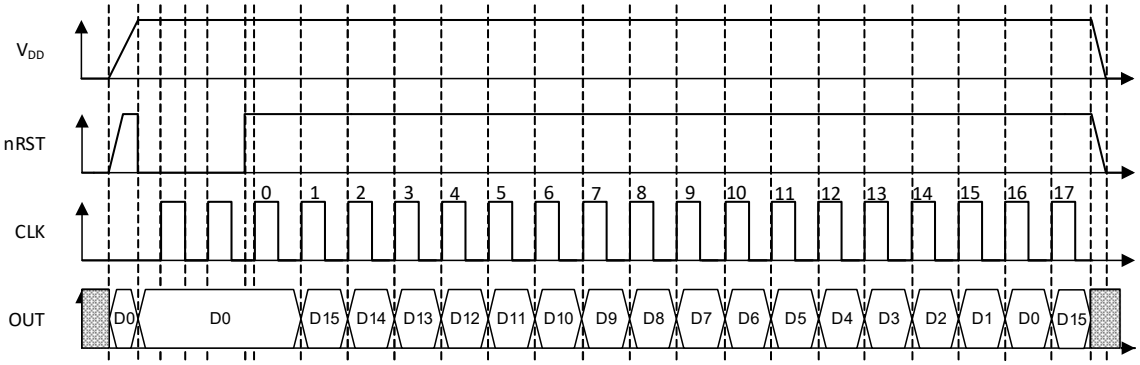


Figure 19. PGen Timing Diagram

7.2.1 2-Bit LUT or PGen Macrocell Used as 2-Bit LUT

Table 11. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	reg [1512]	LSB
0	1	reg [1513]	
1	0	reg [1514]	
1	1	reg [1515]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

- 2-bit LUT3 is defined by registers [1515:1512]

Table 12 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 12. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.3 3-Bit LUT or D Flip-Flop with Set/Reset Macrocells

There are seven macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available, which are selected by reg [1523].

DFF3 operation will flow the functional description below:

- If reg [1522] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.
- If reg [1522] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

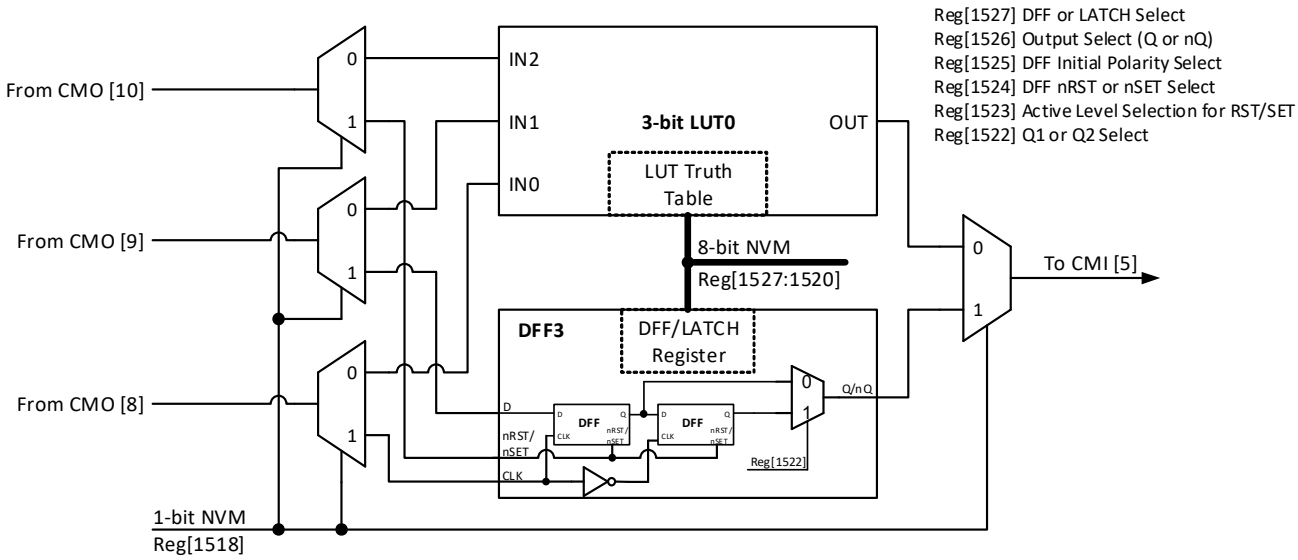


Figure 20. 3-bit LUT0 or DFF3

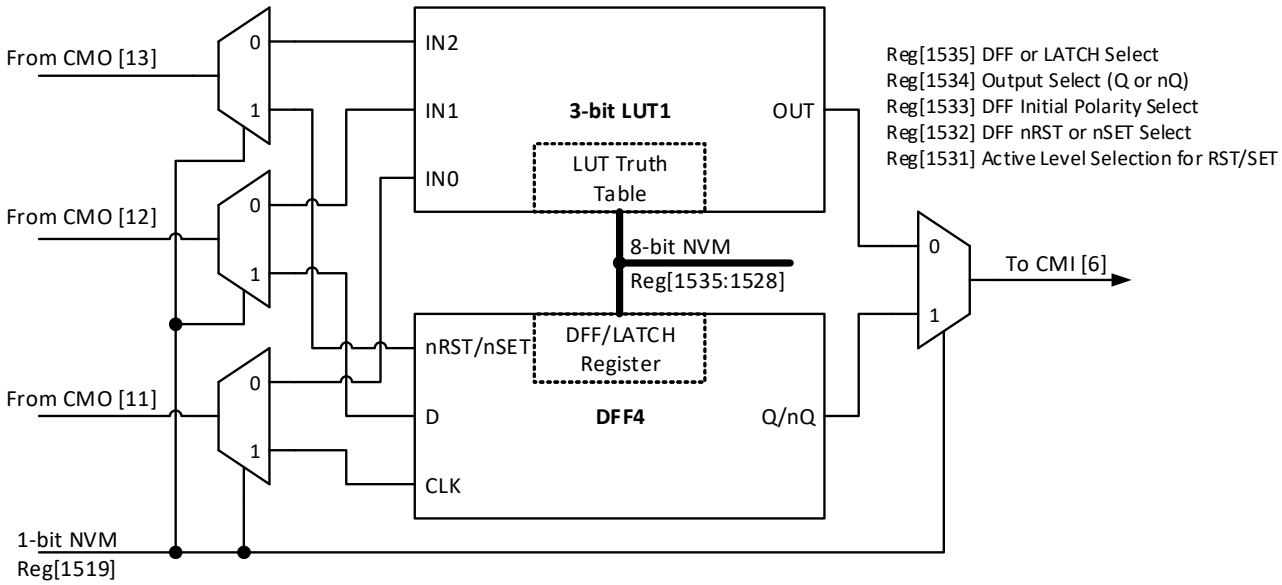


Figure 21. 3-bit LUT1 or DFF4

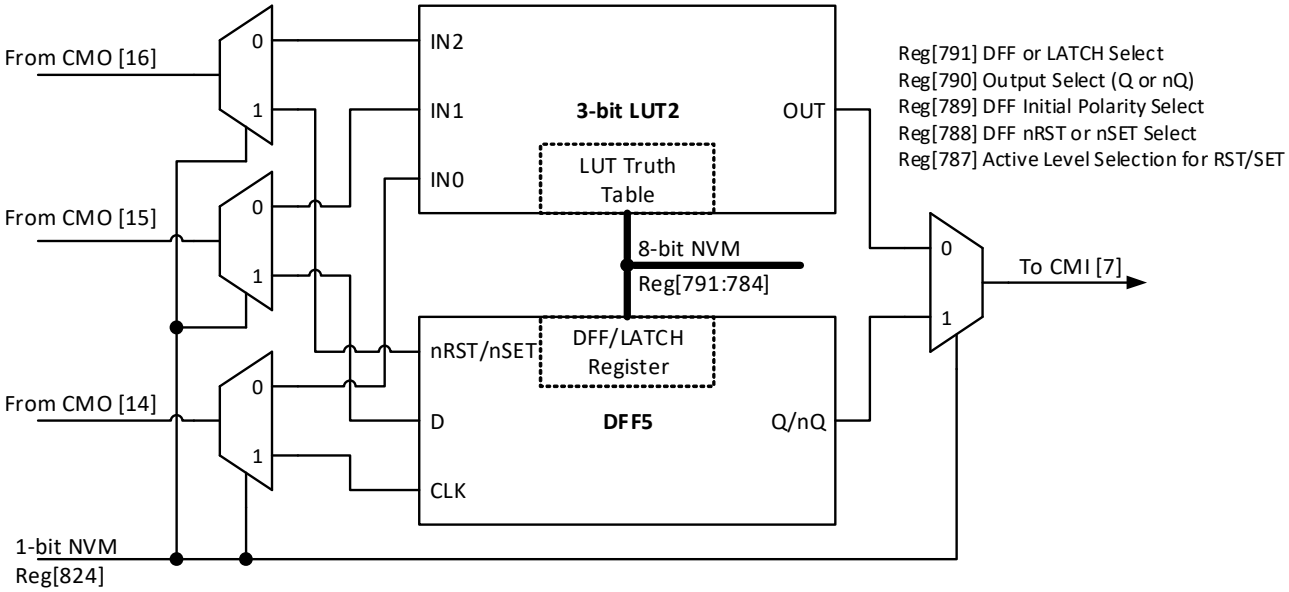


Figure 22. 3-bit LUT2 or DFF5

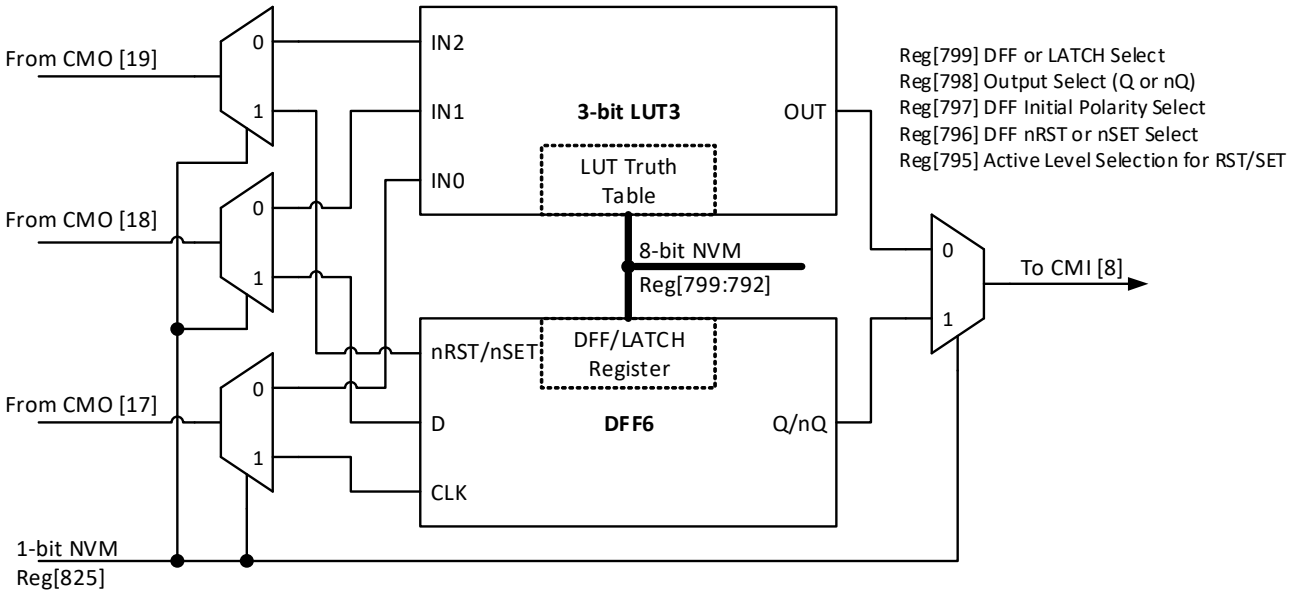


Figure 23. 3-bit LUT3 or DFF6

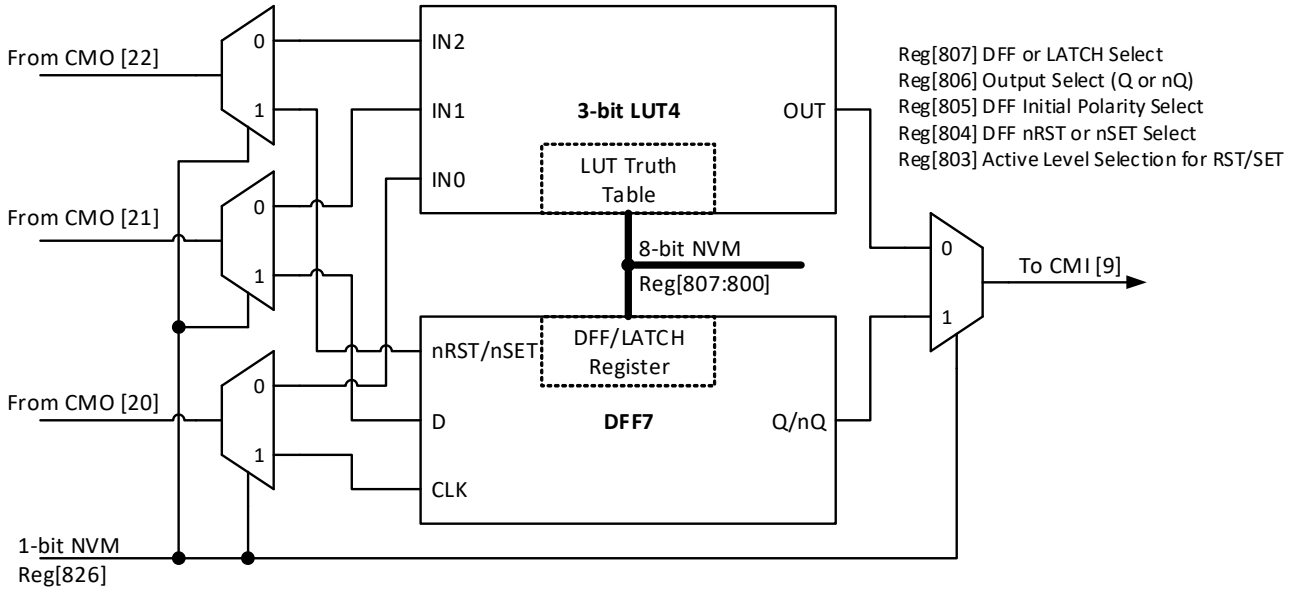


Figure 24. 3-bit LUT4 or DFF7

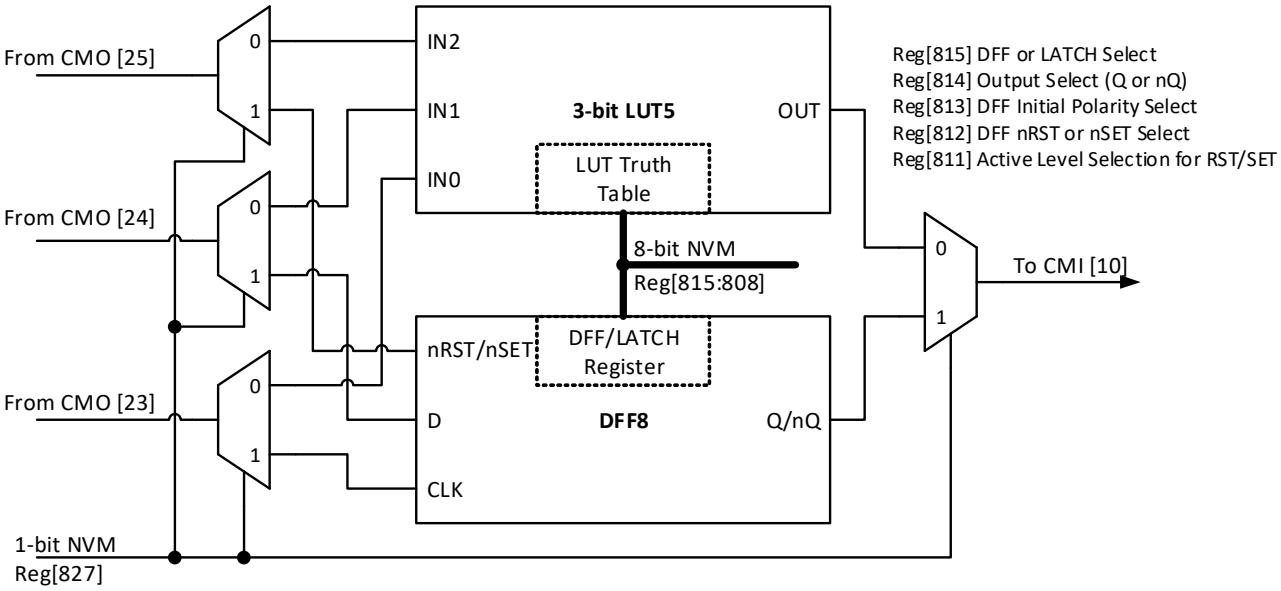


Figure 25. 3-bit LUT5 or DFF8

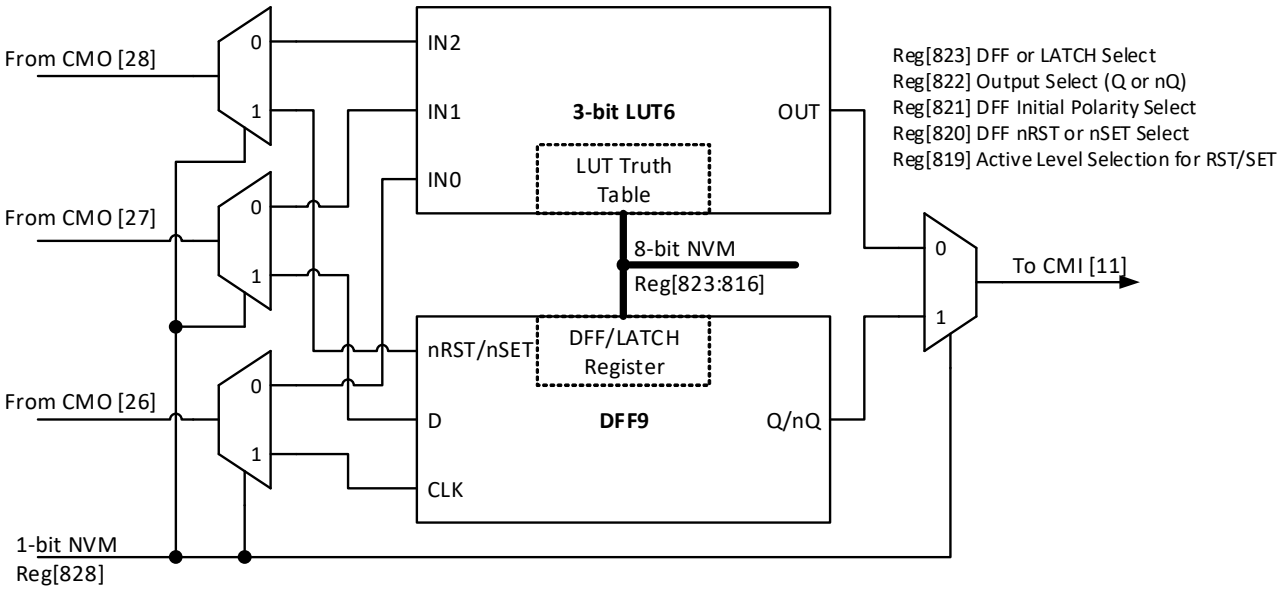


Figure 26. 3-bit LUT6 or DFF9

7.3.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 13. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [1520]	LSB
0	0	1	reg [1521]	
0	1	0	reg [1522]	
0	1	1	reg [1523]	
1	0	0	reg [1524]	
1	0	1	reg [1525]	
1	1	0	reg [1526]	
1	1	1	reg [1527]	MSB

Table 14. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [1528]	LSB
0	0	1	reg [1529]	
0	1	0	reg [1530]	
0	1	1	reg [1531]	
1	0	0	reg [1532]	
1	0	1	reg [1533]	
1	1	0	reg [1534]	
1	1	1	reg [1535]	MSB

Table 15. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [784]	LSB
0	0	1	reg [785]	
0	1	0	reg [786]	
0	1	1	reg [787]	
1	0	0	reg [788]	
1	0	1	reg [789]	
1	1	0	reg [790]	
1	1	1	reg [791]	MSB

Table 16. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [792]	LSB
0	0	1	reg [793]	
0	1	0	reg [794]	
0	1	1	reg [795]	
1	0	0	reg [796]	
1	0	1	reg [797]	
1	1	0	reg [798]	
1	1	1	reg [799]	MSB

Table 17. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [800]	LSB
0	0	1	reg [801]	
0	1	0	reg [802]	
0	1	1	reg [803]	
1	0	0	reg [804]	
1	0	1	reg [805]	
1	1	0	reg [806]	
1	1	1	reg [807]	MSB

Table 18. 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [808]	LSB
0	0	1	reg [809]	
0	1	0	reg [810]	
0	1	1	reg [811]	
1	0	0	reg [812]	
1	0	1	reg [813]	
1	1	0	reg [814]	
1	1	1	reg [815]	MSB

Table 19. 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [816]	LSB
0	0	1	reg [817]	
0	1	0	reg [818]	
0	1	1	reg [819]	
1	0	0	reg [820]	
1	0	1	reg [821]	
1	1	0	reg [822]	
1	1	1	reg [823]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

- 3-bit LUT0 is defined by reg [1527:1520]
- 3-bit LUT1 is defined by reg [1535:1528]
- 3-bit LUT2 is defined by reg [791:784]
- 3-bit LUT3 is defined by reg [799:792]
- 3-bit LUT4 is defined by reg [807:800]
- 3-bit LUT5 is defined by reg [815:808]
- 3-bit LUT6 is defined by reg [823:816]

Table 20 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 20. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.3.2 Initial Polarity Operations

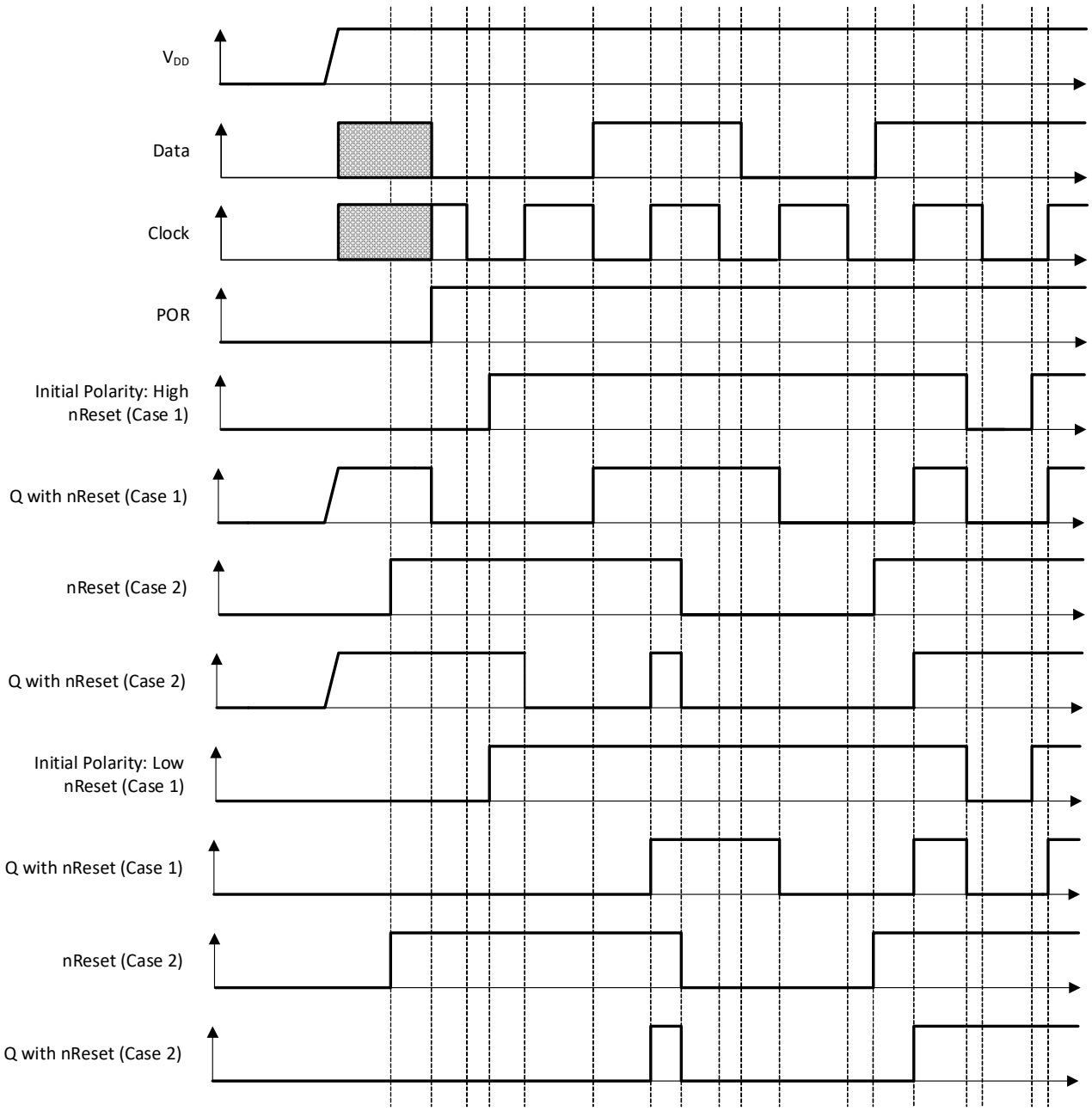


Figure 27. DFF Polarity Operations with nReset

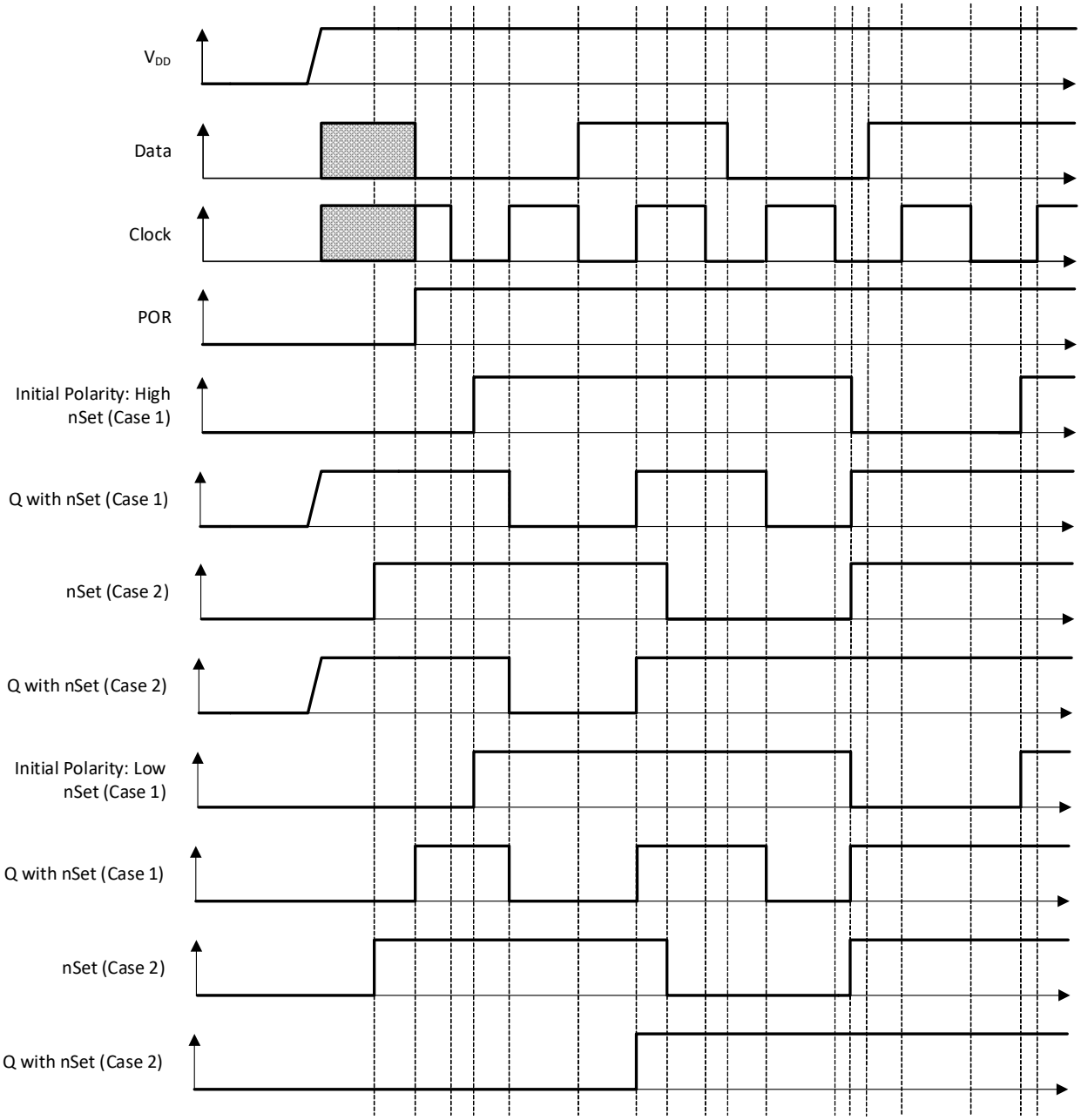


Figure 28. DFF Polarity Operations with nSet

7.4 4-Bit LUT or D Flip-Flop with Set/Reset Macrocell

There is one macrocell that can serve as either a 4-bit LUT or as a D Flip-Flop with Set/Reset inputs. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix.

If reg [842] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.

If reg [842] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK. It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are

both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available, which are selected by reg [843].

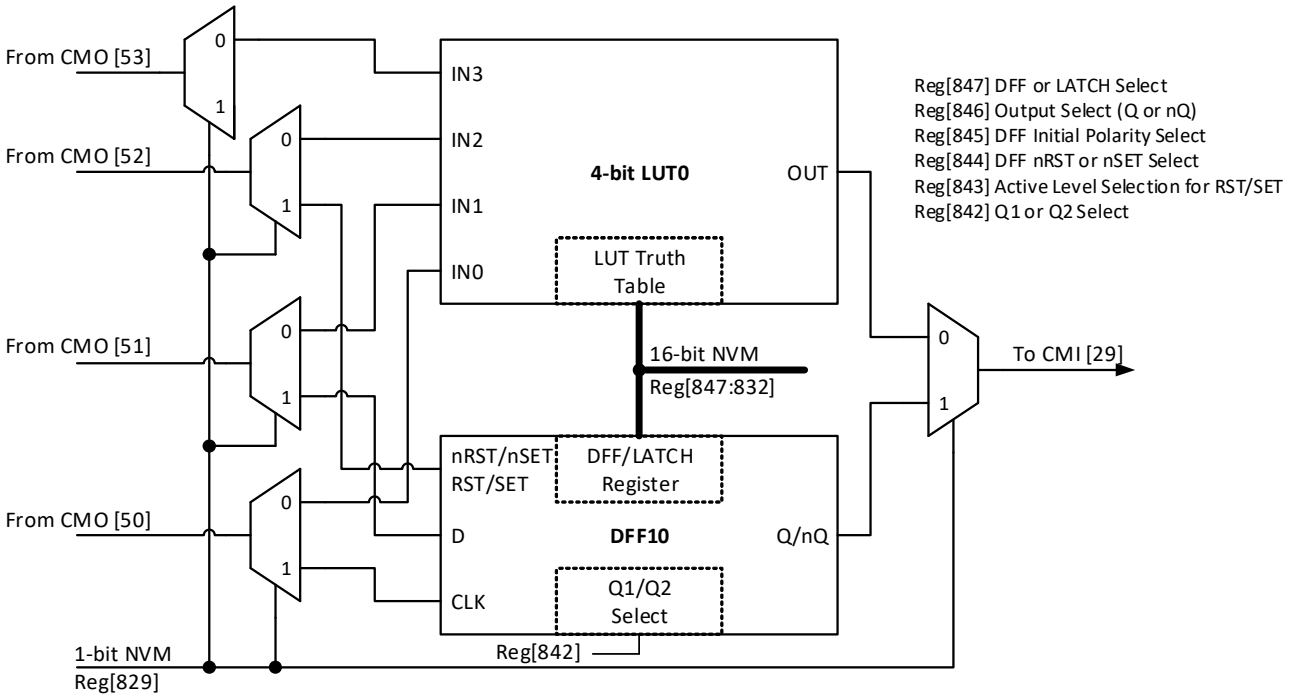


Figure 29. 4-bit LUT0 or DFF10

7.4.1 4-Bit LUT Macrocell Used as 4-Bit LUT

Table 21. 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	reg [832]	LSB
0	0	0	1	reg [833]	
0	0	1	0	reg [834]	
0	0	1	1	reg [835]	
0	1	0	0	reg [836]	
0	1	0	1	reg [837]	
0	1	1	0	reg [838]	
0	1	1	1	reg [839]	
1	0	0	0	reg [840]	
1	0	0	1	reg [841]	
1	0	1	0	reg [842]	
1	0	1	1	reg [843]	
1	1	0	0	reg [844]	
1	1	0	1	reg [845]	
1	1	1	0	reg [846]	
1	1	1	1	reg [847]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

- 4-bit LUT0 is defined by reg [847:832]

Table 22. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

7.5 3-Bit LUT or Pipe Delay/Ripple Counter Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay/Ripple Counter.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a Pipe Delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK), and Reset (nRST). The Pipe Delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell input (IN). Both of the two outputs (OUT0 and OUT1) provide user selectable options for 1 to 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by registers [851:848] for OUT0 and registers [855:852] for OUT1.
The 4-input MUX is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG47004 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the internal Oscillator within the SLG47004). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell. OUT1 Output can be inverted (as selected by reg [859]).

In the Ripple Counter mode, there are 3 options for setting, which use 7 bits. There are 3 bits to set nSET value (SV) in range from 0 to 7. It is a value, which will be set into the Ripple Counter outputs when nSET input goes LOW. End value (EV) will use 3 bits for setting outputs code, which will be last code in the cycle. After reaching the EV, the Ripple Counter goes to the first code by the rising edge on CLK input. The Functionality mode option uses 1 bit. This setting defines how exactly Ripple Counter will operate.

The user can select one of the functionality modes by register: RANGE or FULL. If the RANGE option is selected, the count starts from SV. If UP input is LOW the count goes down: SV→EV→EV-1 to SV+1→SV, and others (if SV is smaller than EV), or SV→SV-1 to EV+1→EV→SV (if SV is bigger than EV). If UP input is HIGH, count starts from SV up to EV, and others.

In the FULL range configuration the Ripple Counter functions as follows. If UP input is LOW, the count starts from SV and goes down to 0. Then current counter value jumps to EV and goes down to 0, and others.

If UP input is HIGH, count goes up starting from SV. Then current counter value jumps to 0 and counts up to EV, and others. See Ripple Counter functionality example in Figure 31.

Every step is executed by the rising edge on CLK input.

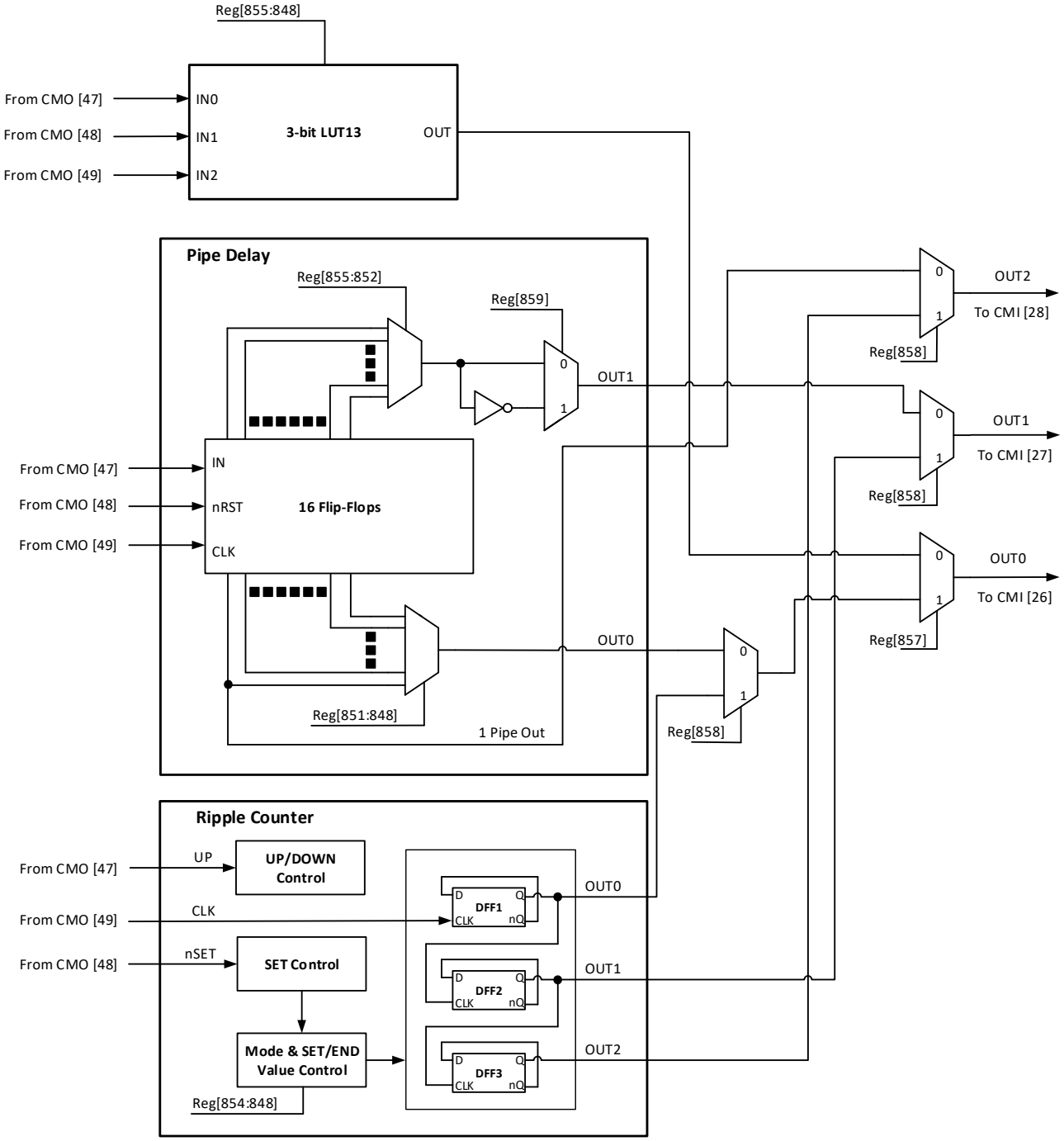


Figure 30. 3-bit LUT13/Pipe Delay/Ripple Counter

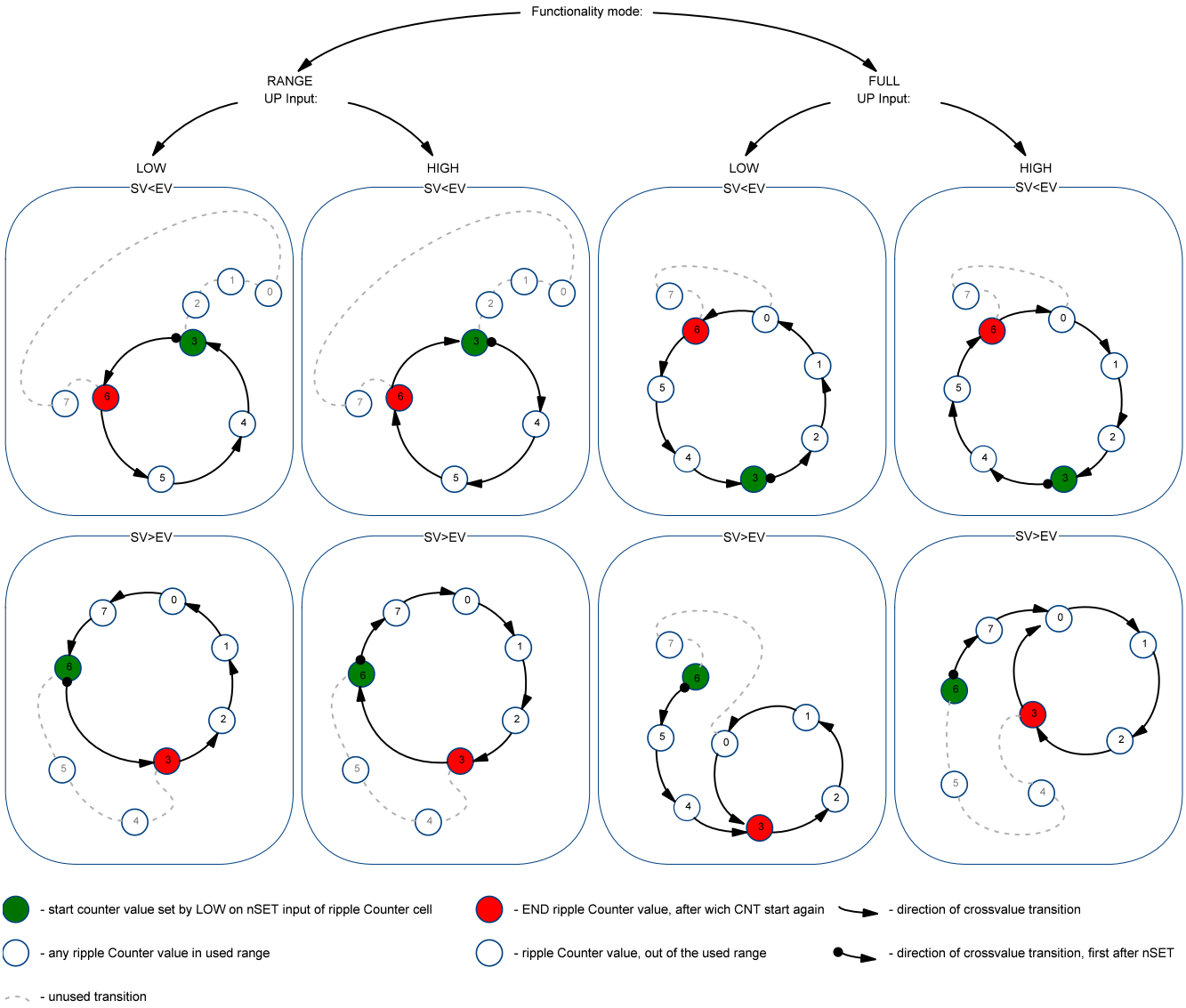


Figure 31. Example of Ripple Counter Functionality

7.5.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUT

Table 23. 3-bit LUT13 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [848]	LSB
0	0	1	reg [849]	
0	1	0	reg [850]	
0	1	1	reg [851]	
1	0	0	reg [852]	
1	0	1	reg [853]	
1	1	0	reg [854]	
1	1	1	reg [855]	MSB

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

- 3-bit LUT13 is defined by reg [855:848]

8. Multi-Function Macrocells

The SLG47004 has seven Multi-Function macrocells that can serve as more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes such as One Shot, Frequency Detect, Edge Detect, and others. Also, the macrocell is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF, see Figure 32.

See the list below for the functions that can be implemented in these macrocells:

- Six macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays.
- One macrocell that can serve as a 4-bit LUT/D Flip-Flop and as 16-Bit Counter/Delay/FSM.

Figure 32. Possible Connections inside Multi-Function Macrocell

Inputs/Outputs for the seven Multi-Function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

8.1 3-Bit LUT or DFF/LATCH with 8-Bit Counter/Delay Macrocells

There are six macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays.

When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix or can be connected to CNT/DLY's input.

When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D), clock (CLK), and Reset/Set (nRST/nSET) inputs of the Flip-Flop, with the output going back to the connection matrix or to the CNT/DLY's input.

When used to implement Counter/Delays, each macrocell has a dedicated matrix input connection. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits. These macrocells can also operate in a One-Shot mode, which will generate an output pulse of user-defined width. They can also operate in a Frequency Detection or Edge Detection mode.

Counter/Delay macrocell has an initial value, which defines its initial value after SLG47004 is powered up. It is possible to select initial Low or initial High, as well as initial value defined by a Delay In signal.

For example, in case initial LOW option is used, the rising edge delay will start operation.

For timing diagrams refer to section 8.3 CNT/DLY/FSM Timing Diagrams.

Note: After two DFF – counters initialize with counter data = 0 after POR.

Initial state = 1 – counters initialize with counter data = 0 after POR.

Initial state = 0 and after two DFF is bypass – counters initialize with counter data after POR.

CNT5 and CNT6 current count value can be read via I^2C. However, it is possible to change the counter data (value counter starts operating from) for any macrocell using I^2C write commands. In this mode, it is possible to load count data immediately (after two DFF) or after counter ends counting. See section 18.7.1 Reading Counter Data via I2C for further details.

8.1.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

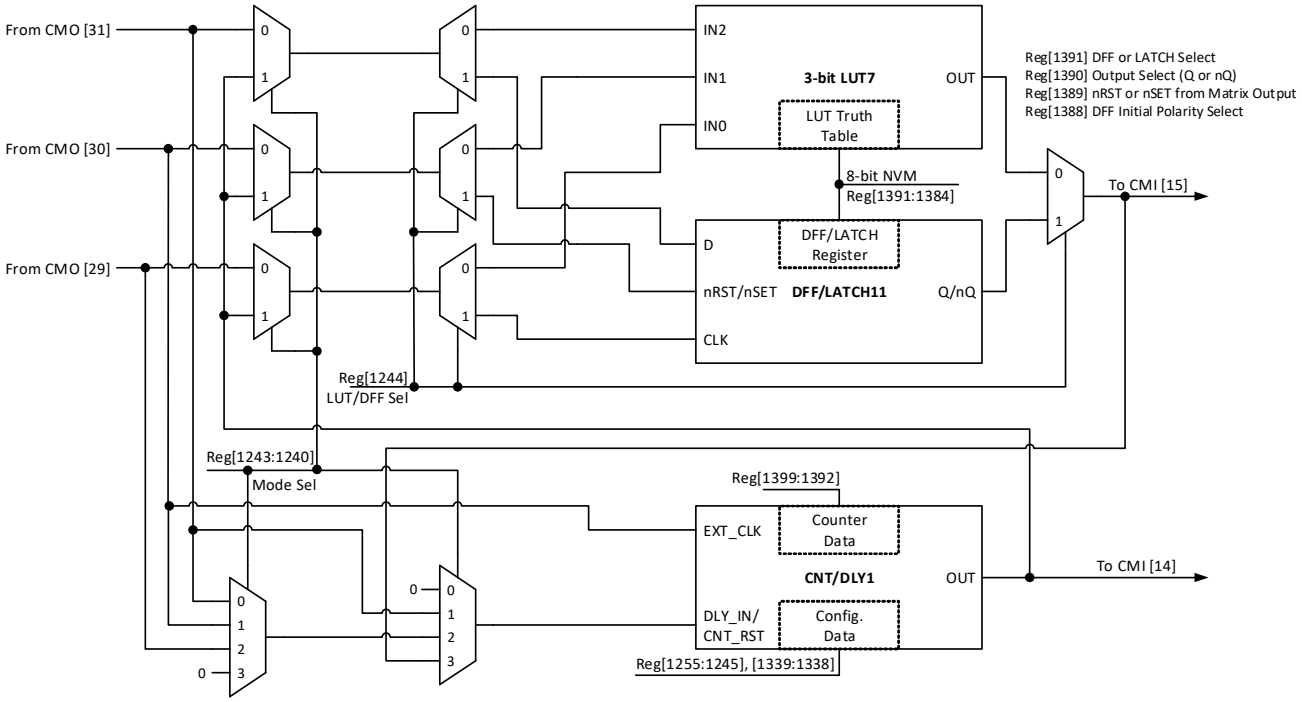


Figure 33. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT7/DFF11, CNT/DLY1)

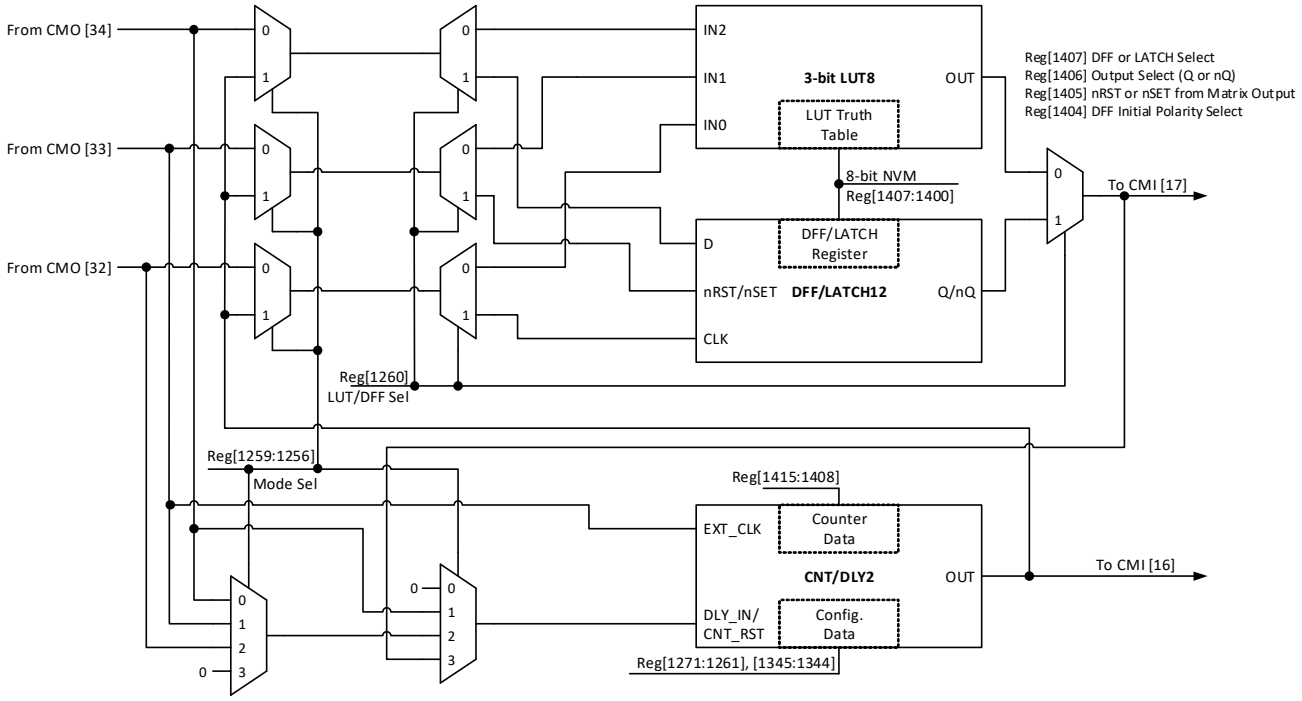


Figure 34. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT8/DFF12, CNT/DLY2)

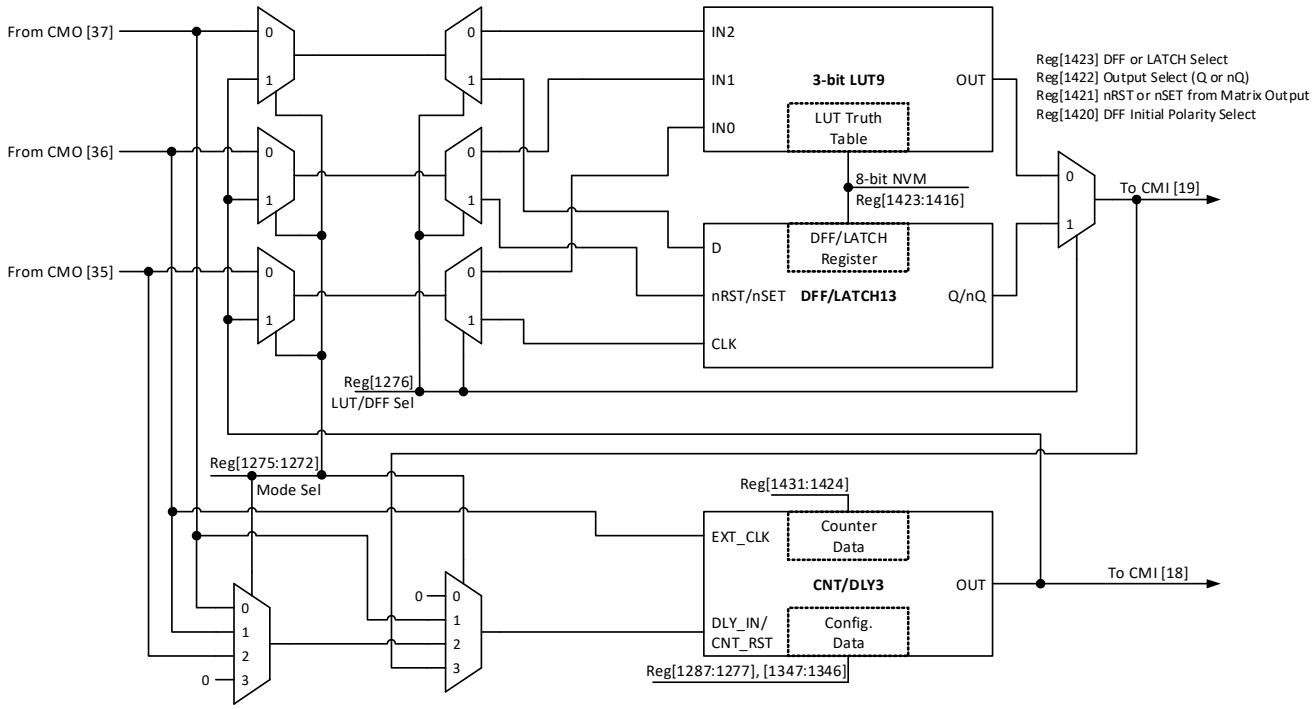


Figure 35. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT9/DFF13, CNT/DLY3)

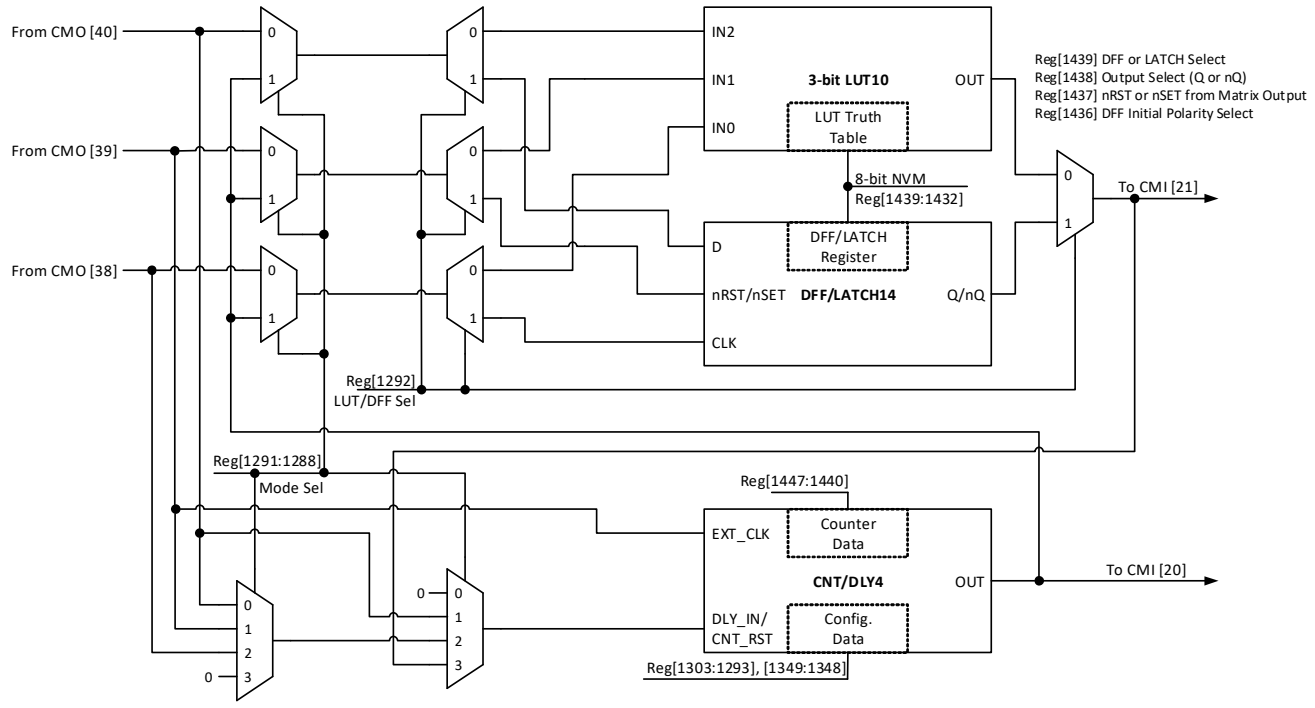


Figure 36. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT10/DFF14, CNT/DLY4)

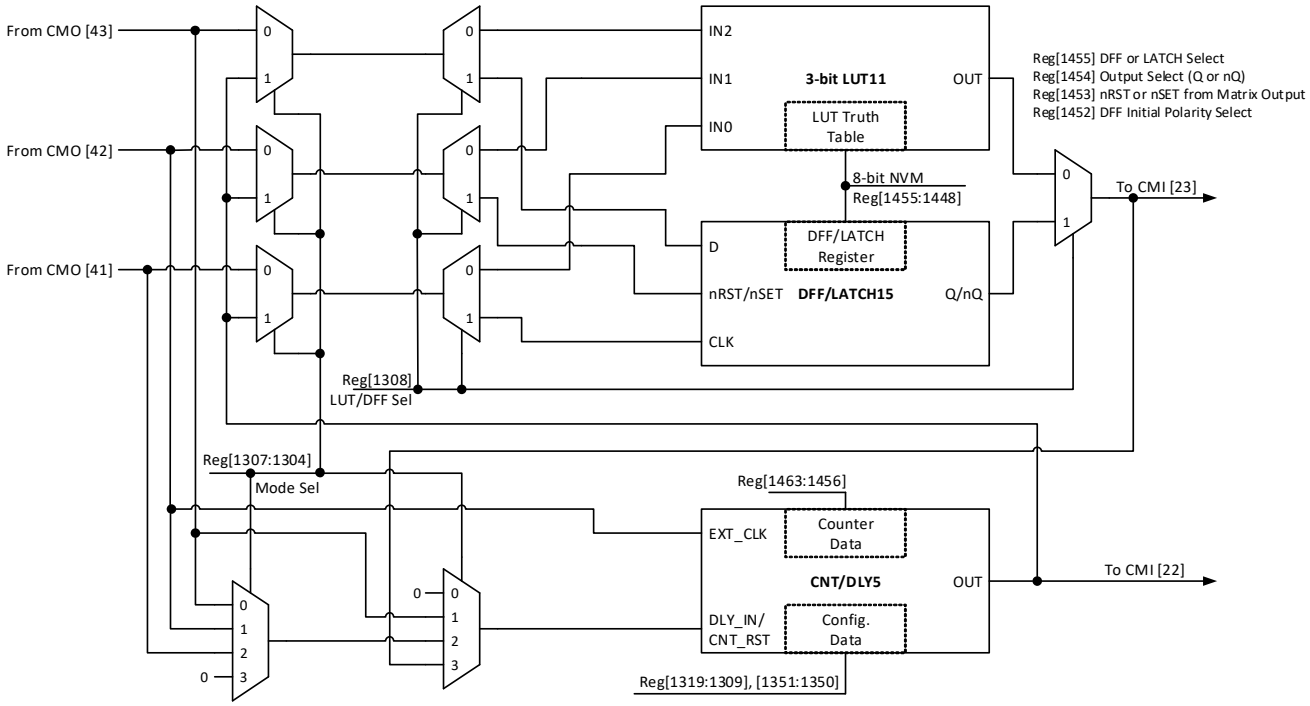


Figure 37. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT11/DFF15, CNT/DLY5)

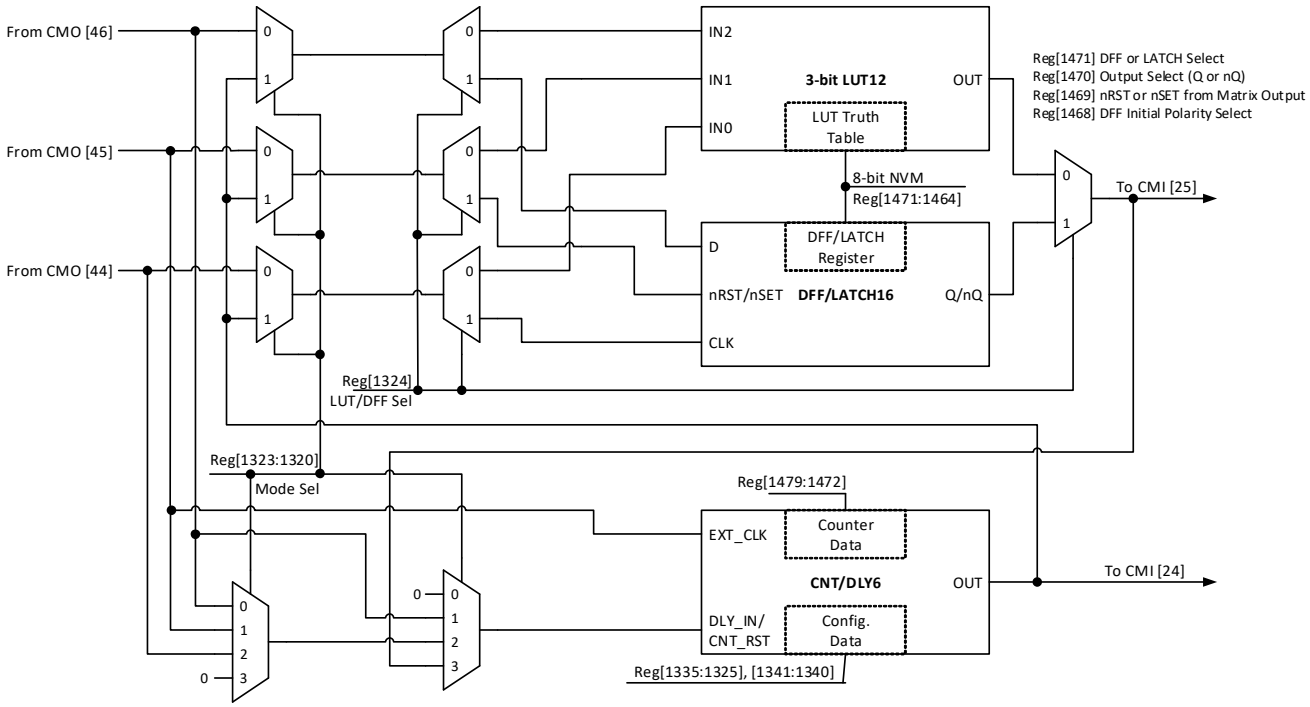


Figure 38. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT12/DFF16, CNT/DLY6)

As shown in Figure 33 to Figure 38, there is a possibility to use LUT/DFF and CNT/DLY simultaneously.

Note: It is not possible to use LUT and DFF at once, one of these macrocells must be selected.

- Case 1. LUT/DFF in front of CNT/DLY. Three input signals from the connection matrix go to previously selected LUT or DFF's inputs and produce a single output which goes to a CND/DLY input. In its turn Counter/Delay's output goes back to the matrix.
- Case 2. CNT/DLY in front of LUT/DFF. Two input signals from the connection matrix go to CND/DLY's inputs (IN and CLK). Its output signal can be connected to any input of previously selected LUT or DFF, after which the signal goes back to the matrix.
- Case 3. Single LUT/DFF or CNT/DLY. Also, it is possible to use a standalone LUT/DFF or CNT/DLY. In this case, all inputs and output of the macrocell are connected to the matrix.

8.1.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

Table 24. 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [1384]	LSB
0	0	1	reg [1385]	
0	1	0	reg [1386]	
0	1	1	reg [1387]	
1	0	0	reg [1388]	
1	0	1	reg [1389]	
1	1	0	reg [1390]	
1	1	1	reg [1391]	MSB

Table 25. 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [1400]	LSB
0	0	1	reg [1401]	
0	1	0	reg [1402]	
0	1	1	reg [1403]	
1	0	0	reg [1404]	
1	0	1	reg [1405]	
1	1	0	reg [1406]	
1	1	1	reg [1407]	MSB

Table 26. 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [1416]	LSB
0	0	1	reg [1417]	
0	1	0	reg [1418]	
0	1	1	reg [1419]	
1	0	0	reg [1420]	
1	0	1	reg [1421]	
1	1	0	reg [1422]	
1	1	1	reg [1423]	MSB

Table 27. 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [1432]	LSB
0	0	1	reg [1433]	
0	1	0	reg [1434]	
0	1	1	reg [1435]	
1	0	0	reg [1436]	
1	0	1	reg [1437]	
1	1	0	reg [1438]	
1	1	1	reg [1439]	MSB

Table 28. 3-bit LUT11 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [1448]	LSB
0	0	1	reg [1449]	
0	1	0	reg [1450]	
0	1	1	reg [1451]	
1	0	0	reg [1452]	
1	0	1	reg [1453]	
1	1	0	reg [1454]	
1	1	1	reg [1455]	MSB

Table 29. 3-bit LUT12 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [1464]	LSB
0	0	1	reg [1465]	
0	1	0	reg [1466]	
0	1	1	reg [1467]	
1	0	0	reg [1468]	
1	0	1	reg [1469]	
1	1	0	reg [1470]	
1	1	1	reg [1471]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

- 3-bit LUT7 is defined by registers [1391:1384]
- 3-bit LUT8 is defined by registers [1407:1400]
- 3-bit LUT9 is defined by registers [1423:1416]
- 3-bit LUT10 is defined by registers [1439:1432]
- 3-bit LUT11 is defined by registers [1455:1448]
- 3-bit LUT12 is defined by registers [1471:1464]

8.2 4-Bit LUT or DFF/LATCH with 16-Bit Counter/Delay Macrocell

There is one macrocell that can serve as either 4-bit LUT/D Flip-Flops or as 16-bit Counter/Delay.

When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix.

When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

When used to implement 16-Bit Counter/Delay function, two of the four input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_IN/CNT Reset) for the Counter/Delay, with the output going back to the connection matrix.

This macrocell has an optional Finite State Machine (FSM) function. There are two additional matrix inputs for Up and Keep to support FSM functionality.

This macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width. This macrocell can also operate in a frequency detection or edge detection mode.

This macrocell can have its active count value read via I^2C. See section 18.7.1 Reading Counter Data via I2C.

Note: After two DFF – counters initialize with counter data = 0 after POR.

Initial state = 1 – counters initialize with counter data = 0 after POR.

Initial state = 0 and after two DFF is bypass – counters initialize with counter data after POR.

8.2.1 4-Bit LUT or DFF/LATCH with 16-Bit CNT/DLY Block Diagram

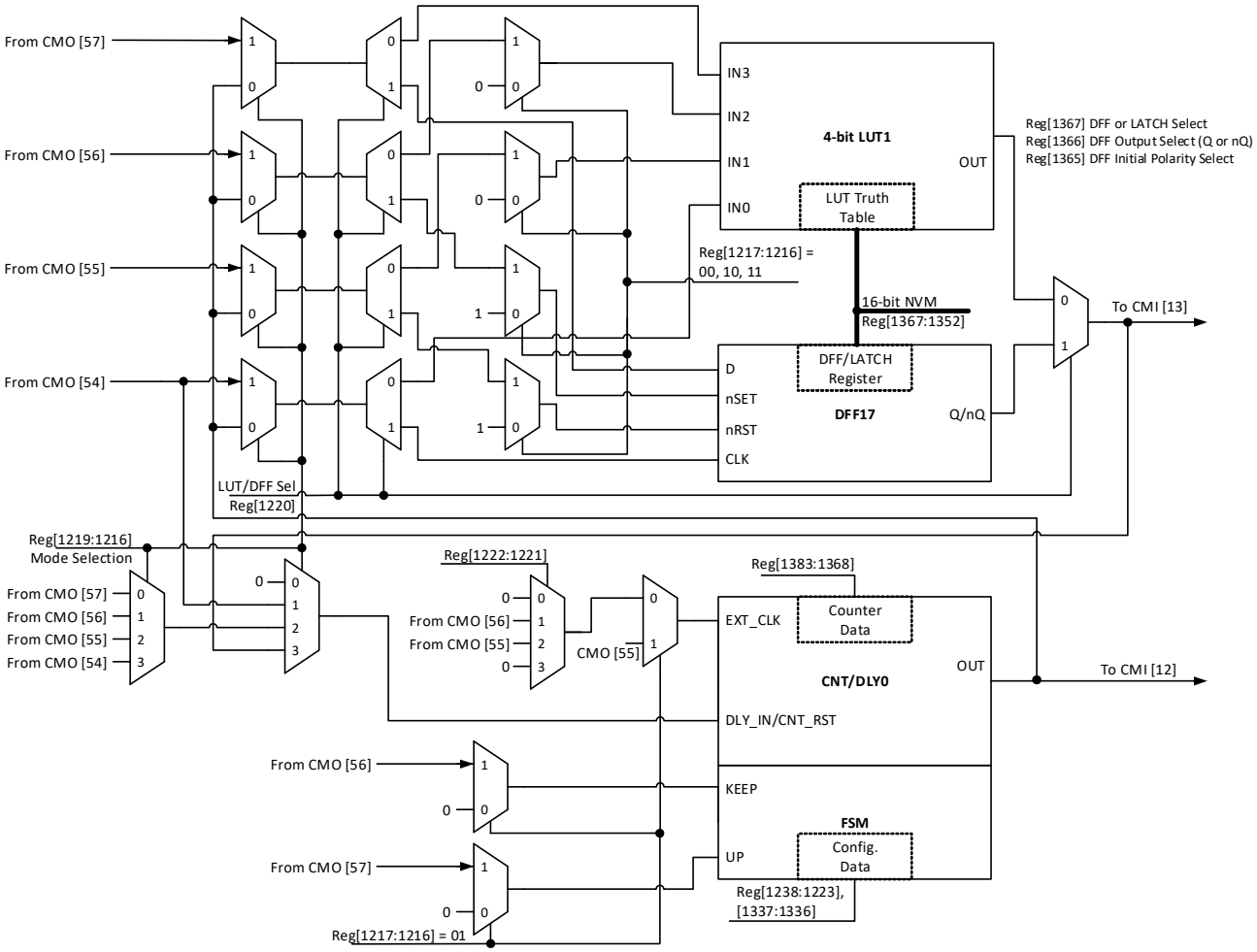


Figure 39. 4-bit LUT1 or CNT/DLY0

8.2.2 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 4-Bit LUTs

Table 30. 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	reg [1352]	LSB
0	0	0	1	reg [1353]	
0	0	1	0	reg [1354]	
0	0	1	1	reg [1355]	
0	1	0	0	reg [1356]	
0	1	0	1	reg [1357]	
0	1	1	0	reg [1358]	
0	1	1	1	reg [1359]	
1	0	0	0	reg [1360]	
1	0	0	1	reg [1361]	
1	0	1	0	reg [1362]	
1	0	1	1	reg [1363]	
1	1	0	0	reg [1364]	
1	1	0	1	reg [1365]	
1	1	1	0	reg [1366]	
1	1	1	1	reg [1367]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

- 4-bit LUT1 is defined by registers [1367:1352]

Table 31. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	1

8.3 CNT/DLY/FSM Timing Diagrams

8.3.1 Delay Mode CNT/DLY0 to CNT/DLY6

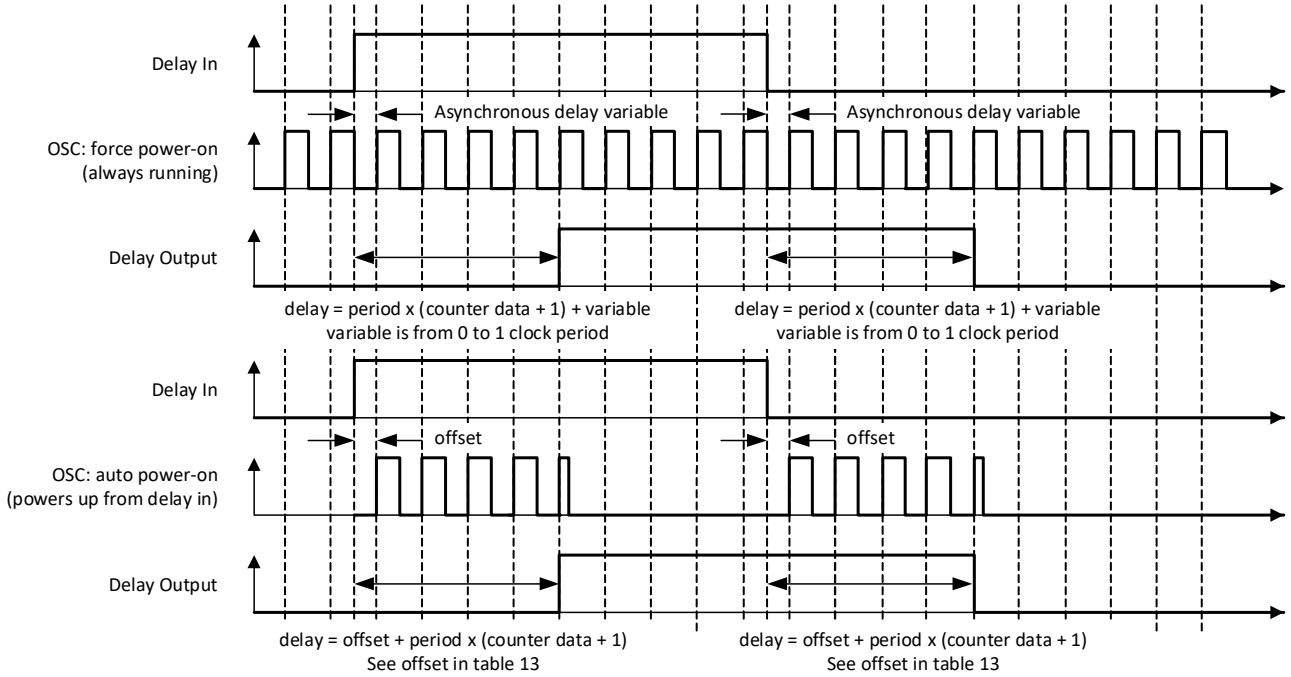


Figure 40. Delay Mode Timing Diagram, Edge Select: Both, Counter Data: 3

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

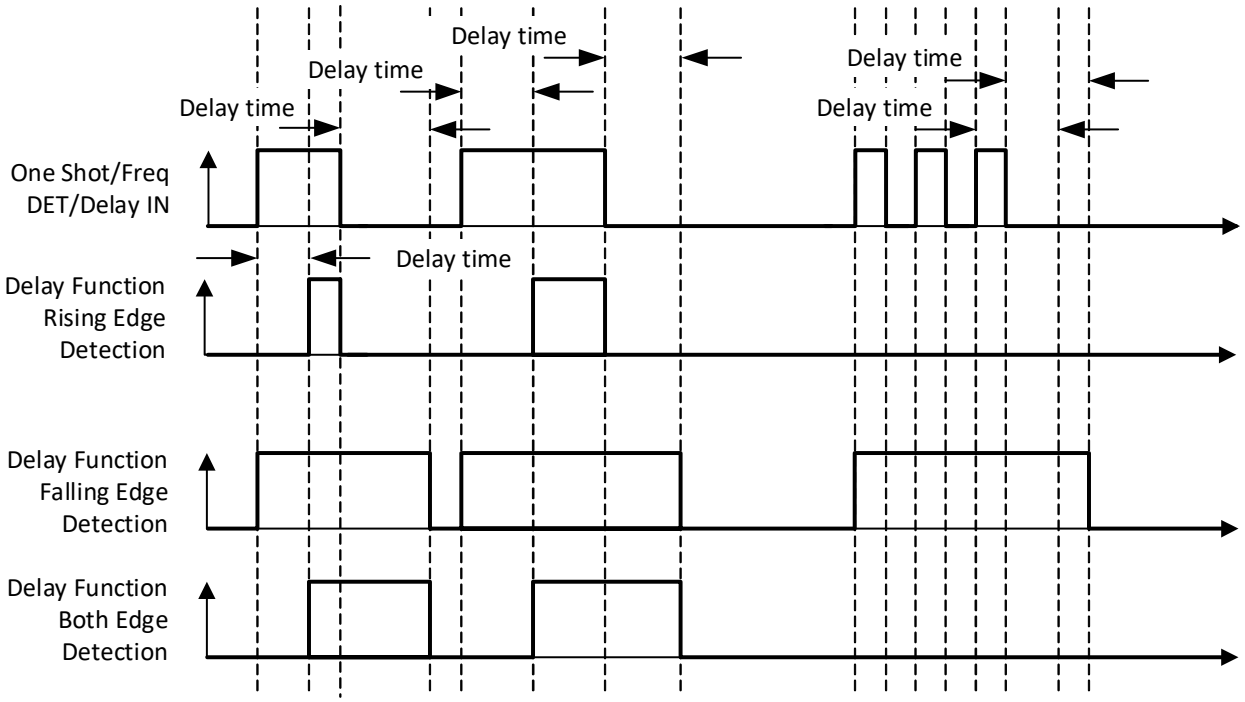


Figure 41. Delay Mode Timing Diagram for Different Edge Select Modes

8.3.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY0 to CNT/DLY6

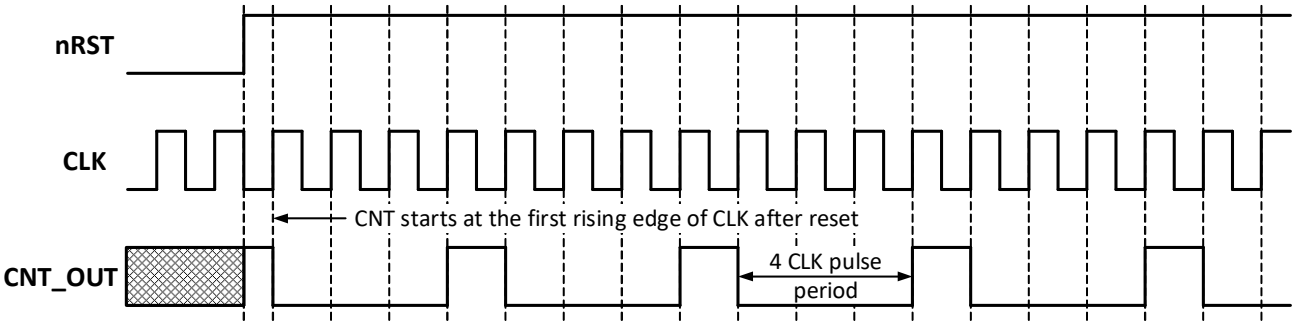


Figure 42. Counter Mode Timing Diagram without Two DFFs Synced Up

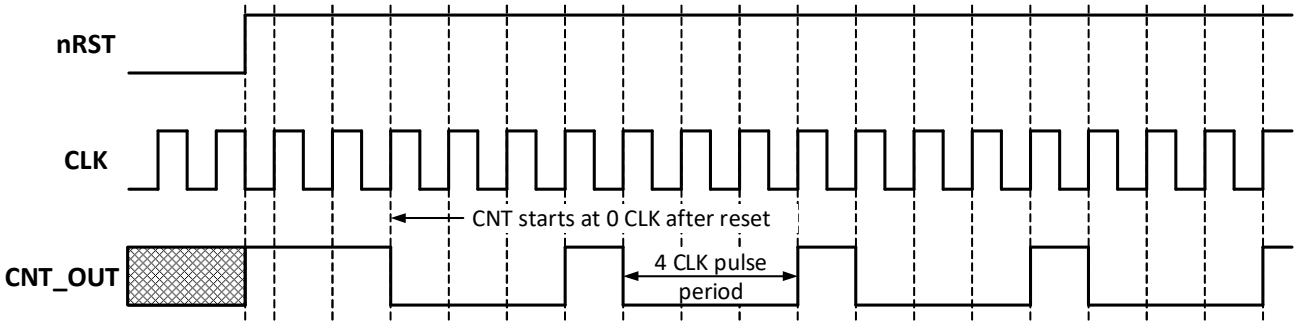


Figure 43. Counter Mode Timing Diagram with Two DFFs Synced Up

8.3.3 One-Shot Mode CNT/DLY0 to CNT/DLY6

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width is determined by counter data and clock selection properties.

The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

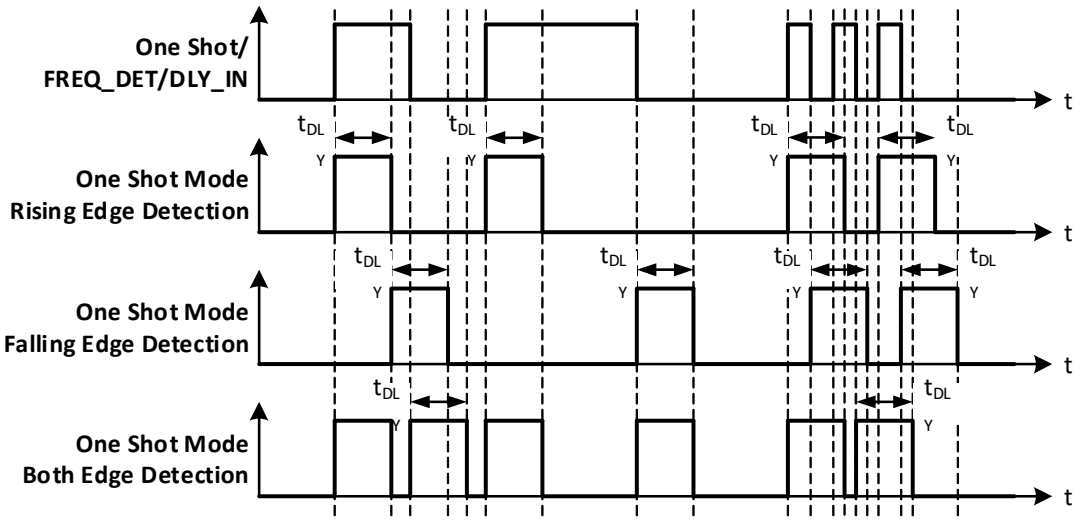


Figure 44. One-Shot Function Timing Diagram

This macrocell generates a high-level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is HIGH.

8.3.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY6

Rising Edge: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

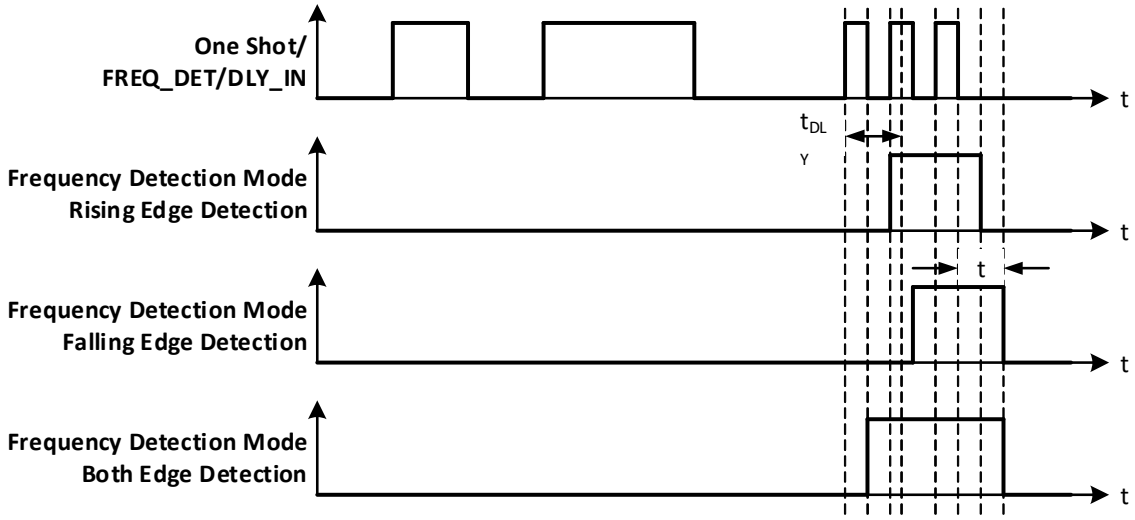


Figure 45. Frequency Detection Mode Timing Diagram

8.3.5 Edge Detection Mode CNT/DLY1 to CNT/DLY6

The macrocell generates high-level short pulse when detecting the respective edge. See section 3.7.1 Typical Delay Estimated for Each Macrocell.

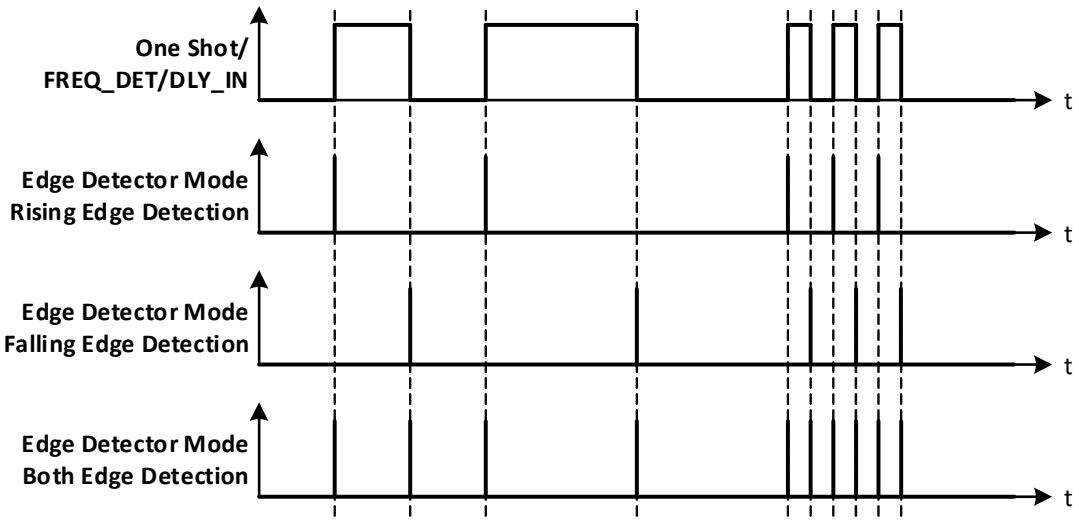


Figure 46. Edge Detection Mode Timing Diagram

8.3.6 Delayed Edge Detection Mode CNT/DLY0 to CNT/DLY6

In Delayed Edge Detection Mode, High-level short pulses are generated on the macrocell output after the configured delay time, if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated.

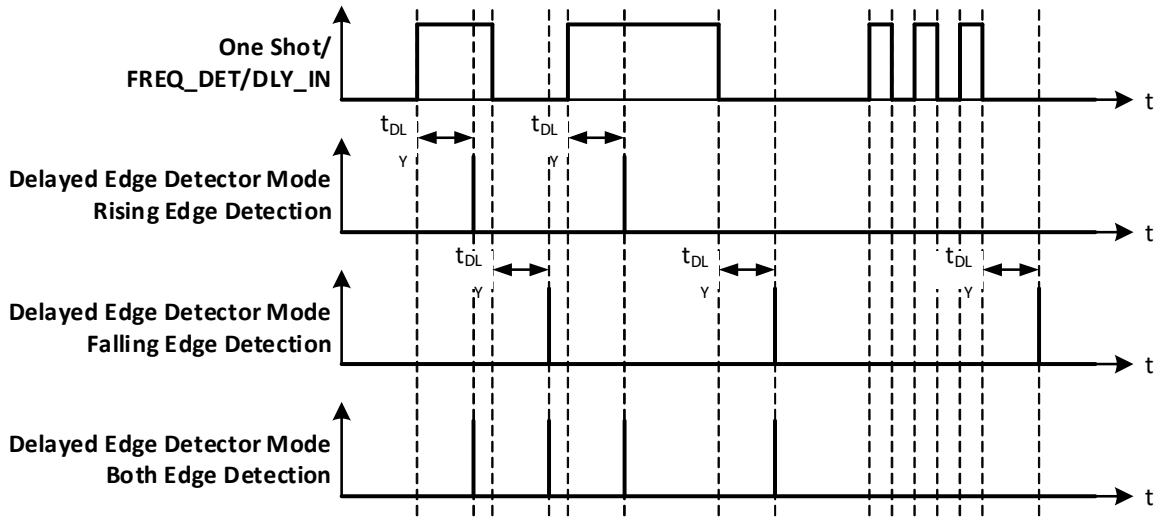
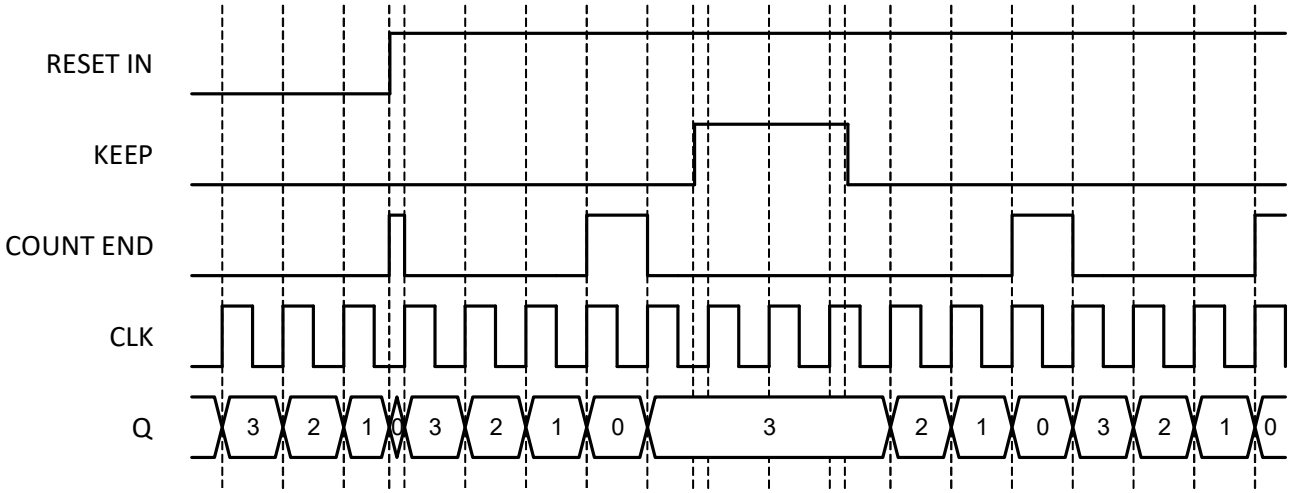


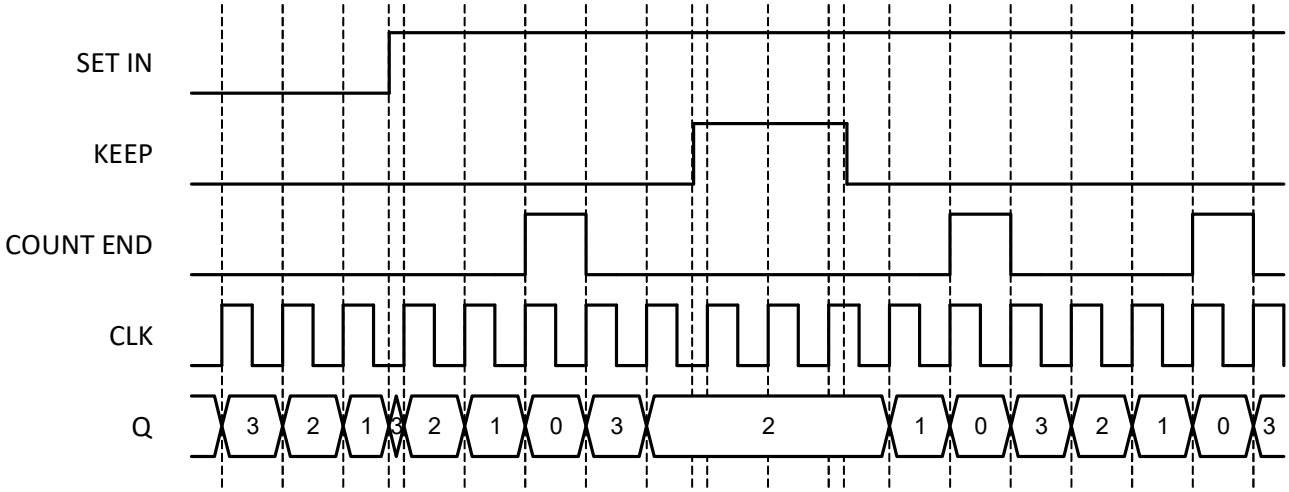
Figure 47. Delayed Edge Detection Mode Timing Diagram

8.3.7 CNT/FSM Mode CNT/DLY0



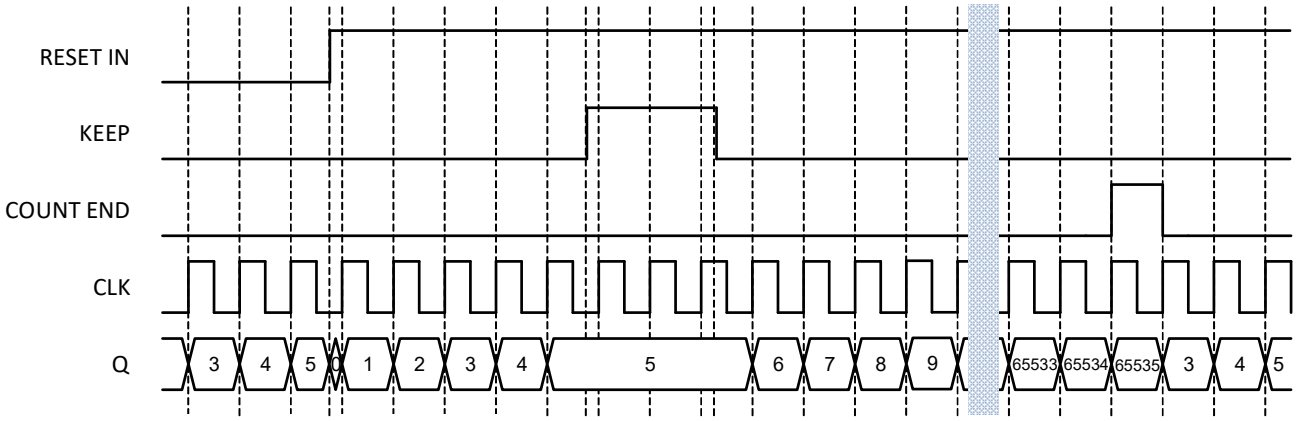
Note 1: CNT Data = 3.
Note 2: Q = current counter value.

Figure 48. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 0)



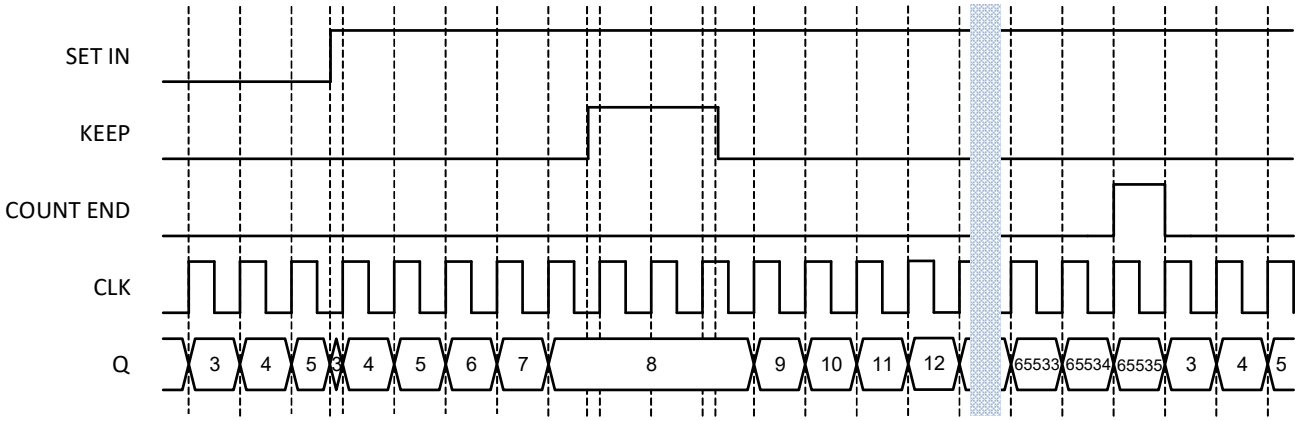
Note 1: CNT Data = 3.
Note 2: Q = current counter value.

Figure 49. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 0)



Note 1: CNT Data = 3.
Note 2: Q = current counter value.

Figure 50. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 1)



Note 1: CNT Data = 3.
Note 2: Q = current counter value.

Figure 51. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 1)

8.3.8 Difference in Counter Value for Counter, Delay, One-Shot, and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. Compared to Counter mode, in Delay/One-Shot/Frequency Detect modes the counter value is shifted for two rising edges of the clock signal, see Figure 52.

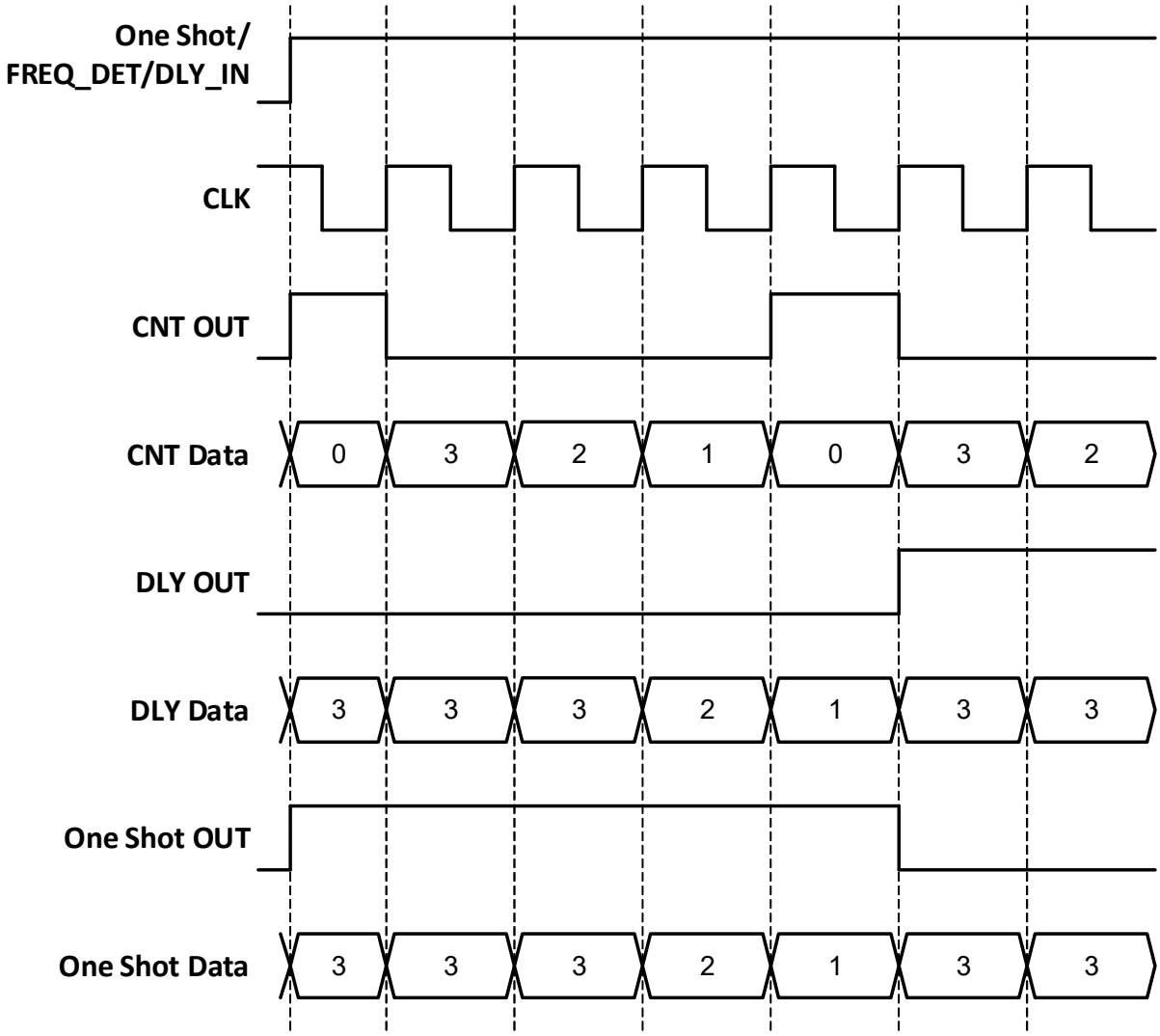


Figure 52. Counter Value, Counter Data = 3

8.4 Wake and Sleep Controller

The SLG47004 has a Wake and Sleep (WS) function for ACMP. The macrocell CNT/DLY0 can be reconfigured for this purpose registers [1224:1223] = 11 and reg [1232] = 1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

Note 1: BG/Analog_Good time is long and should be considered in the wake and sleep timing in case it dynamically powers on/off.
Note 2: Wake time should be long enough to make sure ACMP and V_{REF} have enough time to get a sample before going to sleep.
Note 3: ACMPs power up must be connected to POR.

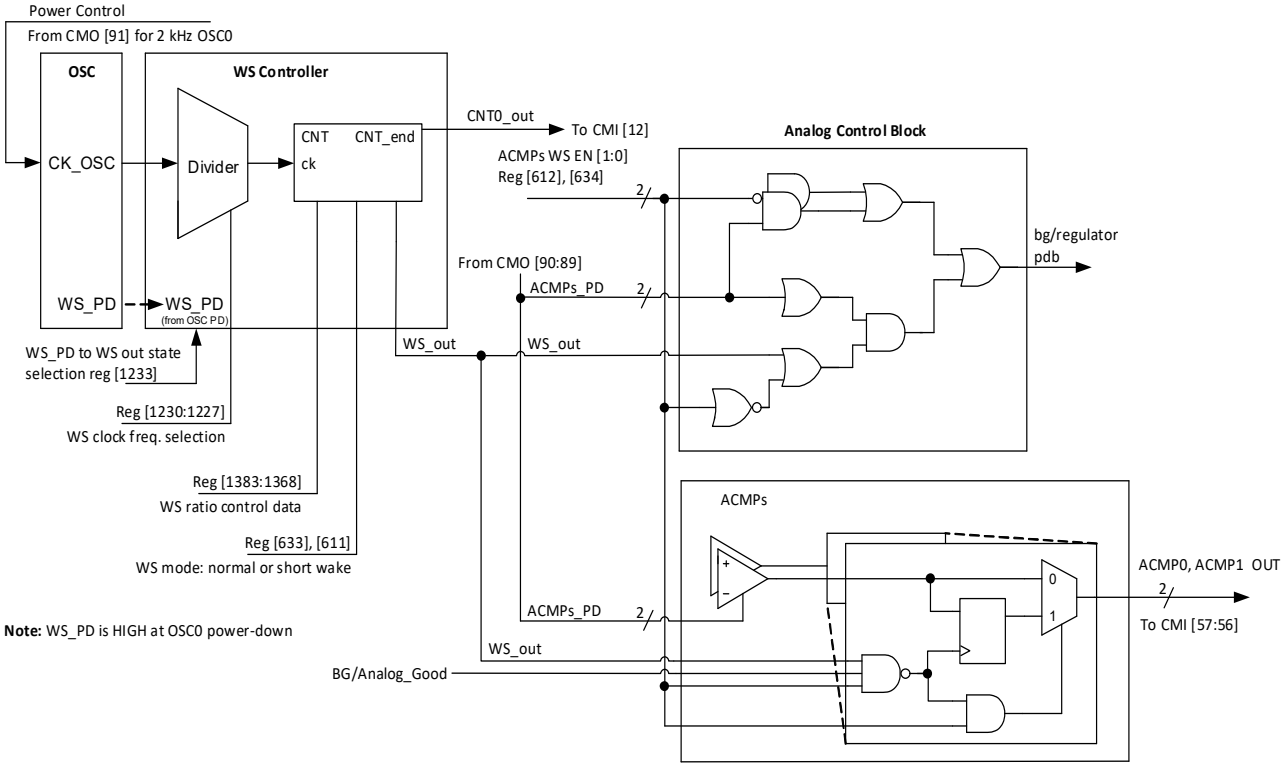
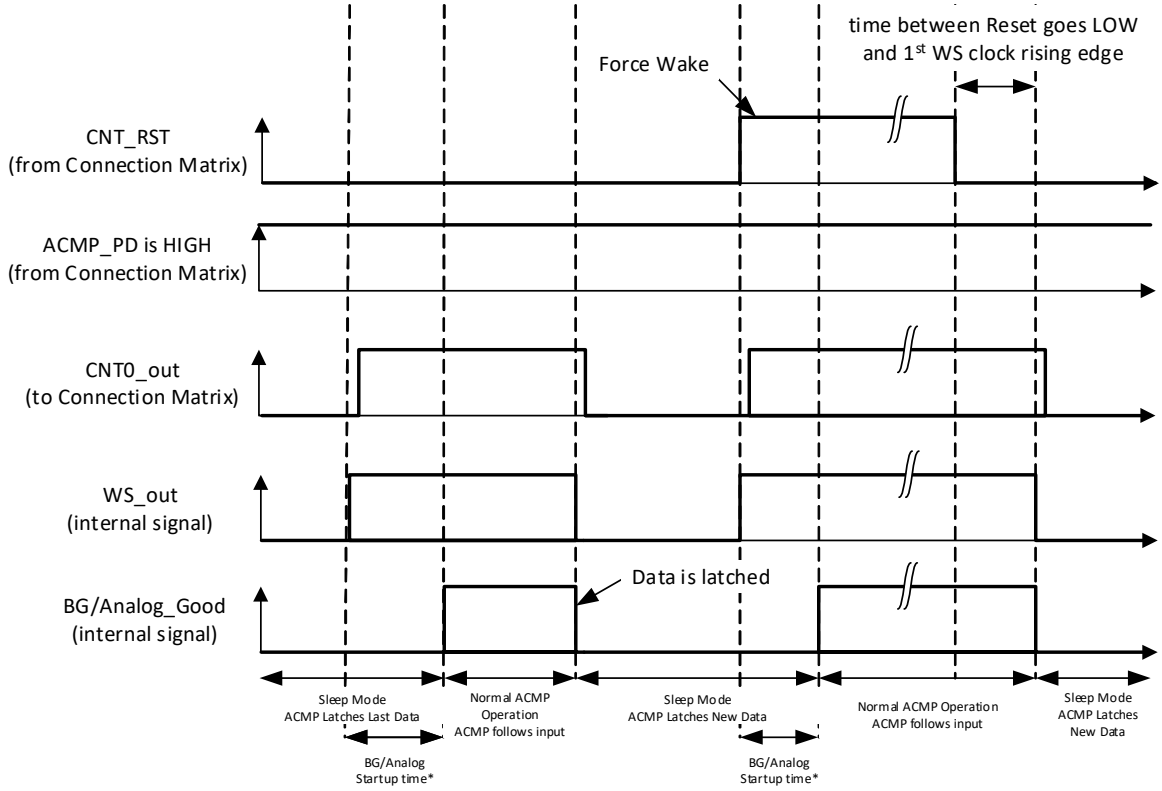
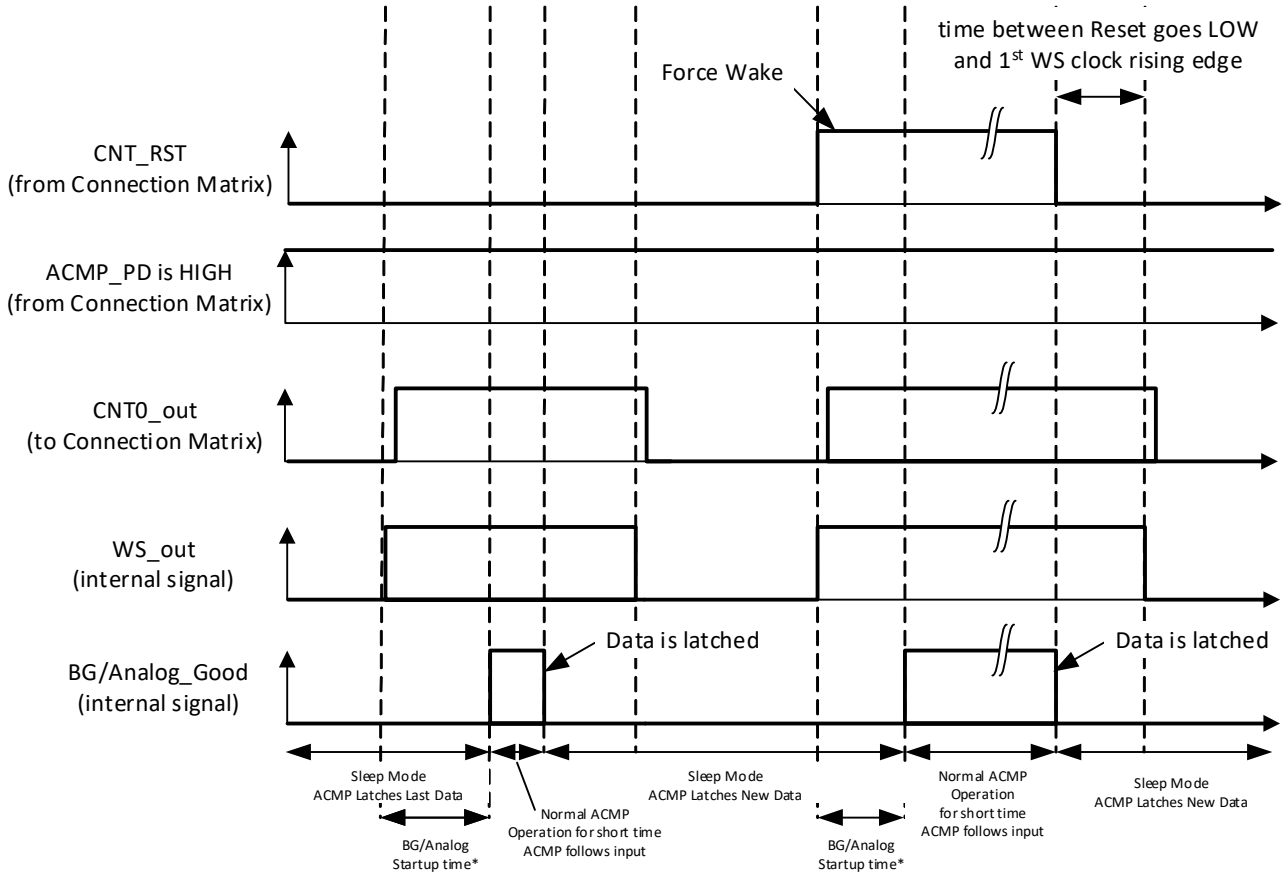


Figure 53. Wake and Sleep Controller



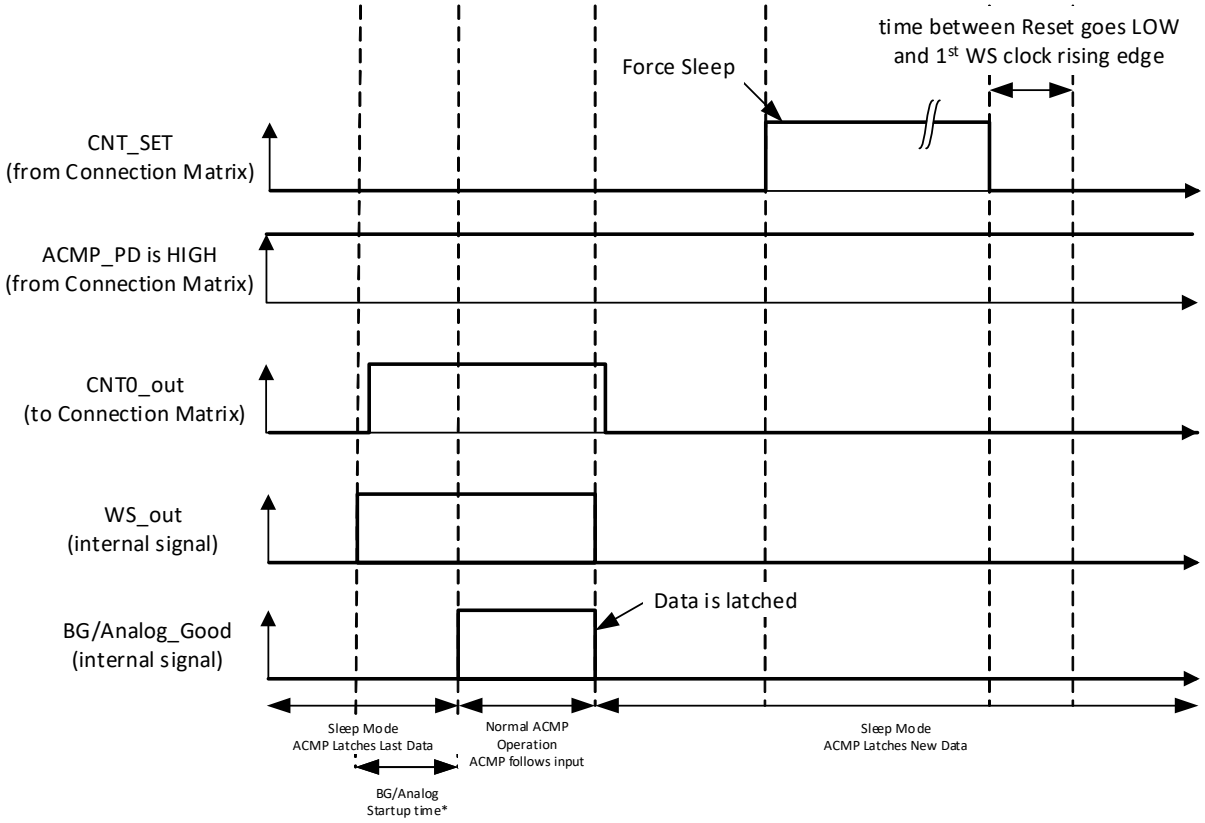
Note: CNT0_out is a delayed WS_out signal for 1 us to make sure the data is correct during LATCH.

Figure 54. Wake and Sleep Timing Diagram, Normal Wake Mode, Counter Reset is Used



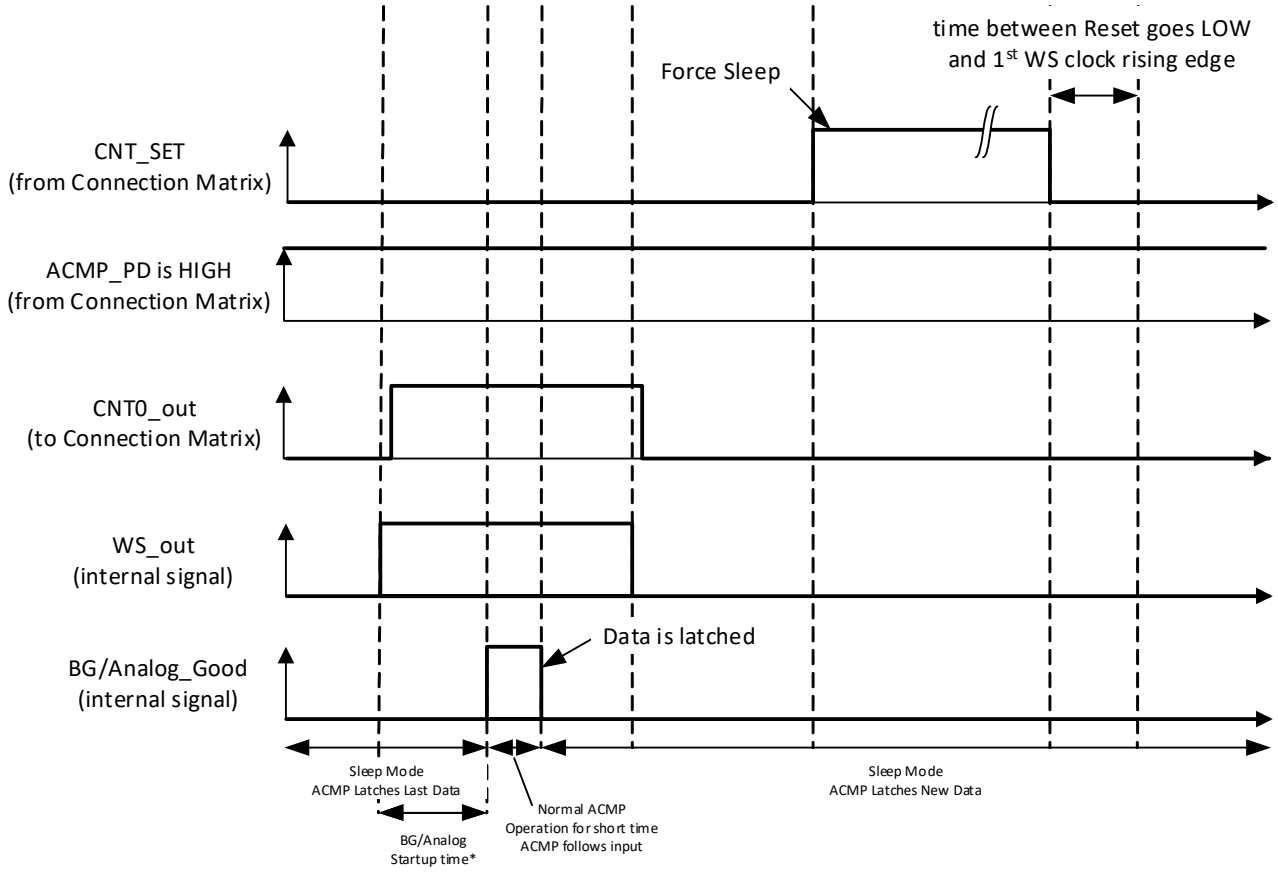
Note: CNT0_out is a delayed WS_out signal for 1 us to make sure the data is correct during LATCH.

Figure 55. Wake and Sleep Timing Diagram, Short Wake Mode, Counter Reset is Used



Note: CNT0_out is a delayed WS_out signal for 1 us to make sure the data is correct during LATCH.

Figure 56. Wake and Sleep Timing Diagram, Normal Wake Mode, Counter Set is Used



Note: CNT0_out is a delayed WS_out signal for 1 us to make sure the data is correct during LATCH.

Figure 57. Wake and Sleep Timing Diagram, Short Wake Mode, Counter Set is Used

Note: If low power BG is powered on/off by WS, the wake time should be longer than 2.1 ms. The BG/analog start up time will take maximal 2 ms. If low power BG is always on, OSC0 period is longer than required wake time. The short wake mode can be used to reduce the current consumption. The short wake mode is edge triggered, when the wake signal is latched by rising edge and released the Power-On signal after the ACMP output data is latched. This allows to have a valid ACMP data for any type of wake signal and have the optimized current consumption.

To use any ACMP under WS controller, the following settings must be done:

- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMPs)
- Register WS → enable (for each ACMP separately)
- CNT/DLY0 set/reset input = 0 (for all ACMPs).

As the OSC any oscillator with any pre-divider can be used. The user can select a period of time while the ACMP is sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep their outputs are latched, so the ACMPs remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low).

  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on.

  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off.

  Both cases WS function is turned off.

- Counter Data (Range: 1 - 65535).

  The user can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn on the ACMPs. When Reset signal goes out, the WS counter will go Low and turn off the ACMPs until the counter counts up to the end. Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn off the ACMPs. When Set signal goes out, the WS counter will go on counting and High level signal will turn on the ACMPs while counter is counting up to the end.

Note: The OSC0 matrix power down to control ACMP WS is not supported for short wait time option.

- Edge Select defines the edge for Q mode.

  High level Set/Reset - switches mode Set/Reset when level is High.

Note: Q mode operates only in case of “High Level Set/Reset”.

- Wake time selection - time required for wake signal to turn the ACMPxH on.

  Normal Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP.

  Short Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on for 1 µs and turn off regardless of WS signal. The WS signal width does not matter.

- Keep - pauses counting while Keep = 1.
- Up - reverses counting.

  If Up = 1, CNT is counting up from user-selected value to 65535.

  If Up = 0, CNT is counting down from user-selected value to 1.

9. Analog Comparators

There are two Low Power Rail-to-Rail General Purpose Analog Comparator (ACMP) macrocells in the SLG47004. For the ACMP macrocells to be used in a GreenPAK design, the power-up signals (ACMP0L_pdb and ACMP1L_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be ON continuously, OFF continuously, or switched on periodically, based on a digital signal coming from the Connection Matrix. When ACMP is powered down, its output is low. Two General Purpose Analog Comparators are optimized for low power operation.

Each of the General Purpose ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage (1x, 0.5x, 0.33x, 0.25x) before connection to the analog comparator. The gain divider is unbuffered and has an input resistance of 2 MΩ (typ.) for 0.5x, 0.33x, 0.25x, and 10 GΩ for 1x. Each of the General Purpose ACMP macrocells has a negative input signal that is either created from an internal V_{REF} or provided by any external source (from external pins). Note that the external V_{REF} signal is filtered with a 2nd order low pass filter with 8 kHz typical bandwidth, see in Figure 58 and Figure 59.

Input bias current < 1 nA (typ.).

Power-Up = 1 → ACMP is powered up.

Power-Up = 0 → ACMP is powered down.

Both General Purpose Analog Comparators have "Low Energy Power Up" setting (reg [608] - ACMP0, reg [630] - ACMP1). When enabled, it allows reducing average power consumption during ACMP power up process. This setting changes power up sequence of analog macrocells:

- Low Energy Power Up reg [608], reg [630] = 0 - all analog macrocells associated with ACMP turns on simultaneously.
- Low Energy Power Up reg [608], reg [630] = 1 - the first macrocell that begins to turn on is Bandgap. Other analog macrocells begin to turn on only after BG_OK signal is valid. This option slightly increases general ACMP Power-On time, while reducing the average current consumption.

During power-up, the ACMP output will remain LOW, and then becomes valid after power up signal goes high for ACMP0L and ACMP1L (see parameter t_{start} in section 3.9 ACMP Specifications).

Each cell also has a flexible hysteresis selection, to offer hysteresis of 32 steps, but not more than V_{REF} voltage. It means that there are 6-bits to select V_{REF} and independent 6-bits to select the hysteresis (no need to have an adder logic).

It's possible to enable low pass filter at the V_{REF} input. But it's highly recommended to enable this LPF only when hysteresis Vhys > 196 mV.

ACMP0L IN+ options are OA0_out, GPIOx (PIN), V_{DD}.

ACMP1L IN+ options are OA1, GPIOx (PIN), ACMP0L_IN+, Temp Sensor OUT.

9.1 ACMP0L Block Diagram

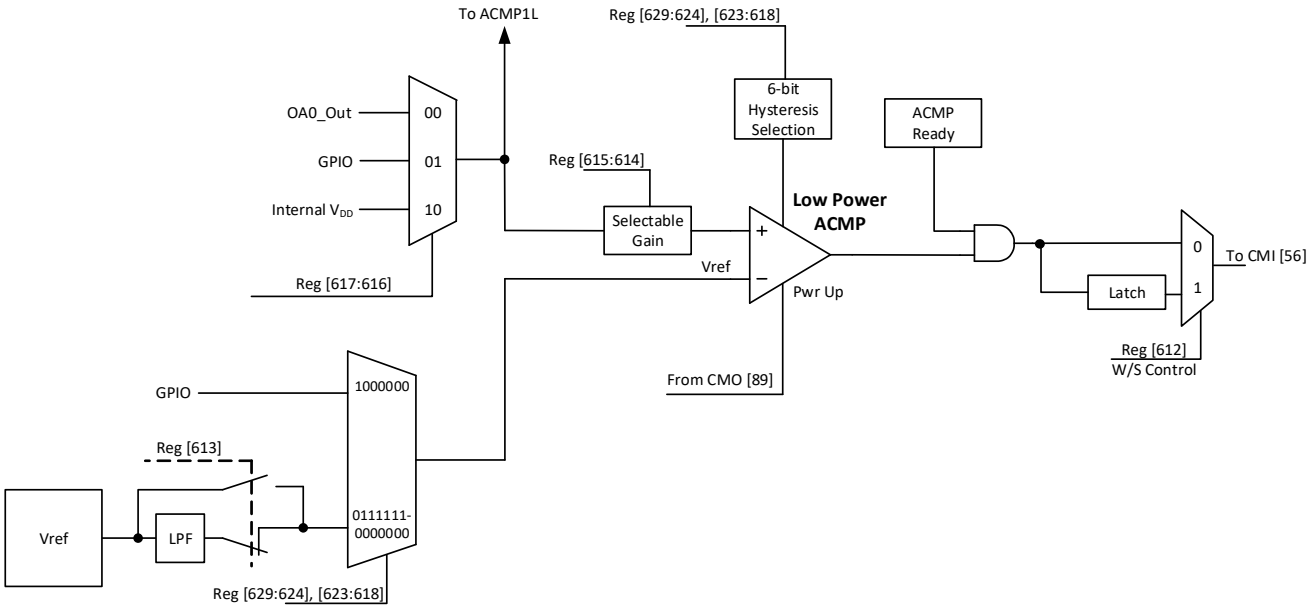


Figure 58. ACMP0L Block Diagram

9.2 ACMP1L Block Diagram

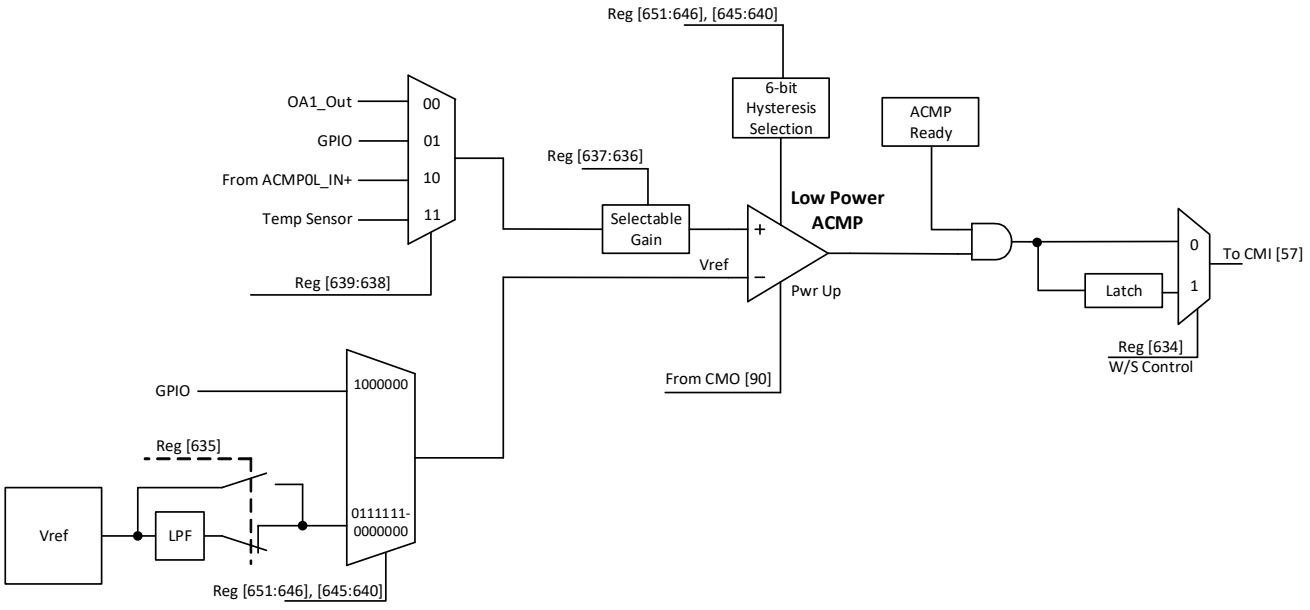


Figure 59. ACMP1L Block Diagram

9.3 Chopper Analog Comparator

There is one Chopper Rail-to-Rail Analog Comparator (ACMP) macrocells in the SLG47004. It is possible to use Chopper ACMP to do in system trim by changing the Rheostat resistance in Auto-Trim mode. It is also possible to use a Chopper ACMP as a general purpose analog comparator.

The chopper ACMP power up signal is controlled either by internal Auto-Trim logic (Set 0/1 of Digital Rheostat 0/1) or by matrix input.

The chopper ACMP is automatically powered on during the calibration time to control the up/down signal of the counter/rheostat, when the Auto-Trim is enabled (reg [909]= 0).

In order to use Chopper ACMP as a standalone comparator (Auto-Trim mode is disabled, reg [909] = 1) user should provide the clock signal to this macrocell. Clock source can be internal oscillators or any pulses from the connection matrix.

Note that clock frequency for the Chopper ACMP shouldn't be greater than f_{ChACMP}. Please refer to section 3.15 100K Digital Rheostat Specifications.

For proper Chopper ACMP operation it is recommended to force the bandgap on. It's highly recommended to force the bandgap on when OSC1 is used as a clock source for Chopper ACMP. Also, if V_{REF} (bandgap) is used in the project, internal V_{REF} should be stable before the 2nd rising edge of Chopper ACMP clock signal (see Figure 60). Please consider the bandgap turn on delay (approximately 1 ms).

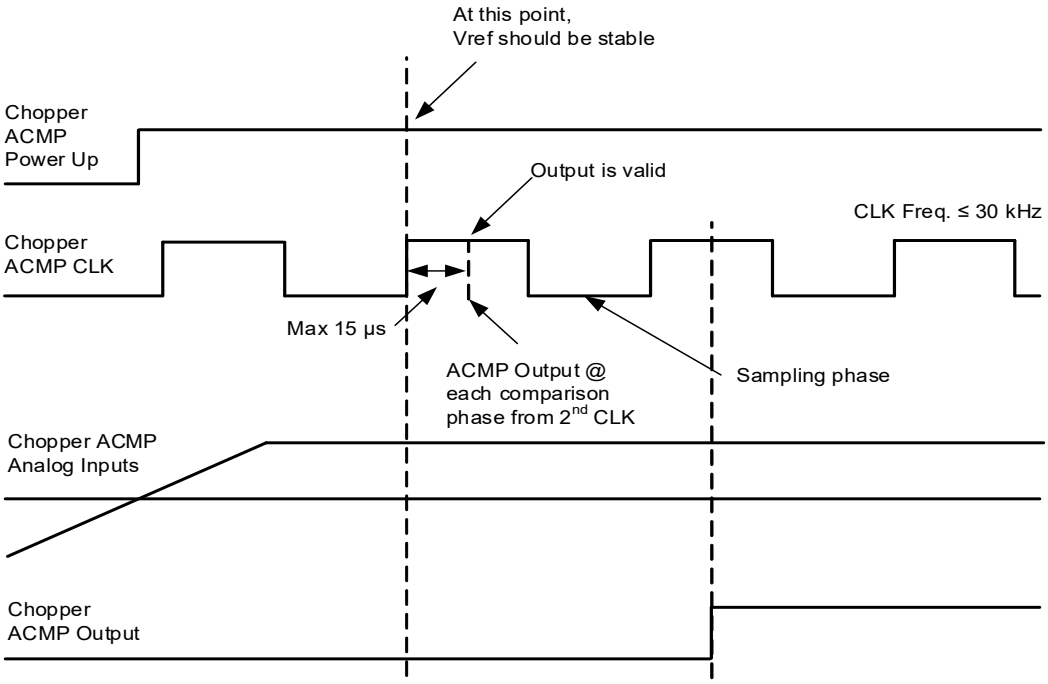


Figure 60. Chopper ACMP CLK Correct Operation. Bandgap Forced On

Output of Chopper ACMP can be optionally inverted by reg [882].

The matrix output [85] is used to control chopper ACMP power up signal for the general purpose usage, see Figure 61. It is possible to use the chopper ACMP as a general purpose ACMP after Auto-Trim procedure is completed, since the power up signal is a logic OR of the latched Set (Digital Rheostat 0/1) signal and matrix signal. If Auto-Trim (Set 0/1 of Digital Rheostat 0/1) is disabled and chopper ACMP channel is set to Auto (Channel 0/1), then ACMP output defaults to Channel 0 while Channel 1 is ignored.

The power-up signals need to be active high in order to use the Chopper ACMP. By connecting to signals coming from the Connection Matrix, it is possible to have ACMP be ON continuously, OFF continuously, or switched on

periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, its output is low.

There are no Gain and Hysteresis selection for chopper ACMP compared to the ACMP0L and ACMP1L.

It's possible to select different reference sources for Chopper ACMP:

- external voltage from pin
- divided internal voltage from internal reference source (from 32 mV to 2048 mV)
- divided internal reference voltage from HD Buffer (64 steps)
- divided V_{DDA} voltage (64 steps).

For more information see section 15. Voltage Reference.

The positive input of the Chopper ACMP can be connected to the Op Amp0 out or Op Amp1 out or In Amp out, or to the external PIN.

The inputs of Chopper ACMP can be reconfigured while operating in AutoTrim mode. There is one configuration of inputs (Figure 61) for case when Set0 (Digital Rheostat 0) signal is latched, and another configuration of Chopper ACMP inputs when Set1 (Digital Rheostat 1) signal is latched. For example, M1 MUX can be configured to operate with In Amp out when Set0 (Digital Rheostat 0) is latched and Chopper_ACMP+ pin when Set1 (Digital Rheostat 1) is latched. The same way, “-” input of Chopper ACMP can be configured to work with any of possible inputs when Set0 (Digital Rheostat 0) or Set1 (Digital Rheostat 1) are latched.

Note that the default configuration is the configuration for Set0 (Digital Rheostat 0) signal. When Chopper ACMP operates as separate ACMP and AutoTrim function is disabled, inputs of Chopper ACMP are defined by registers [893:892].

Note that Chopper ACMP will automatically enable HD Buffer if HD Buffer is selected as a source for Chopper ACMP In-signal (reg 946 = 0) and Chopper ACMP is powered up.

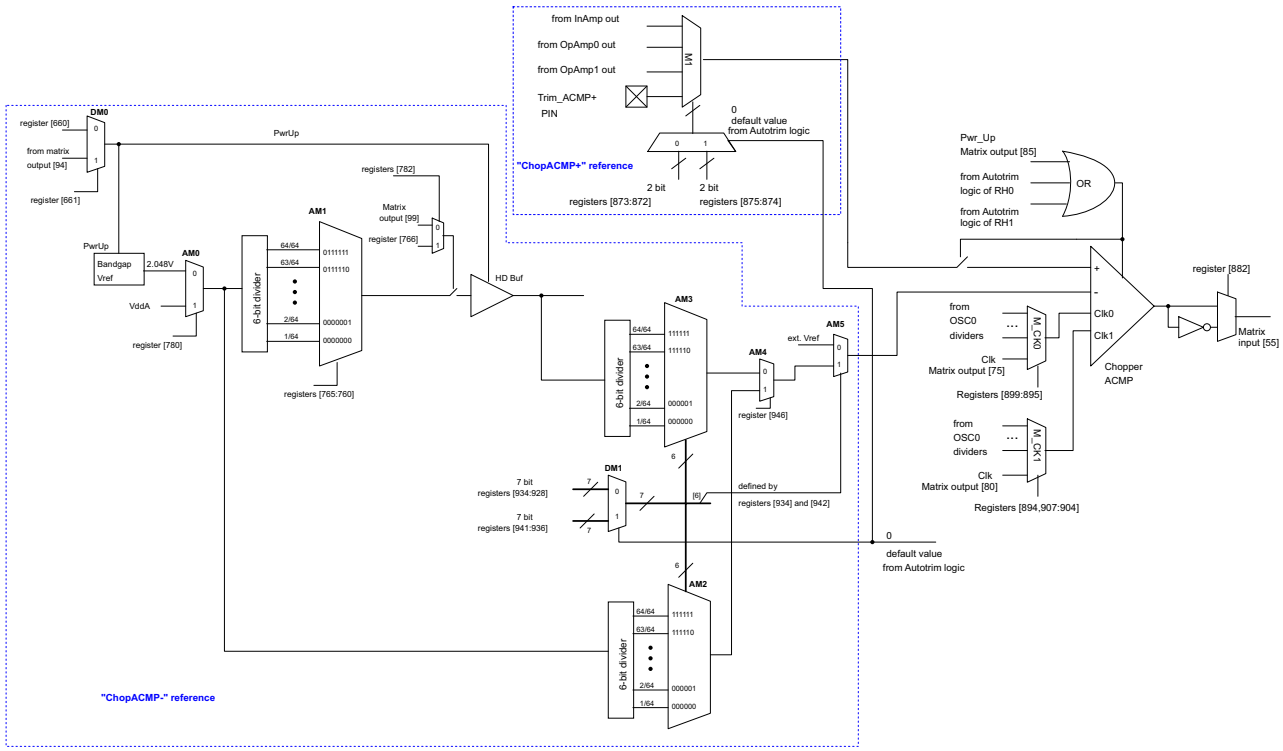


Figure 61. Chopper ACMP Block Diagram

9.4 ACMP Sampling Mode

Both General Purpose Analog Comparators (ACMPL0 and ACMPL1) have an optional sampling mode. In this mode, ACMP is enabled for the shortest amount of time after rising edge at Power Up input to get a valid data. Then ACMP latches its value and goes sleep again.

Registers [610], [632] enable sampling mode for two comparators.

9.5 ACMP Typical Performance

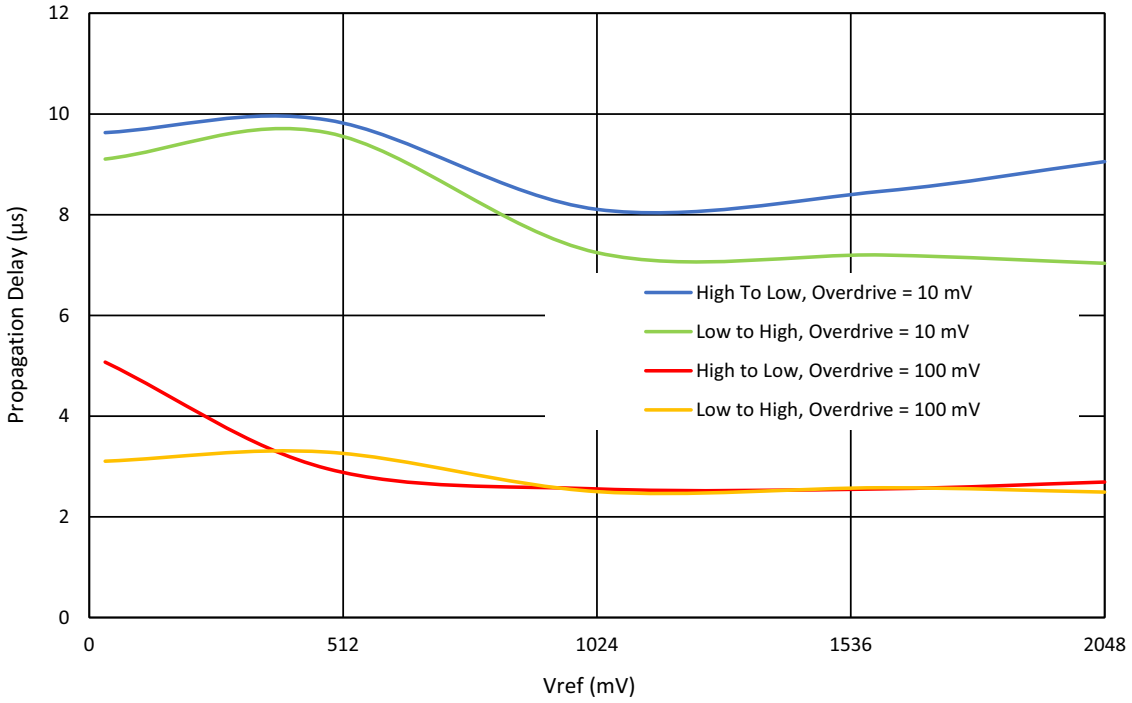


Figure 62. Propagation Delay vs. V_{REF} for ACMPx at T_A = 25 °C, V_{DD} = 2.4 V to 5.5 V, Hysteresis = 0

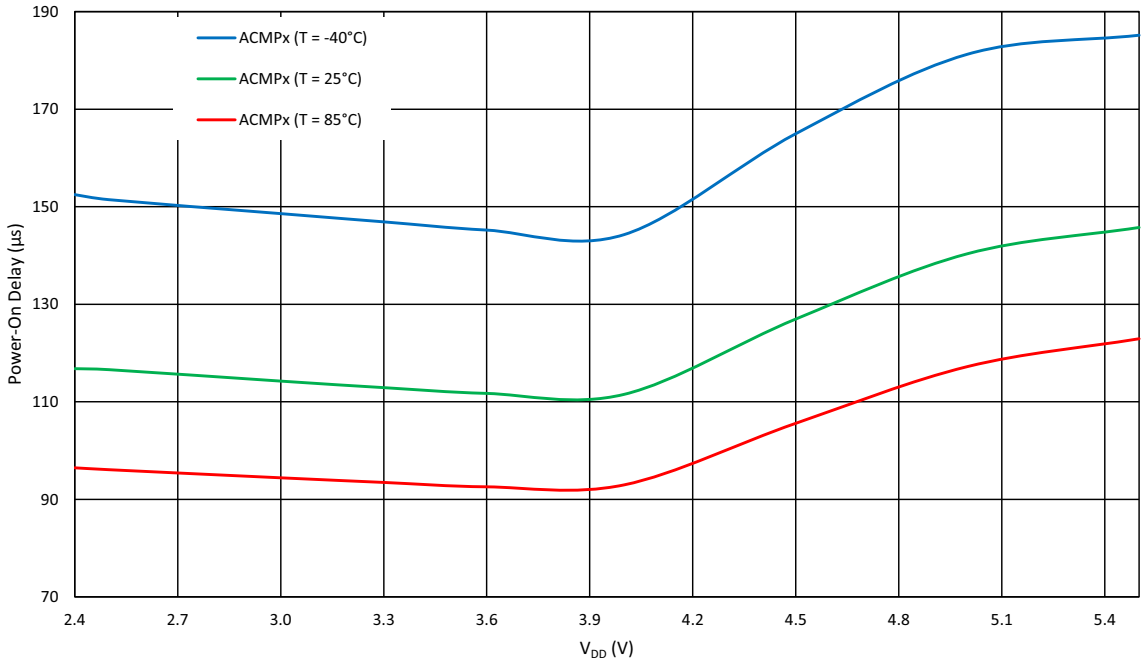


Figure 63. ACMPx Power-On Delay vs. V_{DD} at BG - Forced

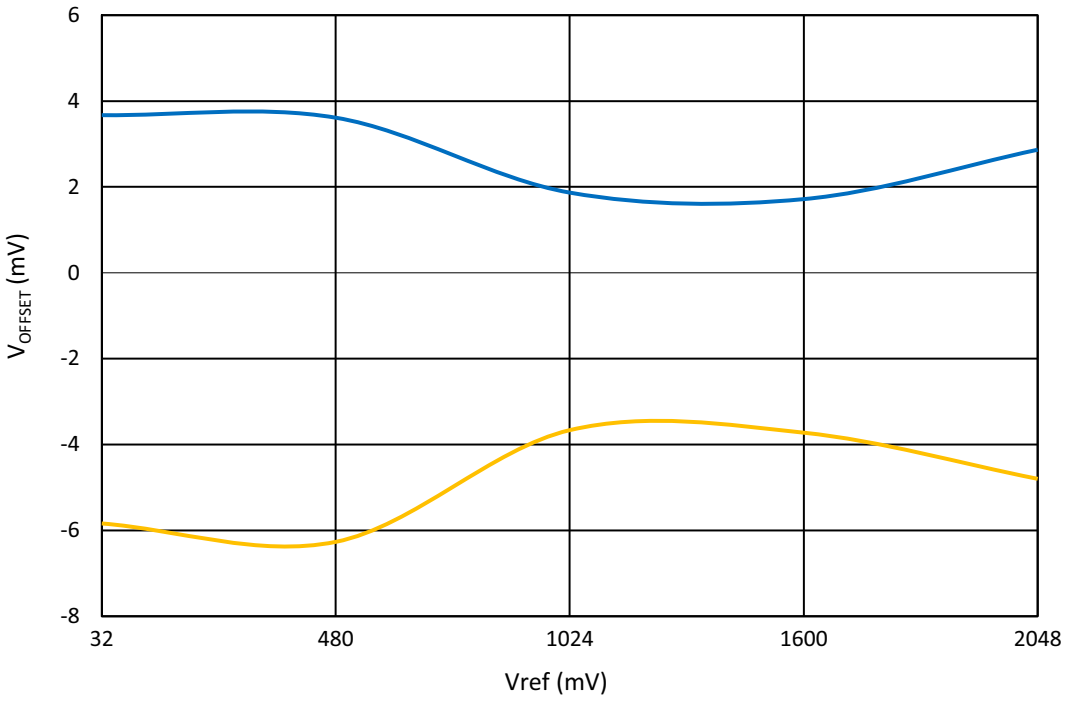


Figure 64. ACMPx Input Offset Voltage vs. V_{REF} at T = -40 °C to 85 °C, V_{DD} = 2.4 V to 5.5 V, Gain = 1

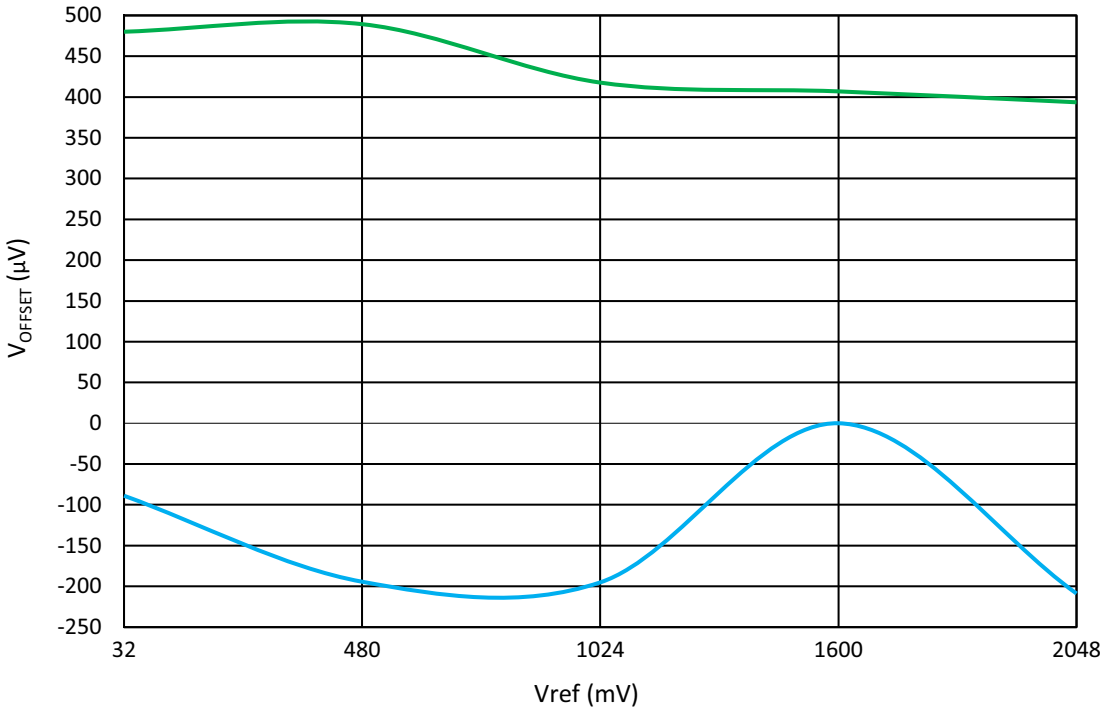


Figure 65. Chopper ACMP Input Offset Voltage vs. V_{REF} at T = -40 °C to 85 °C, V_{DD} = 2.4 V to 5.5 V, Gain = 1

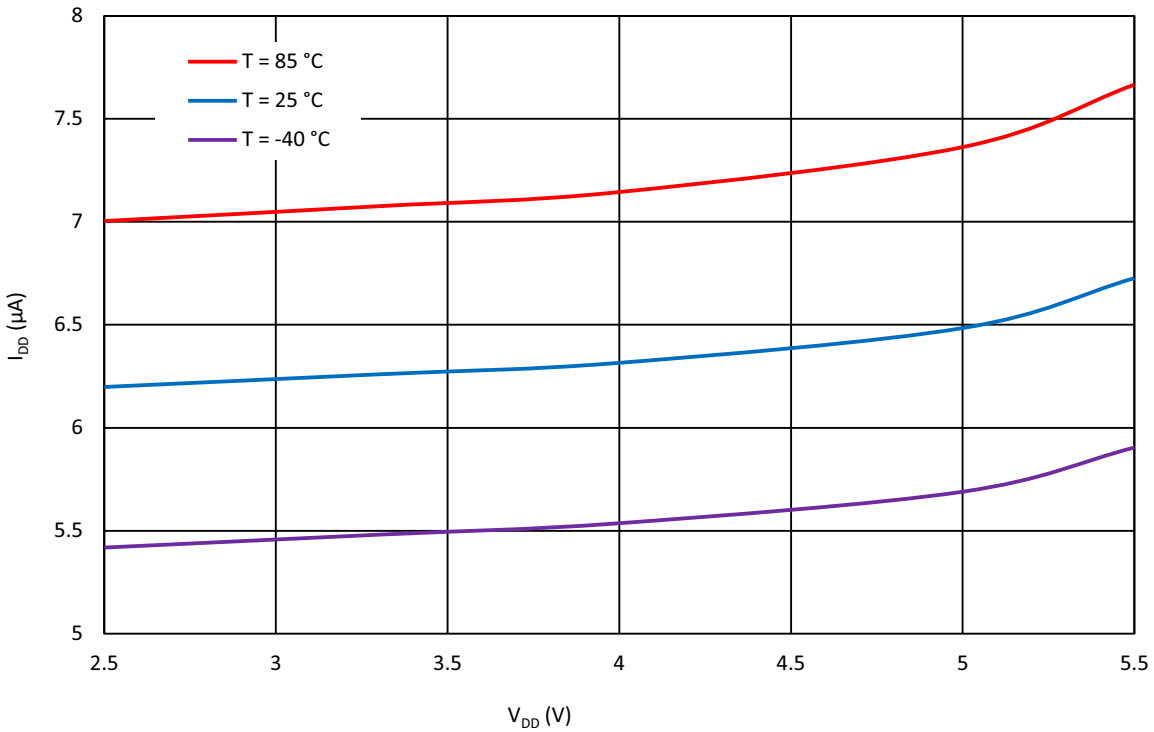


Figure 66. ACMPx Current Consumption vs. V_{DD}

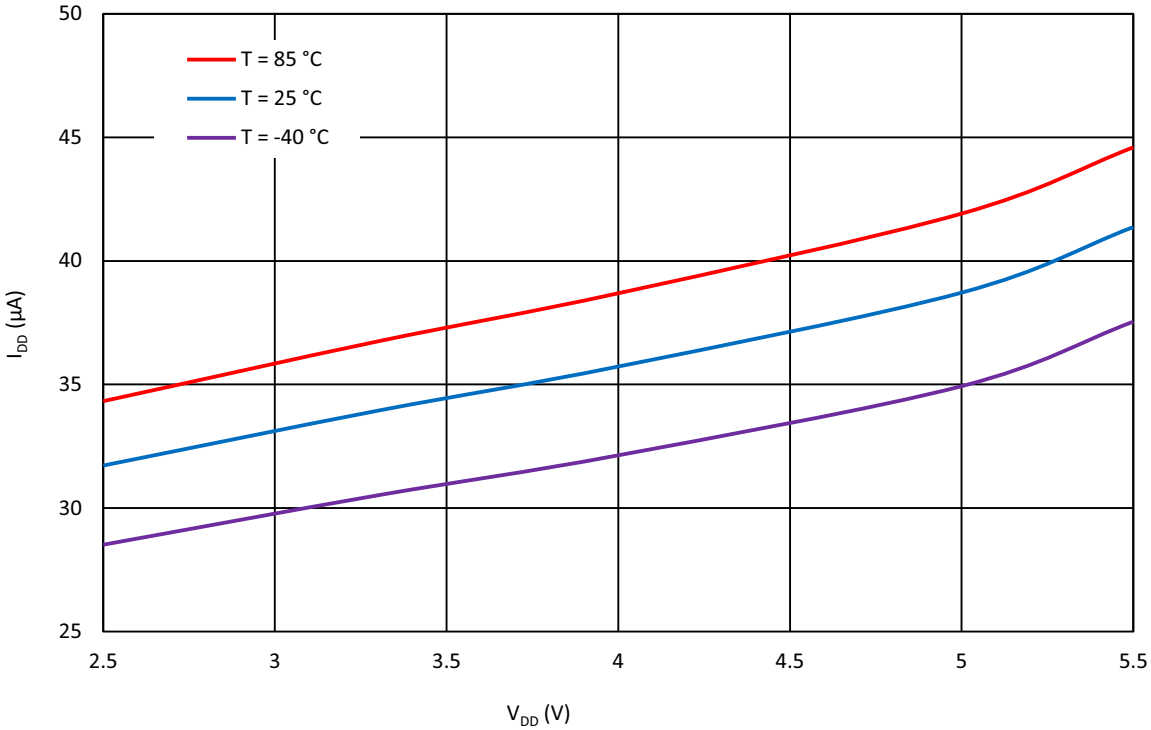


Figure 67. Chopper ACMP Current Consumption vs. V_{DD} (with 2.048 kHz Clock)

10. Programmable Operational Amplifiers

10.1 General Description

The SLG47004 contains three operational amplifiers with rail-to-rail input and output. Two of them (Programmable Op Amps) have the additional functions of driving internal analog FETs (Voltage Regulator and Current Sink modes) and Comparator mode. The third Internal Op Amp is an amplifier with internal resistors, and can be configured as a difference amplifier with Gain = 1. All three Op Amps can function as instrumentation amplifiers. The structures of the Op Amps are shown in Figure 68 and Figure 69.

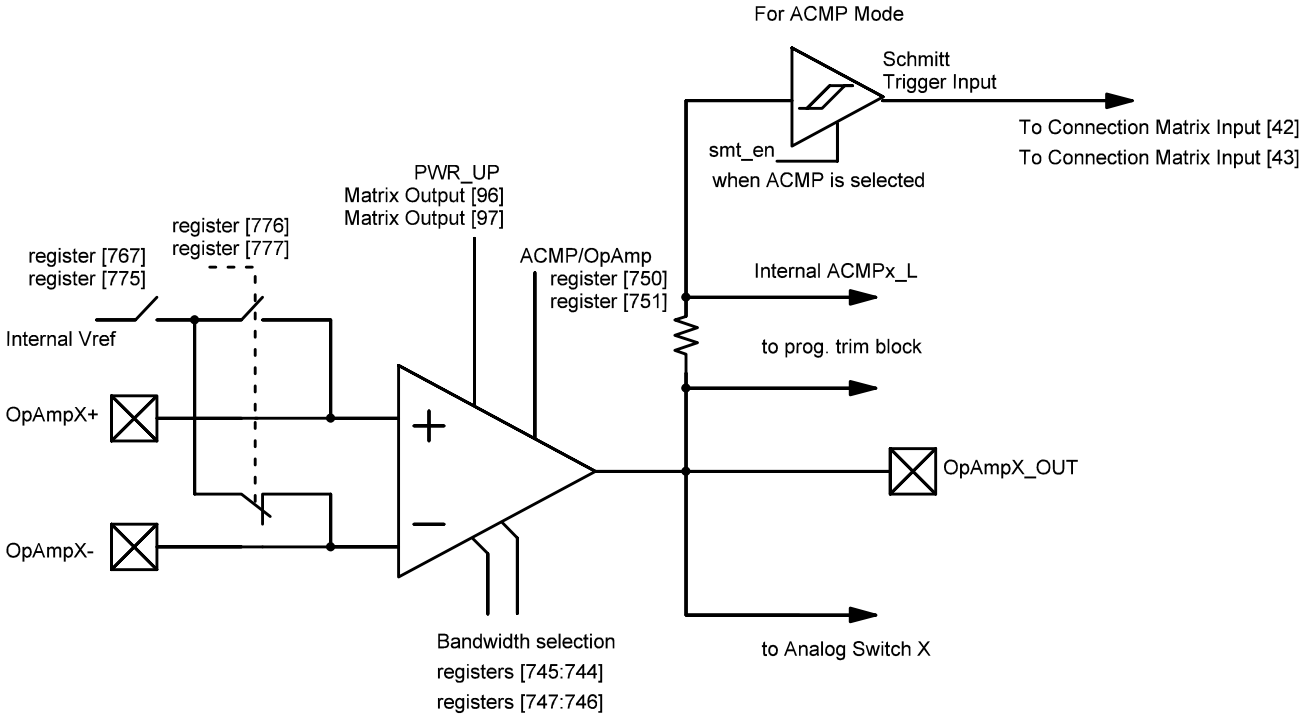


Figure 68. Programmable Operational Amplifier OA0, OA1 Internal Circuit

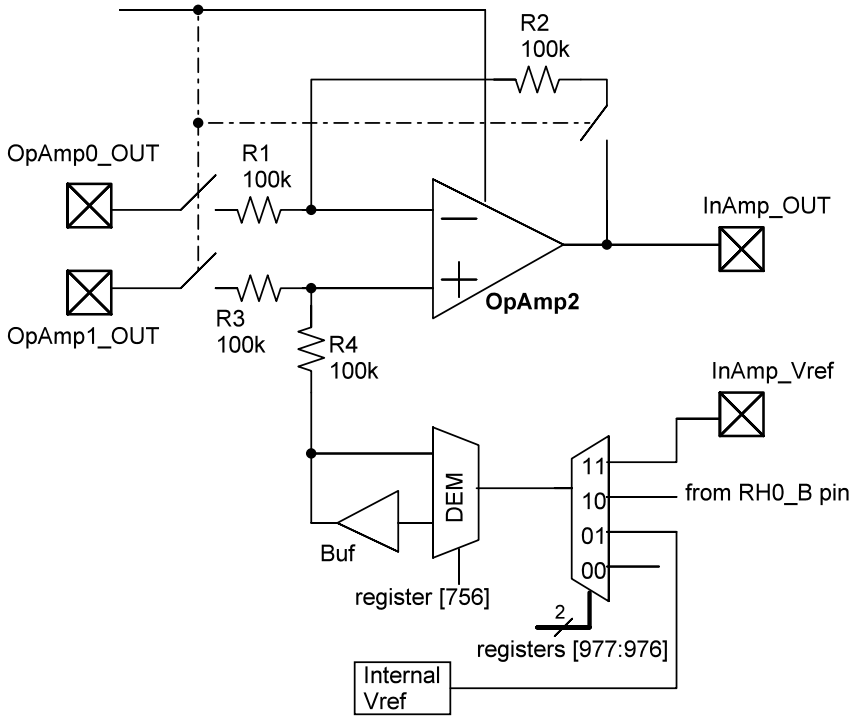


Figure 69. Internal Operational Amplifier Circuit

Each of the two Programmable Op Amp inputs has a hardware connection to the external pin and an optional connection to the internal voltage reference source, which makes it possible to create precise voltage or current source. For more detailed description of Op Amp V_{REF} sources see section 15. Voltage Reference. The output of the operational amplifier is hardwired to an external pin. This output can also be connected to the Programmable Trim block of rheostat macrocell, ACMP non-inverting input (ACMP0L+ for OA0, ACMP1L+ for OA1), or control the corresponding Analog Switch, depending on the mode of operation. Each Programmable Op Amp can also be configured as an analog comparator, in which case its output signal is connected to the Connection Matrix through a dedicated buffer.

Each Programmable Op Amp has a programmable bandwidth that can be set by two register bits. In addition, internal charge pump setting for each Op Amp must be changed according to bandwidth selection, see Table 32.

Internal charge pump can be disabled if input common-mode voltage $V_{CM} < (V_{DDA} - 1.5\ V)$. But it is strongly recommended to keep the default setting (enable charge pump).

The bandwidths may vary up to +/-30 % over PVT. Each operational amplifier is factory trimmed. This trimming is independent of the trimming associated with the onboard digital rheostat (system calibration).

The Internal operational amplifier shares its inputs with the Programmable Op Amps outputs. The voltage reference for the internal amplifier can be sourced from either the internal or external V_{REF}. Note that if the internal V_{REF} is used as a source for the instrumentation amplifier V_{REF}, the user can optionally connect this V_{REF} to the output pin, or disconnect the V_{REF} from output pin and use this pin as GPIO.

Also, if the Internal Op Amp is inactive (In Amp Mode is disabled), the user can use the In Amp_V_{REF} pin as GPIO. The In Amp_Out pin can be configured as GPI.

Table 32. Op Amps Bandwidth Settings

Op Amp Bandwidth Selection	Op Amp0				Op Amp1				Op Amp2 (Internal)			
	Bandwidth Selection		Charge Pump Frequency		Bandwidth Selection		Charge Pump Frequency		Bandwidth Selection		Charge Pump Frequency	
Register Bit	745	744	955	954	747	746	963	962	749	748	971	970
128 kHz	0	0	0	0	0	0	0	0	0	0	0	0
512 kHz	0	1	0	1	0	1	0	1	0	1	0	1
2.048 MHz	1	0	1	0	1	0	1	0	1	0	1	0
8.192 MHz	1	1	1	1	1	1	1	1	1	1	1	1

10.2 Modes of Operation

In order to use any of the Op Amp macrocells in the GreenPAK Designer, the power up signal (PWR_UP) must be set to logic High. By default, all Op Amp macrocells are turned off after SLG47004 startup. During power-up, outputs of all Op Amp will remain in a Hi-Z state and then become valid (see parameter t_{on} in section 3.14 Programmable Operational Amplifier Specifications).

Operational amplifiers turn-on time can be decreased by setting register bits [759:757] to 1. In this case Op Amp analog supporting blocks are always turned on. Note that current consumption of Op Amp will be increased when Op Amp is powered down and bits [759:757] is 1 (see section 3.14 Programmable Operational Amplifier Specifications).

See the list below for the Op Amp operation modes:

- Operational Amplifier mode
- Instrumentation Amplifier mode
- Analog Comparator mode
- Voltage Regulator mode
- Current Sink mode.

10.2.1 Operational Amplifier Mode

In this mode, the Programmable Op Amp operates as a conventional operational amplifier. Also, the Programmable Op Amp can source the corresponding non-inverting ACMP input (see ACMP macrocell settings). The output of the Programmable Op Amp macrocell is in a Hi-Z state while the macrocell is turned off.

Figure 70 shows the example of differential amplifier with input offset voltage compensation with help of digital rheostat and programmable trim block. Zero input voltage equal to output voltage $V_{OUT} = V_{DD}/2$.

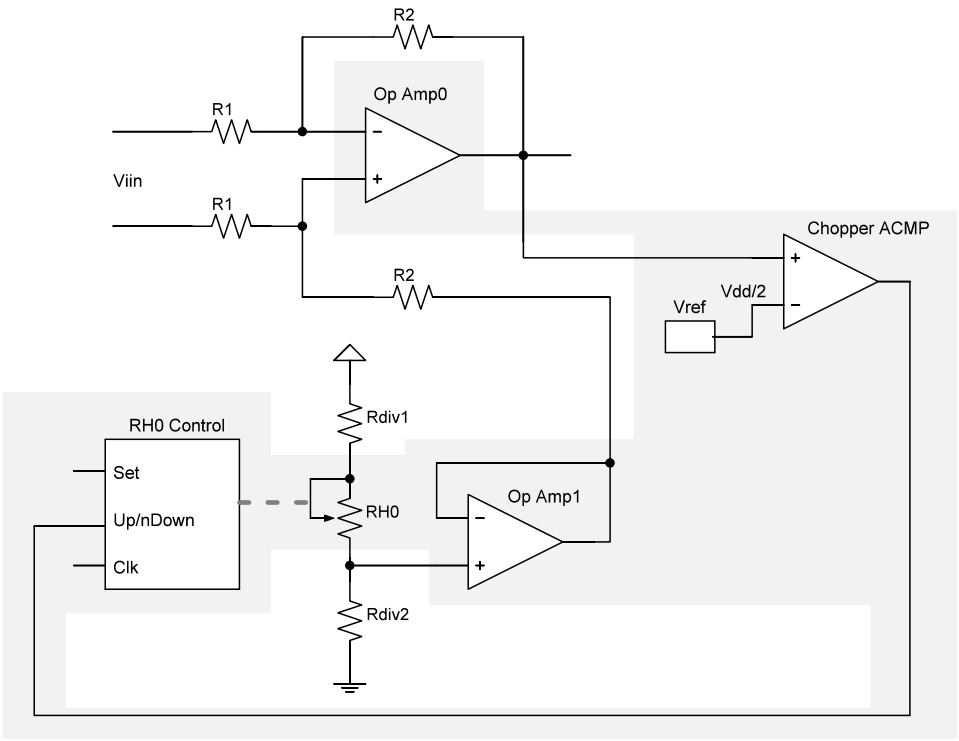


Figure 70. Example of Input Voltage Offset Compensation

10.2.2 Instrumentation Amplifier Mode

If this mode is active (Matrix Output [98] is High level), the two Programmable Op Amps and the single Internal Op Amp work together in Instrumentation Amplifier configuration, shown in Figure 71. When power up signal is logic LOW the output of In Amp is in Hi-Z state.

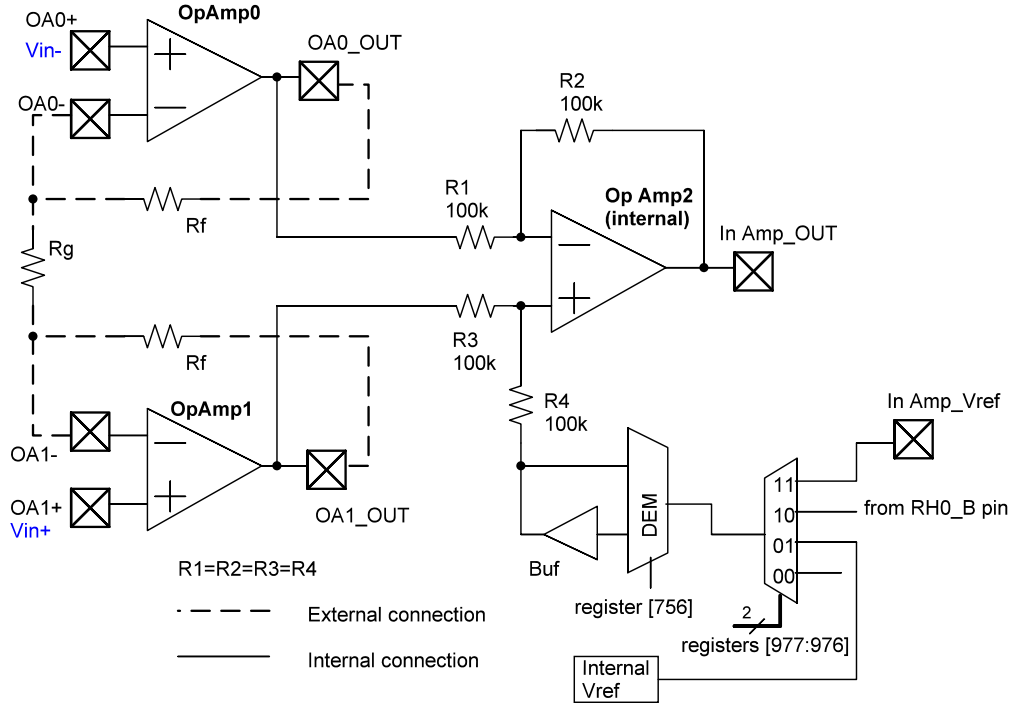


Figure 71. Instrumentation Amplifier Structure

The absolute value of internal resistors R_1, R_2, R_3, R_4 is 100 kΩ. The resistors R_f and R_g are user defined external resistors. The output voltage V_{OUT} of the instrumentation amplifier shown in Figure 71 is

$$V_{OUT} = (1 + 2R_f / R_g)(V_{IN+} - V_{IN-}) + V_{REF}$$

The user can trim both the gain and the offset error of the instrumentation amplifier using two of the Rheostats from the SLG47004. Figure 72 shows the configuration of the instrumentation amplifier in this scenario.

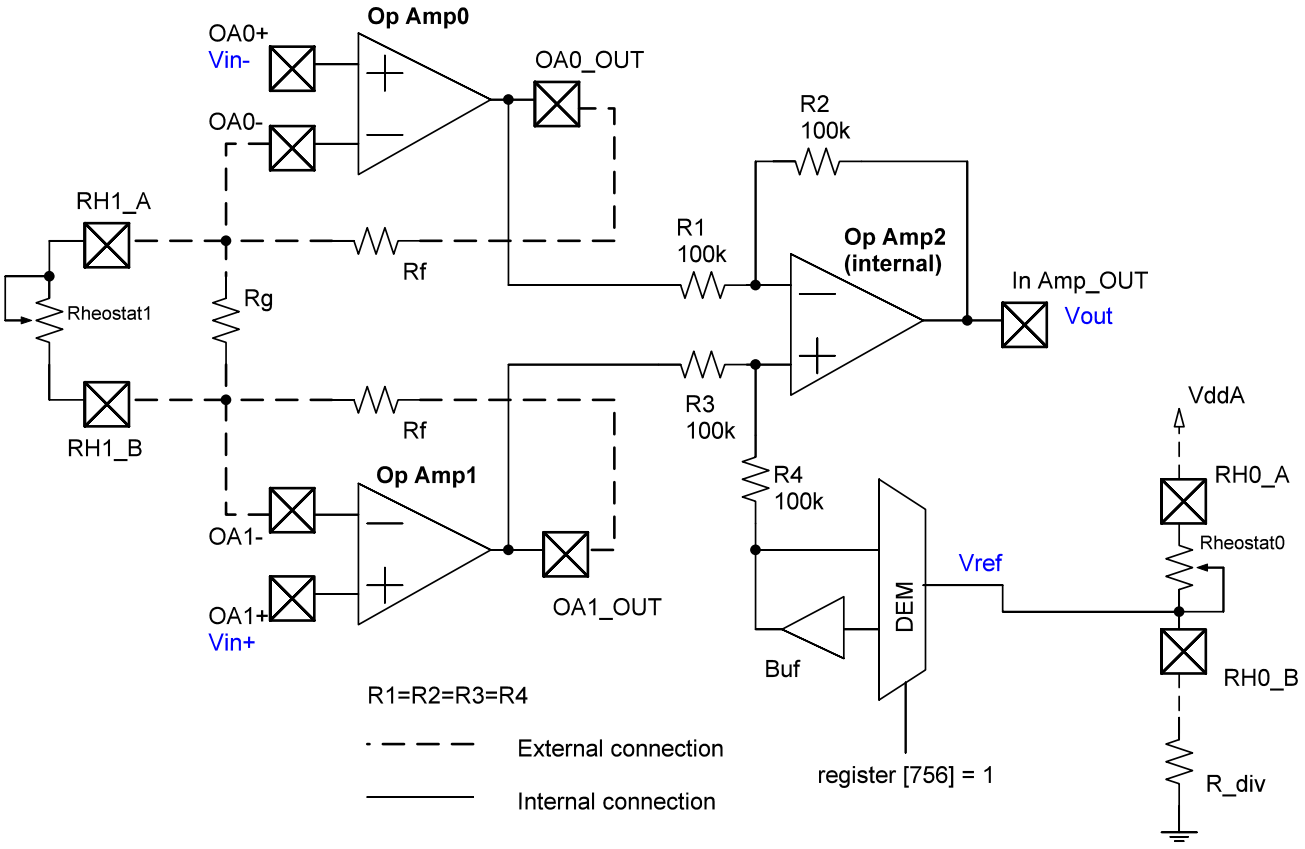


Figure 72. Instrumentation Operational Amplifier Configuration for Users Trim

Note that in Figure 72, the Demux connects to the V_{REF} external input with an internal buffer (reg [756] = 1). This allows us to eliminate the influence of resistor divider R_{div} and Rheostat0 on instrumentation amplifier.

It is possible to use a built-in Auto-Trim function for either setting the zero point of the Wheatstone bridge sensor using the In Amp or tuning a system output voltage to the desired level. However, the following limitations exist for using the built-in Auto-Trim function to trim both total system offset and system gain errors:

- The Auto-Trim procedures of total offset compensation and system gain error must be done iteratively starting and finishing with the total offset compensation: 1st iteration - offset compensation, 2nd iteration - gain trim, 3rd iteration - offset compensation. Extra iterations can be added to achieve a better accuracy. The last iteration should be an offset compensation.
- Total system offset (sensor offset + Op Amp1 offset + Op Amp2 offset) must not be greater than Vsensor_output_range/2.

It's possible to power external components like bridge or ADC from internal HD Buffer of SLG47004 to improve accuracy of system.

10.2.3 Analog Comparator Mode

Both operational amplifiers have an Analog Comparator mode in which they work as conventional rail-to-rail comparators.

10.2.4 Voltage Regulator Mode

In this mode, the Op Amp output drives P-FET (part of Analog Switch). Note that FETs of Analog Switches have different resistances. Analog Switch 0 has Rds_PMOS << Rds_NMOS, while Analog Switch 1 has Rds_NMOS << Rds_PMOS. That's why it is recommended to implement voltage regulator mode using Analog Switch 0. In this mode the Op Amp output is High when the macrocell is turned off. Figure 73 (A) shows the typical implementation of the voltage source function. Optionally, the user can use this mode to implement a constant current source with load connected to ground (Figure 73, B, C). Note that Op Amp must operate in operational amplifier mode (reg [750] = 0 for Op Amp0, reg [751] = 0 for Op Amp1).

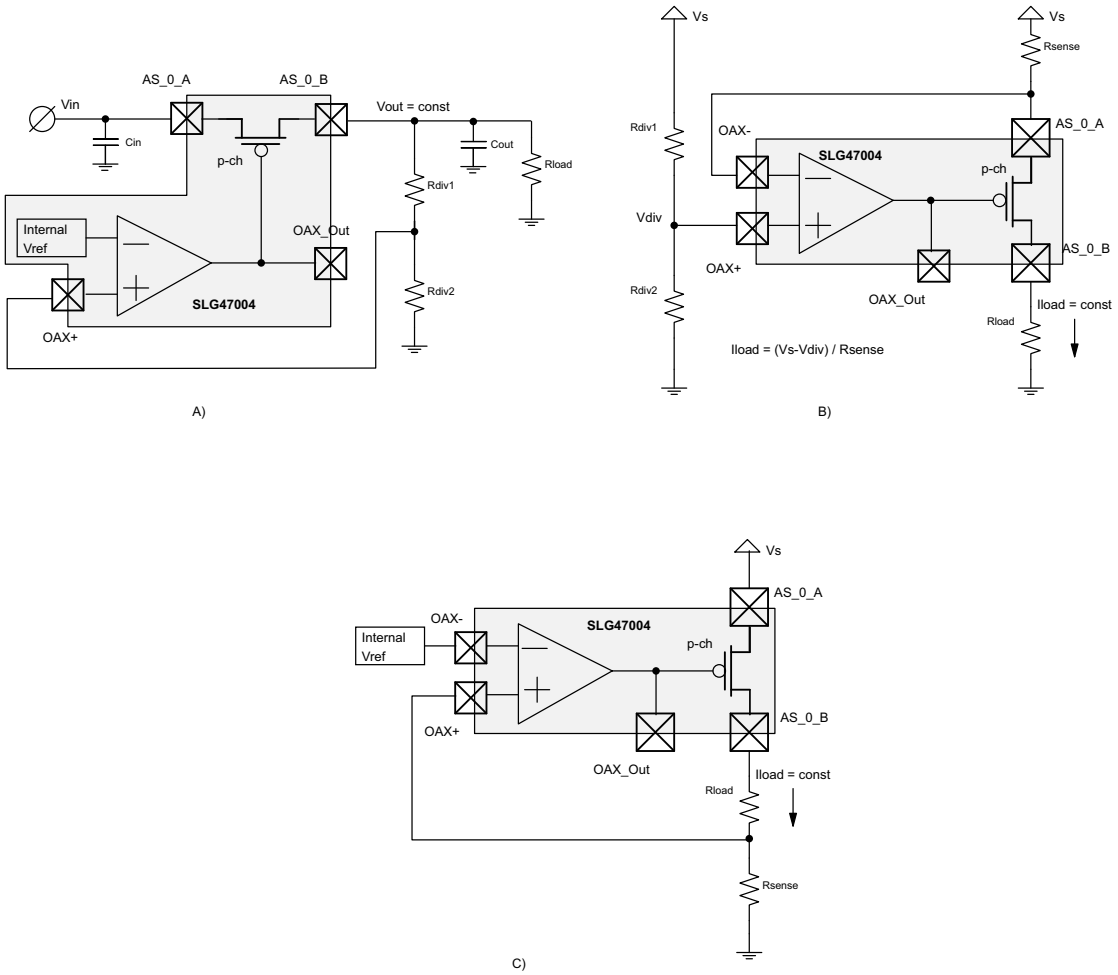


Figure 73. Typical Implementation of Voltage Regulator (A) and Current Sources (B, C)

Note that in this mode only an enhanced P channel FET of An_Sw_0 is used.

10.2.5 Current Sink Mode

Also, the Op Amp output can drive the N-FET (part of the Analog Switch) in order to implement a constant current sink. Note that FETs of Analog Switches have different resistances. Analog Switch 0 has Rds_PMOS << Rds_NMOS, while Analog Switch 1 has Rds_NMOS << Rds_PMOS. That's why it is recommended to implement current sink mode using Analog Switch 1. In this mode, the Op Amp output is LOW when the macrocell is turned off. Figure 74 shows a typical implementation of this Current Sink Function. Note that Op Amp must operate in operational amplifier mode (reg [750] = 0 for Op Amp0, reg [751] = 0 for Op Amp1).

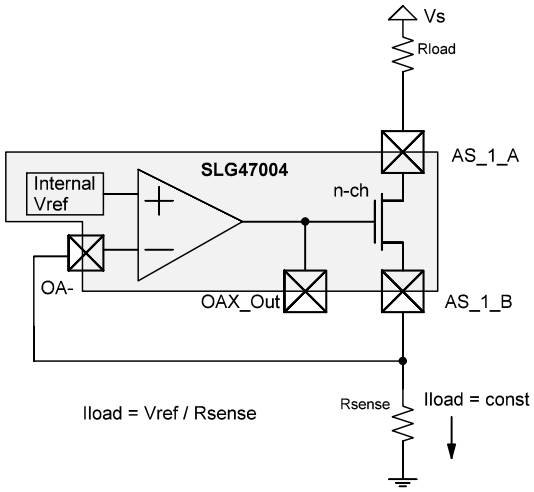


Figure 74. Constant Current Sink

Note that in this mode only an enhanced N channel FET of An_Sw_1 is used.

10.3 Op Amps Typical Performance

T_A = 25 °C, V_{DDA} = 5.0 V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 80 pF, unless otherwise stated.

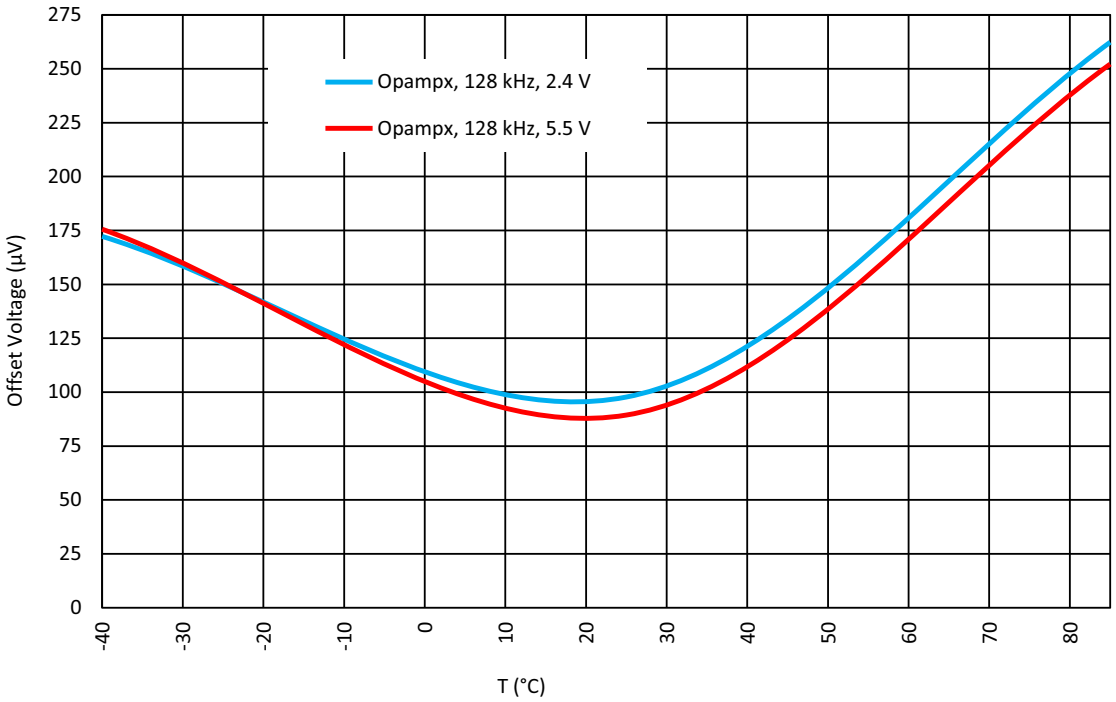


Figure 75: Op Ampx Input Offset Voltage vs. T_A at Input CM Voltage = V_{DD}/2, BW = 128 kHz

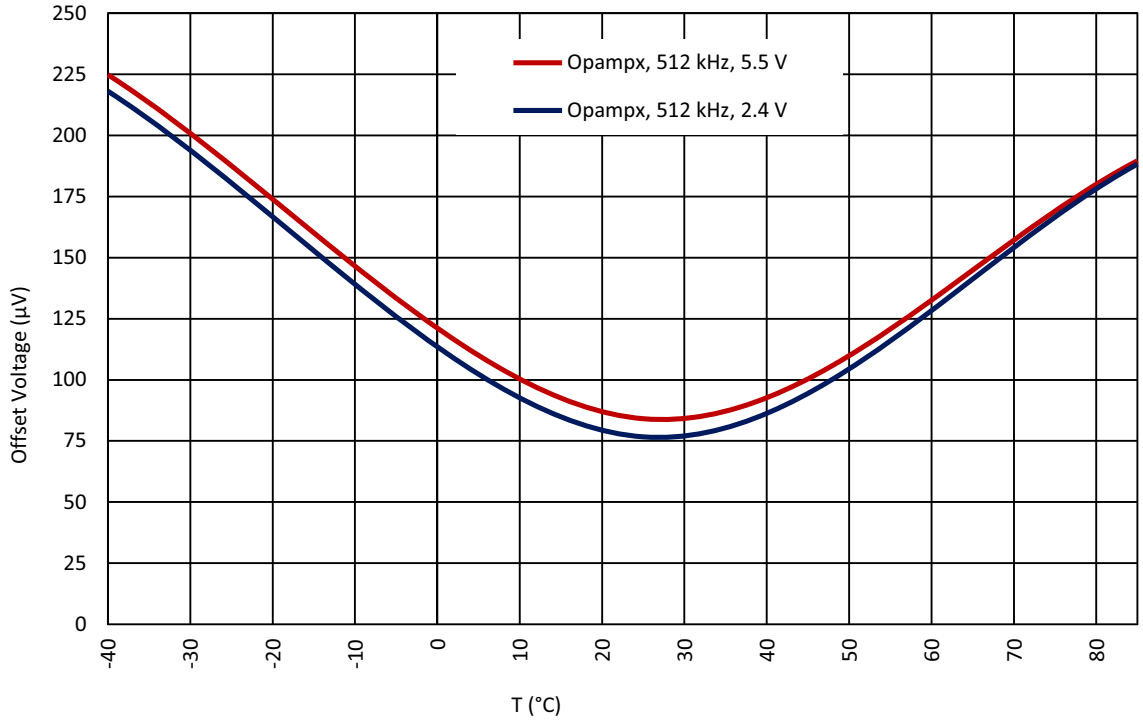


Figure 76: Op Ampx Input Offset Voltage vs. T_A at Input CM Voltage = V_{DD}/2, BW = 512 kHz

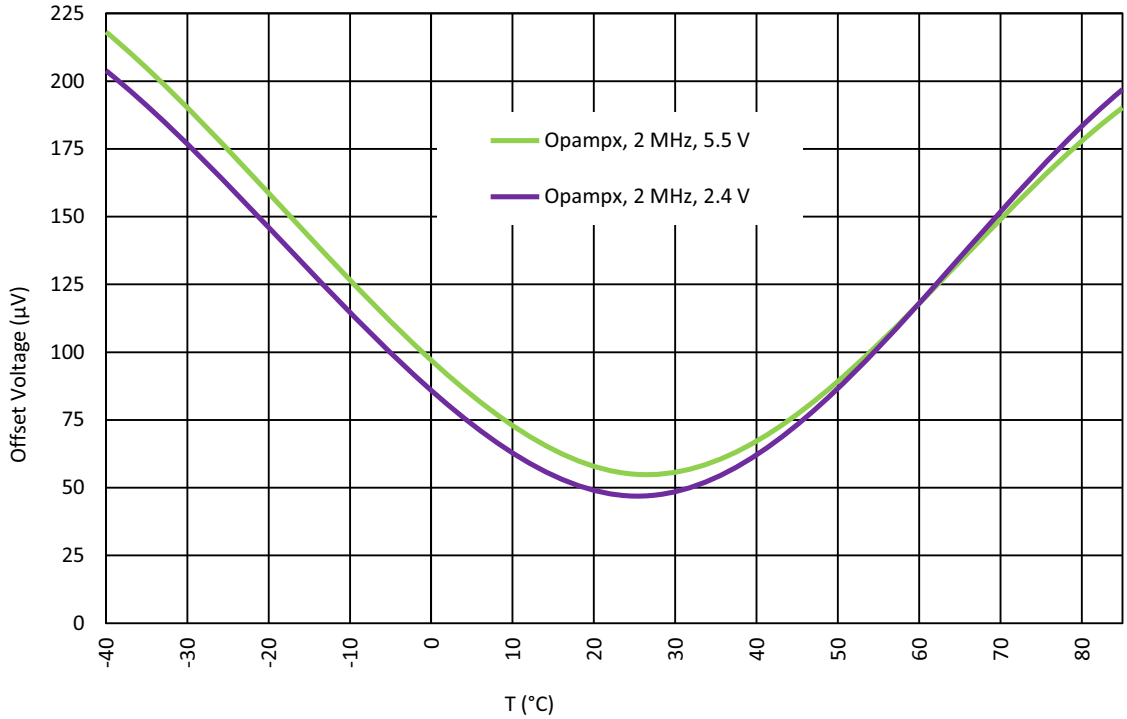


Figure 77: Op Ampx Input Offset Voltage vs. T_A at Input CM Voltage = V_{DD}/2, BW = 2 MHz

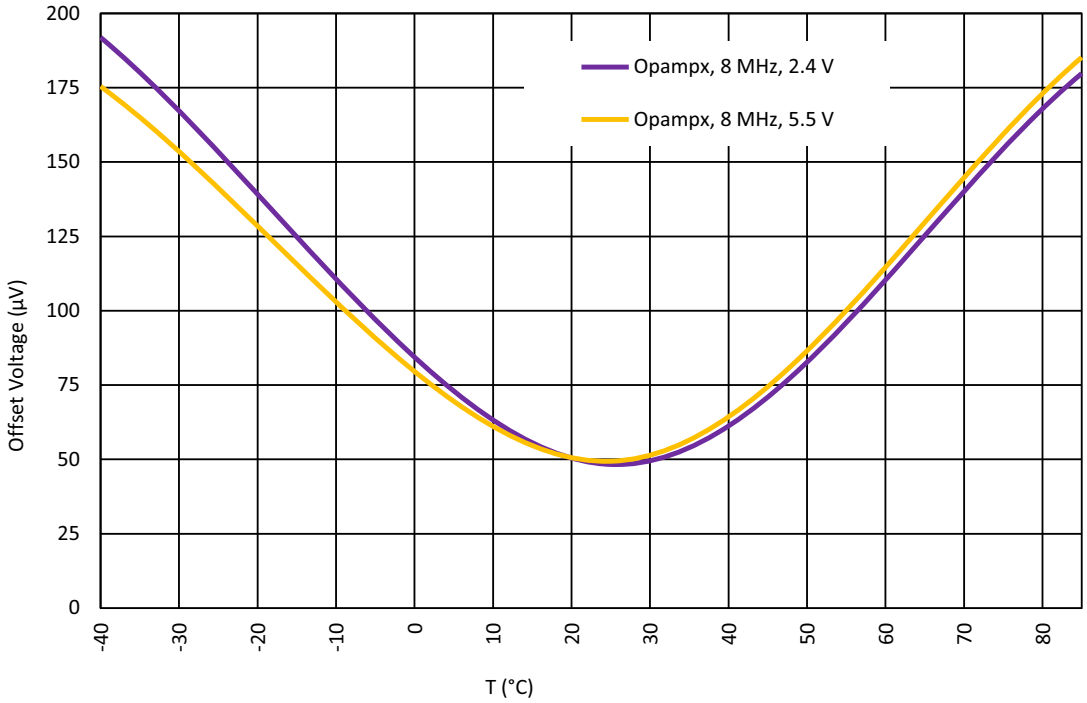


Figure 78: Op Ampx Input Offset Voltage vs. T_A at Input CM Voltage = V_{DD}/2, BW = 8 MHz

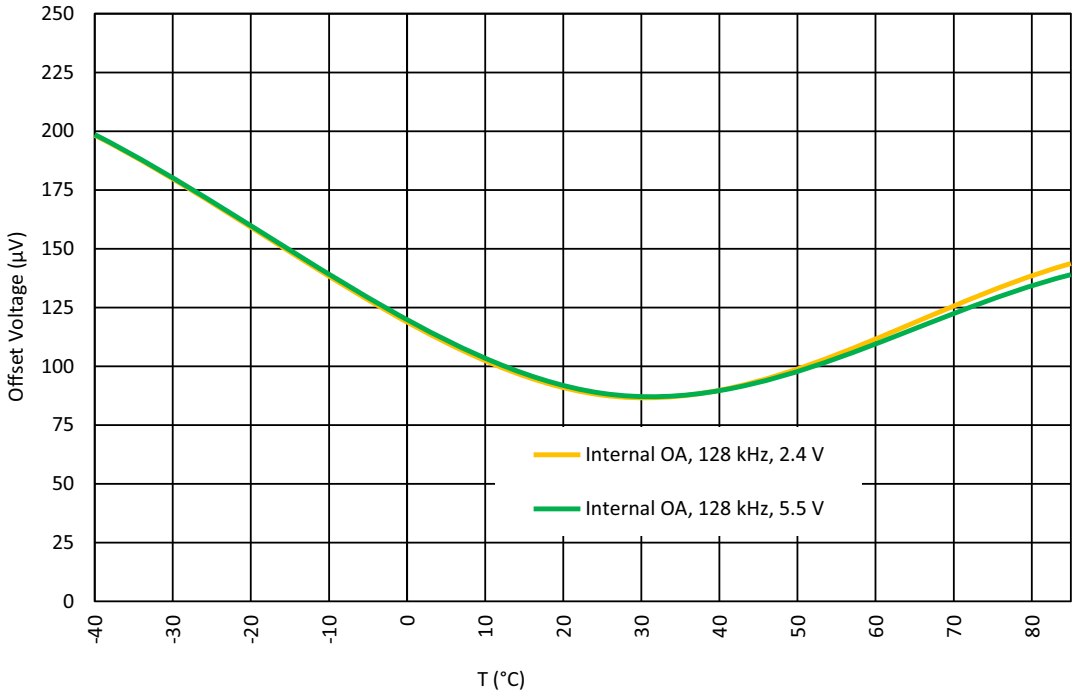


Figure 79. Internal Op Amp Input Offset Voltage vs. T_A at Input CM Voltage = V_{DD}/2, BW = 128 kHz

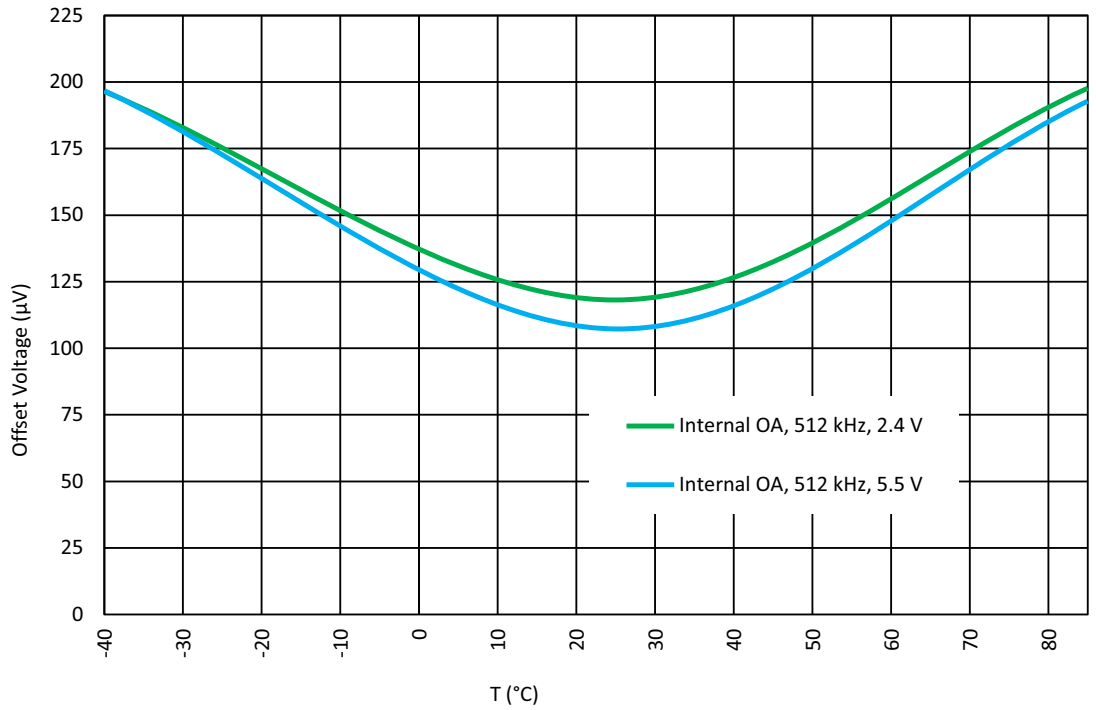


Figure 80. Internal Op Amp Input Offset Voltage vs. T_A at Input CM Voltage = V_{DD}/2, BW = 512 kHz

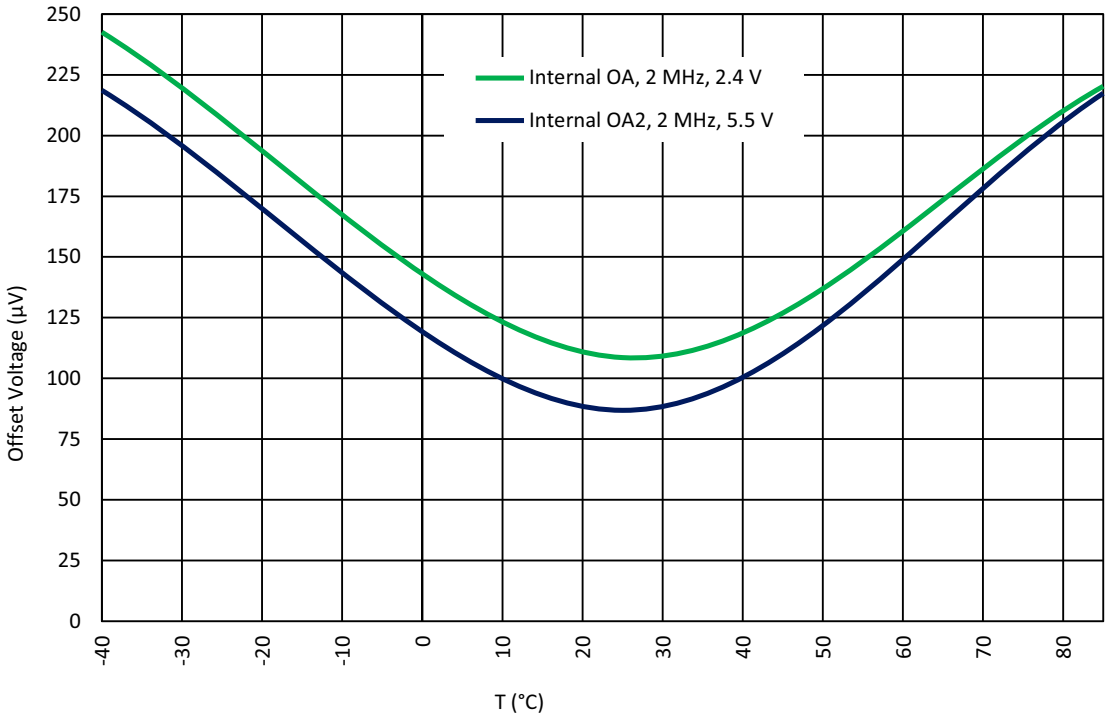


Figure 81. Internal Op Amp Input Offset Voltage vs. T_A at Input CM Voltage = V_{DD}/2, BW = 2 MHz

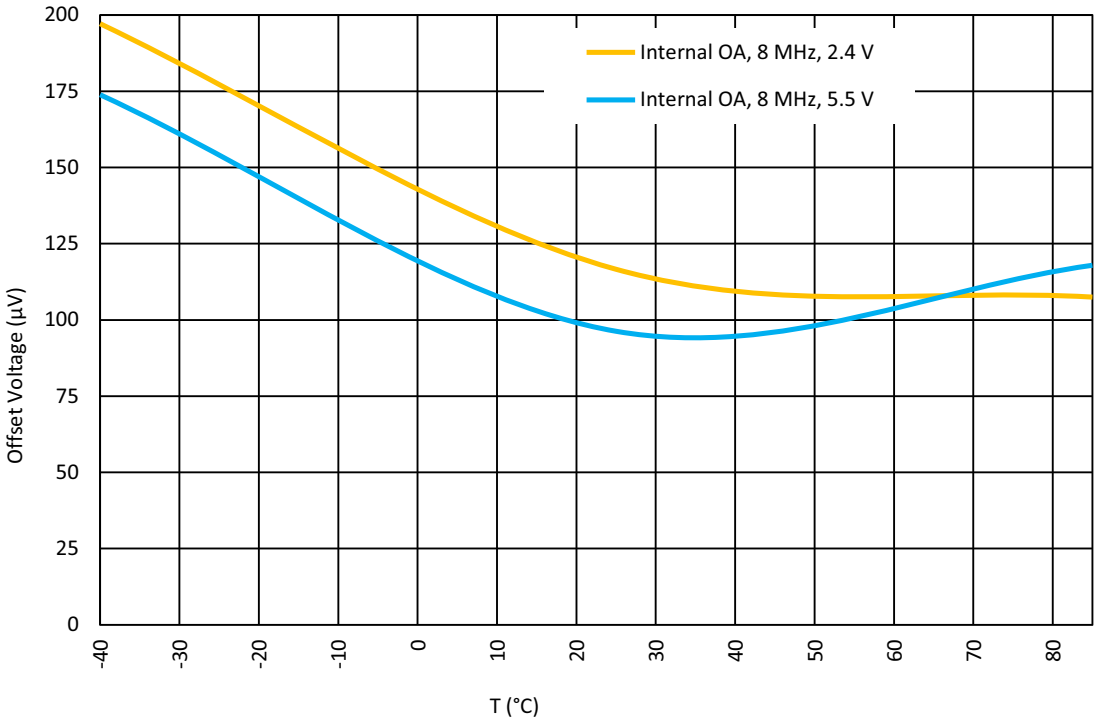


Figure 82. Internal Op Amp Input Offset Voltage vs. T_A at Input CM Voltage = V_{DD}/2, BW = 8 MHz

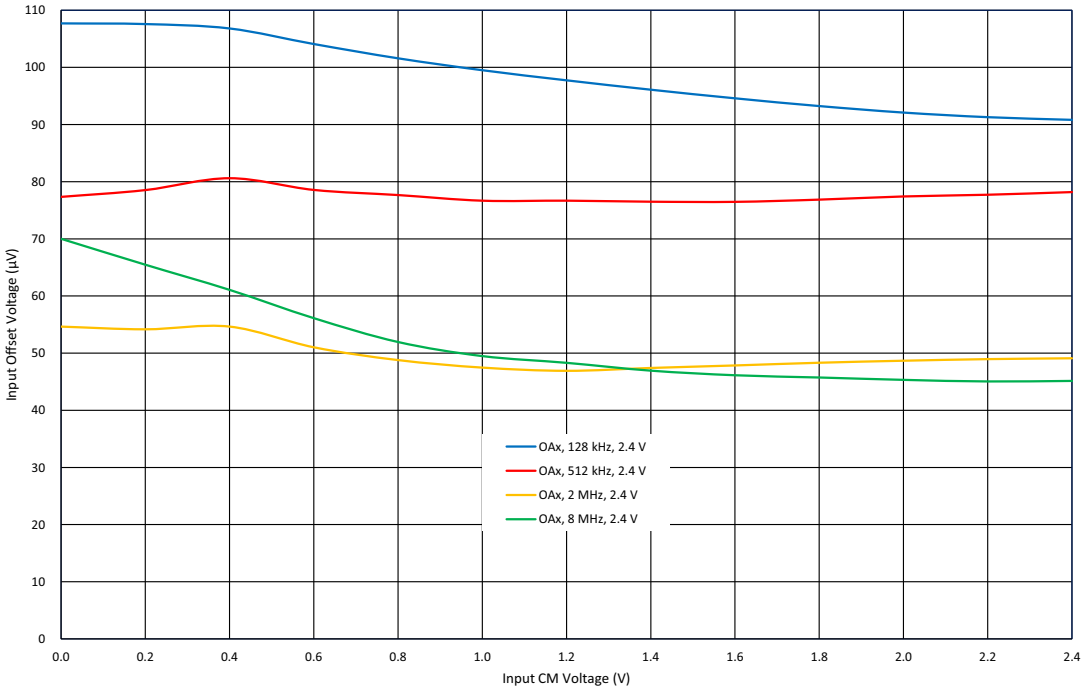


Figure 83. OpAmp0, 1 Input Offset Voltage vs. Input CM Voltage at T_A = 25 °C, V_{DDA} = 2.4 V

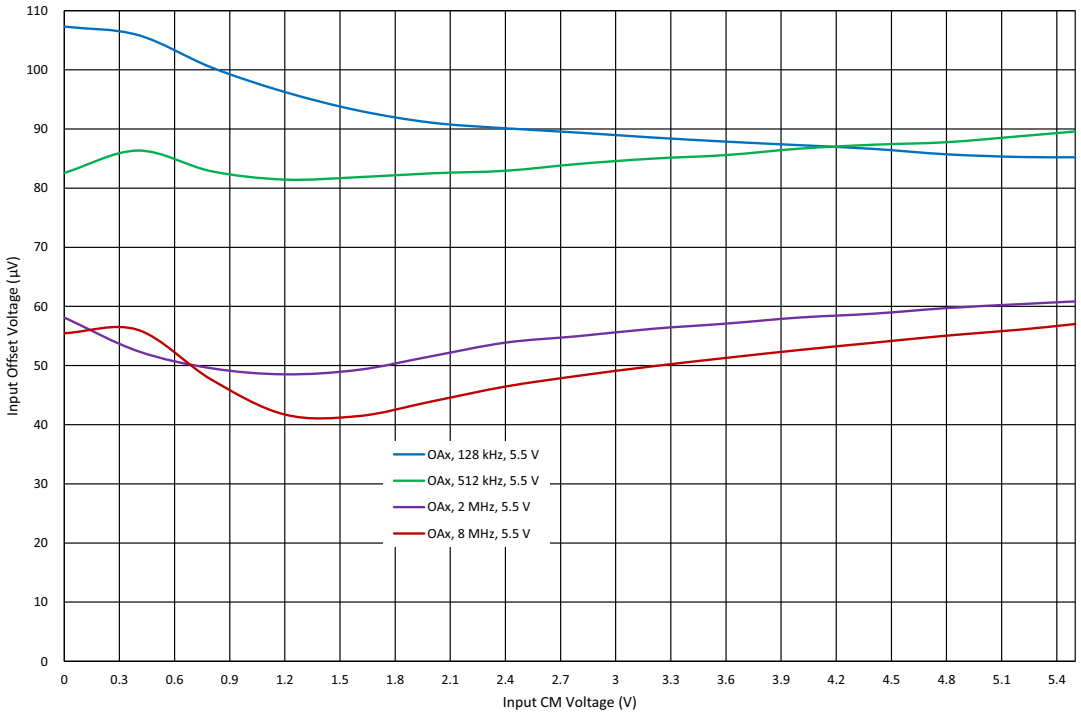


Figure 84. OpAmp0, 1 Input Offset Voltage vs. Input CM Voltage at T_A = 25 °C, V_{DDA} = 5.5 V

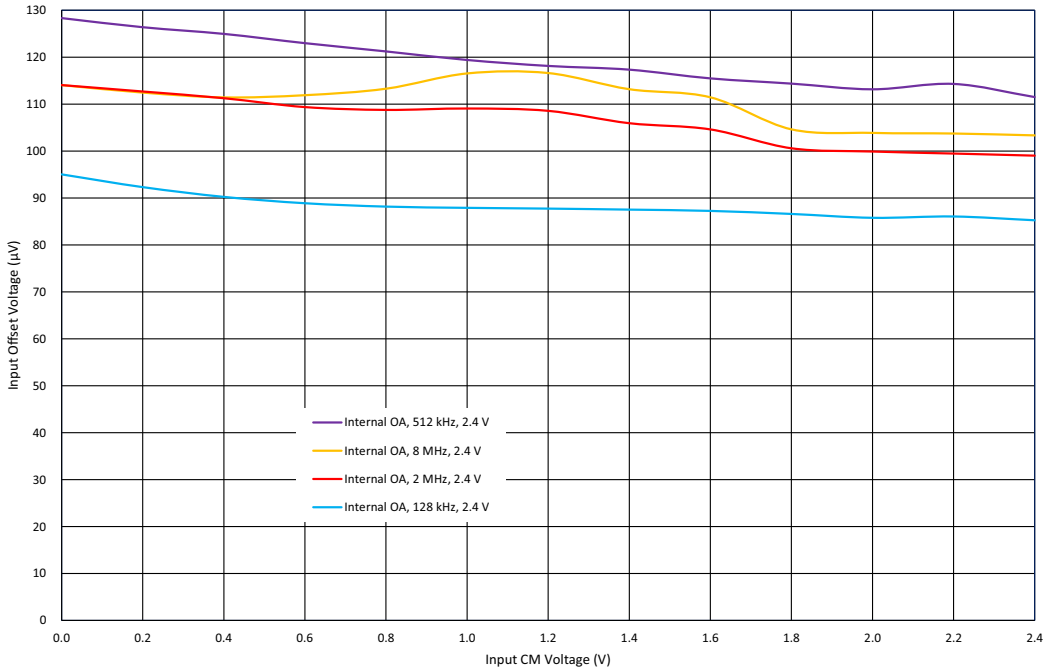


Figure 85. Internal OpAmp Input Offset Voltage vs. Input CM Voltage at T_A = 25 °C, V_{DDA} = 2.4 V

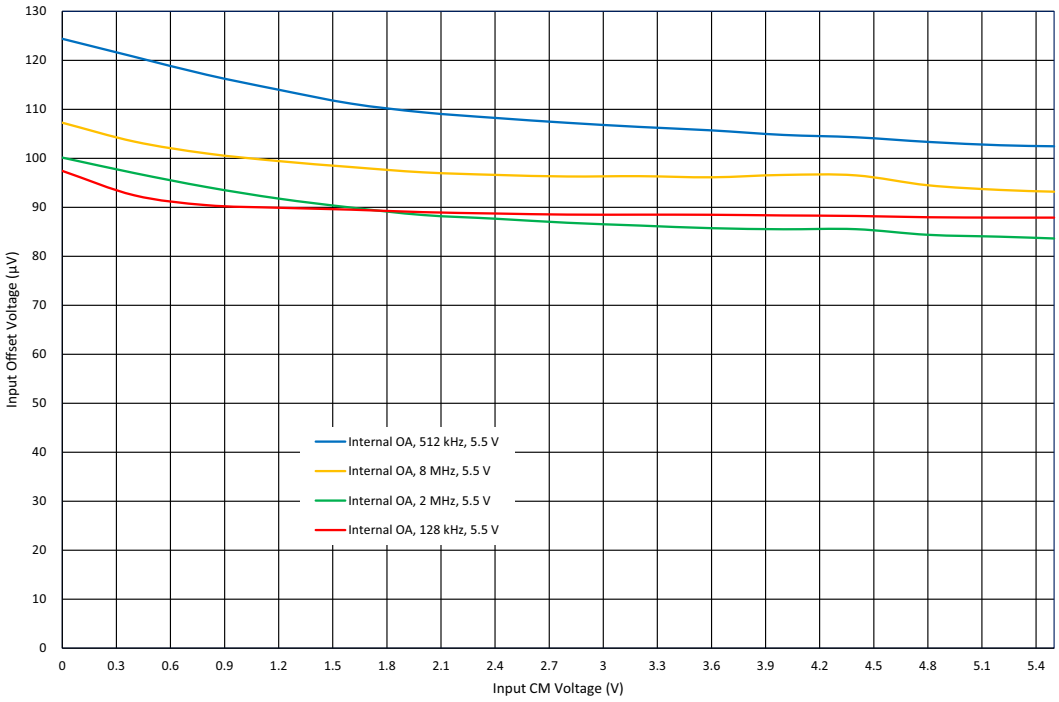


Figure 86. Internal OpAmp Input Offset Voltage vs. Input CM Voltage at T_A = 25 °C, V_{DDA} = 5.5 V

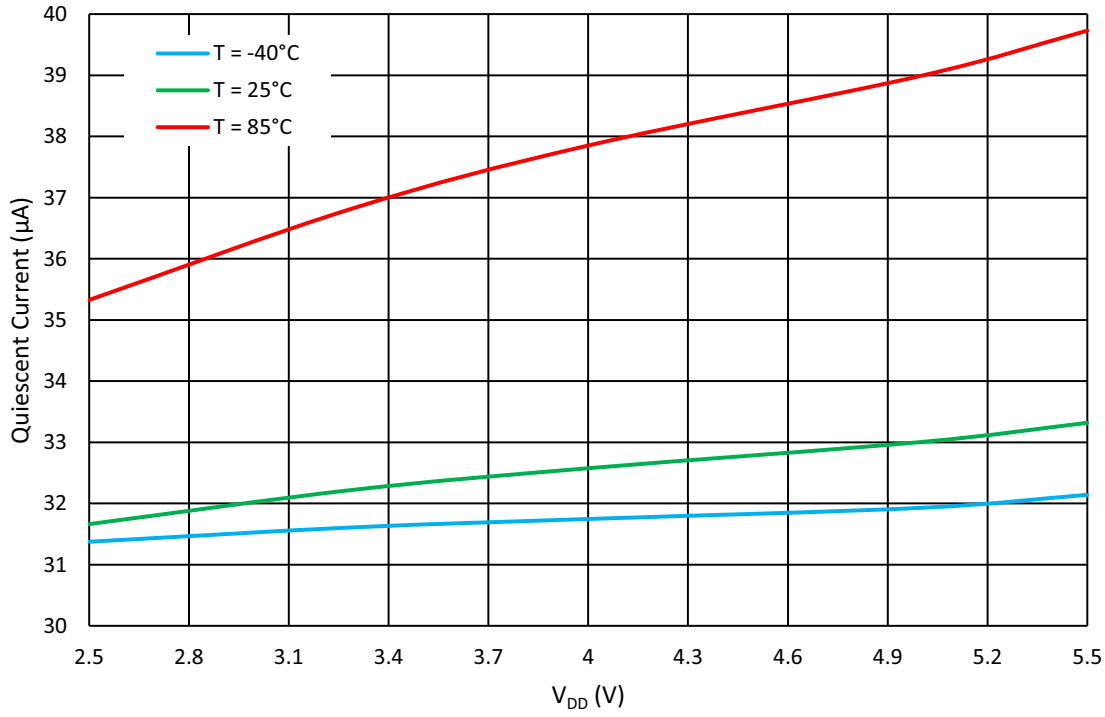


Figure 87. Quiescent Current vs. Power Supply Voltage for BW = 128 kHz

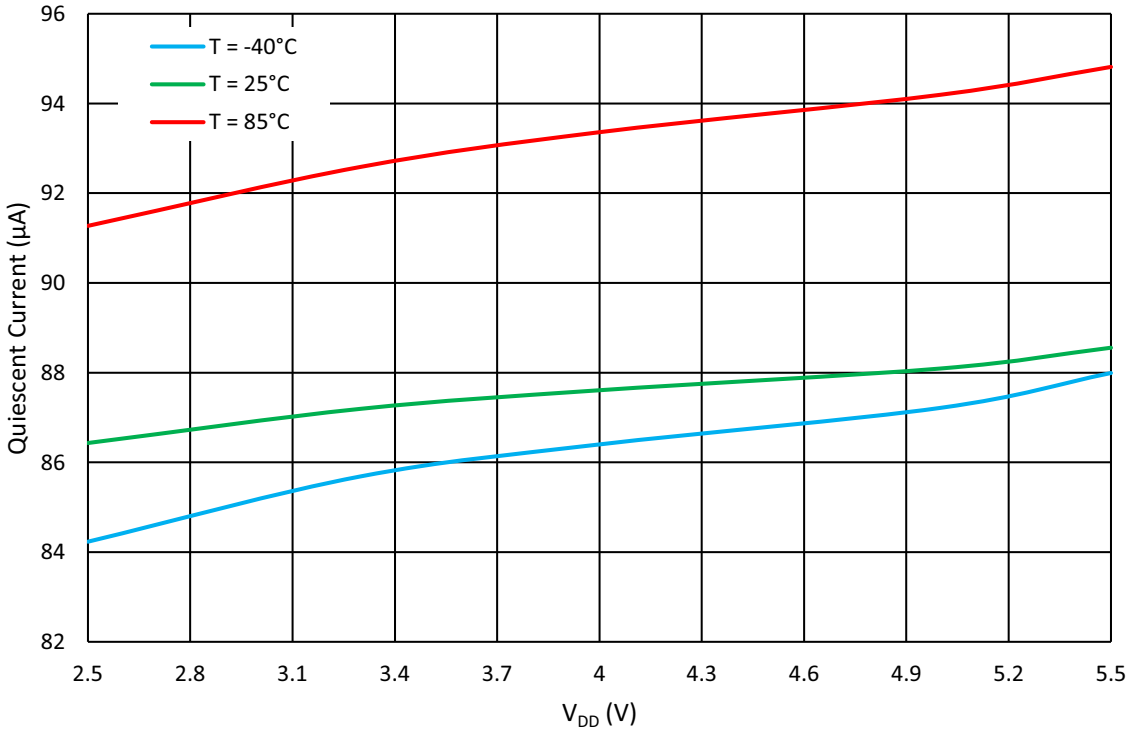


Figure 88. Quiescent Current vs. Power Supply Voltage for BW = 512 kHz

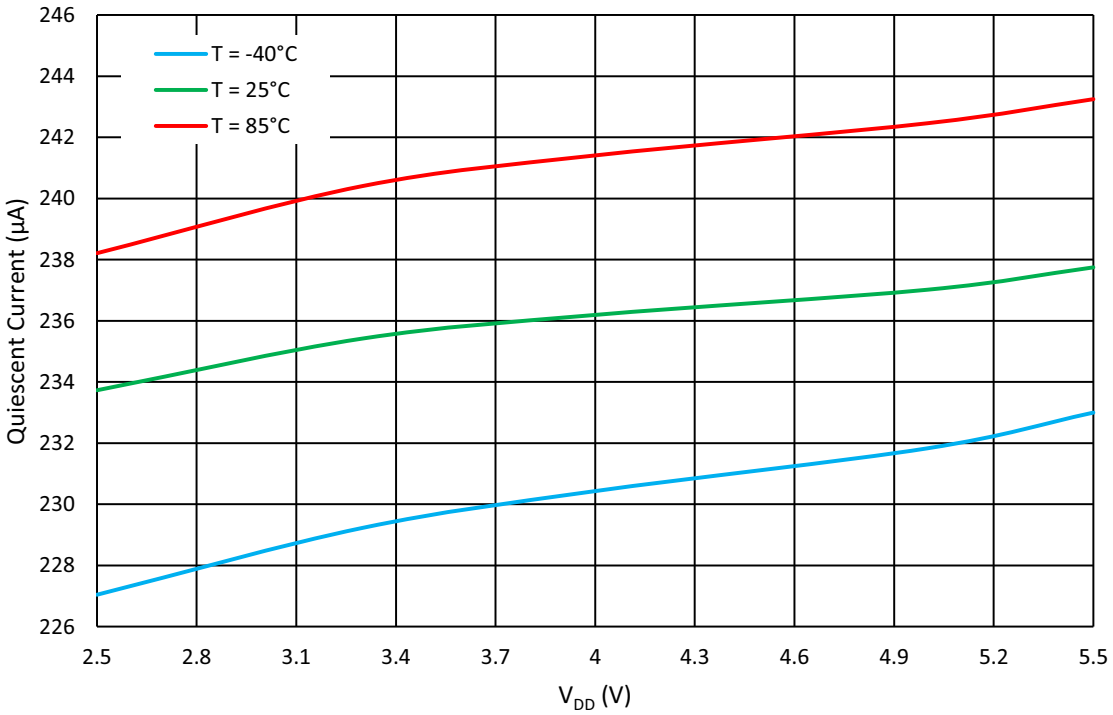


Figure 89. Quiescent Current vs. Power Supply Voltage for BW = 2 MHz

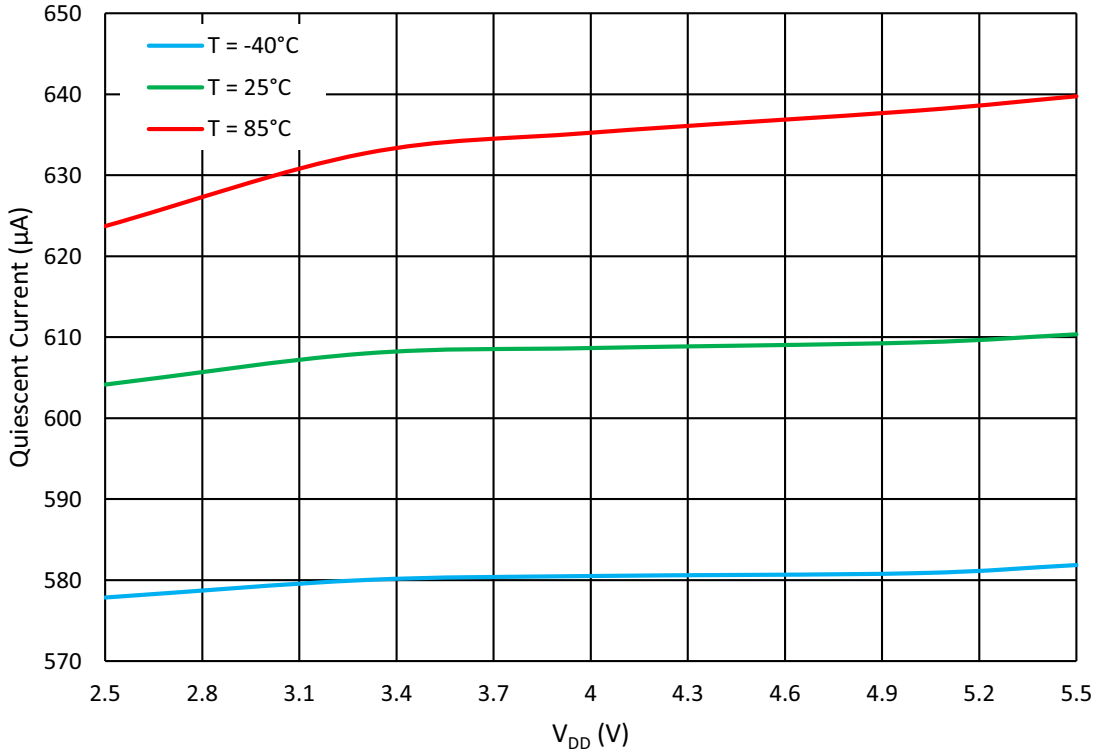


Figure 90. Quiescent Current vs. Power Supply Voltage for BW = 8 MHz

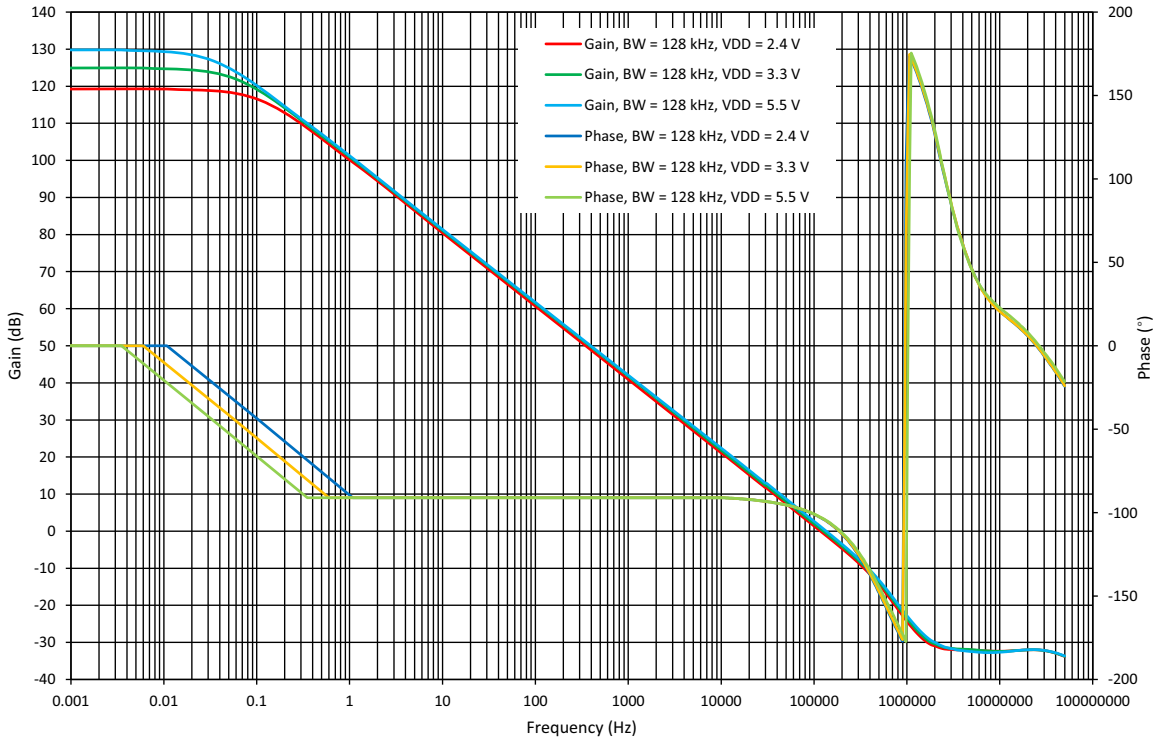


Figure 91. OA0 Open Loop Gain and Phase vs. Frequency for BW = 128 kHz

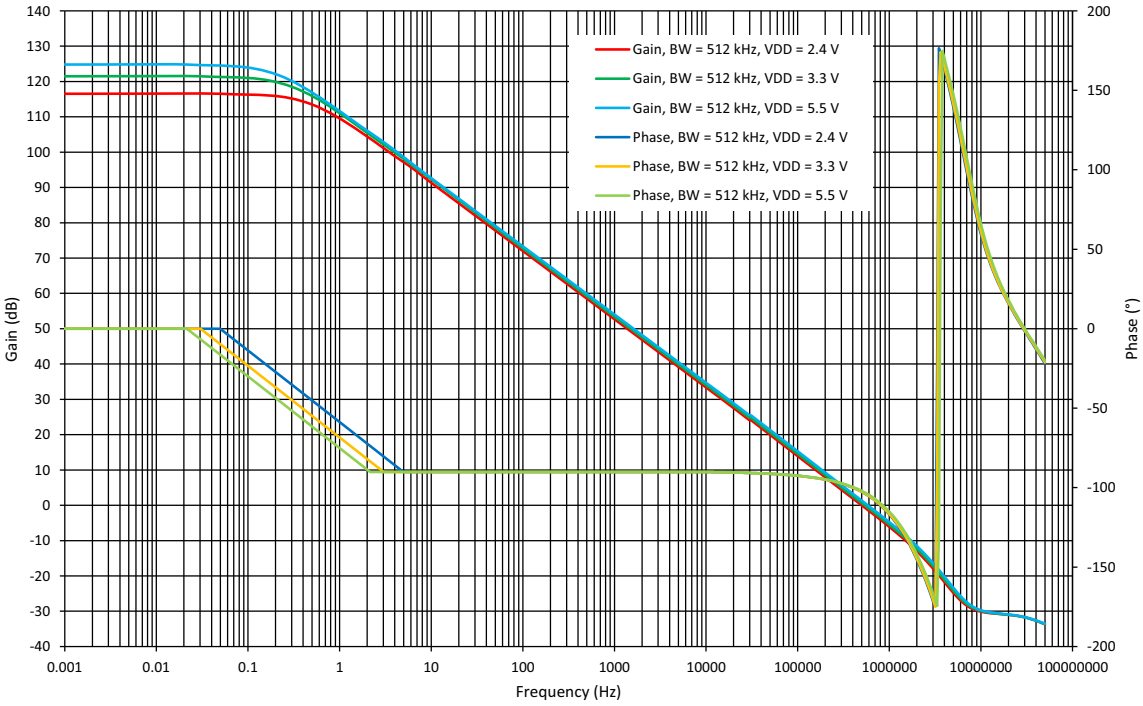


Figure 92. OA0 Open Loop Gain and Phase vs. Frequency for BW = 512 kHz

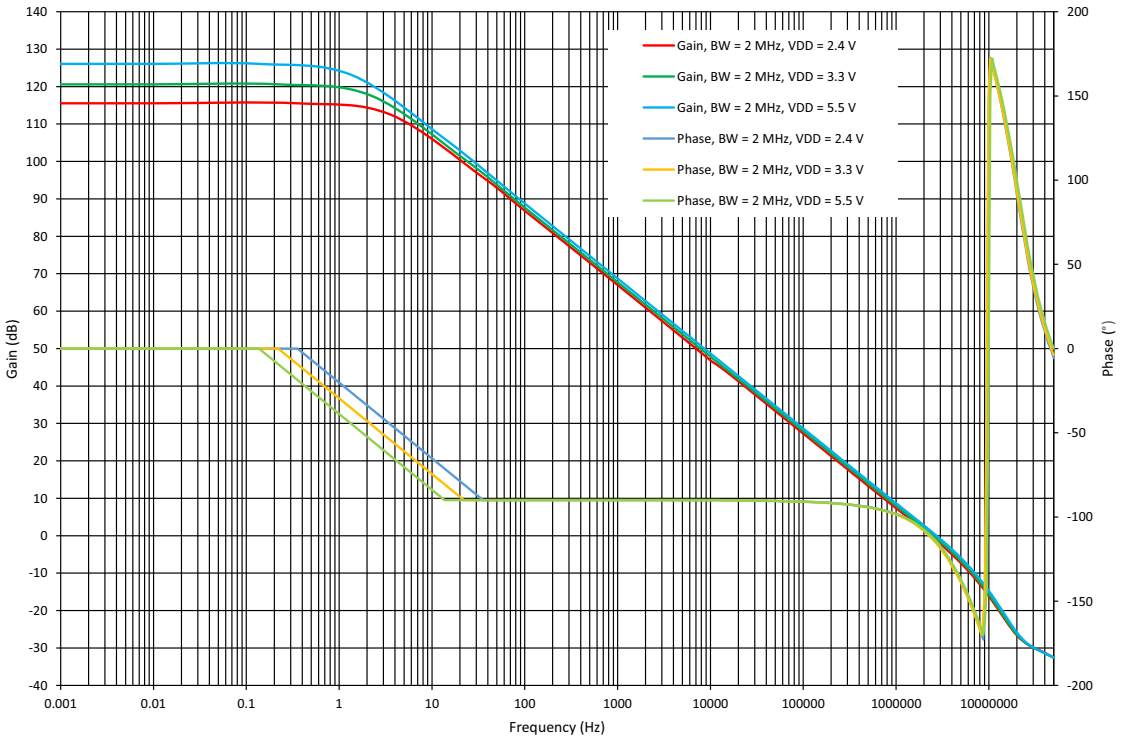


Figure 93. OA0 Open Loop Gain and Phase vs. Frequency for BW = 2 MHz

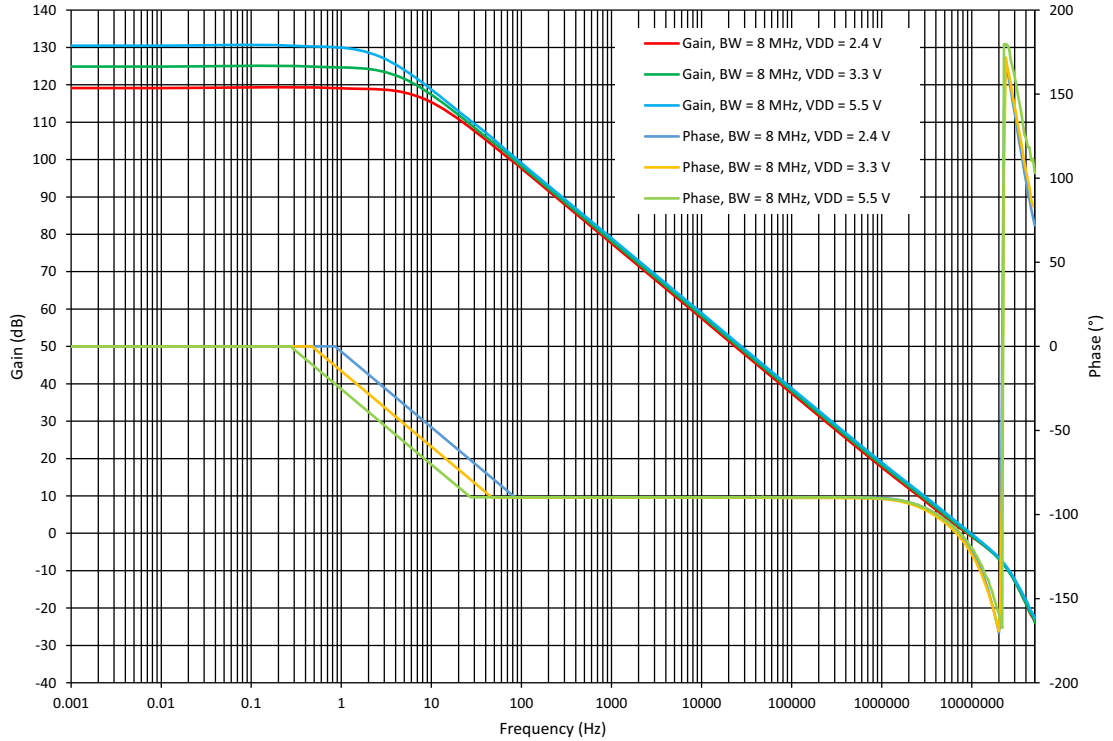


Figure 94. OA0 Open Loop Gain and Phase vs. Frequency for BW = 8 MHz

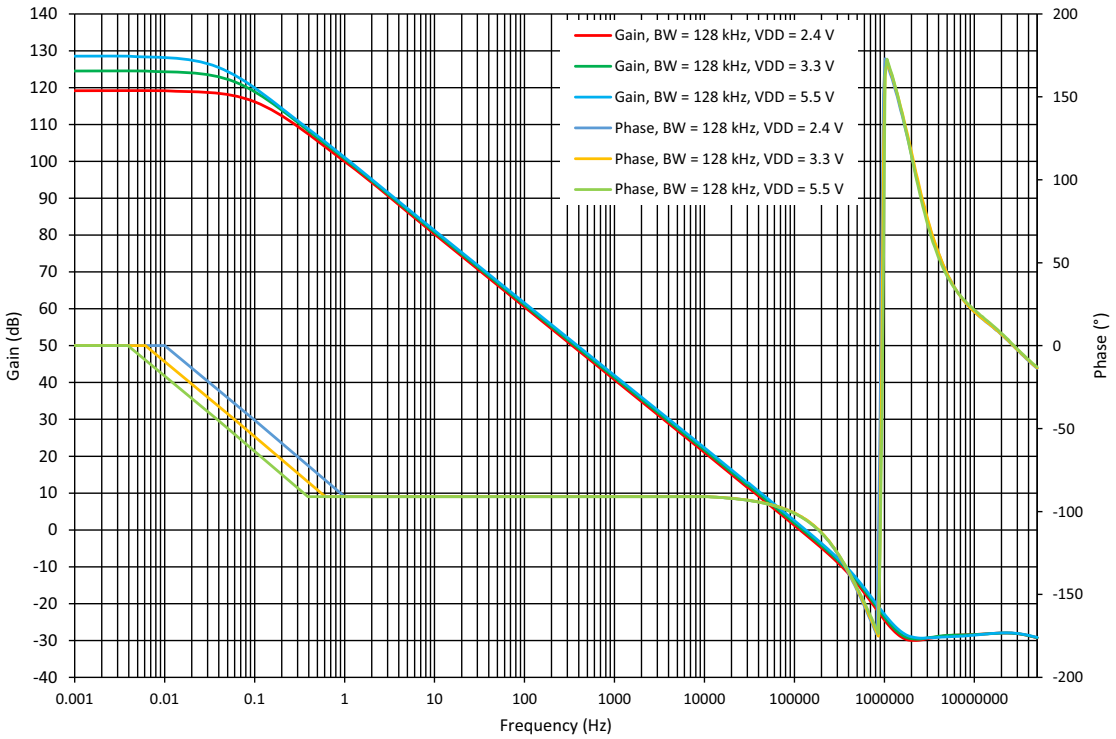


Figure 95. OA1 Open Loop Gain and Phase vs. Frequency for BW = 128 kHz

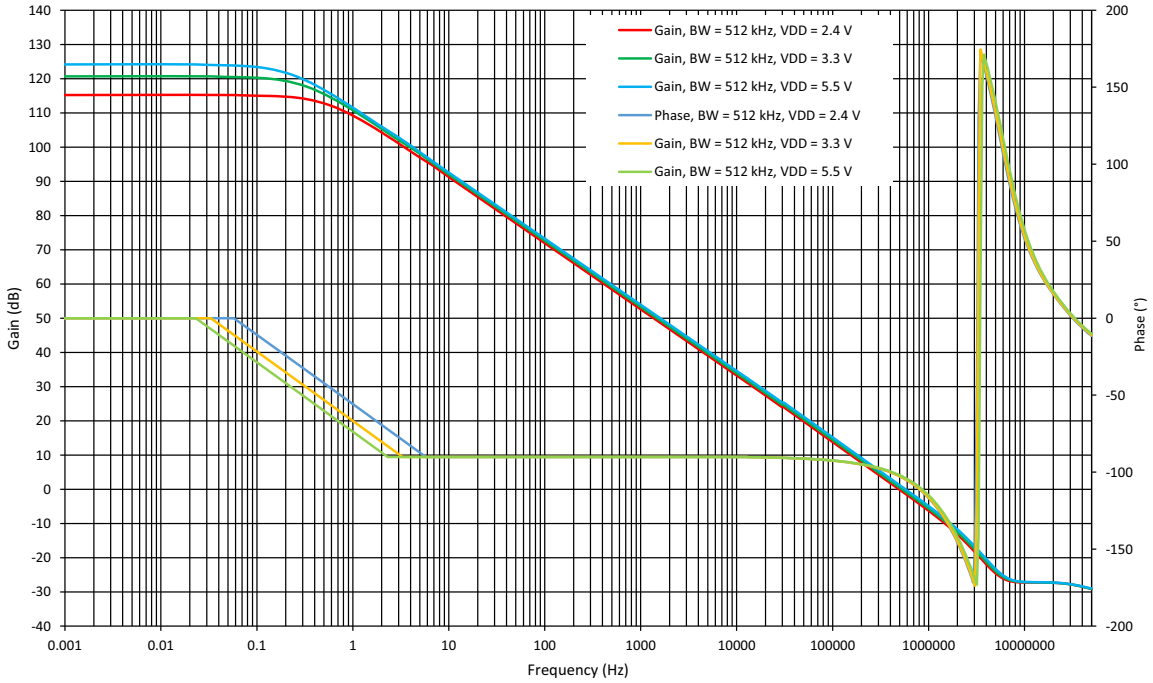


Figure 96. OA1 Open Loop Gain and Phase vs. Frequency for BW = 512 kHz

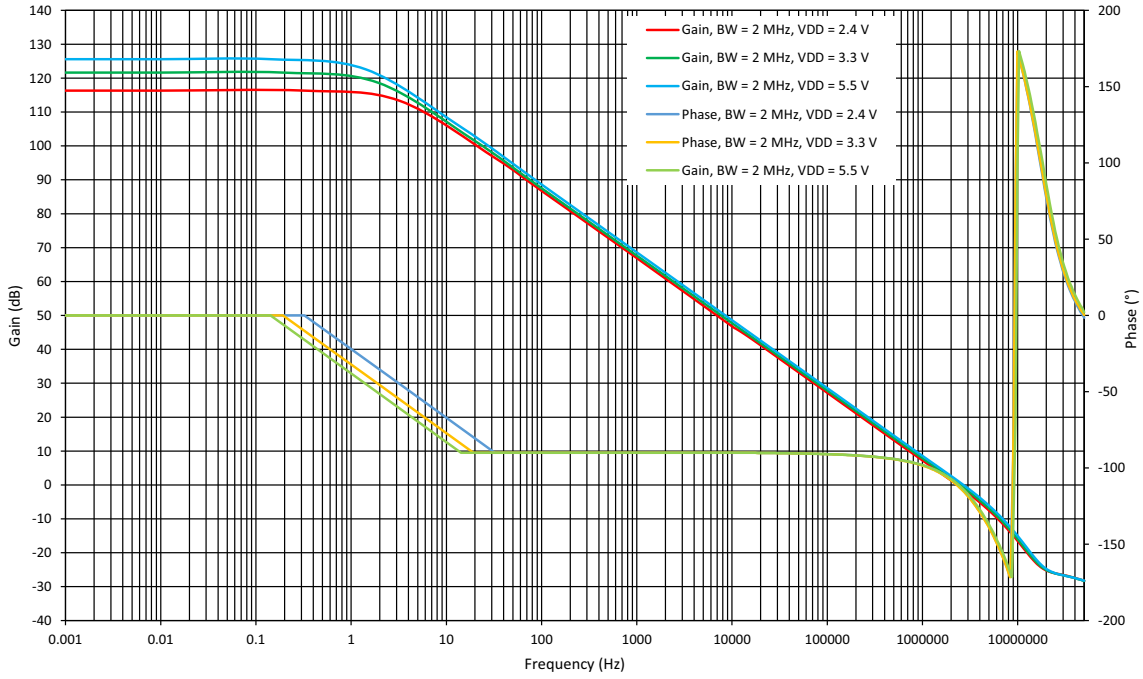


Figure 97. OA1 Open Loop Gain and Phase vs. Frequency for BW = 2 MHz

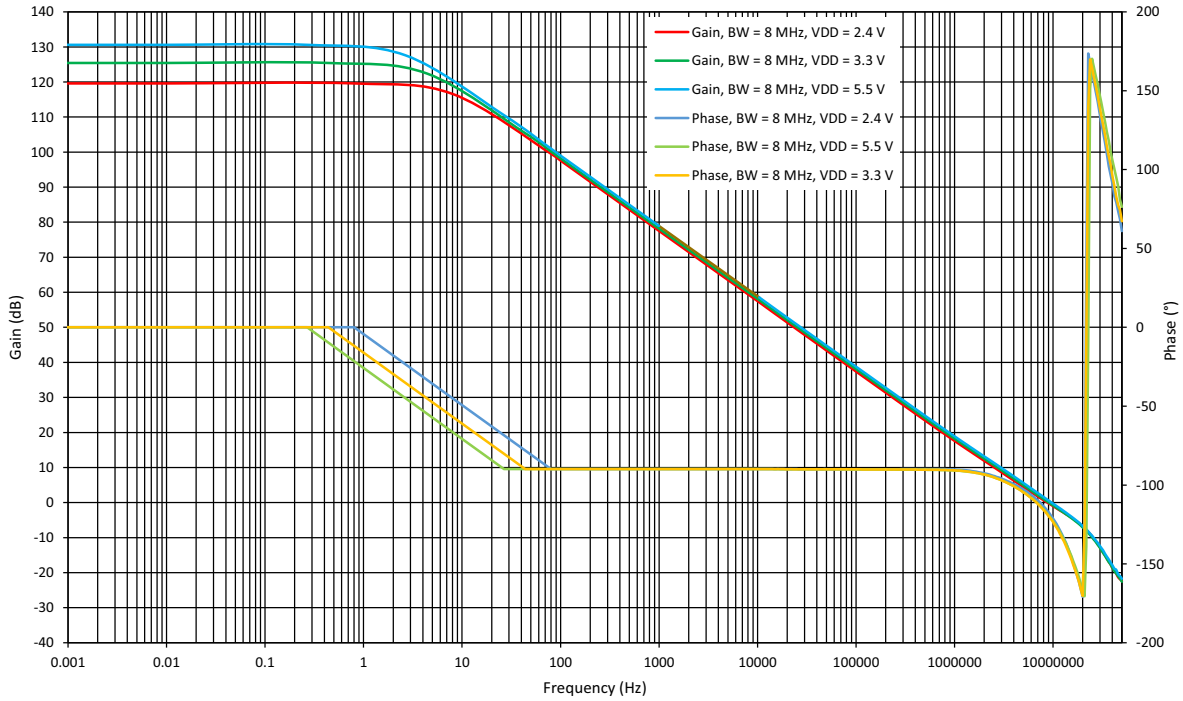


Figure 98. OA1 Open Loop Gain and Phase vs. Frequency for BW = 8 MHz

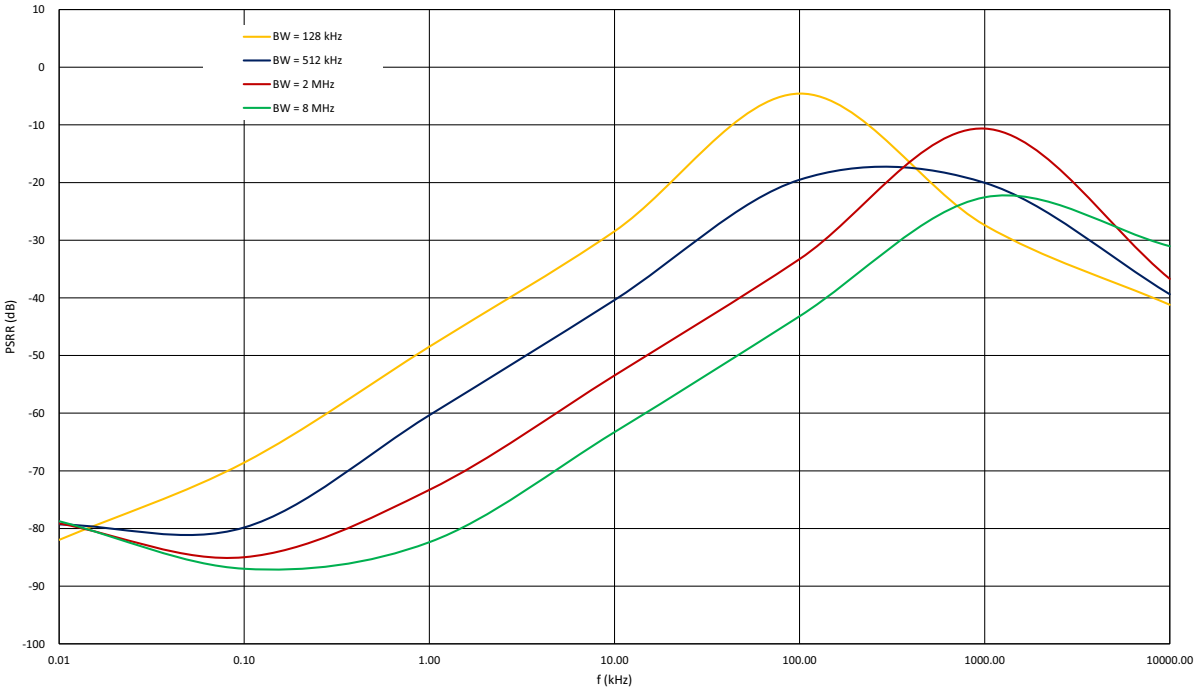


Figure 99. PSRR vs. Frequency V_{DD} = 2.4 V to 5.5 V

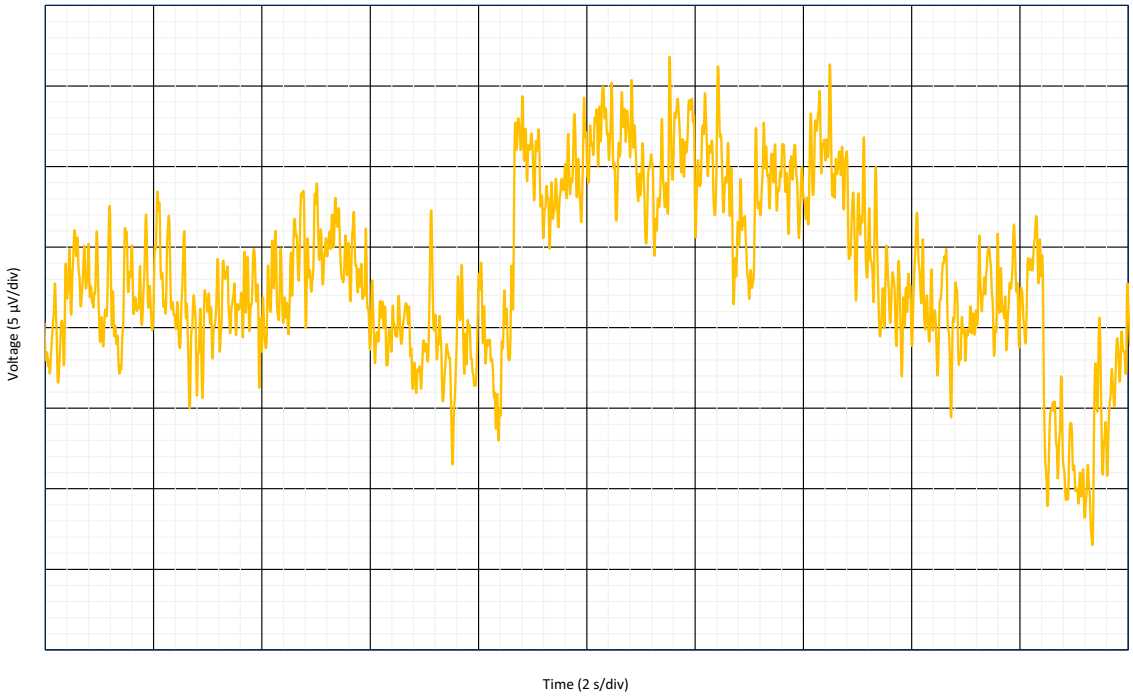


Figure 100. 0.1 Hz to 10 Hz Noise, BW = 128 kHz

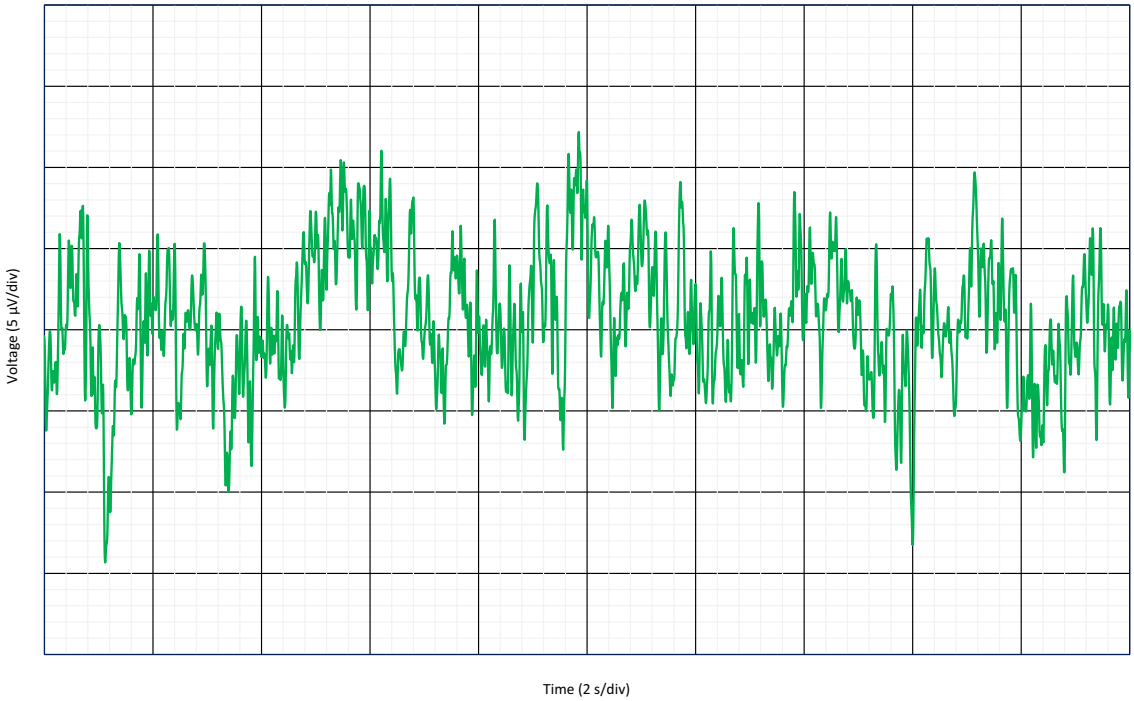


Figure 101. 0.1 Hz to 10 Hz Noise, BW = 512 kHz

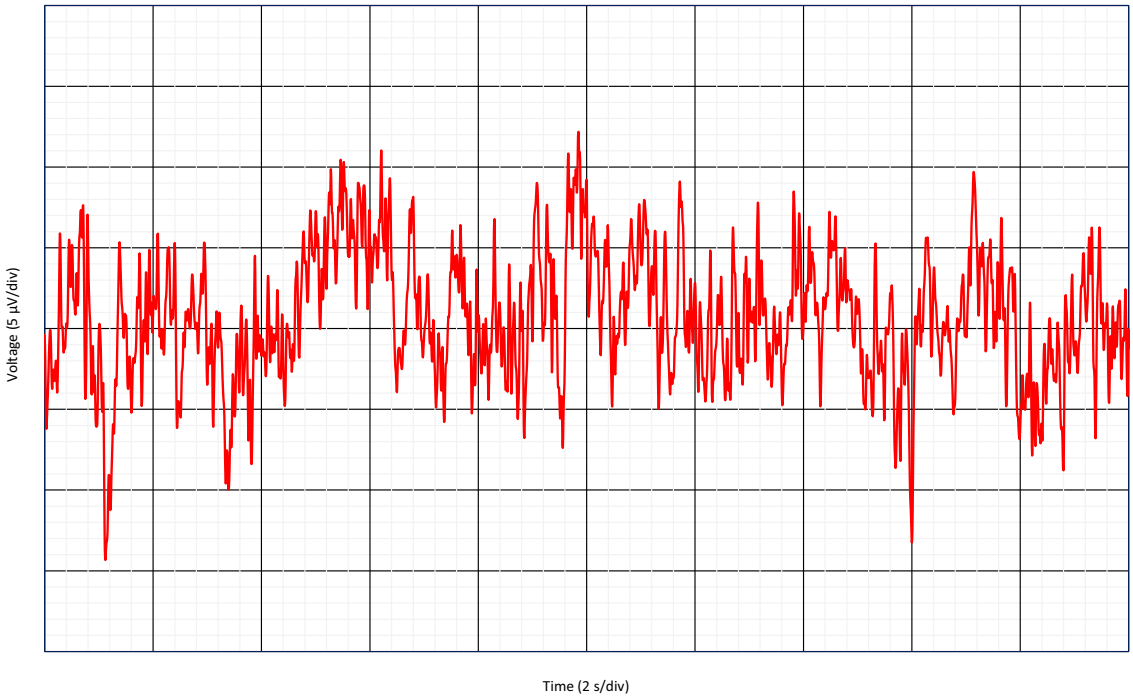


Figure 102. 0.1 Hz to 10 Hz Noise, BW = 2 MHz

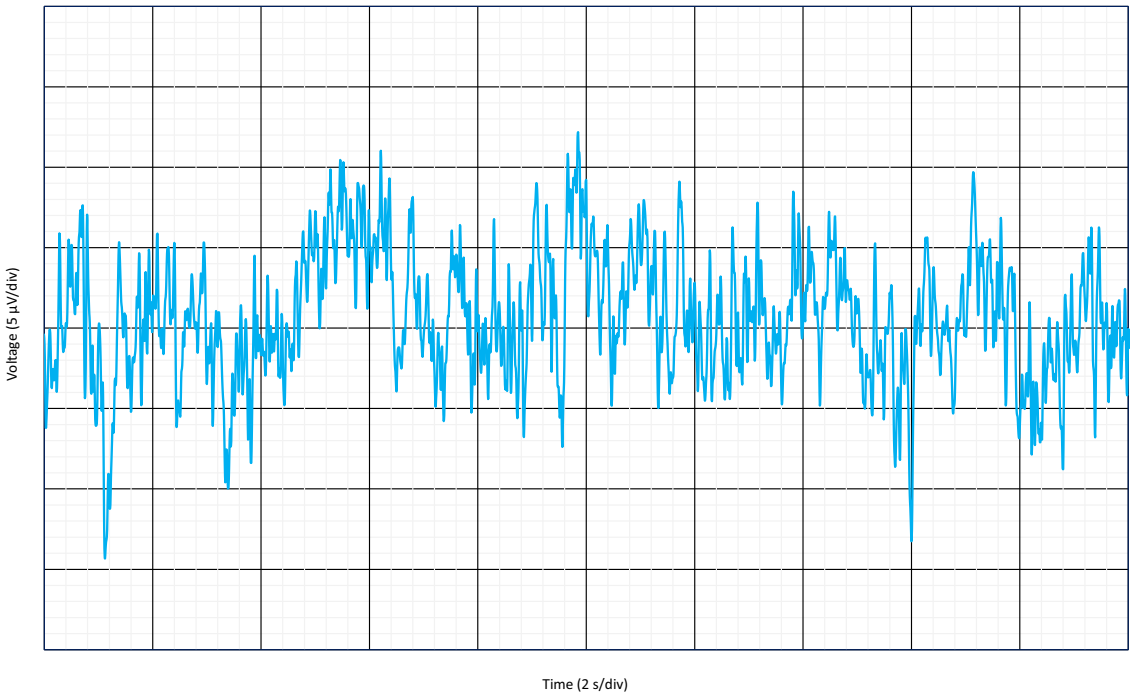


Figure 103. 0.1 Hz to 10 Hz Noise, BW = 8 MHz

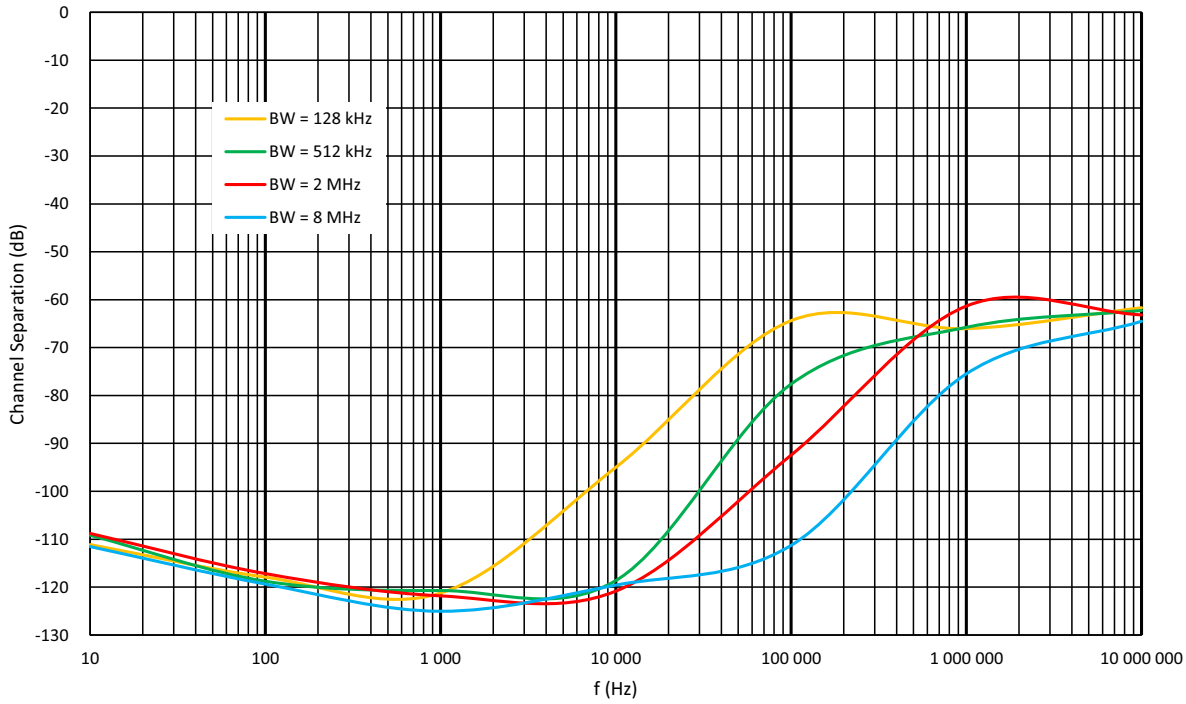


Figure 104. Channel Separation vs. Frequency

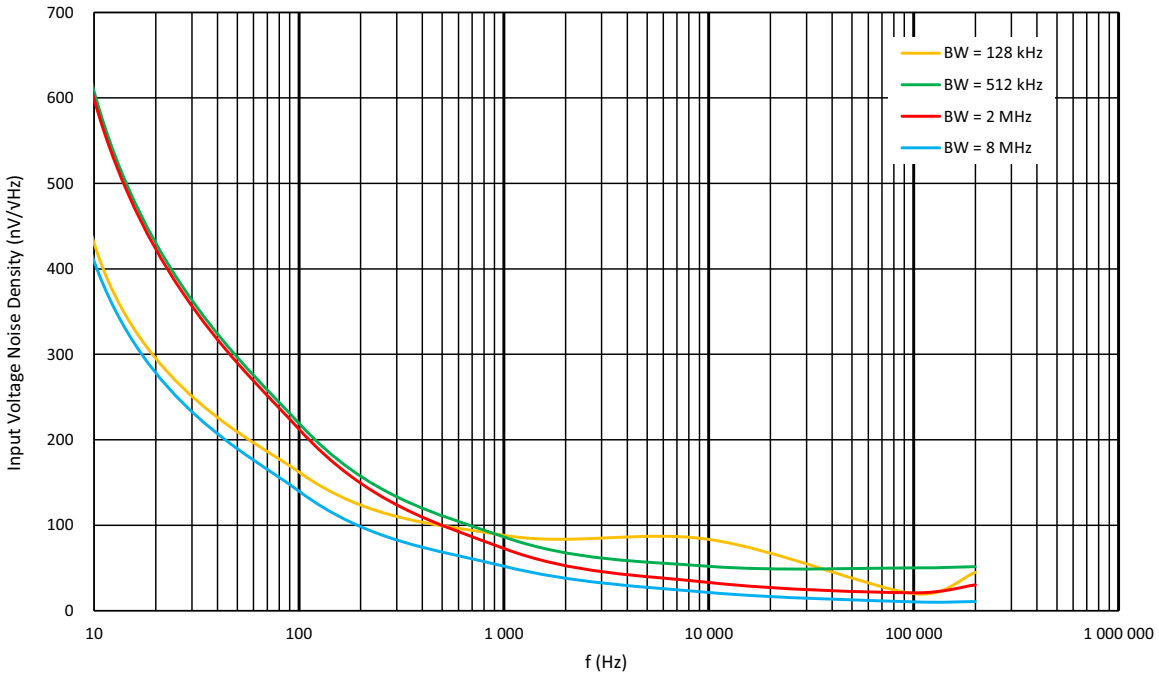


Figure 105. Op Ampx Noise Voltage Density vs. Frequency

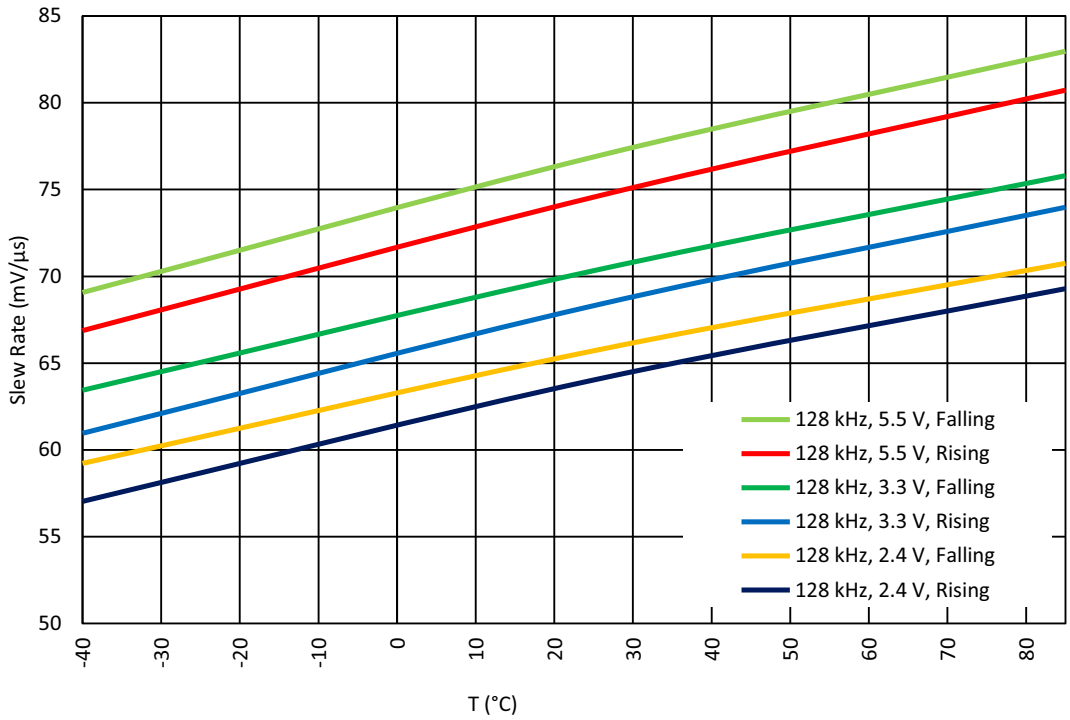


Figure 106. Slew Rate vs. Ambient Temperature G = 1 V/V; R_L = 50 kΩ for BW = 128 kHz

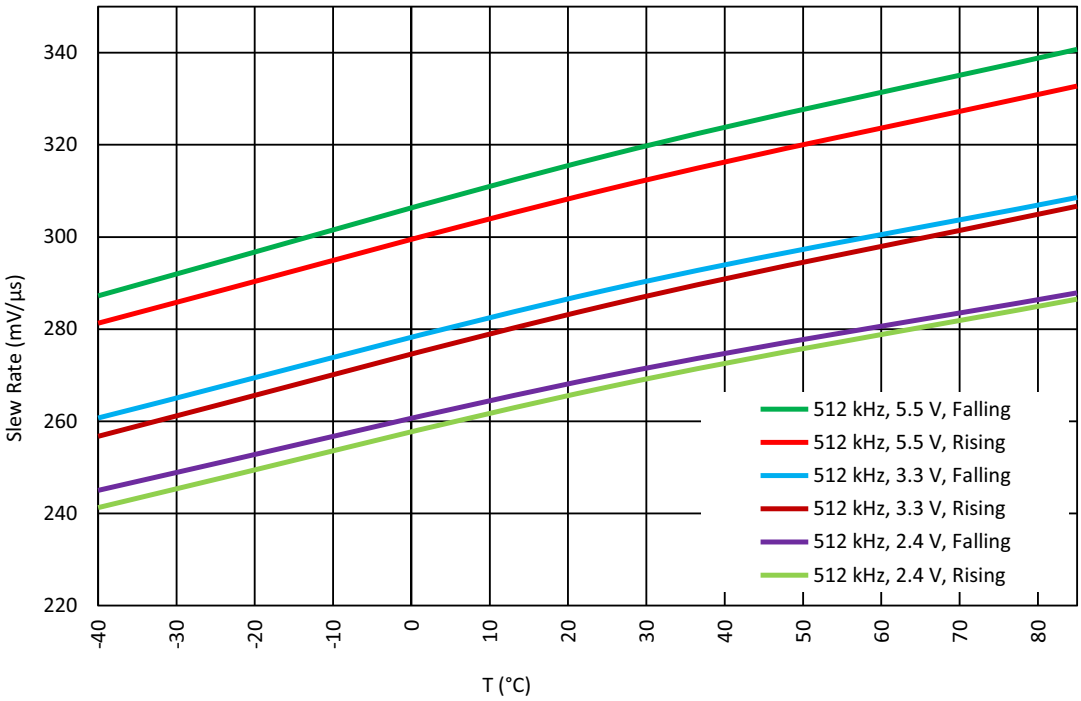


Figure 107. Slew Rate vs. Ambient Temperature G = 1 V/V; R_L = 50 kΩ for BW = 512 kHz

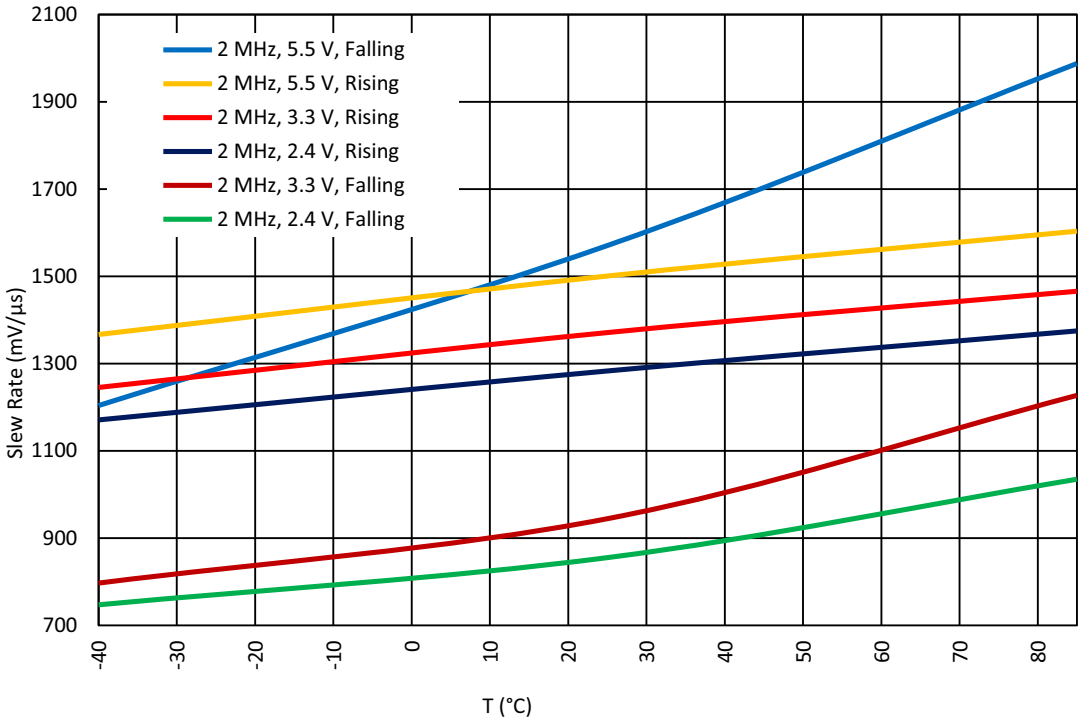


Figure 108. Slew Rate vs. Ambient Temperature G = 1 V/V; R_L = 50 kΩ for BW = 2 MHz

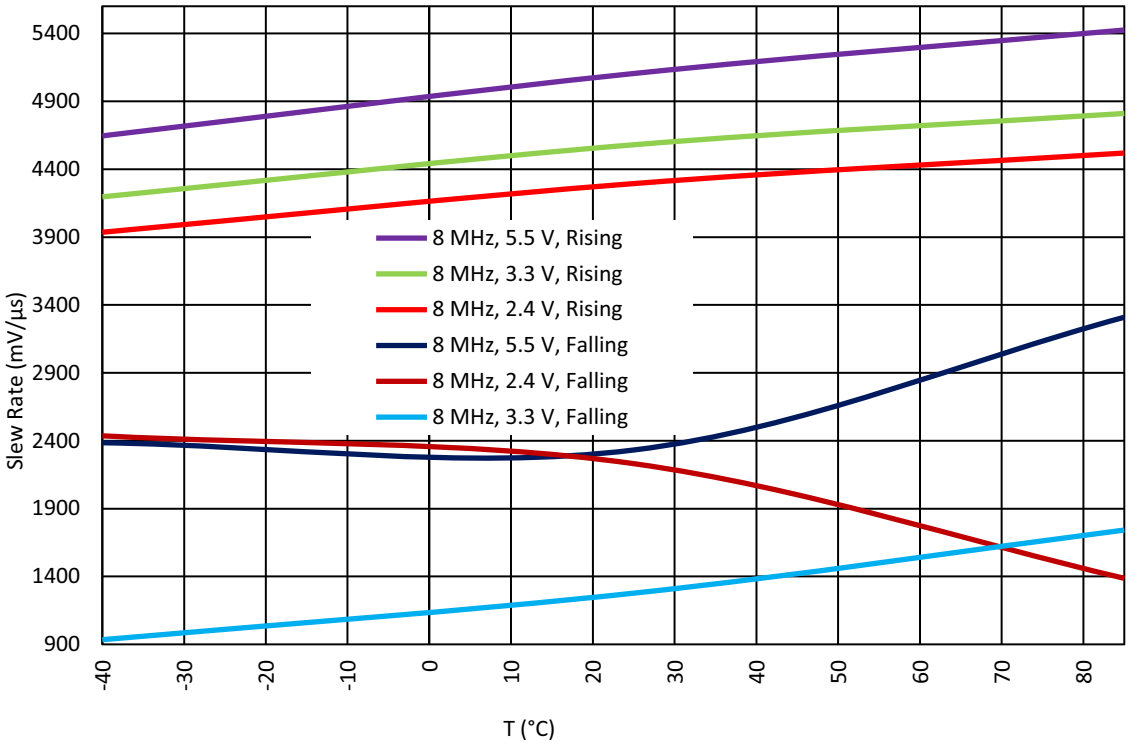


Figure 109. Slew Rate vs. Ambient Temperature G = 1 V/V; R_L = 50 kΩ for BW = 8 MHz

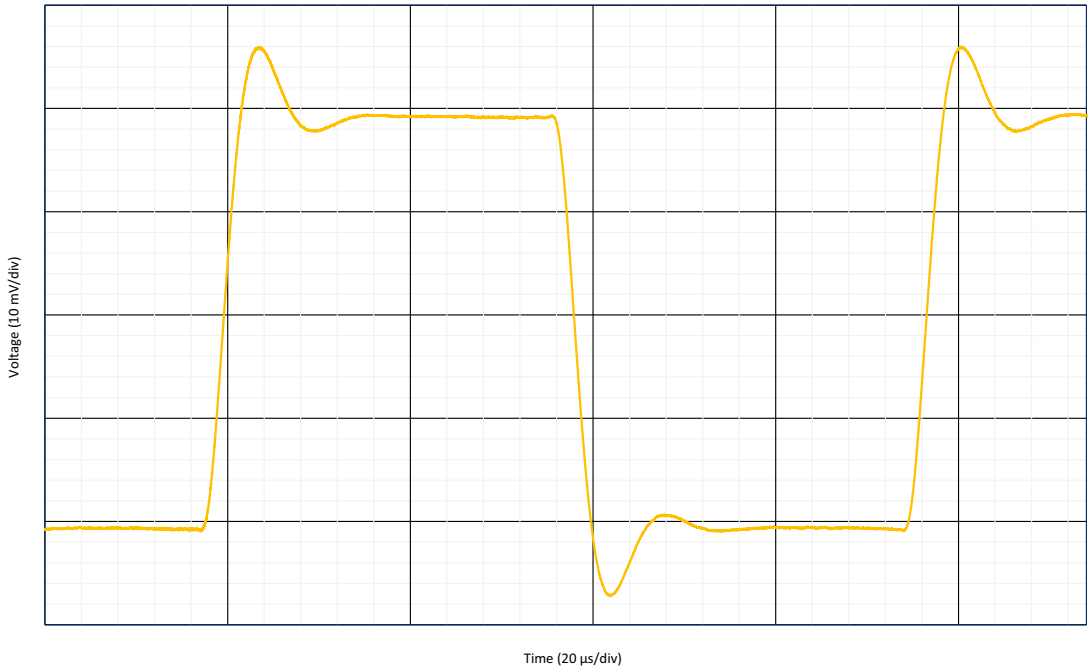


Figure 110. Small Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

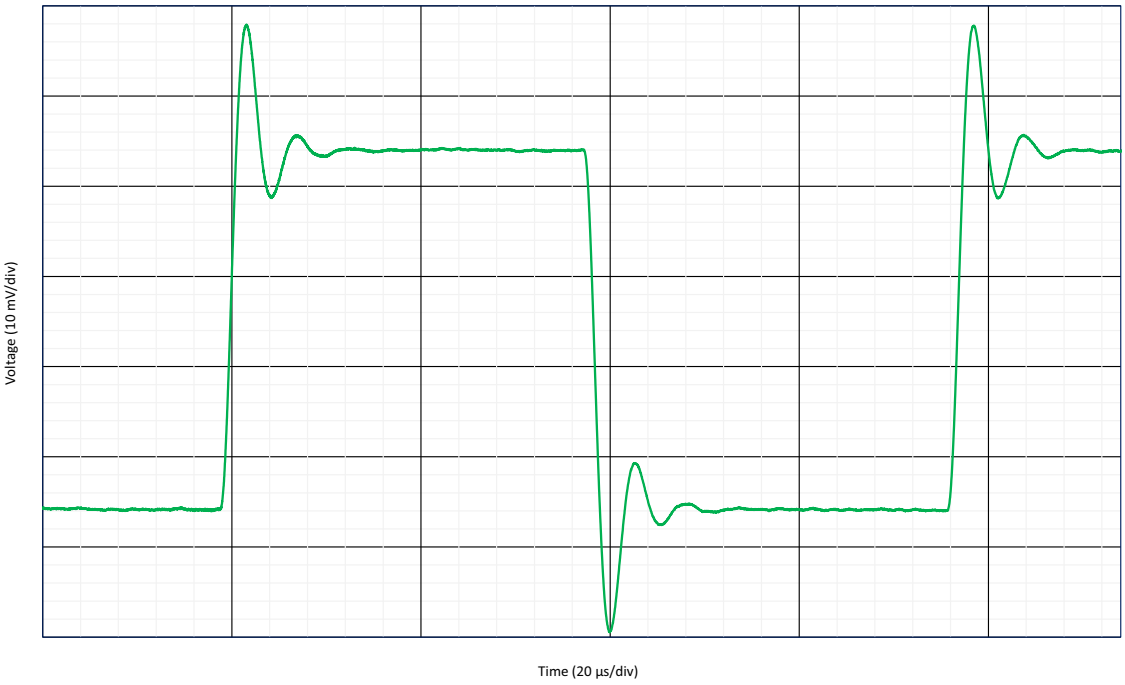


Figure 111. Small Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

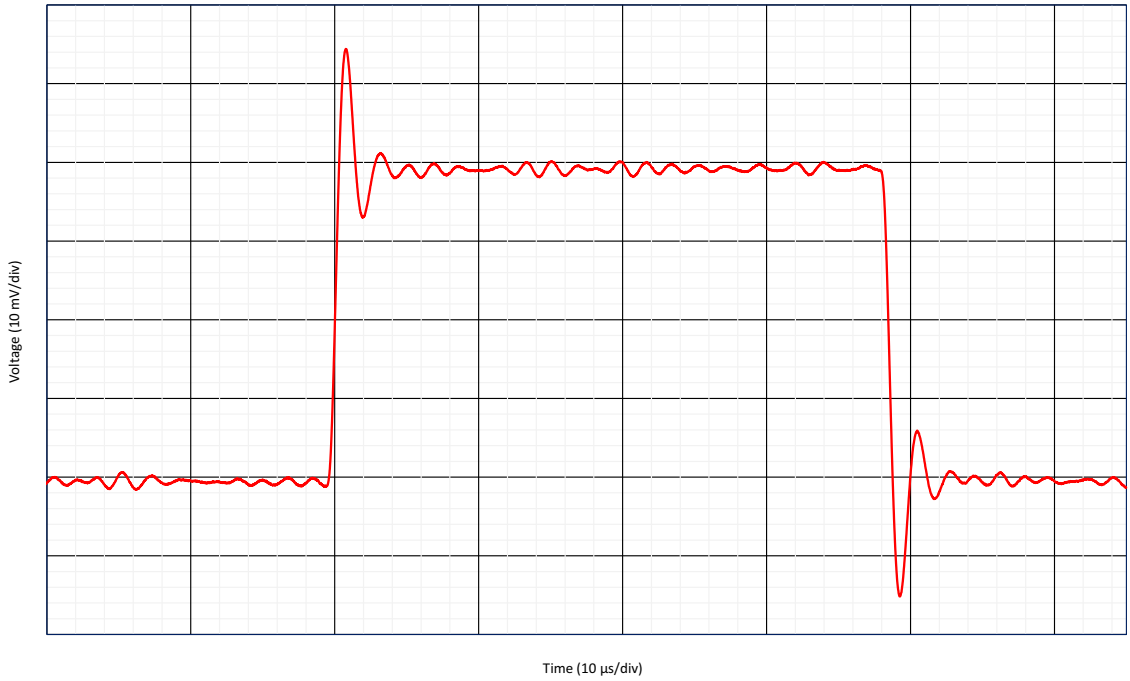


Figure 112. Small Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

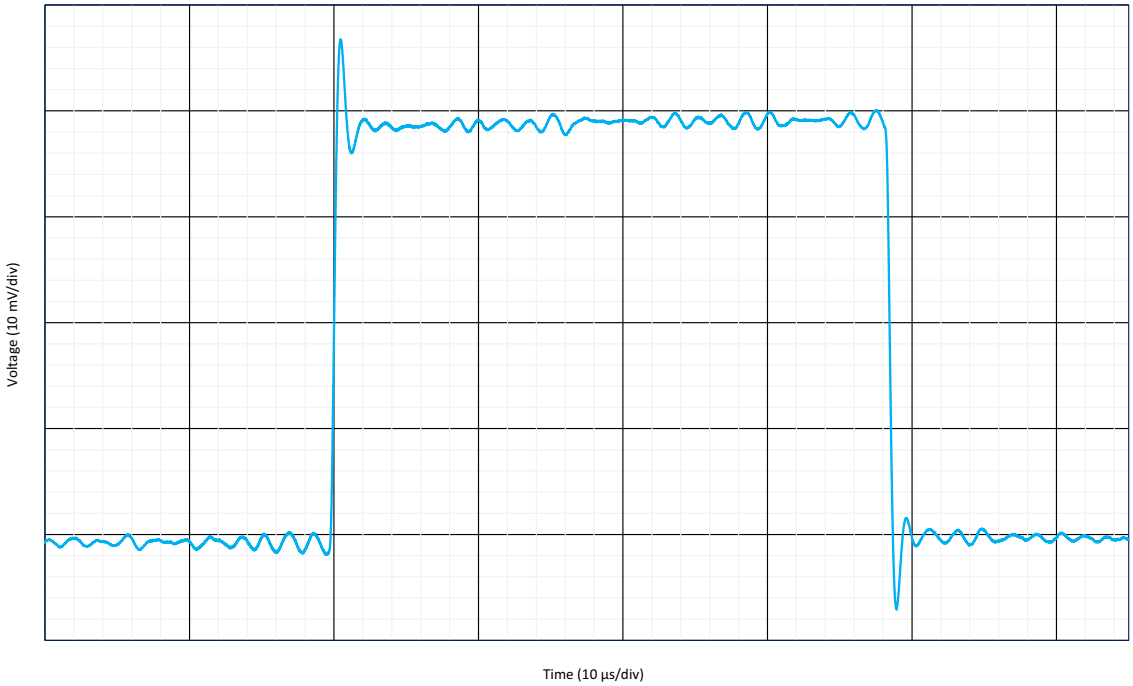


Figure 113. Small Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

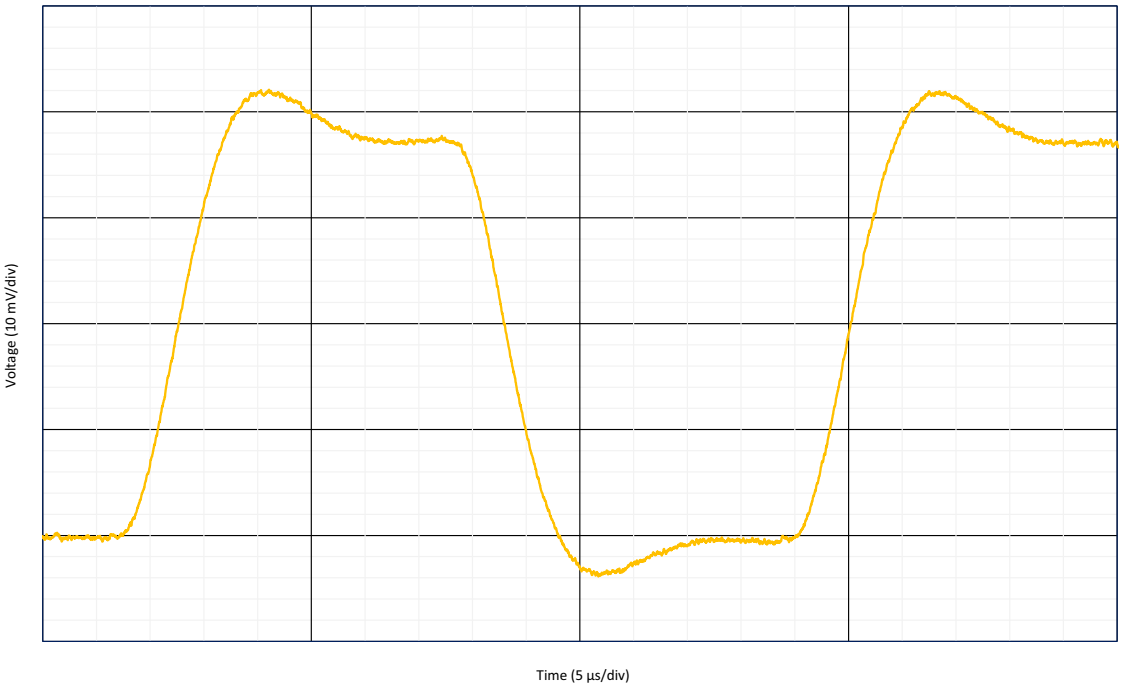


Figure 114. Small Signal Non-Inverting Step Response G = 1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

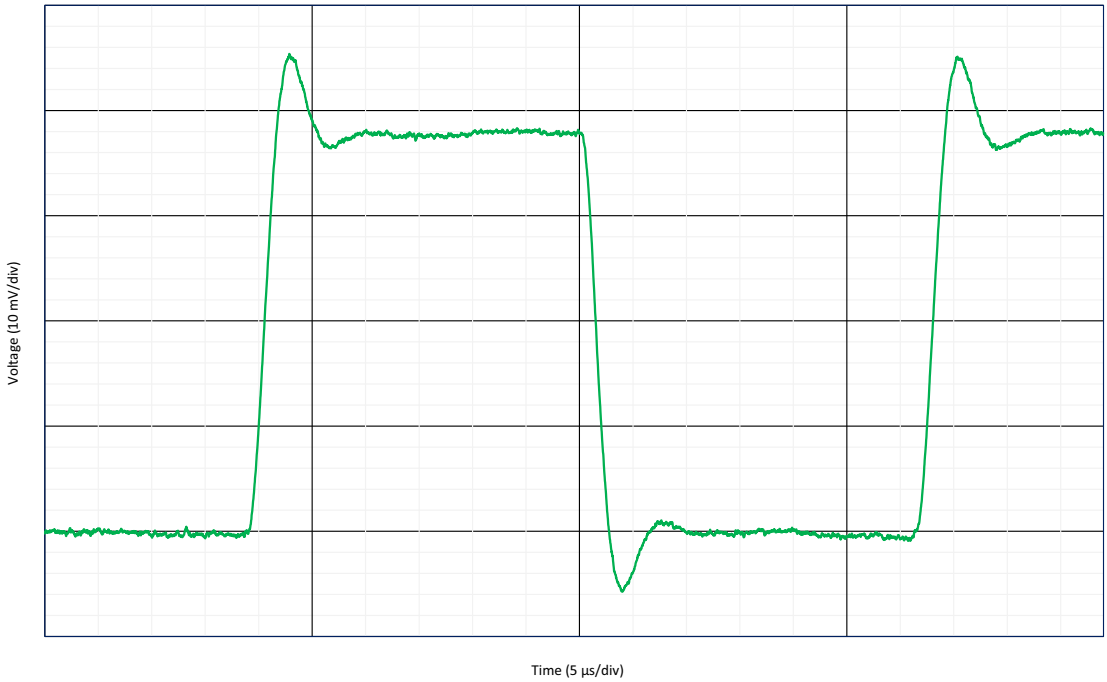


Figure 115. Small Signal Non-Inverting Step Response G = 1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

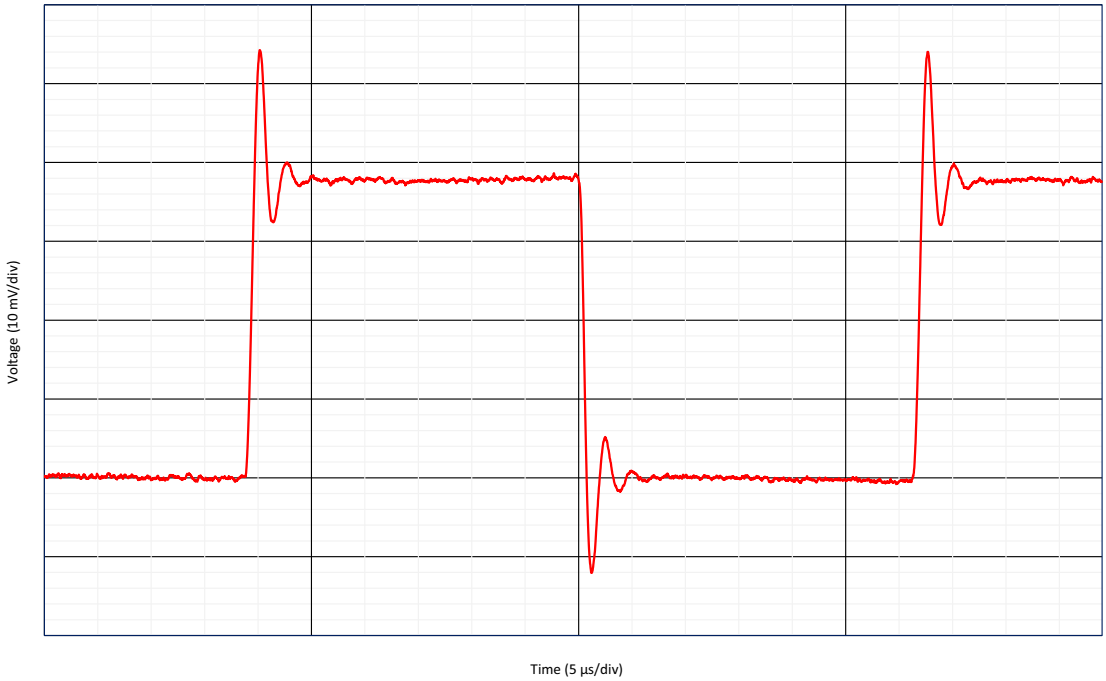


Figure 116. Small Signal Non-Inverting Step Response G = 1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

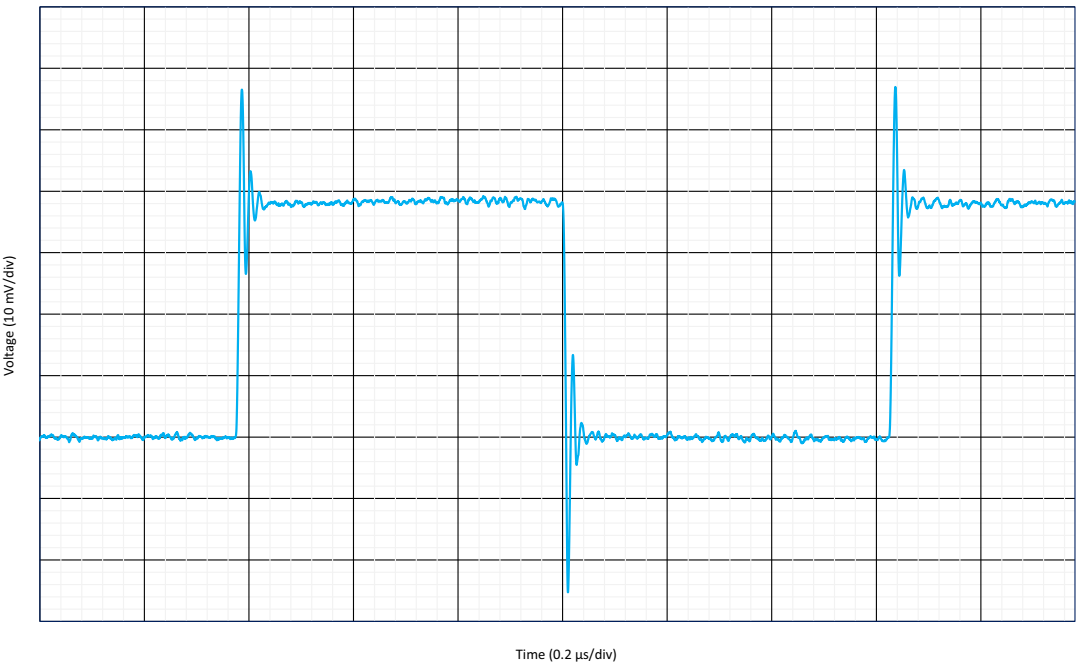


Figure 117. Small Signal Non-Inverting Step Response G = 1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

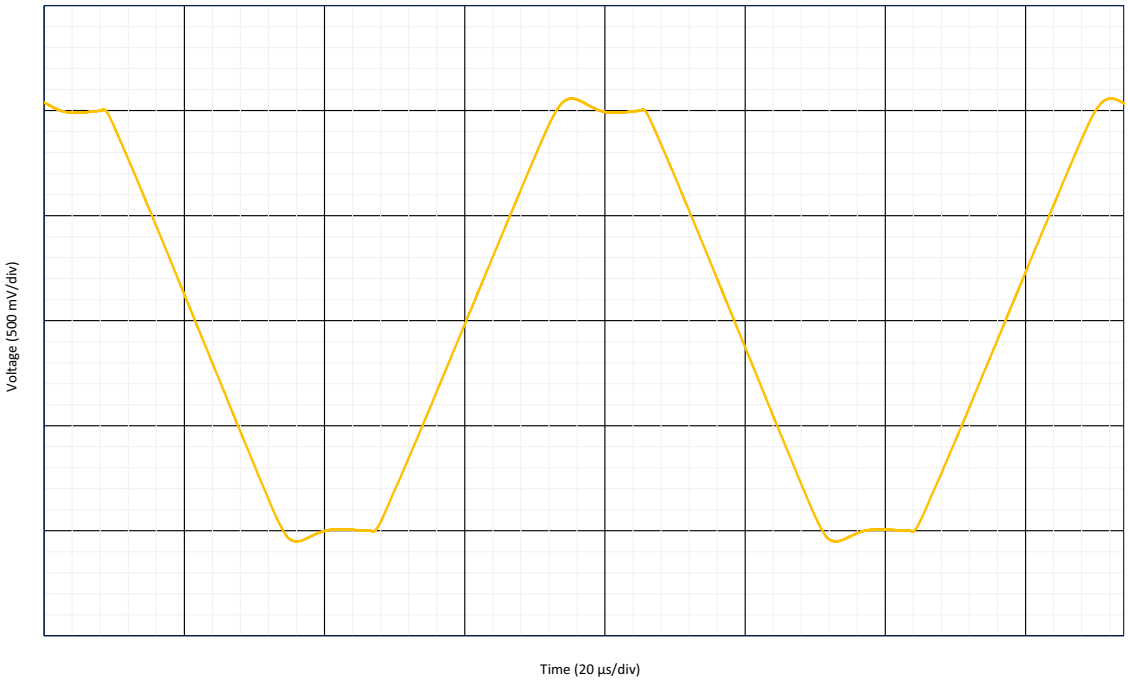


Figure 118. Large Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 80 pF, BW = 128 kHz

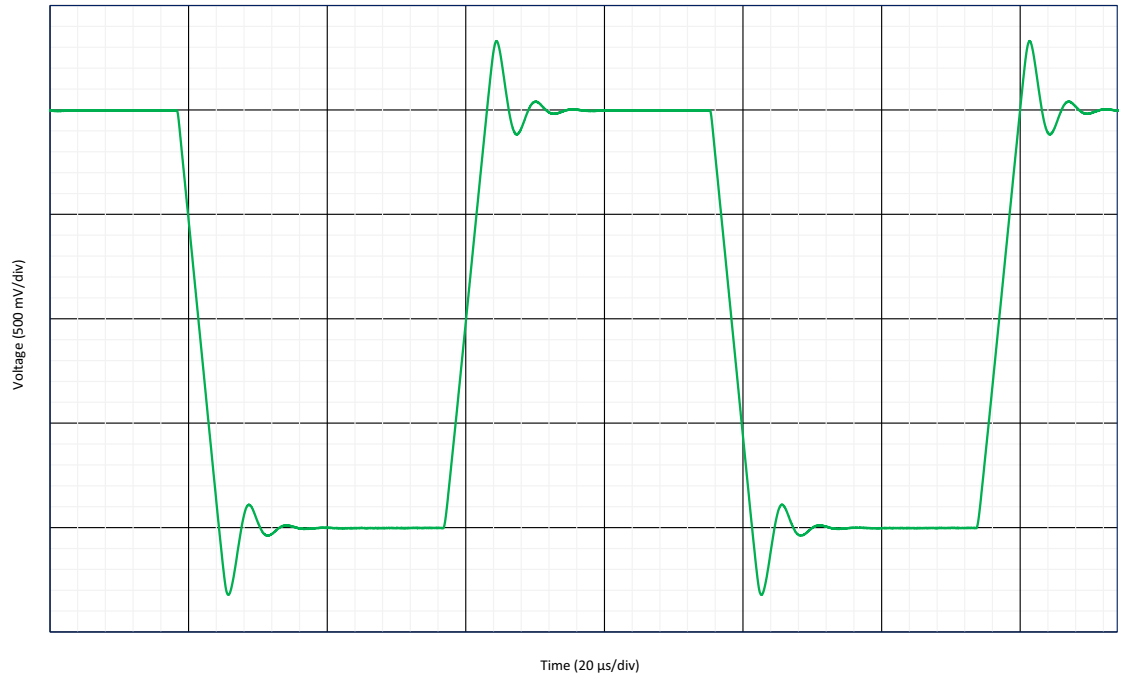


Figure 119. Large Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 80 pF, BW = 512 kHz

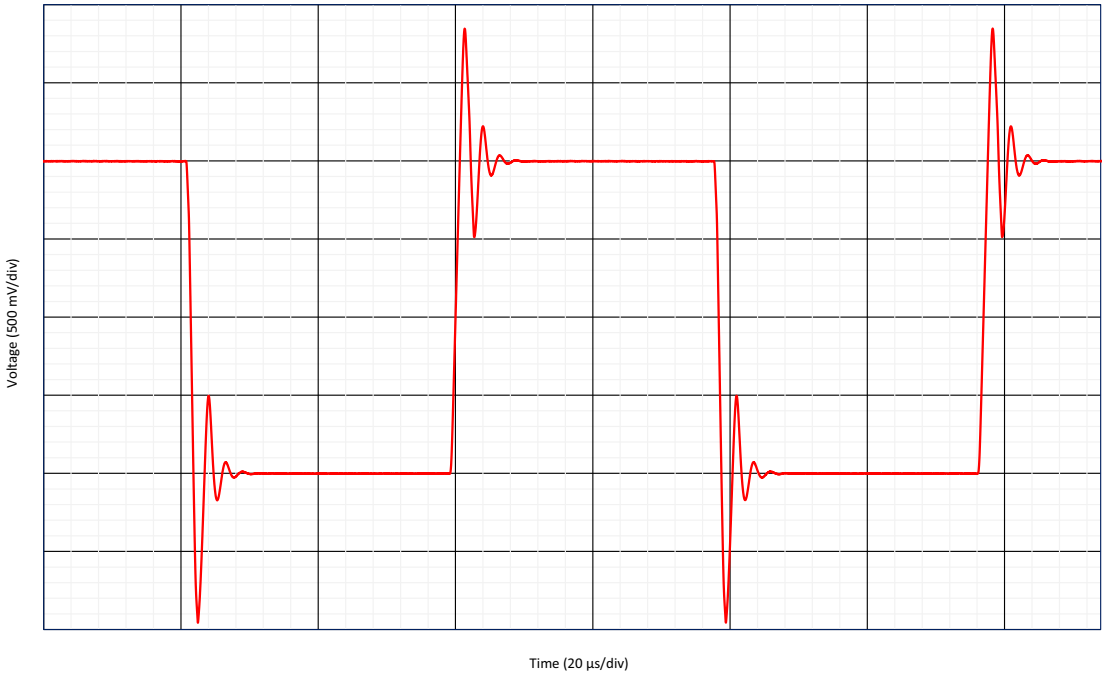


Figure 120. Large Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 80 pF, BW = 2 MHz

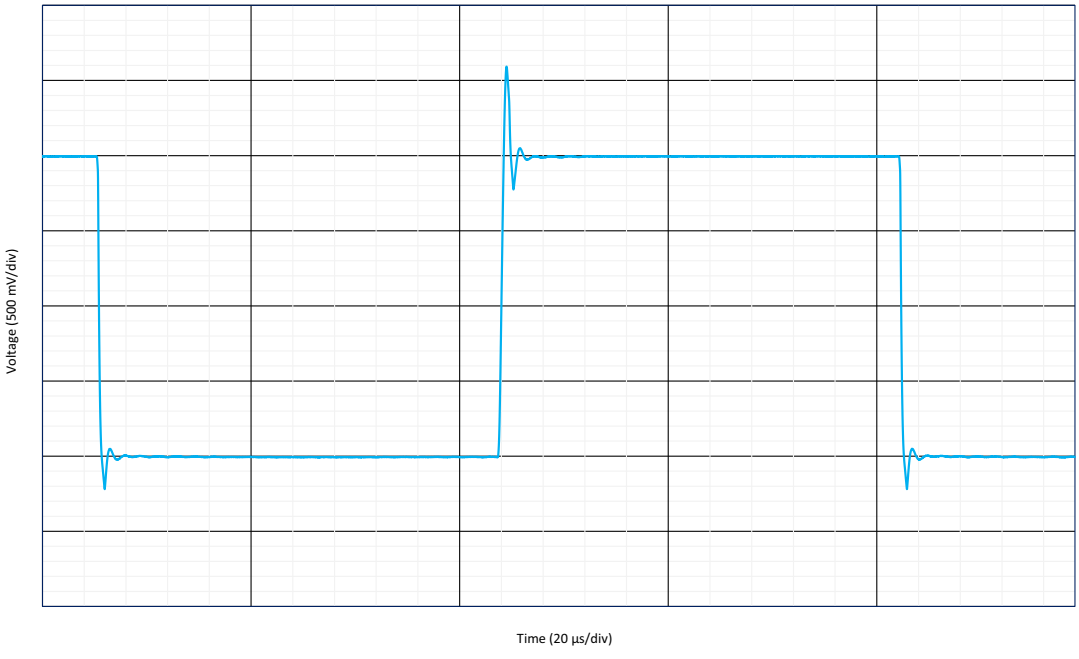


Figure 121. Large Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 80 pF, BW = 8 MHz

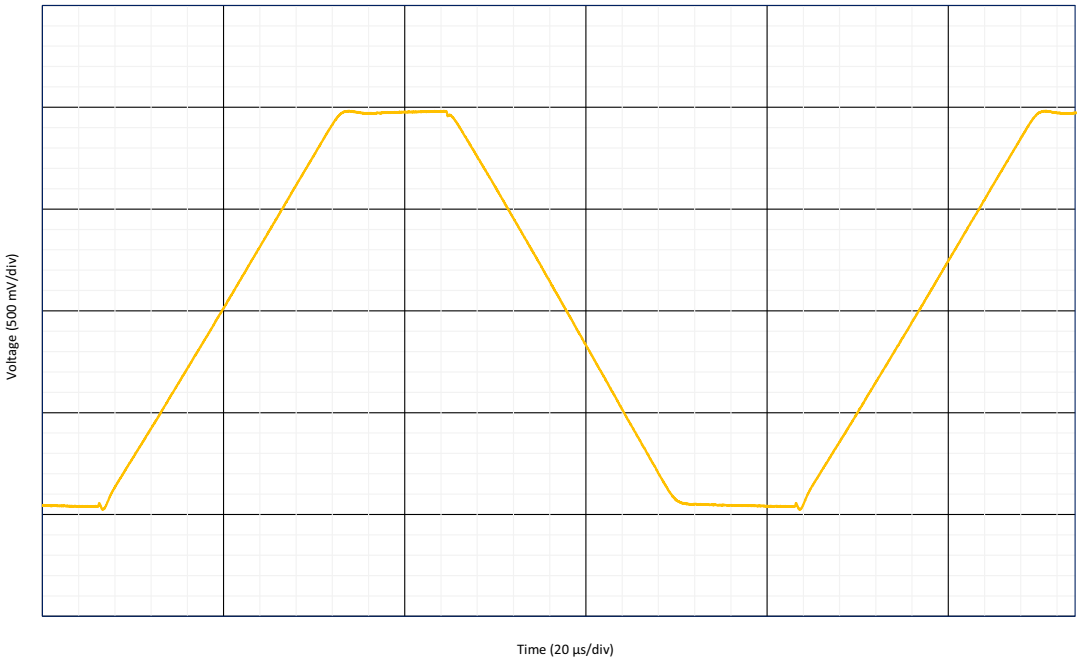


Figure 122. Large Signal Non-Inverting Step Response G = 1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

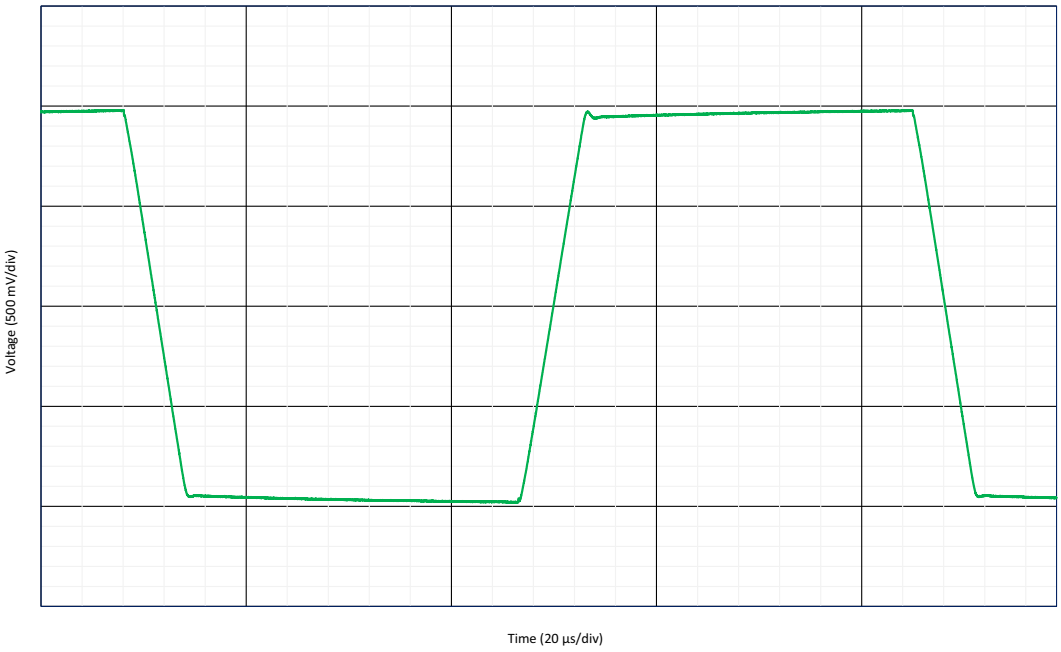


Figure 123. Large Signal Non-Inverting Step Response G = 1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

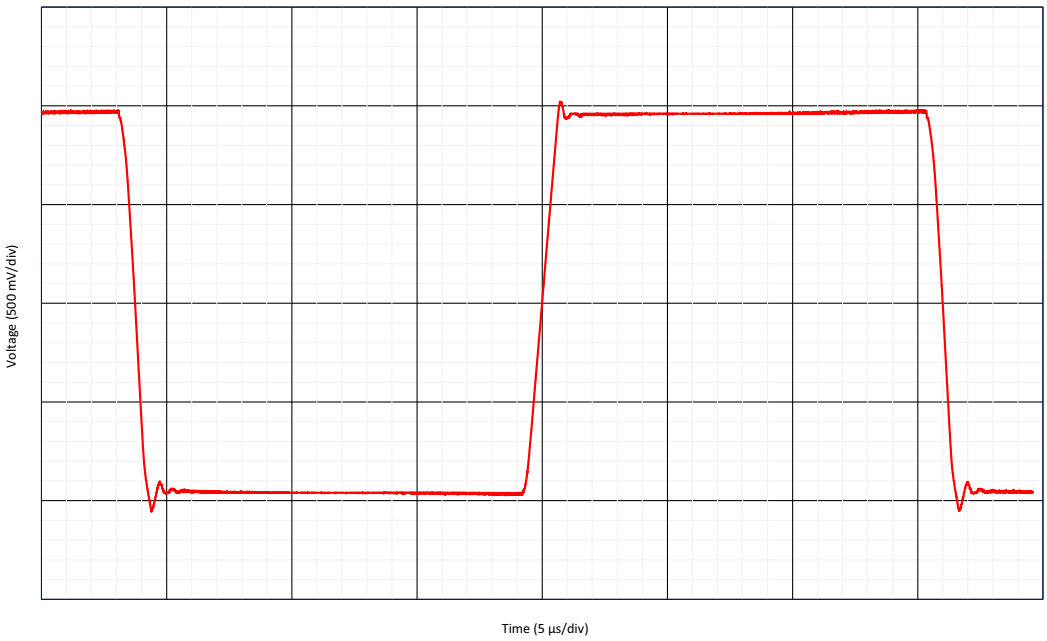


Figure 124. Large Signal Non-Inverting Step Response G = 1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

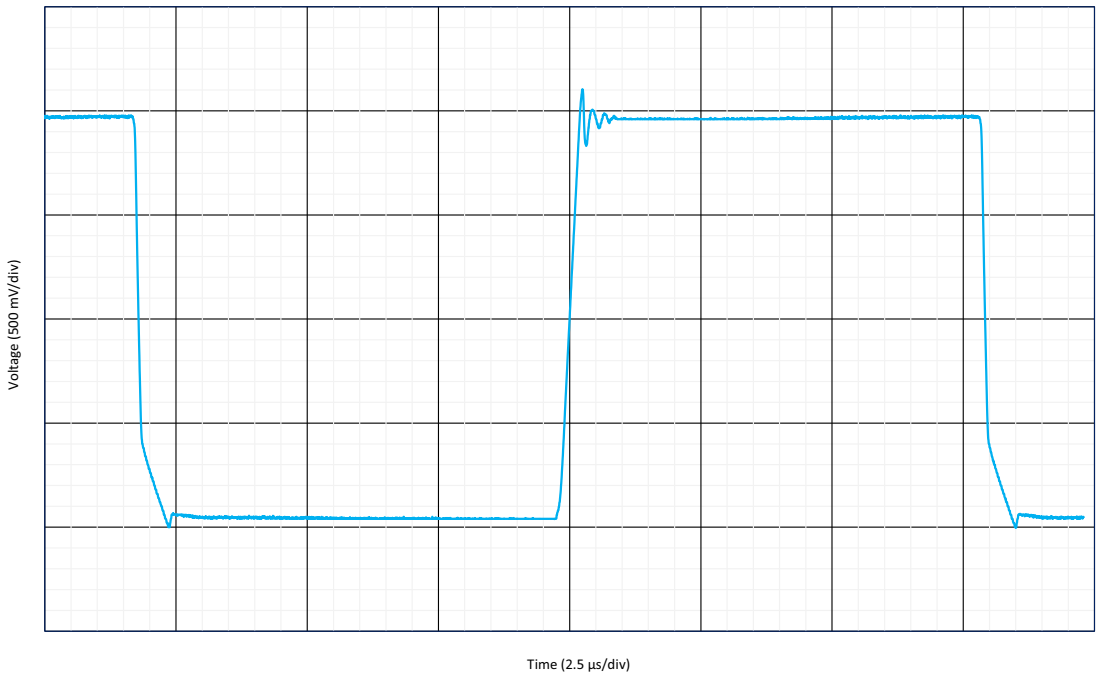


Figure 125. Large Signal Non-Inverting Step Response G = 1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

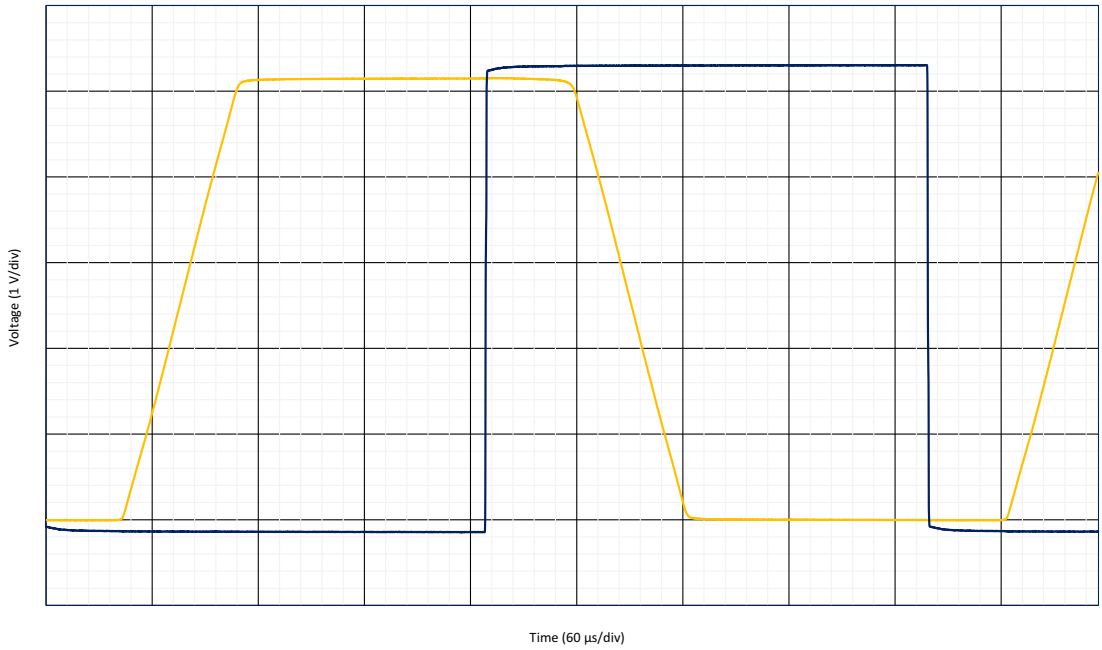


Figure 126. Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

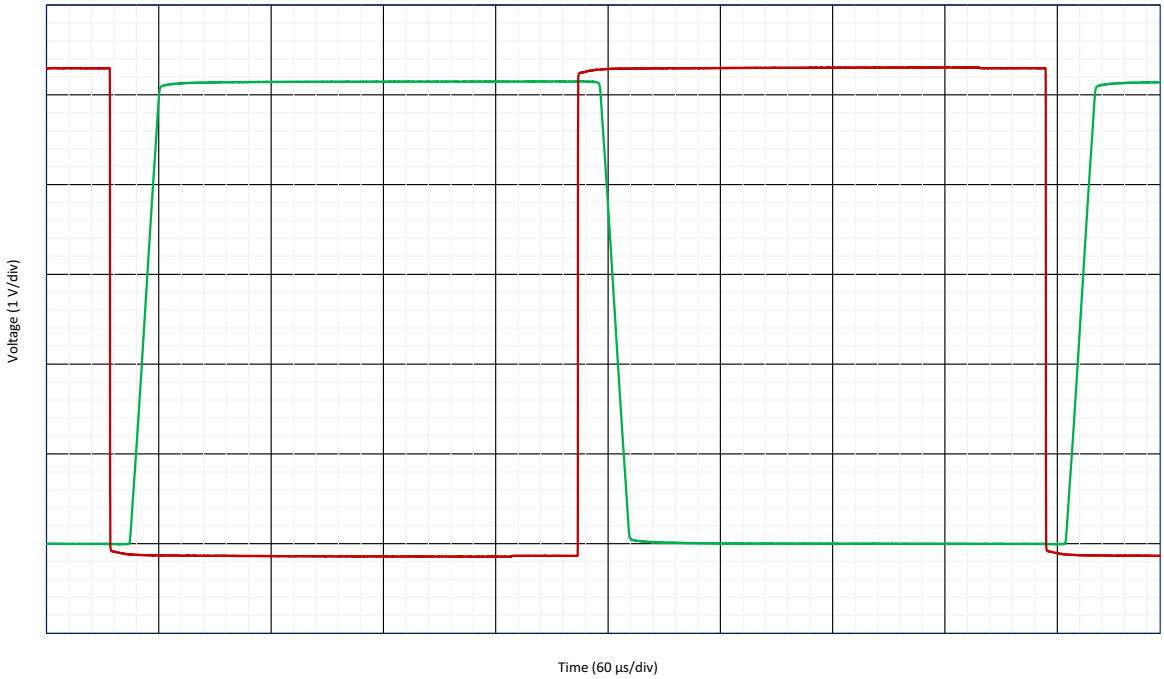


Figure 127. Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

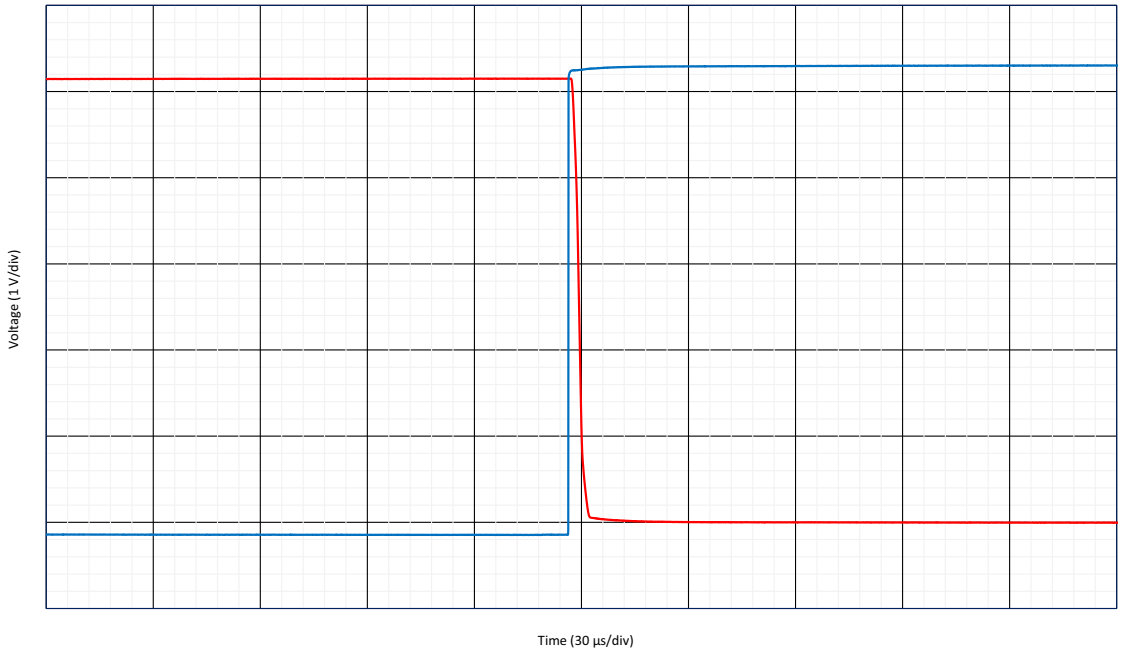


Figure 128. Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

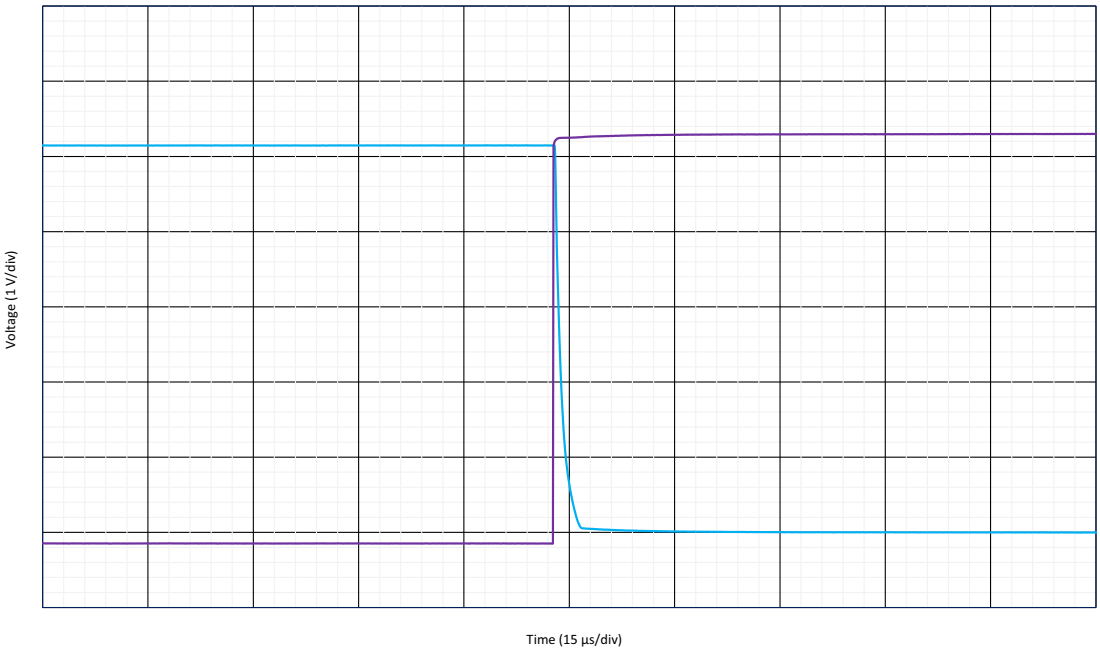


Figure 129. Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

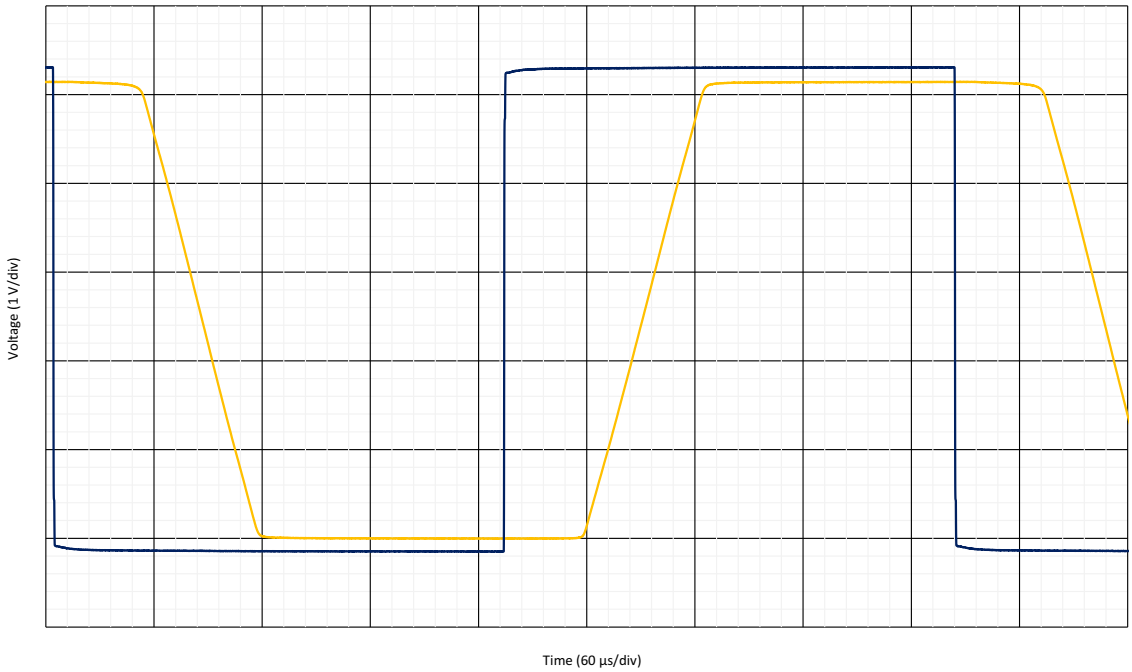


Figure 130. Non-Inverting Overload Recovery G = 1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

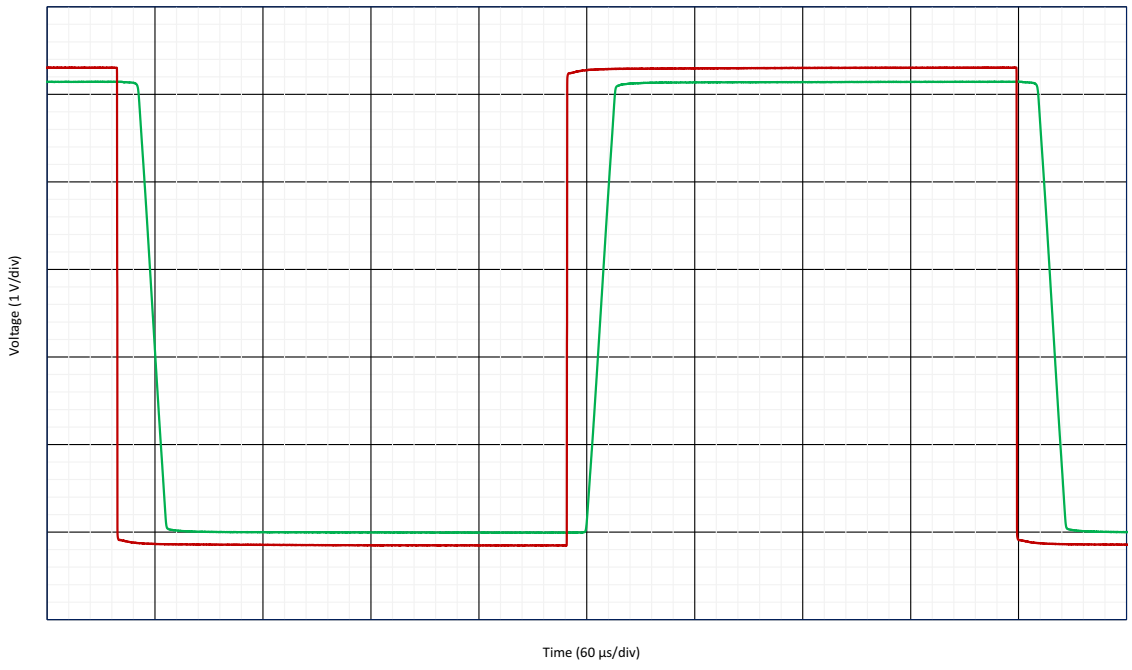


Figure 131. Non-Inverting Overload Recovery G = 1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

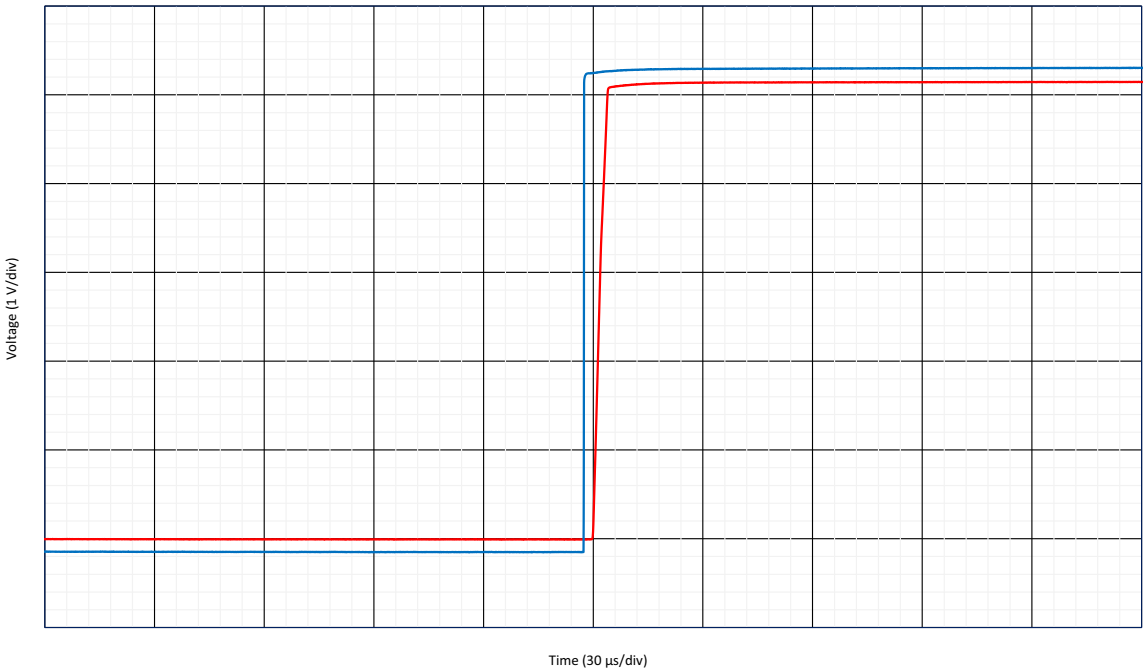


Figure 132. Non-Inverting Overload Recovery G = 1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

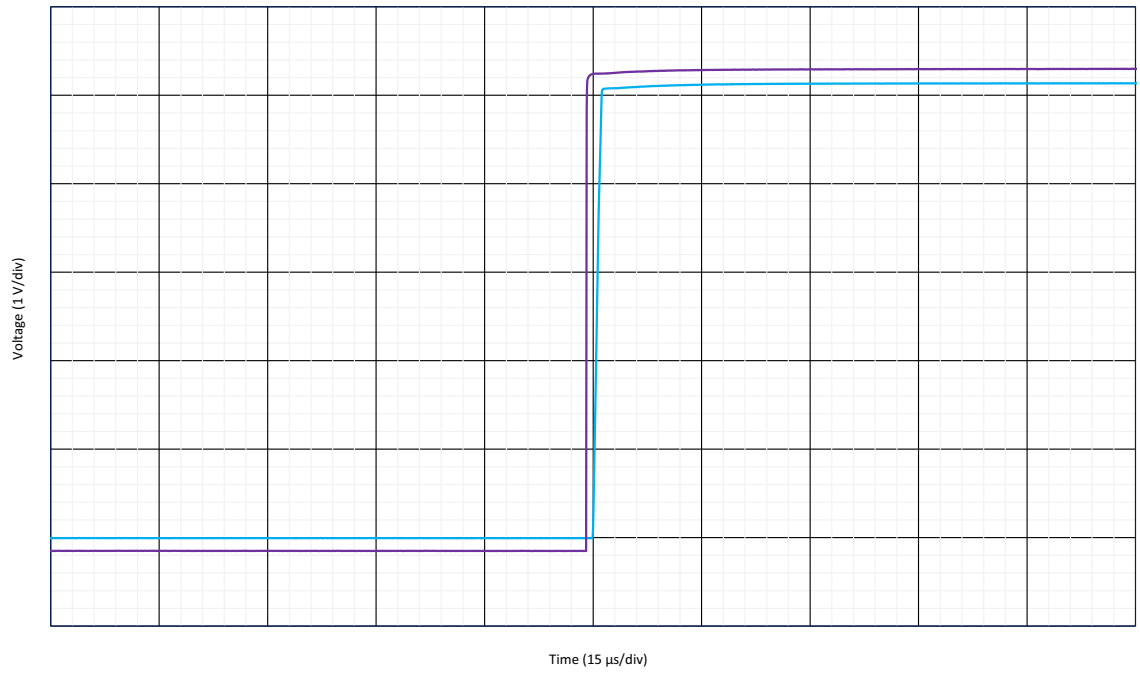


Figure 133. Non-Inverting Overload Recovery G = 1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

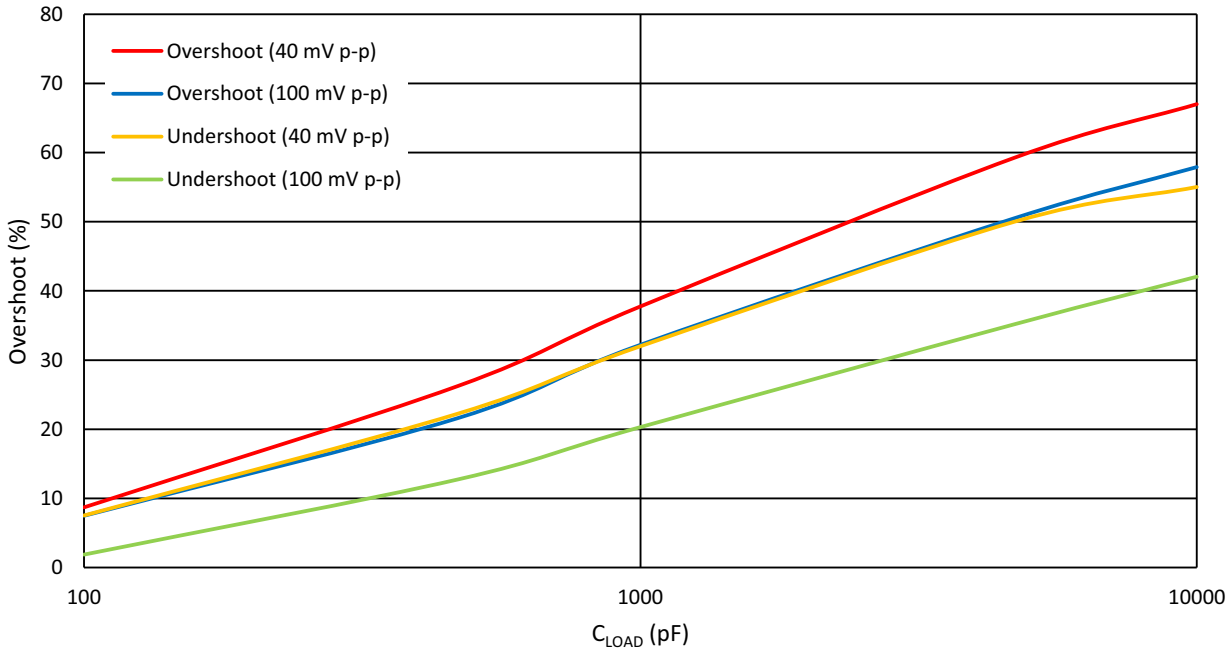


Figure 134. Small Signal Overshoot vs. Capacitive Load V_{DD} = 3.3 V, G = 1 V/V, BW = 128 kHz

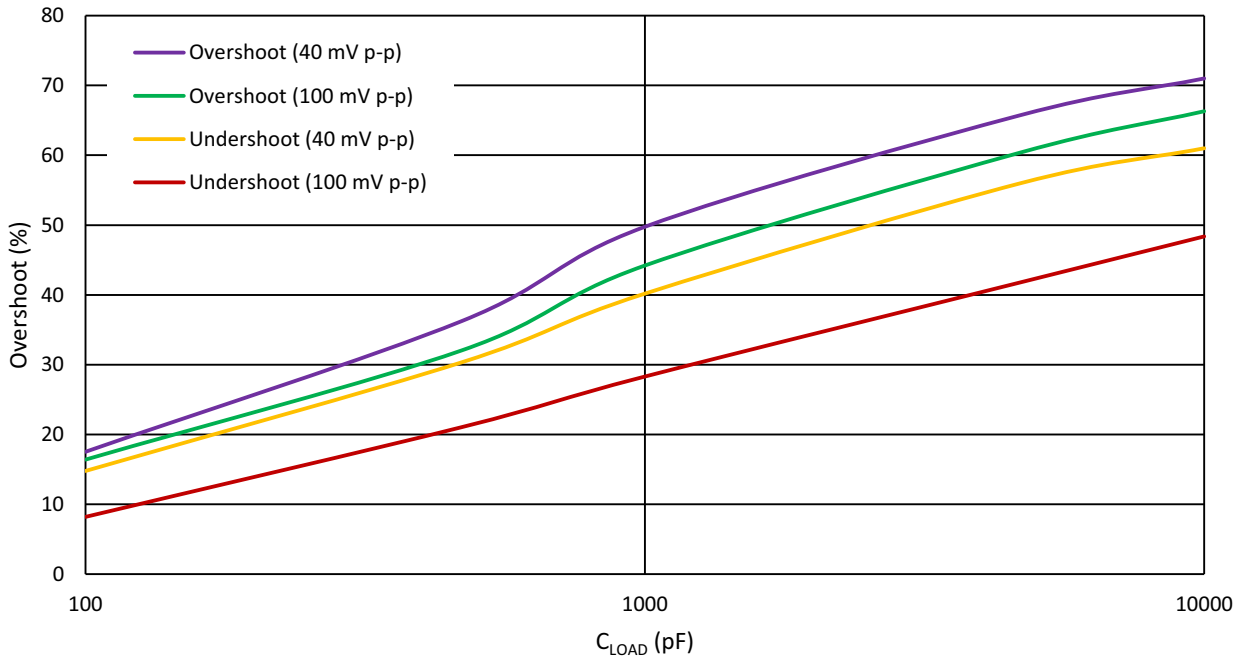


Figure 135. Small Signal Overshoot vs. Capacitive Load V_{DD} = 3.3 V, G = 1 V/V, BW = 512 kHz

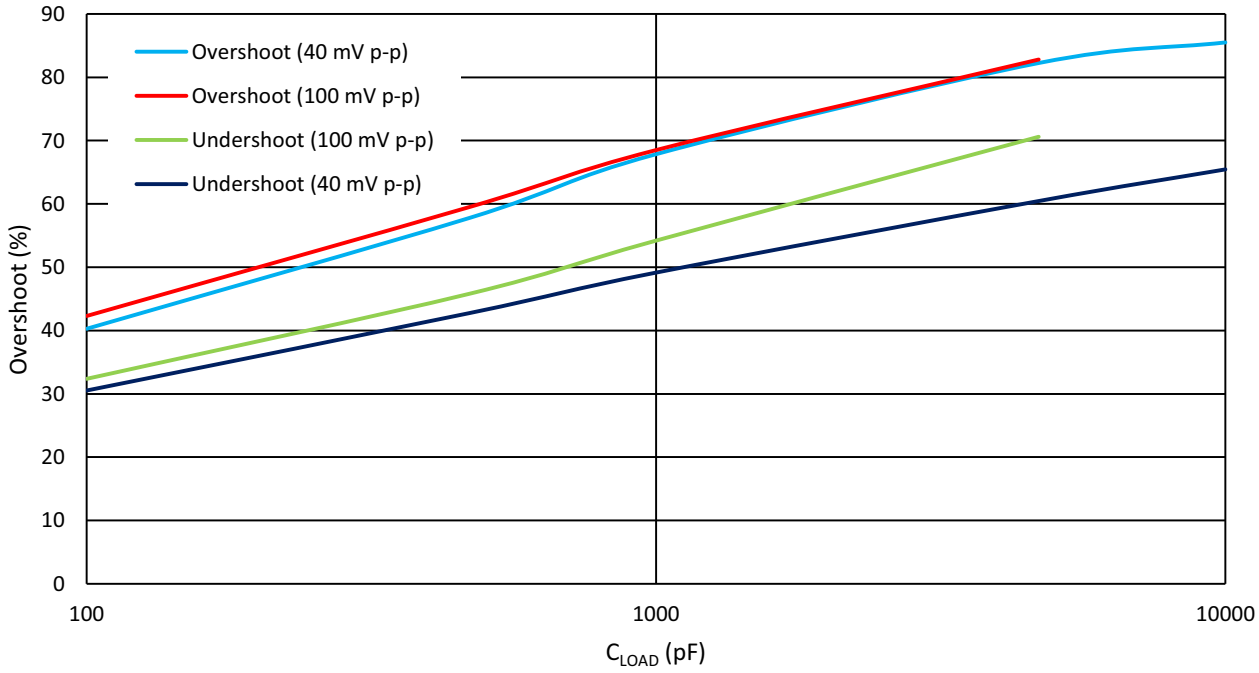


Figure 136. Small Signal Overshoot vs. Capacitive Load V_{DD} = 3.3 V, G = 1 V/V, BW = 2 MHz

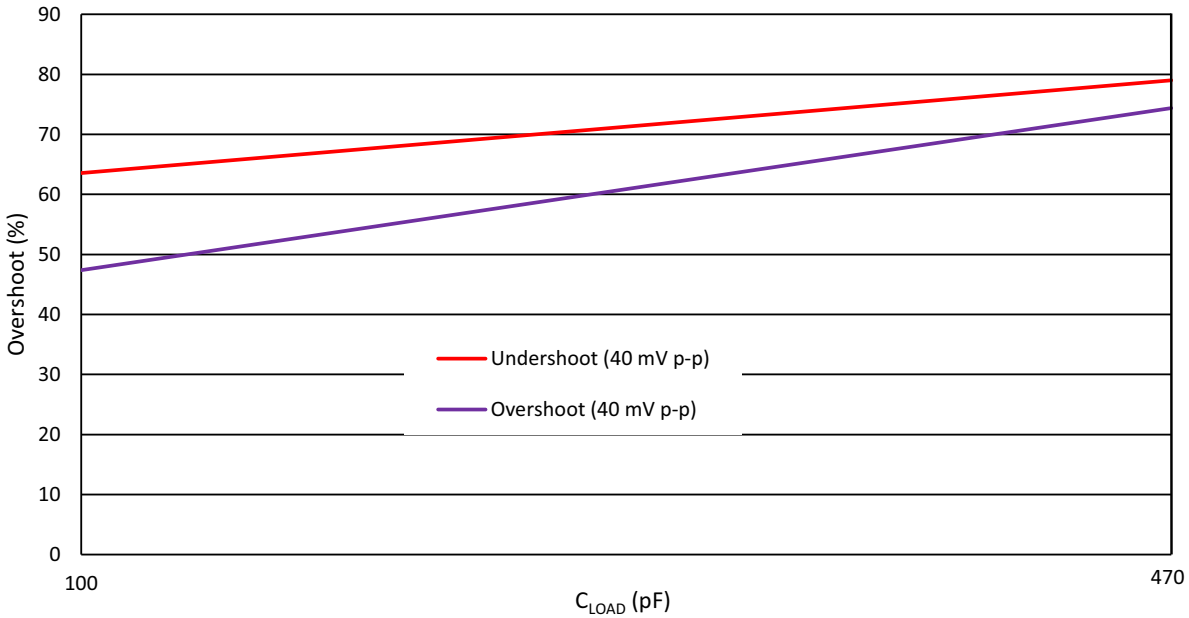


Figure 137. Small Signal Overshoot vs. Capacitive Load V_{DD} = 3.3 V, G = 1 V/V, BW = 8 MHz

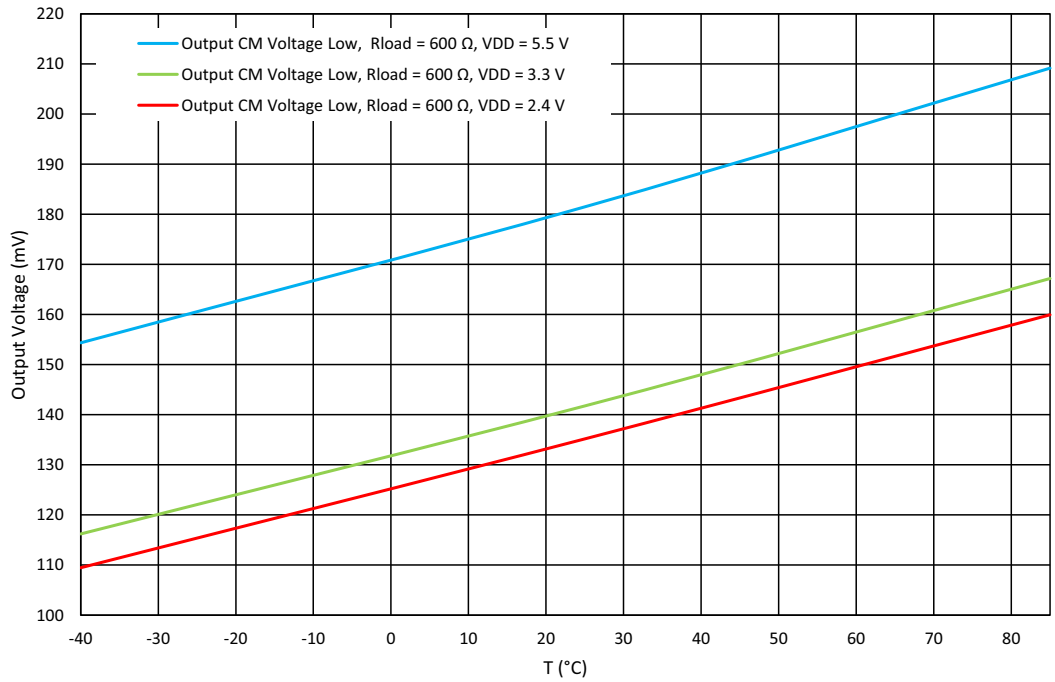


Figure 138. Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 128 kHz, R_{LOAD} = 600 Ω

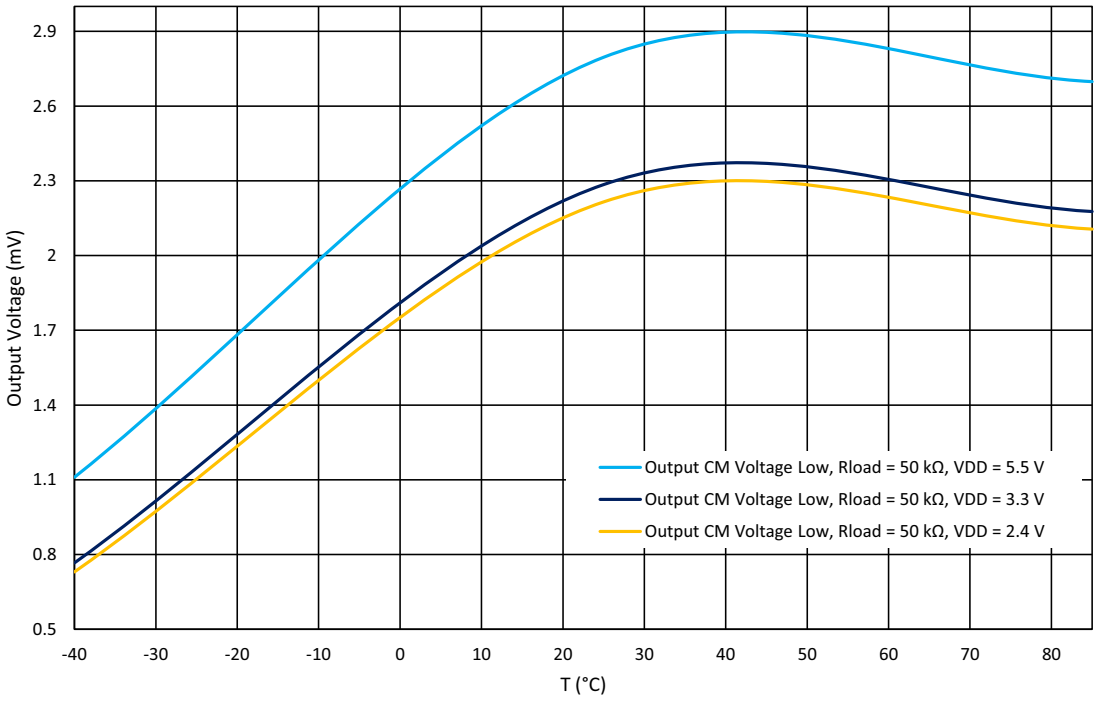


Figure 139. Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 128 kHz, R_{LOAD} = 50 kΩ

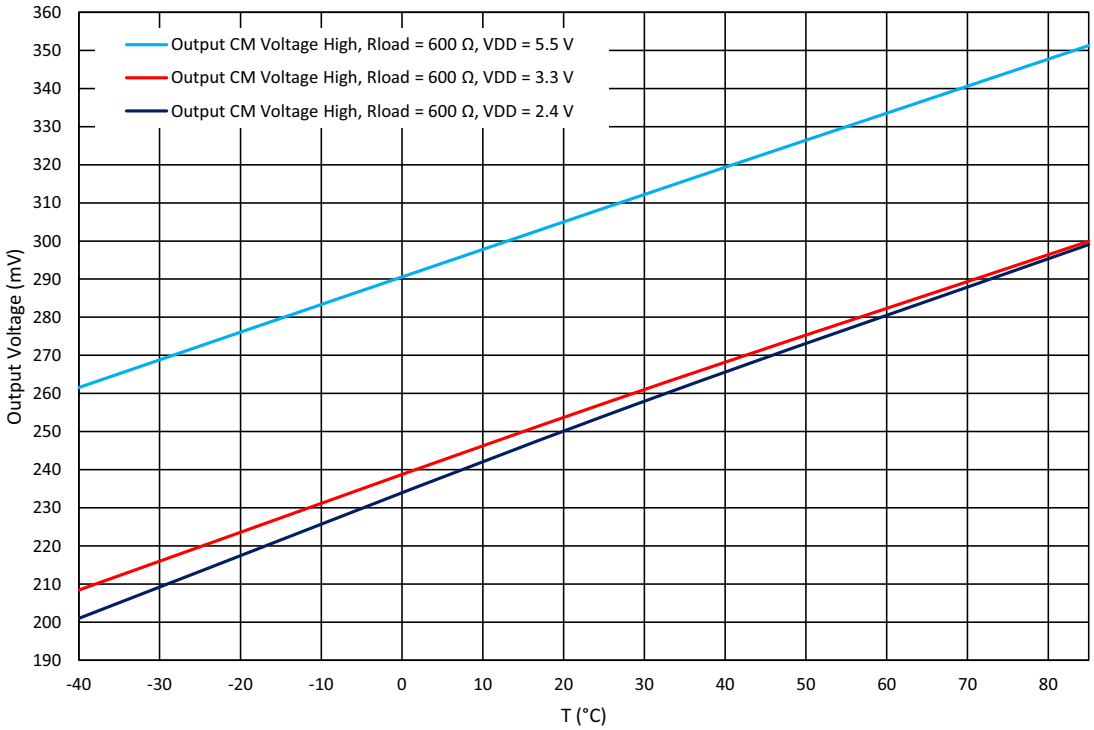


Figure 140. Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 128 kHz, R_{LOAD} = 600 Ω

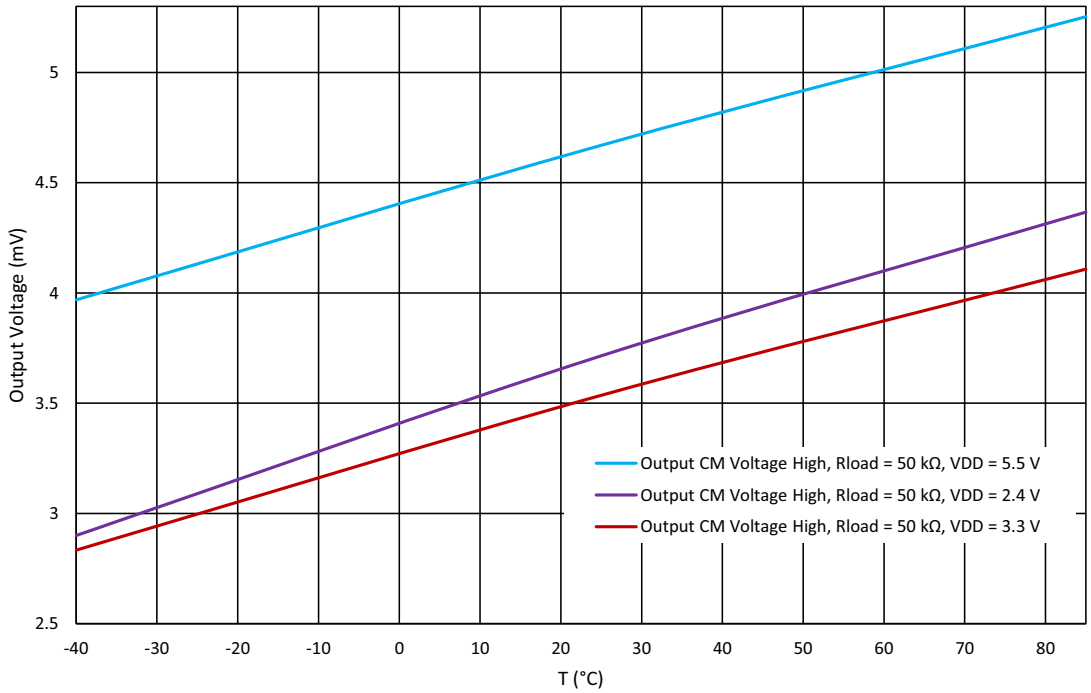


Figure 141. Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 128 kHz, R_{LOAD} = 50 kΩ

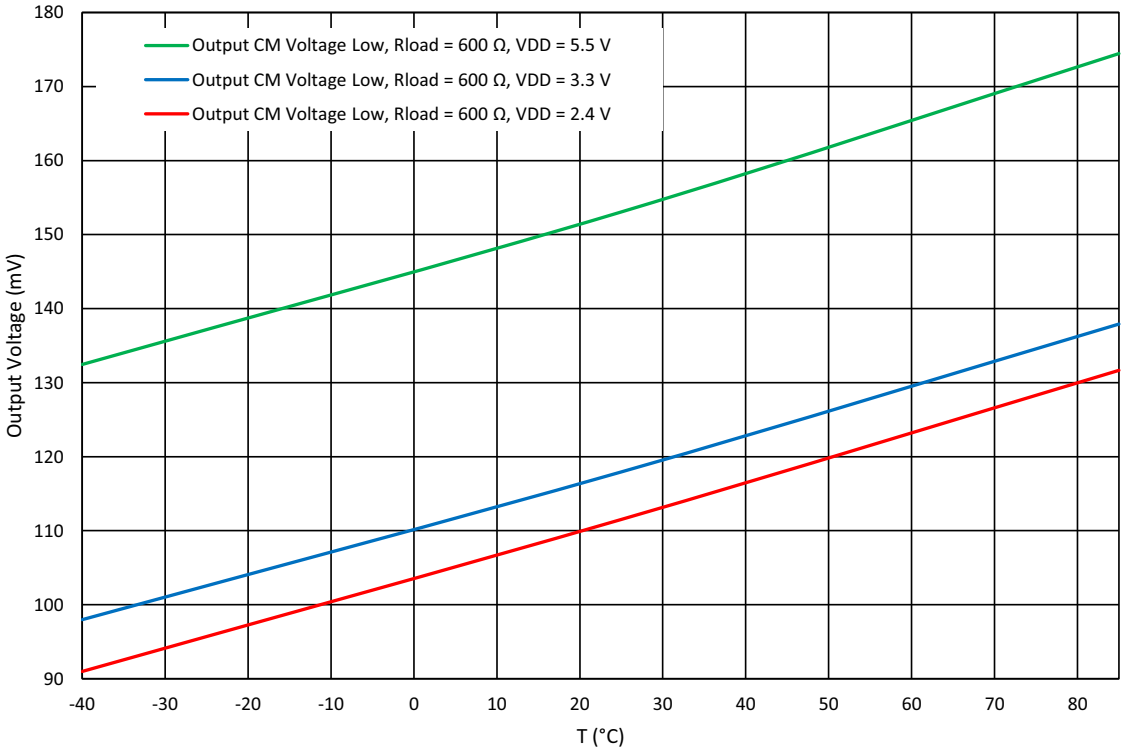


Figure 142. Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 512 kHz, R_{LOAD} = 600 Ω

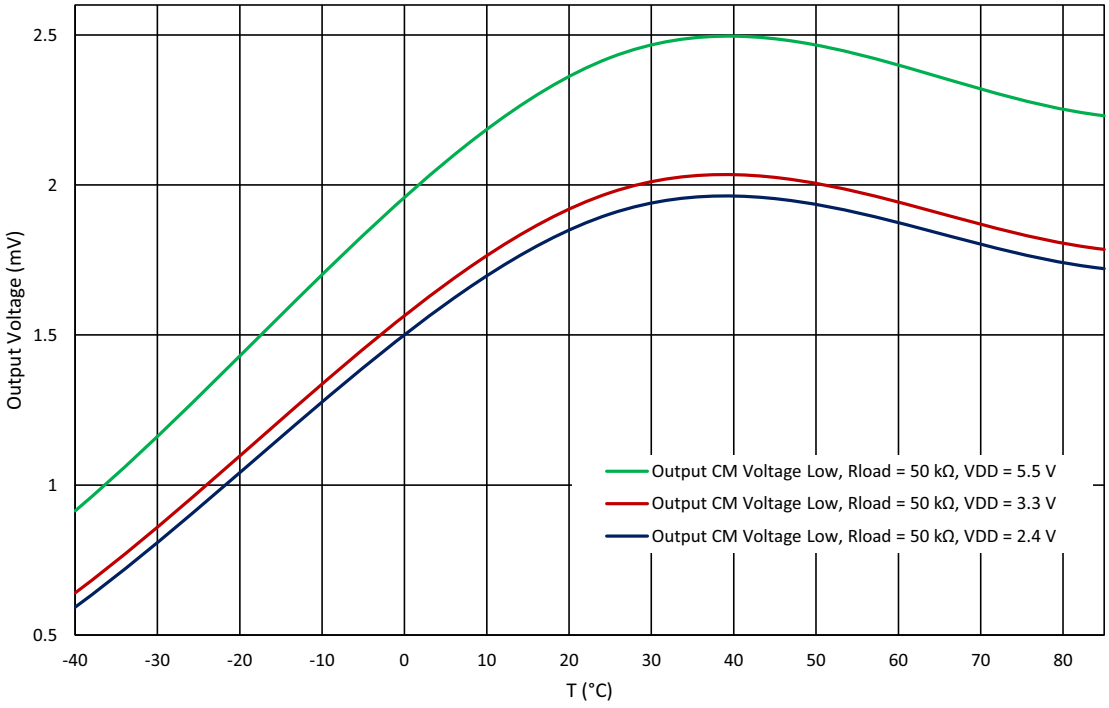


Figure 143. Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 512 kHz, R_{LOAD} = 50 kΩ

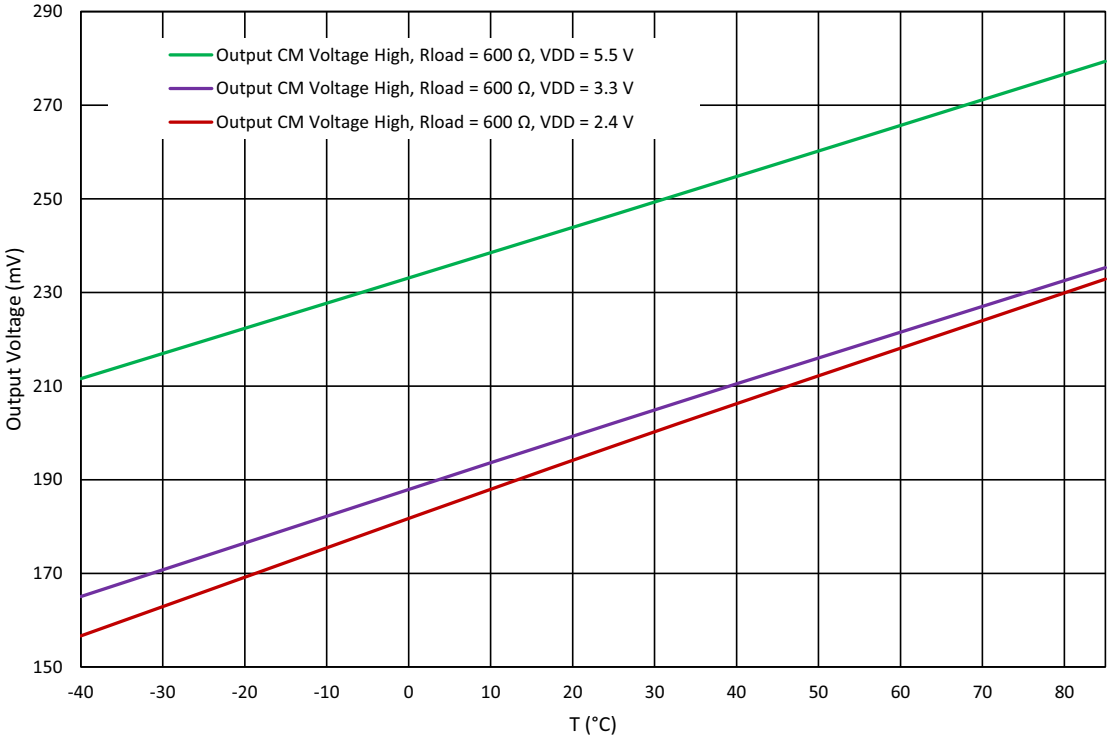


Figure 144. Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 512 kHz, R_{LOAD} = 600 Ω

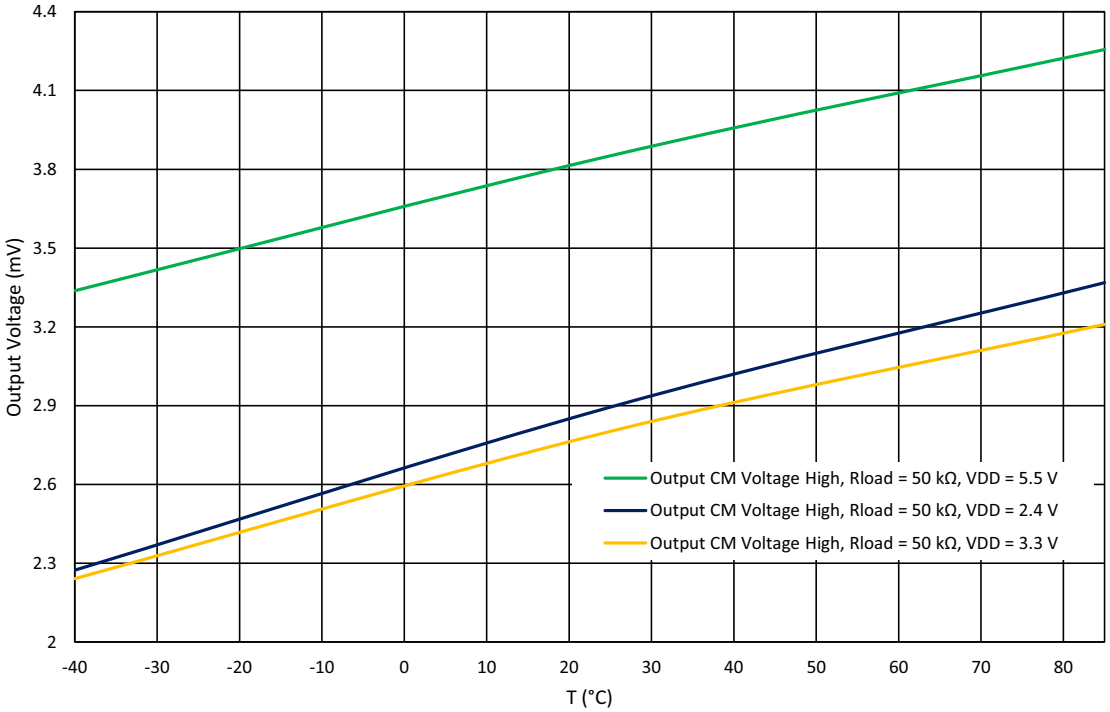


Figure 145. Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 512kHz, R_{LOAD} = 50 kΩ

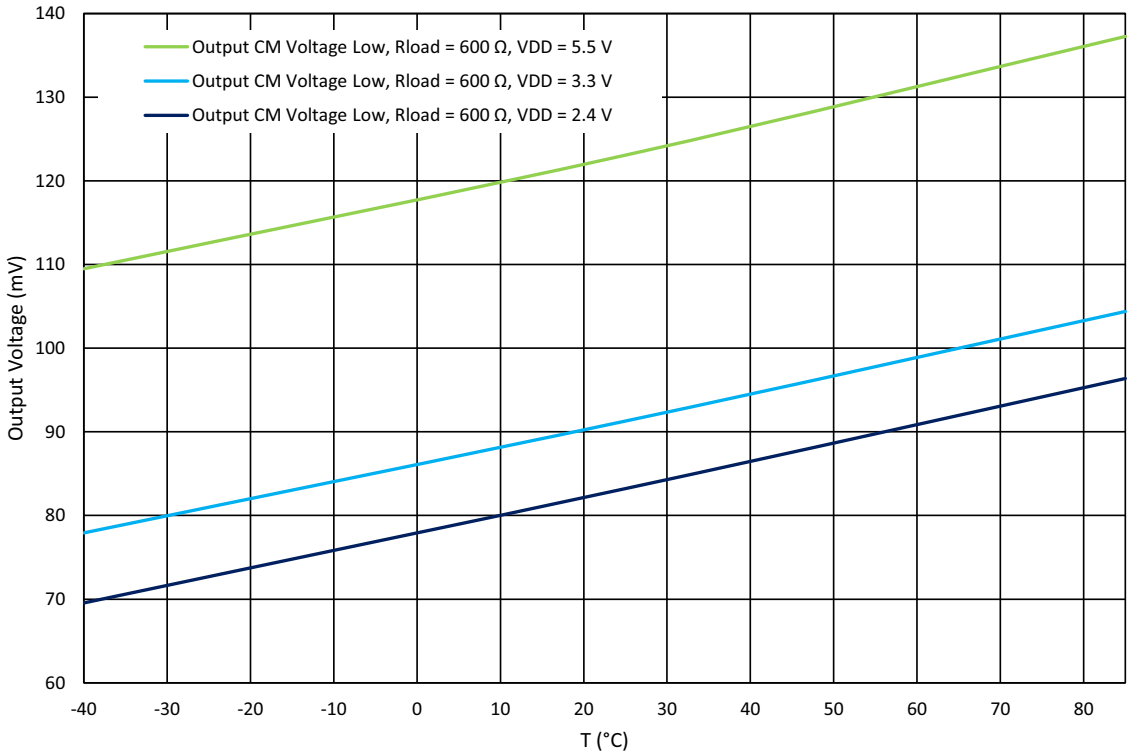


Figure 146. Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 2 MHz, R_{LOAD} = 600 Ω

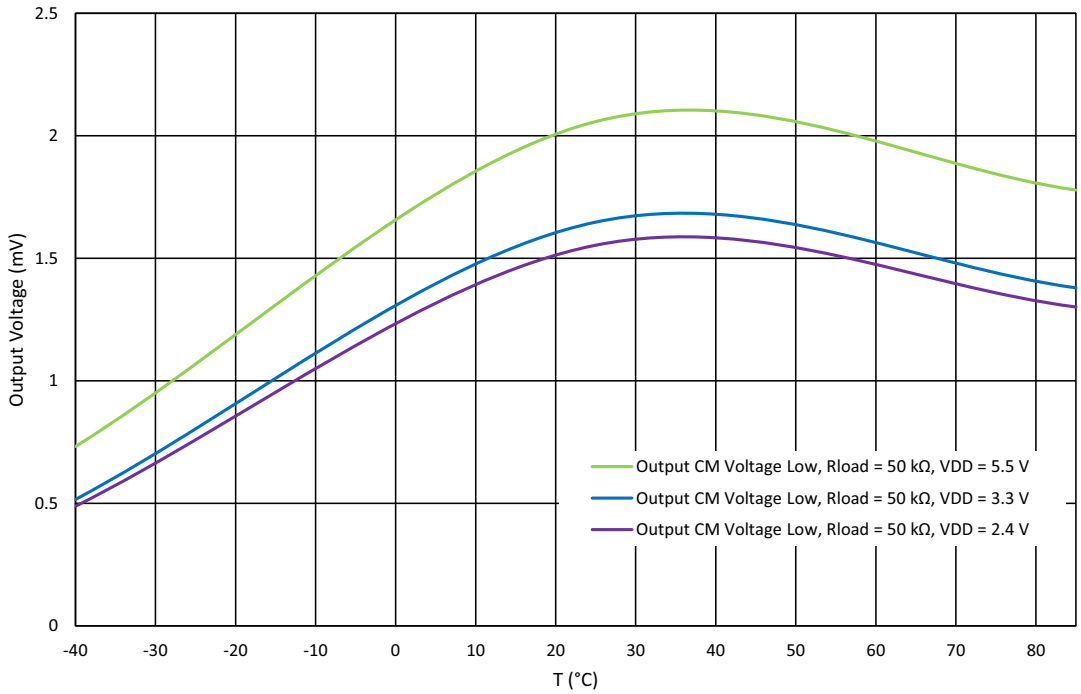


Figure 147. Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 2 MHz, R_{LOAD} = 50 kΩ

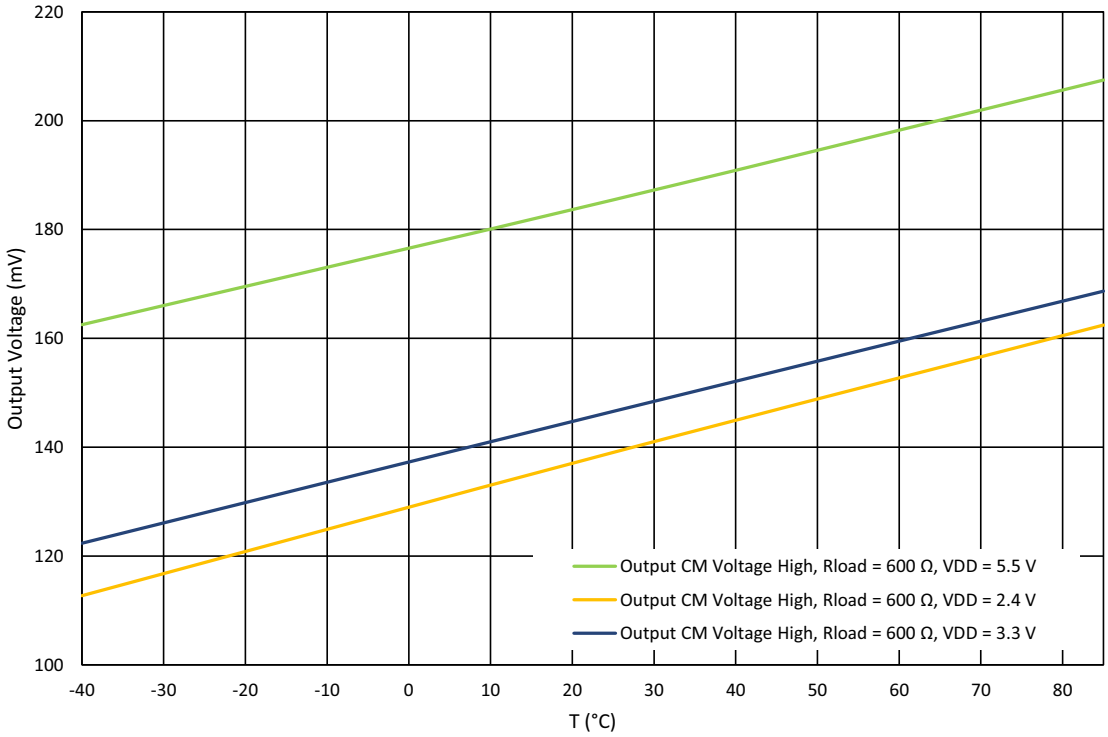


Figure 148. Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 2 MHz, R_{LOAD} = 600 Ω

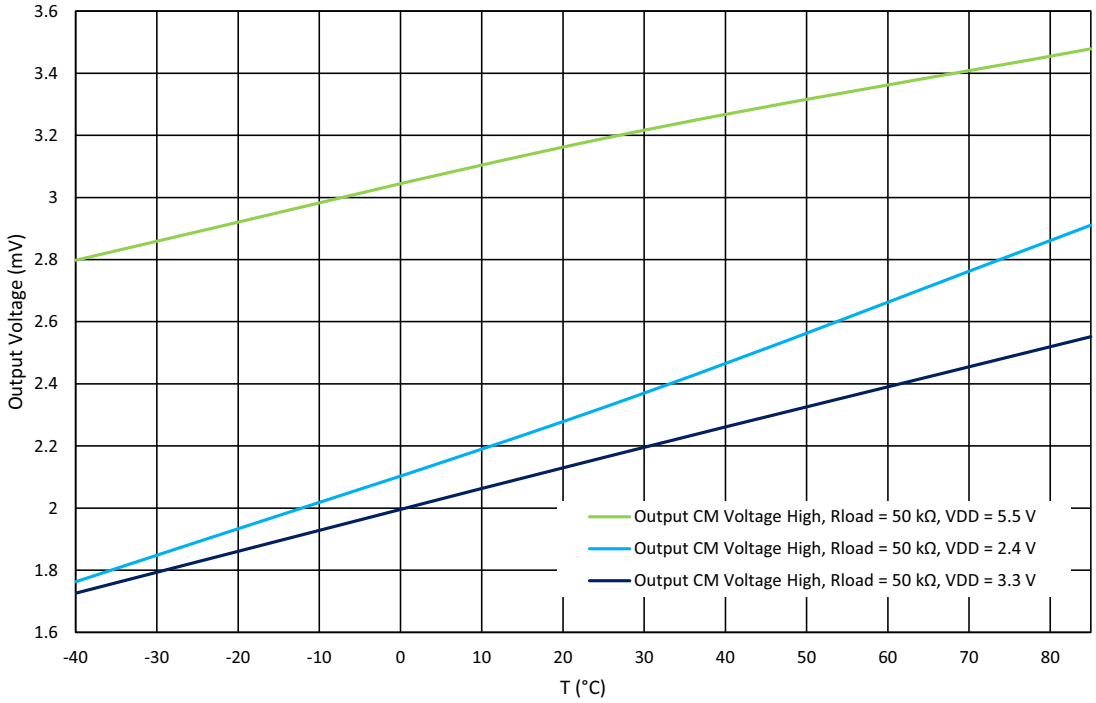


Figure 149. Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 2 MHz, R_{LOAD} = 50 kΩ

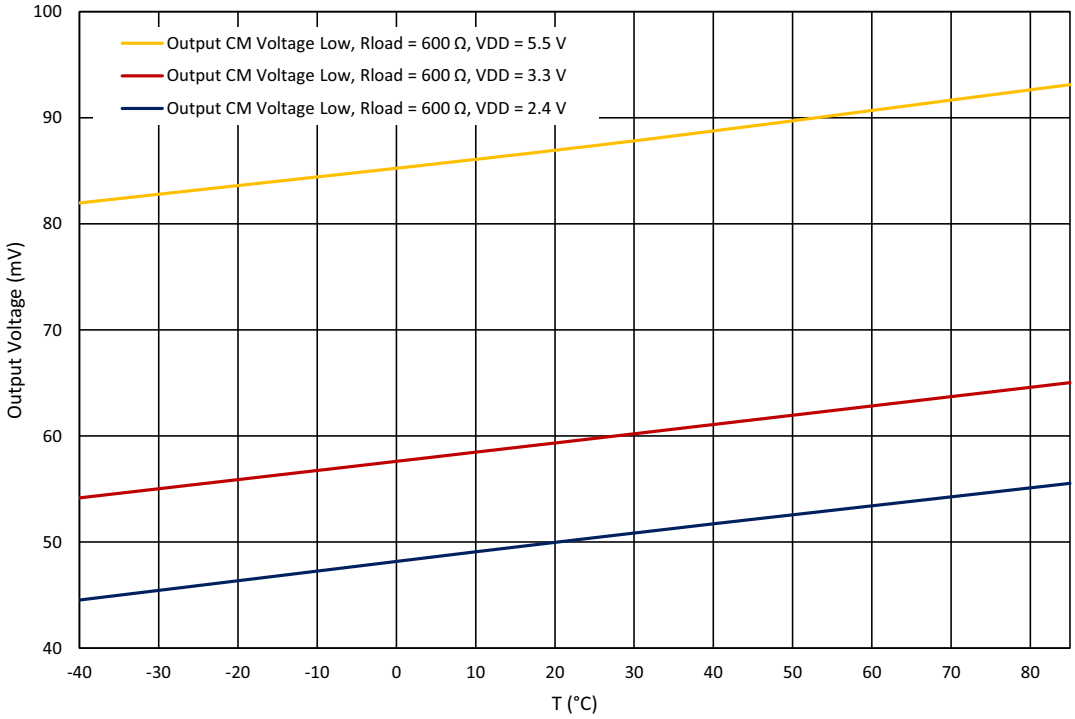


Figure 150. Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 8MHz, R_{LOAD} = 600 Ω

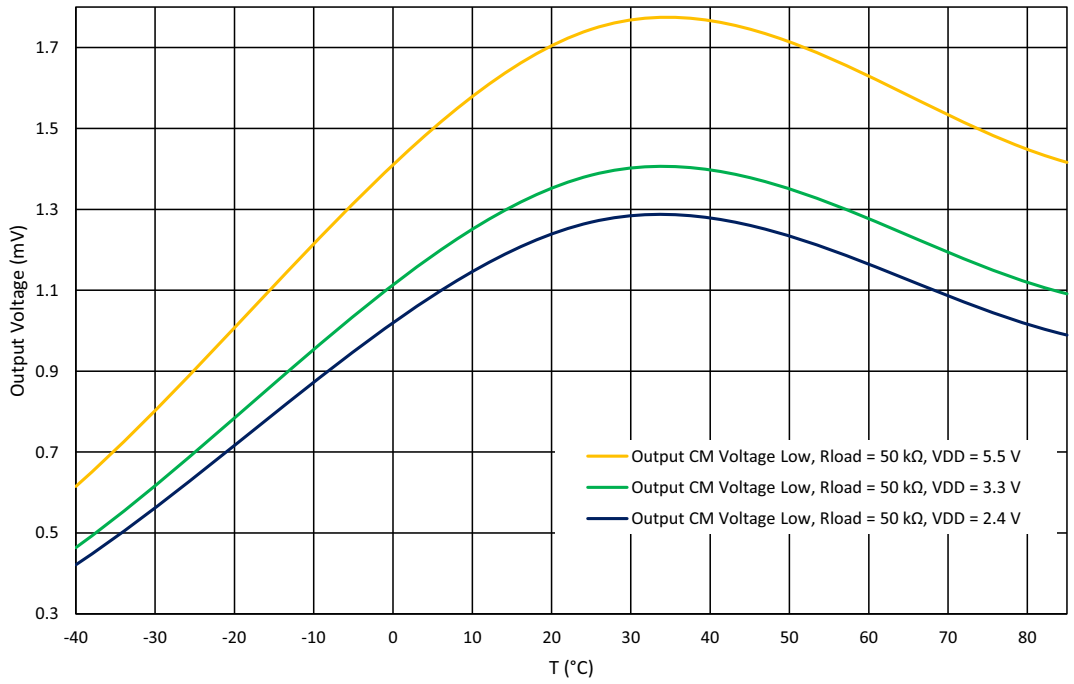


Figure 151. Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 8 MHz, R_{LOAD} = 50 kΩ

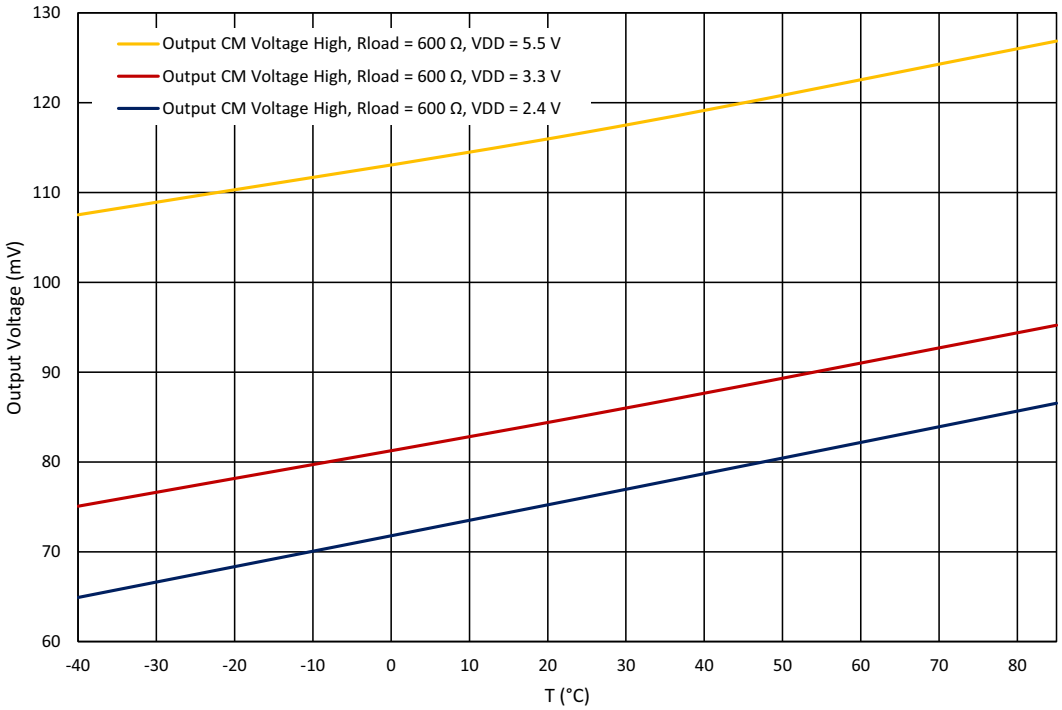


Figure 152. Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 8 MHz, R_{LOAD} = 600 Ω

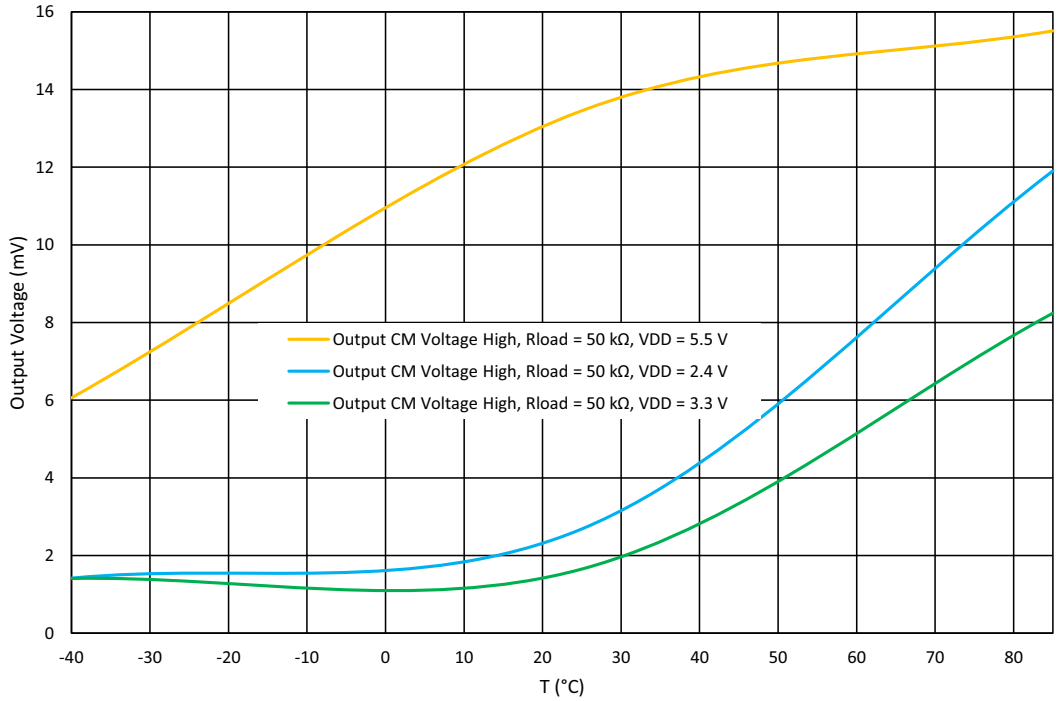


Figure 153. Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 8 MHz, R_{LOAD} = 50 kΩ

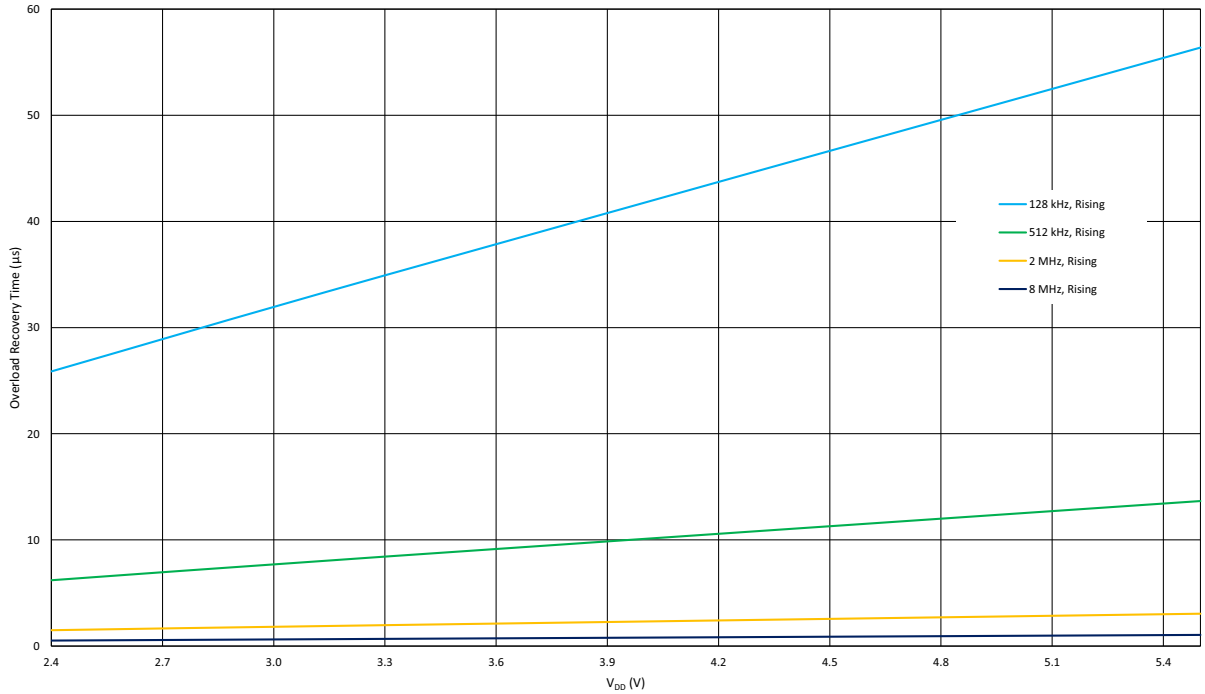


Figure 154. Overload Recovery Time vs. Power Supply Voltage R_L = 50 kΩ; G = 1 V/V, Rising

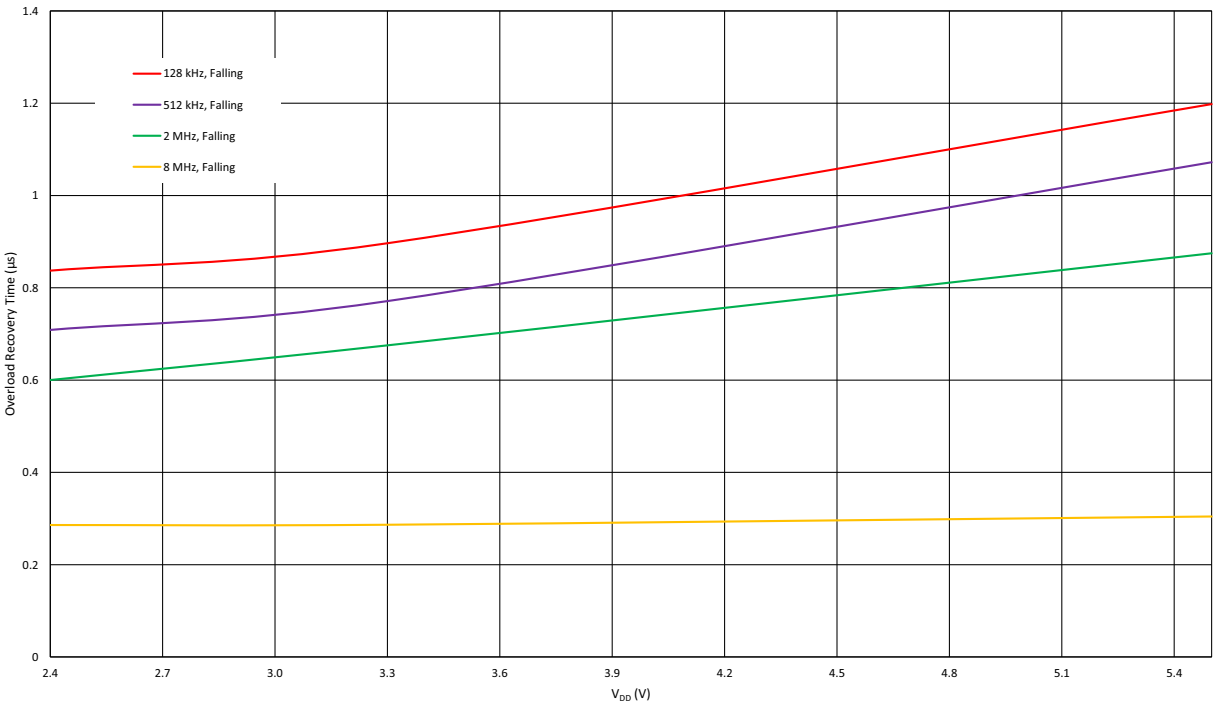


Figure 155. Overload Recovery Time vs. Power Supply Voltage R_L = 50 kΩ; G = 1 V/V, Falling

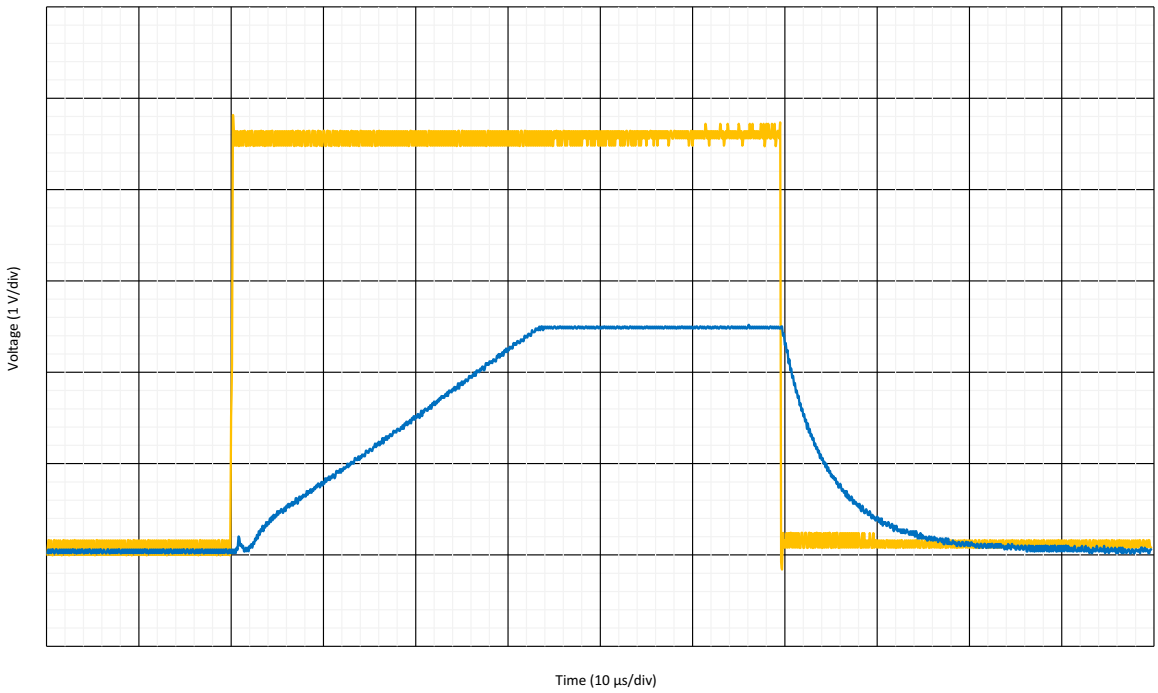


Figure 156. Output Response to Power Down Signal G = 1 V/V; R_L = 50 kΩ; C_L = 20 pF; V_{IN} = V_S/2, BW = 128 kHz

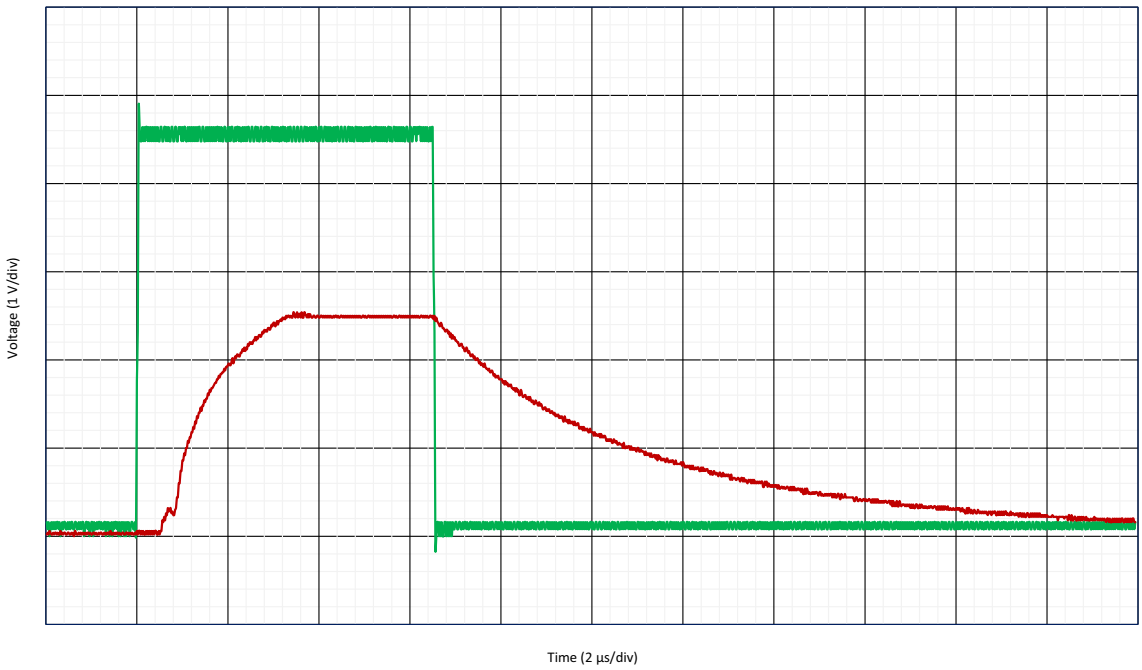


Figure 157. Output Response to Power Down Signal G = 1 V/V; R_L = 50 kΩ; C_L = 20 pF; V_{IN} = V_S/2, BW = 512 kHz

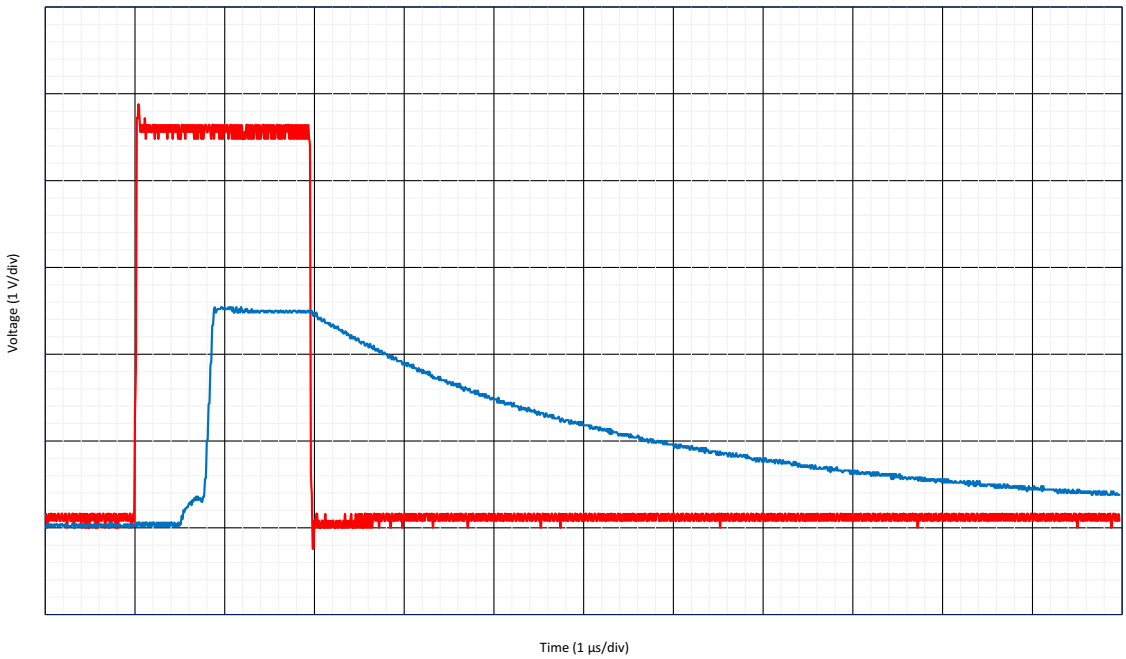


Figure 158. Output Response to Power Down Signal G = 1 V/V; R_L = 50 kΩ; C_L = 20 pF; V_{IN} = V_S/2, BW = 2 MHz

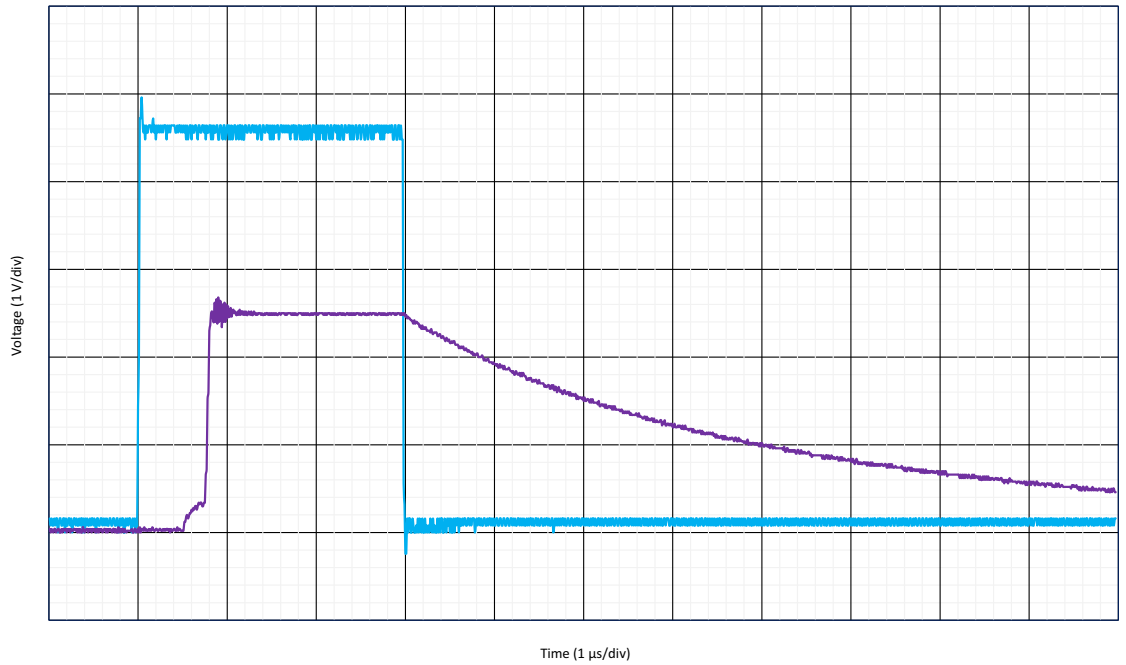


Figure 159. Output Response to Power Down Signal G = 1 V/V; R_L = 50 kΩ; C_L = 20 pF; V_{IN} = V_S/2, BW = 8 MHz

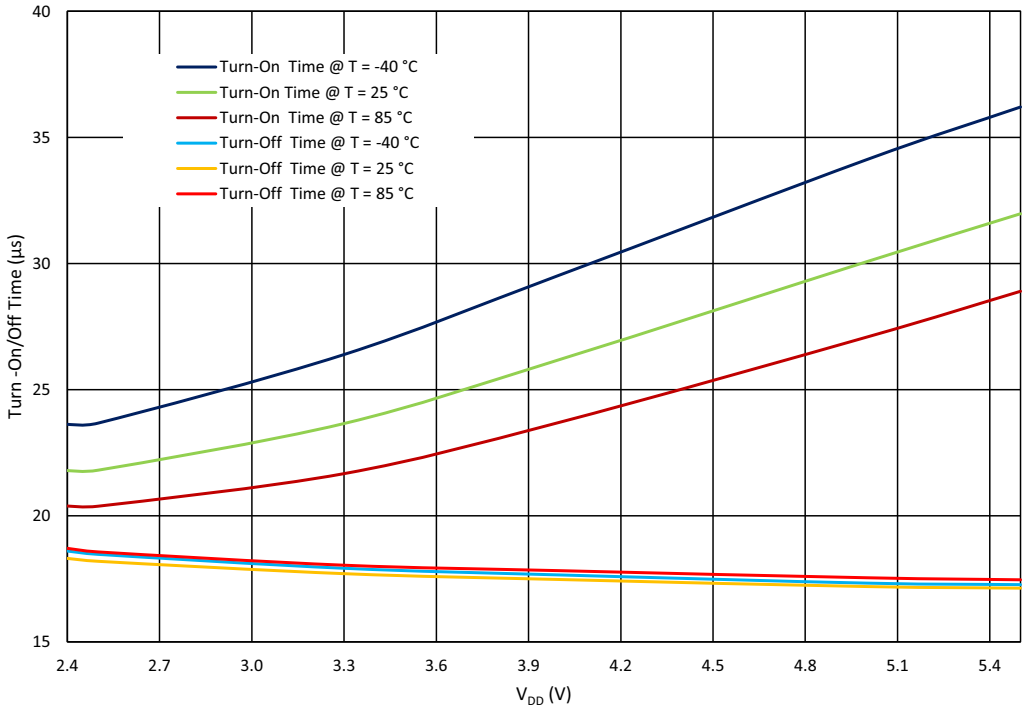


Figure 160. Op Ampx Turn-On/Off Time vs. V_{DD} at V_{IN} = V_{DD}/2, BW = 128 kHz

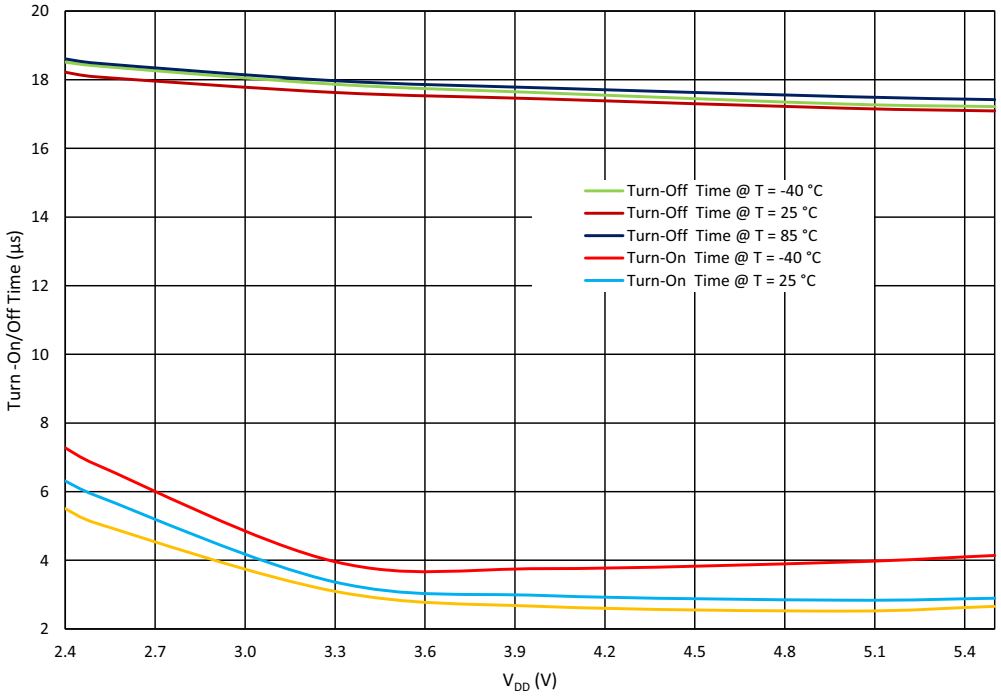


Figure 161. Op Ampx Turn-On/Off Time vs. V_{DD} at V_{IN} = V_{DD}/2, BW = 512 kHz

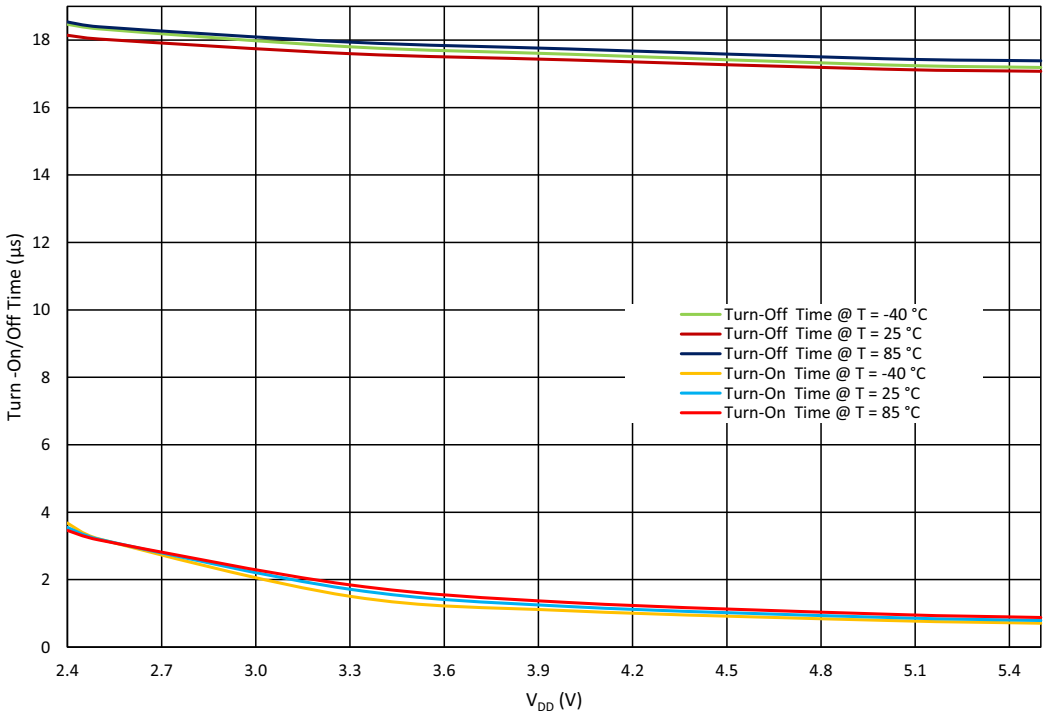


Figure 162. Op Ampx Turn-On/Off Time vs. V_{DD} at V_{IN} = V_{DD}/2, BW = 2 MHz

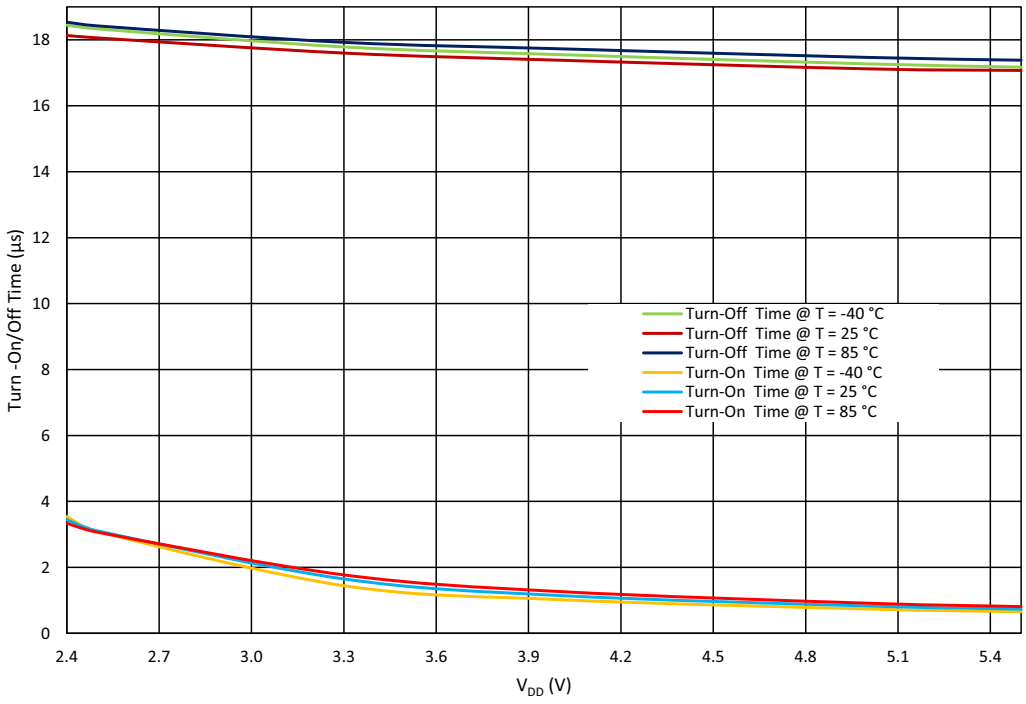


Figure 163. Op Ampx Turn-On/Off Time vs. V_{DD} at V_{IN} = V_{DD}/2, BW = 8 MHz

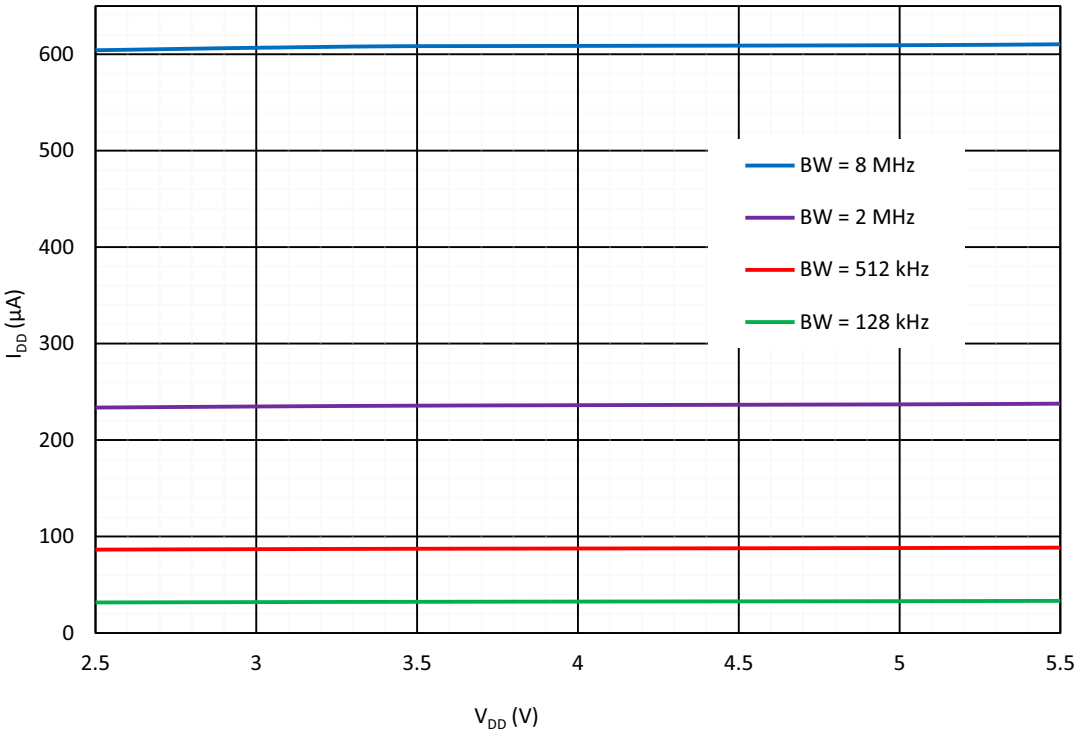


Figure 164. Op Amps Quiescent Current Consumption vs. V_{DD}

11. Analog Switch Macrocell

11.1 Analog Switch General Description

The SLG47004 contains two single-pole/single throw (SPST) normally open analog switches (AS). The structure of the Analog Switches is shown in Figure 165 and Figure 166.

Each analog switch can be controlled from the following sources:

- Connection matrix
- Operational Amplifier macrocell.

Small NMOS (small PMOS) of Analog Switch must be enabled when macrocell is controlled by logic signal from connection matrix. Otherwise, small NMOS (small PMOS) must be disabled when macrocell is controlled by Op Amp.

Table 33 and Table 34 show possible operation modes of analog switches.

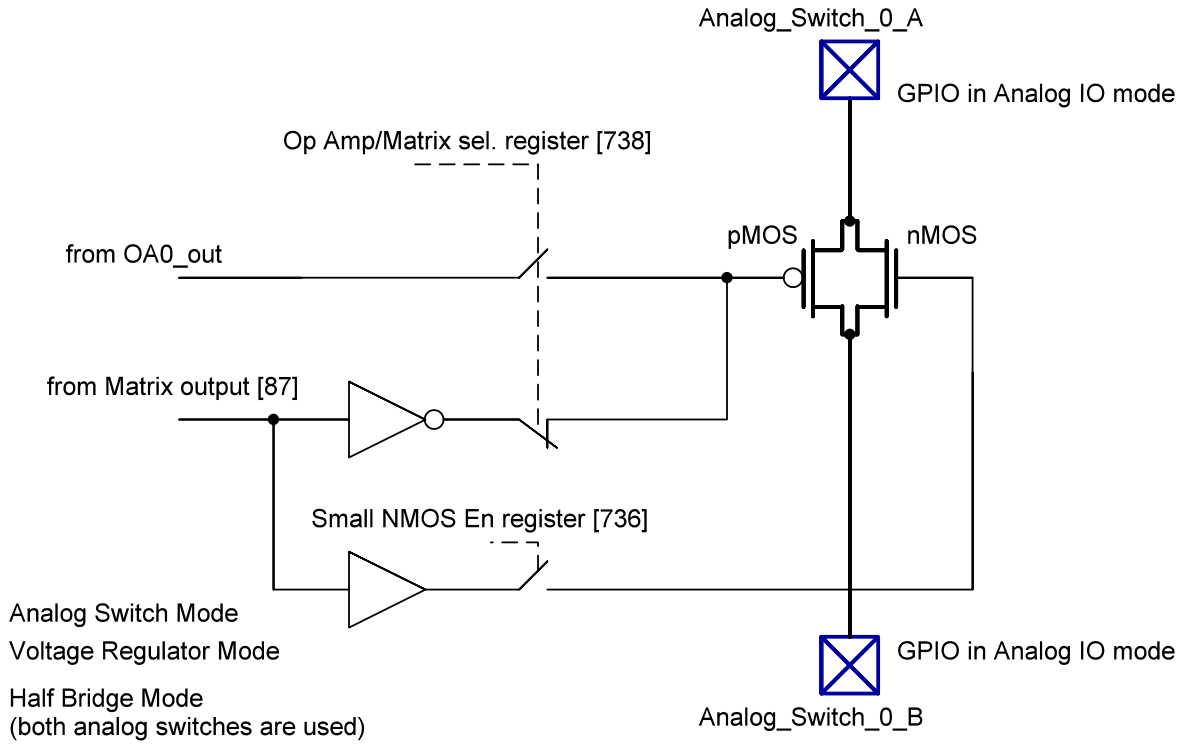


Figure 165. Analog Switch 0 Control Circuit

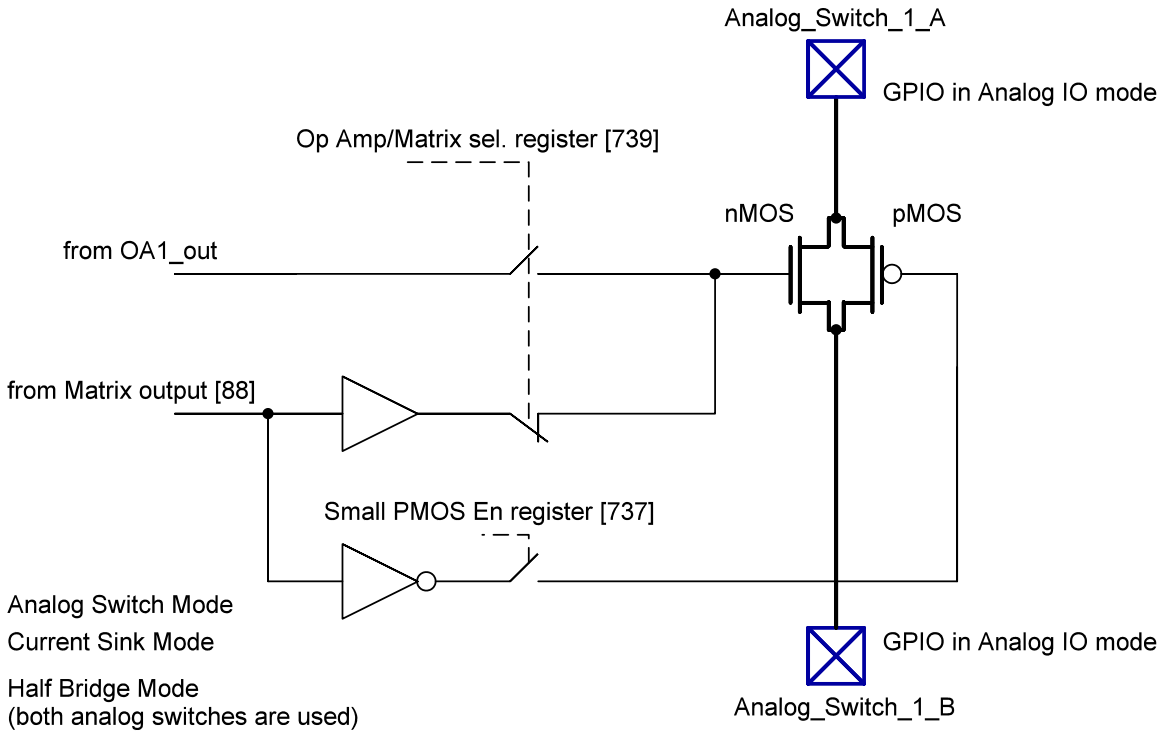


Figure 166. Analog Switch 1 Control Circuit

Table 33. Analog Switch 0 Modes of Operation

Mode of Operation	Half Bridge Mode Enable Reg [740]	Matrix Op Amp Control Reg [738]	Small nMOS Enable Reg [736]
Analog Switch mode with big PMOS only (control from connection matrix)	0	0	0
Analog Switch mode with all FETs enabled (control from connection matrix)	0	0	1
Voltage Regulator mode	0	1	0
Half Bridge mode with big PMOS only (control from connection matrix)	1	x	0
Half Bridge mode with all FETs enabled (control from connection matrix)	1	x	1

Table 34. Analog Switch 1 Modes of Operation

Mode of Operation	Half Bridge Mode Enable Reg [740]	Matrix Op Amp Control Reg [739]	Small nMOS Enable Reg [737]
Analog Switch mode with big MMOS only (control from connection matrix)	0	0	0
Analog Switch mode with all FETs enabled (control from connection matrix)	0	0	1
Current Sink mode	0	1	0
Half Bridge mode with big NMOS only (control from connection matrix)	1	x	0
Half Bridge mode with all FETs enabled (control from connection matrix)	1	x	1

11.2 Half Bridge Mode

Two switches can be externally connected in series to create a half bridge. Please refer to tables Table 33 and Table 34 to enable half bridge mode. Additional logic will be connected to the analog switches to simplify control. Figure 167 shows the half bridge structure with two analog switches.

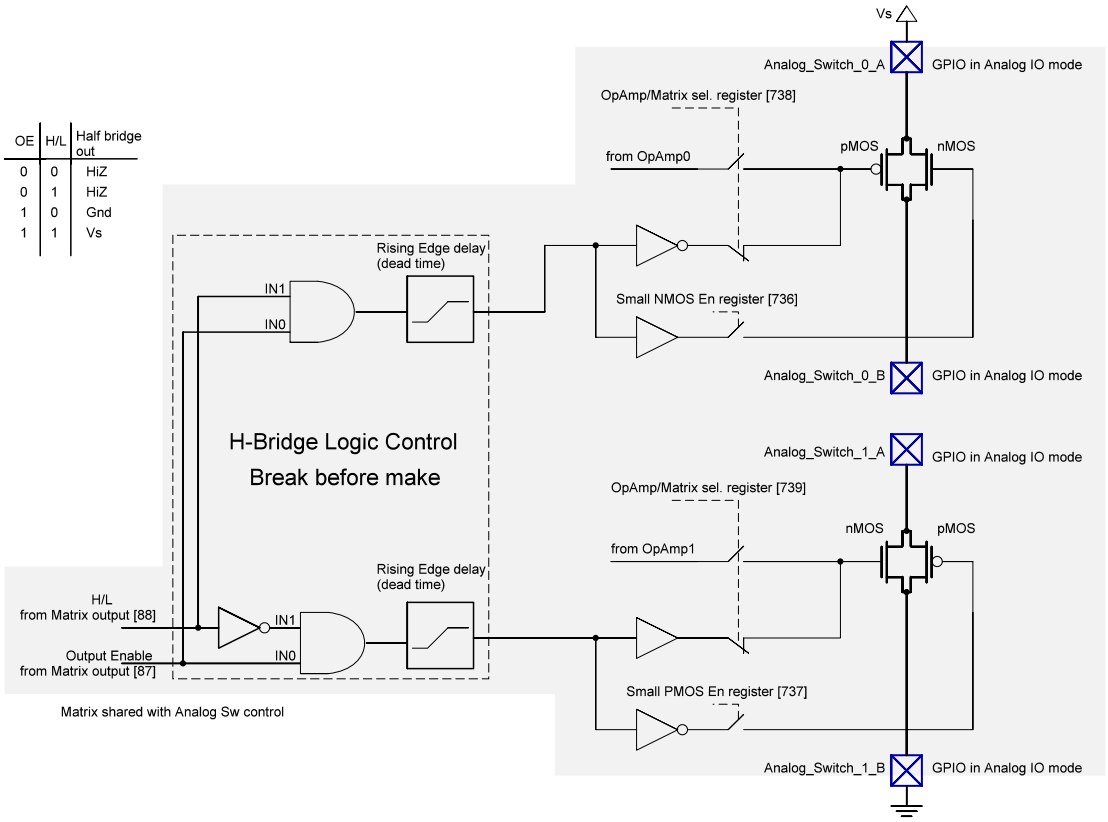


Figure 167. Structure of Half Bridge

11.3 Analog Switches Typical Performance

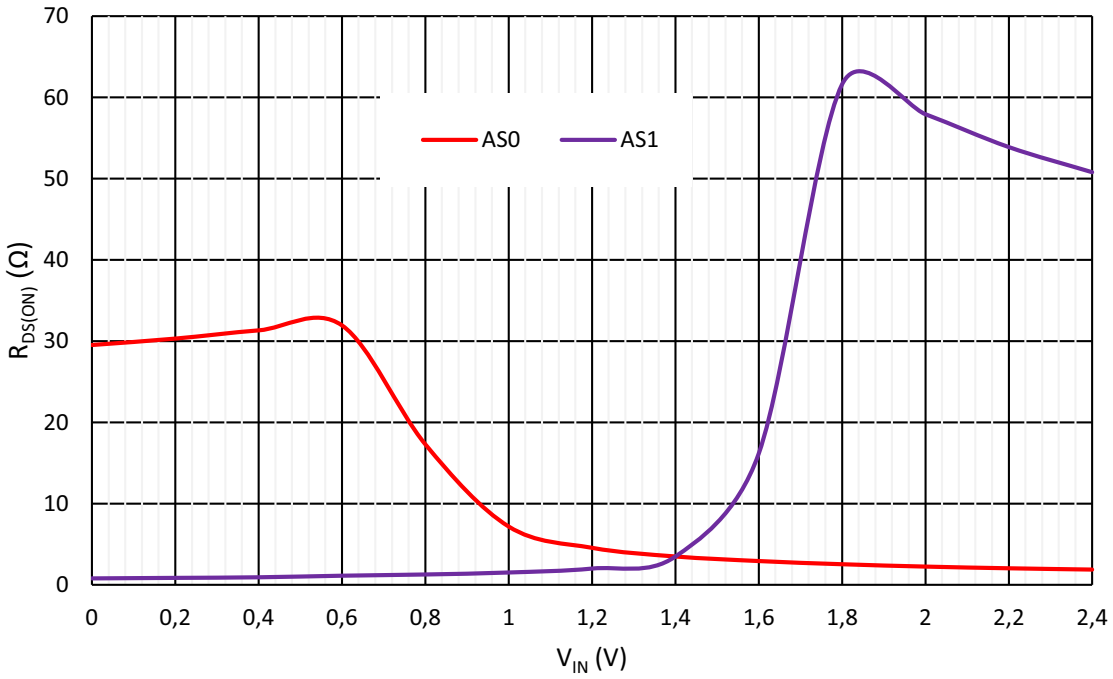


Figure 168. Typical R_{ON} vs. Input Voltage (V_i) for V_i = 0 to V_{DDA}, I_{LOAD} = 1 mA, V_{DDA} = 2.4 V

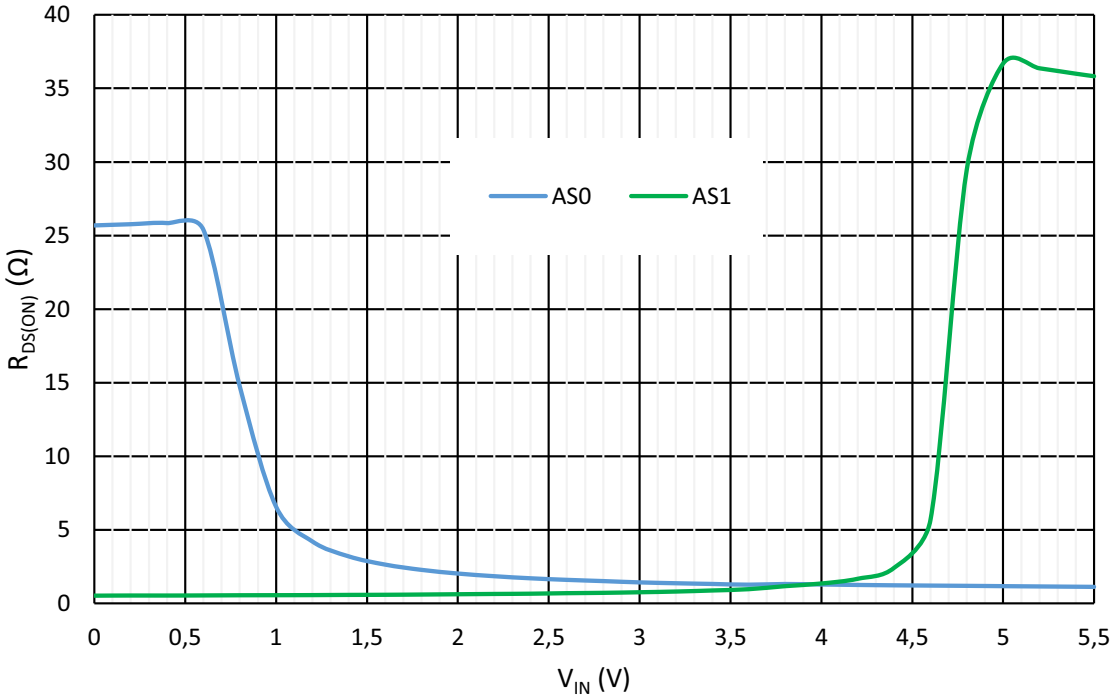


Figure 169. Typical R_{ON} vs. Input Voltage (V_i) for V_i = 0 to V_{DDA}, I_{LOAD} = 1 mA, V_{DDA} = 5.5 V

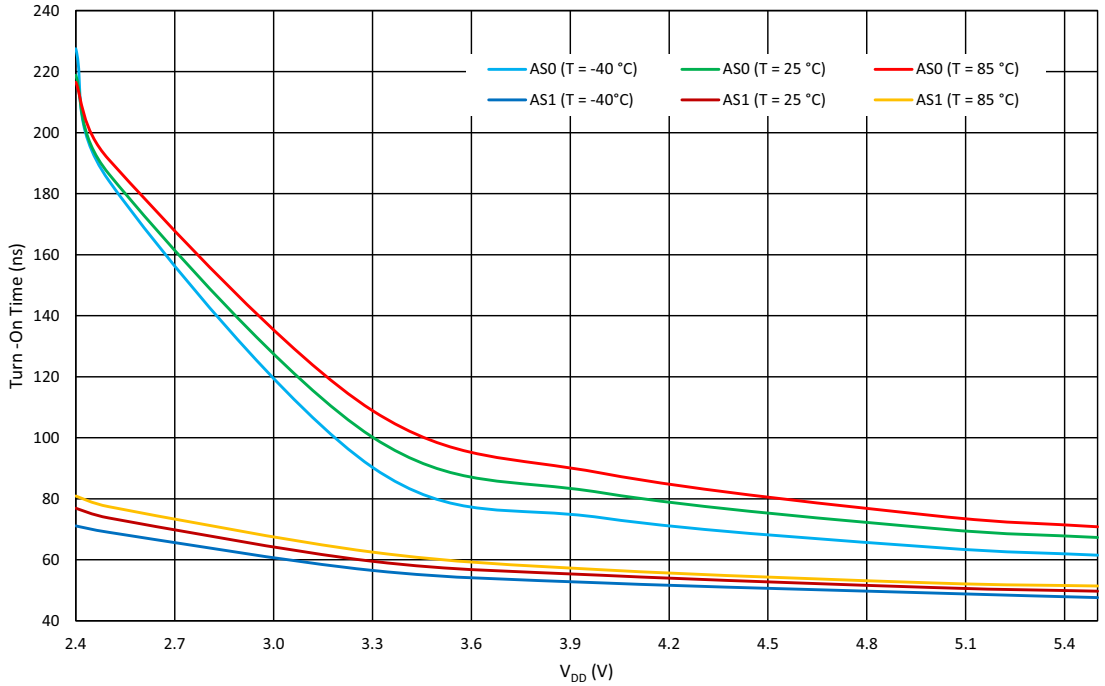


Figure 170. Turn-On Time vs. V_{DD} at R_{LOAD} = 100 Ω to GND, $V_{IN} = V_{DD}/2$

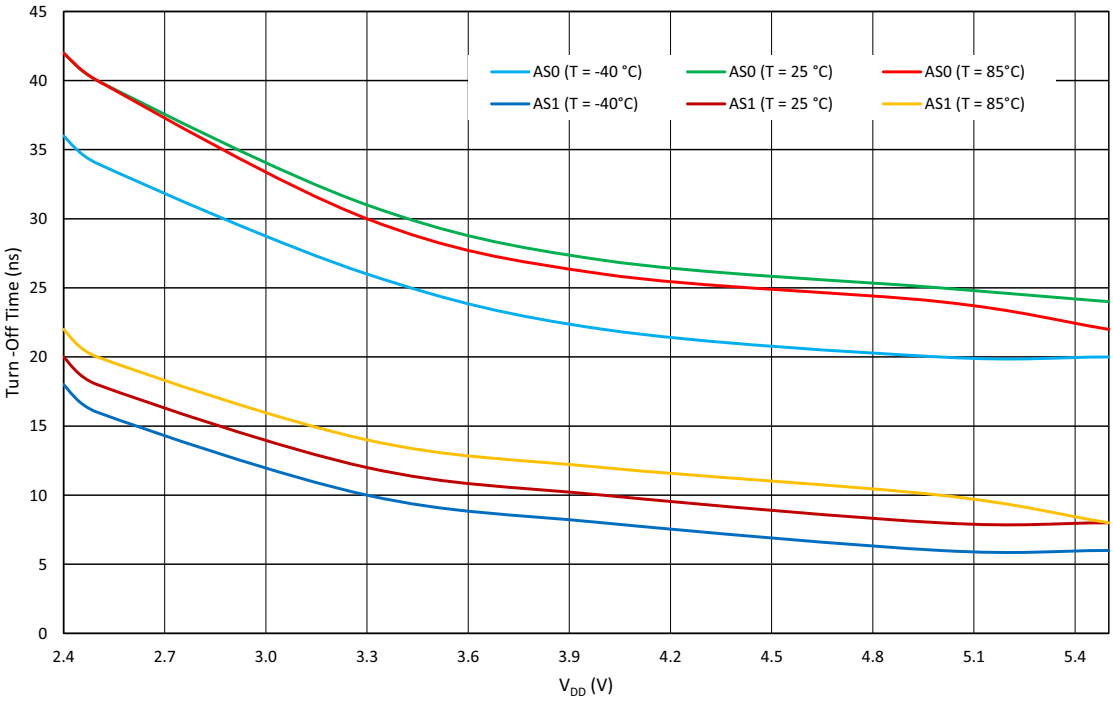


Figure 171. Turn-Off Time vs. V_{DD} at R_{LOAD} = 100 Ω to GND, $V_{IN} = V_{DD}/2$

12. Digital Rheostats and Programmable Trim Block

The SLG47004 contains two 10-bit Digital Rheostats. The structure of both macrocells is shown in Figure 172. The range of digital code that corresponds to the rheostat resistance ranges from 0 to 1023 (1024 taps). Code 0 corresponds to the minimum resistance between the RHx_A and RHx_B terminals. As the code value increases, the resistance between the RHx_A and RHx_B terminals monotonically increases. Consequently, when the code value decreases, the resistance between the RH0_A and RH0_B terminals decreases as well (see section 12.2 Calculating Actual Resistance). The voltage on any rheostat pin can be in the range from AGND to V_{DDA}, as well as be dynamically changed during operation.

To guarantee proper operation of digital rheostats charge pump must be turned on (matrix input [86] must be logic High or registers [912] = 1, [913] = 1). Optionally user can turn off rheostats charge pump to decrease energy consumption. But it's strongly recommended to use the charge pump if V_{DD} < 4.5 V.

The rheostat resistance can be changed in three ways:

- Changing the Rheostat value using the I^2C interface.
- Manually changing the rheostat value using clock and up/down signals, similar to the counter.
- Using the Built-in Auto-Trim mode, where the rheostat value change is done using a special logic based on the signal from the Chopper ACMP.

Each rheostat also has three Switching Speed Modes:

- Regular mode (Reg [915] = 0, Reg [914] = 0) - up to 1 kHz. In this mode, Low Power Bandgap Chopper Oscillator that oscillates around 120 kHz is used as a source for the charge pump clock. This setting has a lower quiescent current at the expense of a longer recovery time after input voltage spikes.
- Fast mode (Reg [915] = 0, Reg [914] = 1) - up to 100 kHz. In this mode, the 2 MHz OSC is used as a source for the charge pump clock. This setting has a faster recovery time for input voltage spikes at the expense of a larger quiescent current. Please note that this selection forces On the OSC1 (2.048 MHz).
- Auto Selection (Reg [915] = 1, Reg [914] = either) when trim is used. When Auto-Trim is active, the fast mode is used. After the Auto-Trim process completes, the regular mode is used.

Note: The maximum switching speed can be achieved if no external capacitive load is connected to the rheostat terminals.

The Programmable Trim (PT) blocks of rheostats macrocell contain analog MUXs, digital MUXs, Chopper ACMP, and additional logic. The two analog MUXs (M1 and M2) and the Chopper ACMP are both shared between the two rheostats. All analog and digital MUXs are set by NVM bits and can be overwritten with I^2C.

The M_CK0 and M_CK1 MUXs select the clock source from internal pre-dividers of the internal oscillators or from the connection matrix. The internal clock sources for the rheostats are OSC0, OSC0/8, OSC0/64, OSC0/512, OSC0/4096, OSC0/32768, OSC0/262144, OSC1, OSC1/8, OSC1/64, and OSC1/512. The PT blocks of the rheostat use the same clock scheme as Counter/Delay Macrocells (refer to section 16.5 CNT/DLY Clock Scheme). M_CH0 and M_CH1 select the Chopper comparator or a matrix output as the signal source for the main rheostat up/down counter direction. The output of the Chopper ACMP is connected with the Up/Down inputs of the PT blocks by default. The output of the Chopper ACMP can be optionally inverted by setting reg [882] to '1'.

M1 MUX selects the input for the Chopper comparator to be connected either internally to one of 3 integrated Op Amps (Op Amp0 out, Op Amp1 out, In Amp Out) or externally to a PIN. M2 MUX is simplified symbol of Chopper ACMP reference selection blocks. The Chopper ACMP reference ("-" input) can be: analog signal from pin, divided internal V_{REF} voltage (6-bit divider), or divide V_{DDA} voltage (6-bit divider). In Auto-Trim mode each of Rheostats has it own settings for Chopper ACMP inputs. For more information about Chopper ACMP V_{REF} see section 9.3 Chopper Analog Comparator.

The power-up signal for the Chopper ACMP can be handled either by matrix output signal or Set0/Set1 signal from the PT macrocell. In Auto-Trim mode (Auto_Cal _Dis_RHx NVM bit = 0) additional internal logic enables the clocking of the corresponding PT macrocell counter and disables clocking when one of the stop conditions is reached. See a detailed description in section 12.4 Trimming Process Using Programmable Trim Block. In Figure 172 when Auto_Cal _Dis_RHx NVM bit = 0 (Auto-Trim mode is enabled), the clocking pulses for the internal PT

macrocell counter are under control of additional logic. When Auto_Cal _Dis_RHx NVM bit = 1 (Auto-Trim mode is disabled), all additional logics (Set signal, internal Set signal, Idle/Active signal) operate the same way, but clock pulses are always enabled and generated externally by the user. Calibration channel can be selected automatically (1st channel is channel 0, second channel is channel 1) or can be set manually by registers [893:892].

The inputs of Chopper ACMP can be reconfigured while operating in Auto-Trim mode. There is one configuration of inputs (M1, M2 configuration, Figure 172). for the case when Set0 signal is latched, and another configuration of M1, M2 MUXs when Set1 signal is latched. For example, M1 MUX can be configured to operate with In Amp out when Set0 is latched and Chopper_ACMP+ pin when Set1 is latched. The same way, M2 can be configured to work with any of M2 inputs when Set0 or Set1 are latched. Note that the default configuration is the configuration for Set0 signal. When Chopper ACMP operates as separate ACMP and Auto-Trim function is disabled, M1 and M2 MUXs operates with configuration for Set0 signal.

Keep in mind that two Auto-Trim processes cannot be done simultaneously. When the Auto-Trim process for one rheostat is active, all signals on the Set input for another rheostat will be ignored. See a detailed description in section 12.4.1 Trimming Process with Auto-Trim Option Enabled. The initial user defined value of Digital Rheostat resistance can be programmed into the NVM. The initial value will be loaded during the Power-On event and this value will be used as the initial rheostat resistance, as well as a starting point for count down or count up.

Both read and write operations are allowed for rheostat resistance value, stored in NVM. Also, both read and write operations are allowed for current rheostat resistance value. RH0 read operation - registers [1561:1552], write operation - registers [1545:1536]. RH1 read operation - registers [1689:1680], write operation - registers [1673:1664].

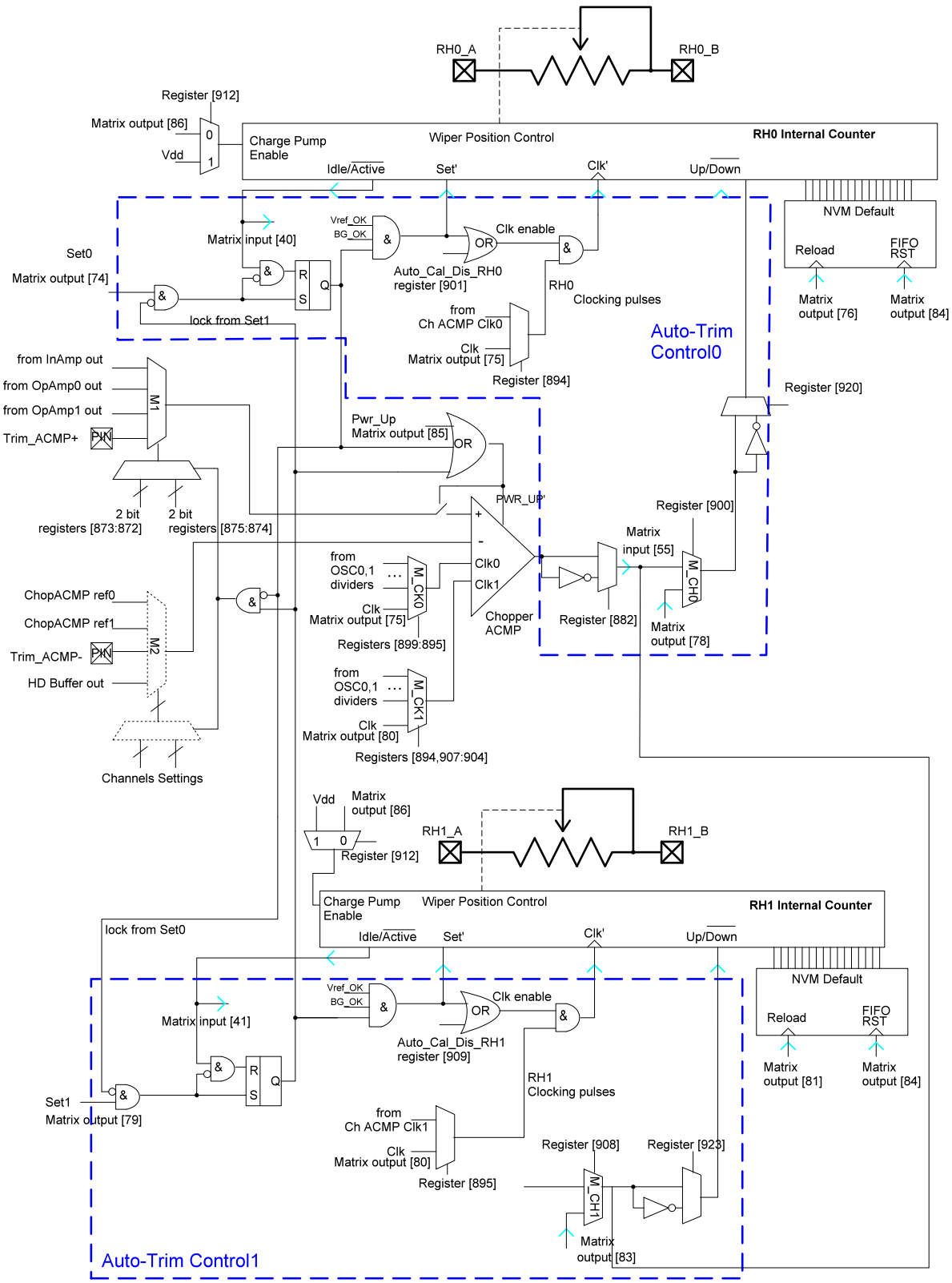


Figure 172. Programmable Trim Blocks and Digital Rheostat's Internal Circuit

PT macrocell signals:

- “Set”: external Set signal begins the Auto-Trim process when Auto_Cal _Dis_RHx bit is cleared (registers [901]). Otherwise, this signal has no effect. The behavior of the PT macrocell in Auto-Trim mode is described below.
- “Reload”: when Reload goes high the rheostat value stored in the NVM will be loaded into the rheostat (Register and Counter) overwriting any current setting. This signal is edge sensitive. It has no effect while the Auto-Trim procedure is active. For detailed information see section 12.3 Digital Rheostat Value Self-Programming into the NVM.
- “Program”: when Program goes high the Internal Counter value of the rheostat will be programmed into the MTP overwriting any current value in the NVM. This procedure can be done up to 1000 times. This signal is also edge sensitive. It has no effect while the Auto-Trim procedure is active. For detailed information see section 12.3 Digital Rheostat Value Self-Programming into the NVM. To enable "Program" signal from connection matrix RH_PRB register must be cleared (RH_PRB [1796] = 0). If RH_PRB [1796] register is set to 1, the access to NVM is disabled for "Program" signal. Refer to section 19.6 Emulated EEPROM Write Protection.
- “Clock”: this input has the following options: the PT macrocell can be clocked internally or from matrix. When clocked internally, the clock is automatically enabled/disabled by the Set input logic in Auto-Trim mode. The internal clock is synchronized with the Chopper ACMP clock.
- “Up/Down”: the rheostat counter counts up when the signal is High and down when the signal is Low.
- “Idle/Active”: this is the connection matrix input, that is logic HIGH by default. It goes LOW with rising edge on SET input if Auto-Trim mode is enabled (Auto_Cal _Dis_RHx NVM bit = 0). After the end of Auto-Trim procedure (one of stop conditions occurs) this signal sets to logic HIGH again.
- “FIFO nReset”: low level at this input clears internal FIFO buffer for commands Reload and Program for both rheostats. User should provide high logic level at this input for the normal rheostat operation.

There is also an overflow protection option, for which the counter will stop counting up when the maximum value (0x3FF) is reached or stop counting down when the minimum value (0x00) is reached. The digital rheostat is initialized/powered in the first place. The rheostat value is Hi-Z (or highest resistance if it is impossible to disconnect the rheostat) during the Power-On sequence.

12.1 Potentiometer Mode

This mode allows two 2-pin rheostats to work as one 3-pin potentiometer. When this mode is active (reg [917] = 1), user changes the value of RH0 internal counter. In this mode, the value of RH1 counter is the inverted value of RH0 counter (Figure 173). Note that the RH0_B pin and the RH1_A pin must be connected externally. Also, note that the Auto-Trim function isn't allowed in Potentiometer Mode.

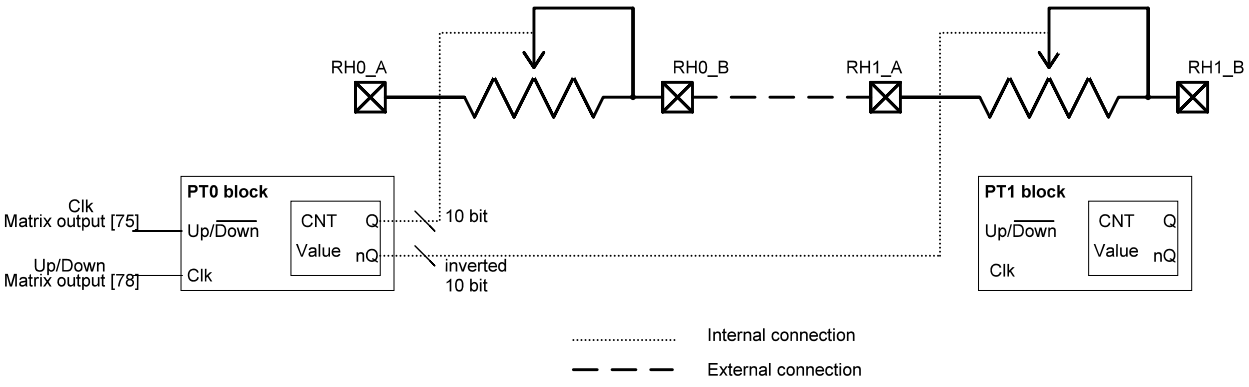


Figure 173. Rheostats in Potentiometer Mode

12.2 Calculating Actual Resistance

In applications where the absolute rheostat resistance is critical, the user can calculate it using the rheostat tolerance data, the minimum rheostat resistance, and the desired code.

The 16-bit tolerance data for both rheostats has been programmed into registers 0xE6 to 0xE9. These registers can be used to calculate the total rheostat resistance. The 16th bit defines the sign (0 = +, 1 = -) of the tolerance. The other fifteen bits correspond to the absolute value of the rheostat tolerances variation from 100 kΩ measured at 25 °C.

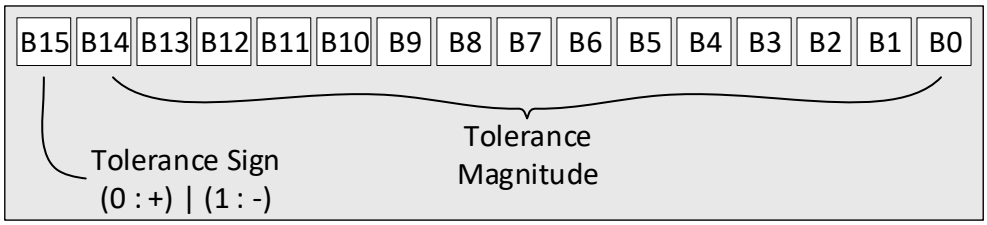


Figure 174. Rheostat Tolerance Registers

Note that the rheostat tolerance data is programmed into registers 0xE6 to 0xE9. To avoid losing this tolerance data, special attention must be paid when erasing and reprogramming page 14 in the NVM.

The rheostat value at a given code depends on the total digital rheostat resistance. The equations below can be used to calculate the rheostat resistance.

$$R_{Code} = (R_{DR} - R_{DR\ MIN}) \times (code/1023) + R_{DR\ MIN}$$

$$R_{DR} = 100 \times 10^3 + (sign_{RH\_Tolerance} \times R_{RH\_Tolerance})$$

where:

R_{Code} - Rheostat Resistance at a Given Code
R_{DR} - Total Digital Rheostat Resistance
$R_{DR\ MIN}$ - Minimum Rheostat Resistance
code - Rheostat Position Ranging from 0x000 to 0x3FF
$sign_{RH\_Tolerance}$ - the MSB of the Rheostat's Tolerance Data
$R_{RH\_Tolerance}$ - the 15 LSBs of the Rheostat's Tolerance Data.
For example, let's say that 0x2B67 has been written into the rheostat tolerance registers within the GreenPAK's NVM. B15 corresponds to a positive sign while B14:0 translates into a decimal value of 11111. R_{DR} calculates to approximately 111,111 Ω and can be used with the minimum rheostat resistance to calculate the resistance at a given code. Note that the minimum rheostat resistance must be measured to obtain precise results, but a range is provided in section 3.15 100K Digital Rheostat Specifications.

12.3 Digital Rheostat Value Self-Programming into the NVM

The current value of rheostat is stored in the Internal Counter. This value can be programmed into the MTP by setting logic HIGH at "Program" input. In this case, SLG47004 will generate a specific memory control sequence to rewrite a new value into the NVM. There is a separate NVM page that is dedicated for the Digital Rheostat value.

There is a dedicated bit RH_PRB, that enables/disables "Program" signal of PT block to change NVM rheostats resistance values. If RH_PRB[1796] = 0, "Program" signal is enabled. If RH_PRB[1796] = 1, "Program" signal is disabled. Note that RH_PRB bit has no effect on I2C access to NVM. To enable/disable I2C access to rheostat

resistance value, stored in NVM, user must change NPRB0, NPRB1 bits. Refer to section 18.5 Chip Configuration Data Protection.

SLG47004 can latch up to four "Program" and "Reload" signals of RH0 and RH1 (Reload RH0, Program RH0, Reload RH1, Program RH1). The same signal can't be latched second time, until it is processed. All latched signals will be processed in the order of arrival (FIFO buffer), since only one signal can access NVM at the same time. If Auto-Trim process of RH0 or RH1 is active and one or more "Reload", "Program" signals for corresponding rheostat come, SLG47004 will wait until the end of Auto-Trim process and then process will latch "Reload", "Program" signals. Set0 or Set1 signal can be latched at any time and processed when rheostat clocking isn't disabled by "Program" or "Reload" signals.

User can clear the FIFO buffer by setting low logic level at FIFO nReset input of PT blocks.

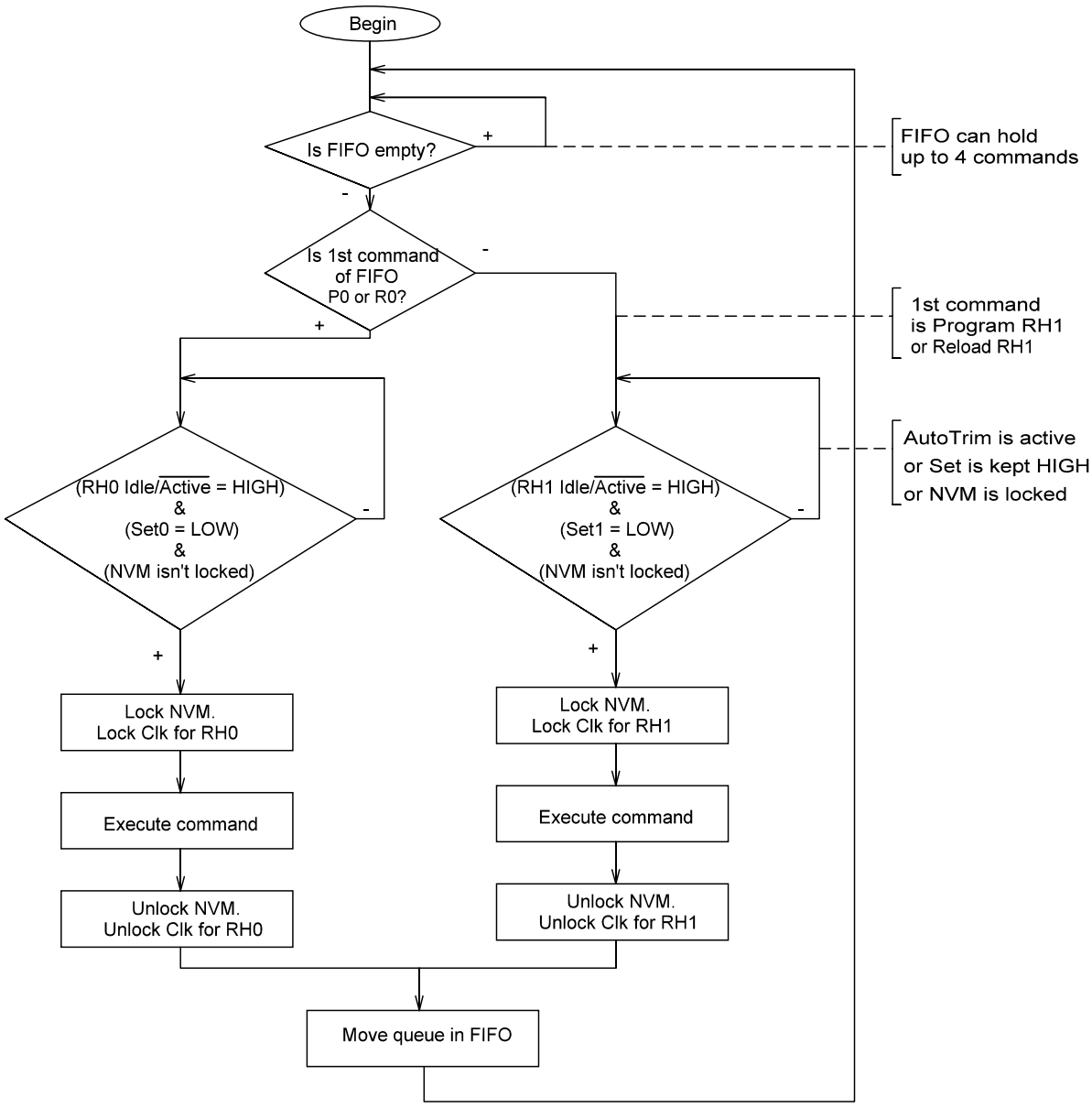


Figure 175. Flowchart of "Program" and "Reload" Signals

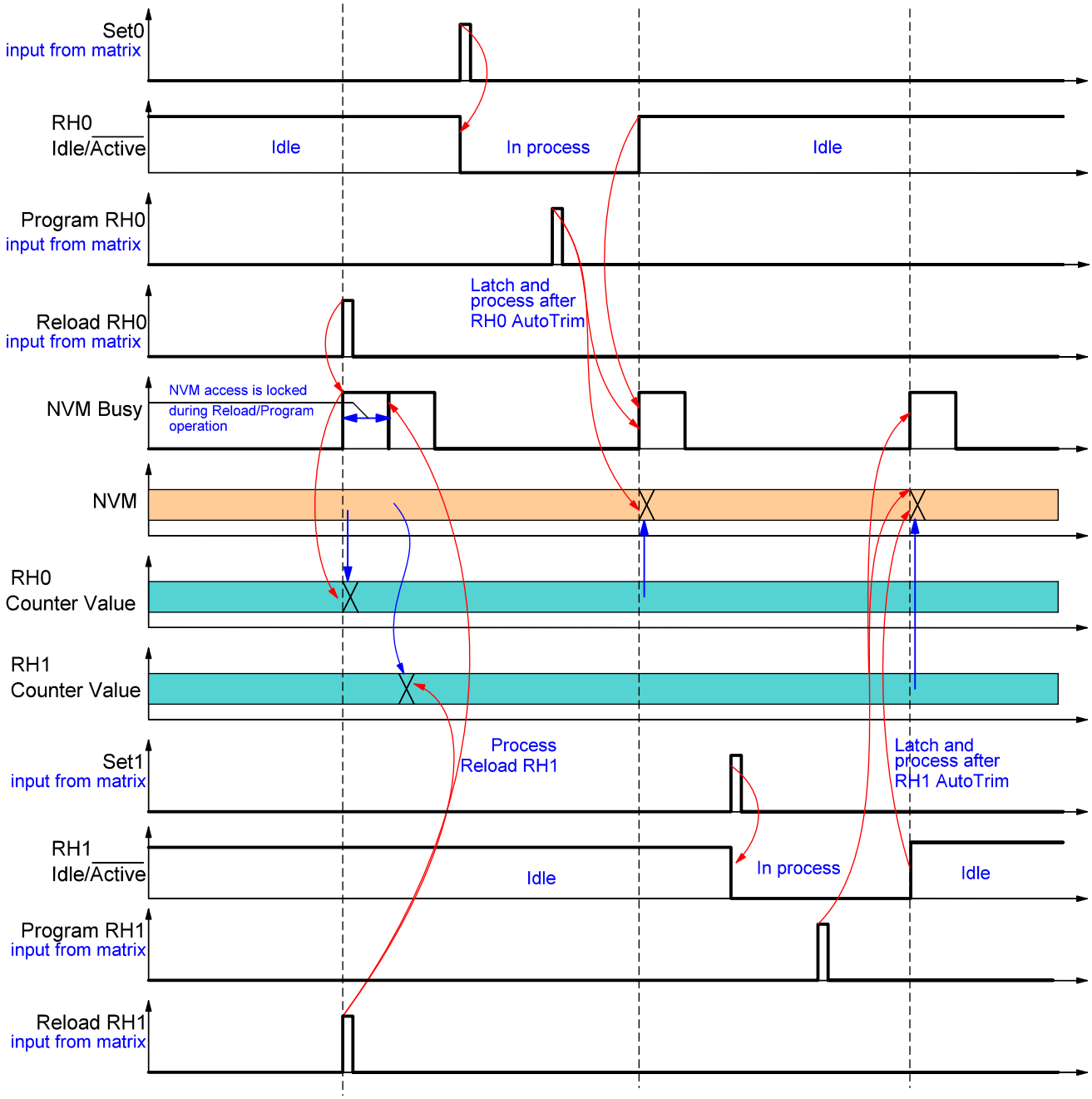


Figure 176. Example of Latching and Processing "Program" and "Reload" Signals

Since the access to the MTP NVM is disabled during NVM self-programming procedure, the device will not acknowledge it via I2C interface. This can be used to determine when the erase/programming cycle is completed (this feature can be used to maximize bus throughput). ACK polling can be used in this case.

If the device is still busy during the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be re-sent. Once the cycle is complete, then the device will return the ACK and the controller can proceed with the next Read or Write command.

12.4 Trimming Process Using Programmable Trim Block

There are several ways of implementing the trimming process using the PT block. One of the essential features of the PT macrocell is the Auto-Trim function described below. It allows the user to design simple calibration circuits for a wide variety of applications.

12.4.1 Trimming Process with Auto-Trim Option Enabled

For using the Auto-Trim function the following preliminary steps must be taken:

- Clear Auto_Cal _Dis_RHx NVM bit (0 is default value). This enables Auto-Trim function.
- Configure M1 MUX (registers [875:872]). It can be user system voltage feedback. If Auto-Trim function is used for two rheostats, M1 MUX must be configured for both rheostats (for cases when Set0 is latched and when Set1 is latched).
- Configure M2 MUX. It can be user desired set point threshold. If Auto-Trim function is used for two rheostats, M2 MUX must be configured for both rheostats (for cases when Set0 is latched and when Set1 is latched). Remember, that M2 MUX is simplified symbol of Chopper ACMP reference selection blocks.
- Configure M_CH0 (M_CH1) MUX to work with Chopper ACMP (M_CH0,1 MUXs are configured to work with Chop ACMP by default).
- Configure inverting or non-inverting Chopper ACMP output (registers [923], [920] and [882]).
- Select clock source (internal clock from internal pre-dividers or from connection matrix). Note that in Auto-Trim mode clock source frequency for the PT Block is limited by the Chopper Comparator time response. Therefore, the clock source frequency must not be greater than <f_{ChACMP}> kHz.
- Start the Auto-Trim process by setting the Set0 (Set1) input of PT block to a High level. The Auto-Trim process stops if one of three stop conditions occur:
  - 2nd time change on Up/Down input at the moment of rising edge on Clock input (see Figure 177).
  - the value of rheostat reaches its maximum (1023).
  - the value of rheostat reaches its minimum (0).

  Stop conditions result in a change of the Idle/Active signal, which resets the internal Auto-Trim logic.

  Note that the Set input is edge sensitive, but if the user keeps a High logic level at this input after reaching the set point, the PT block will continue to operate and continue to switch rheostat around the set point.
- To start new Auto-Trim process user should reapply a High level on Set input.

The detailed flow of Auto-Trim process is shown in Figure 177, Figure 178, Figure 179.

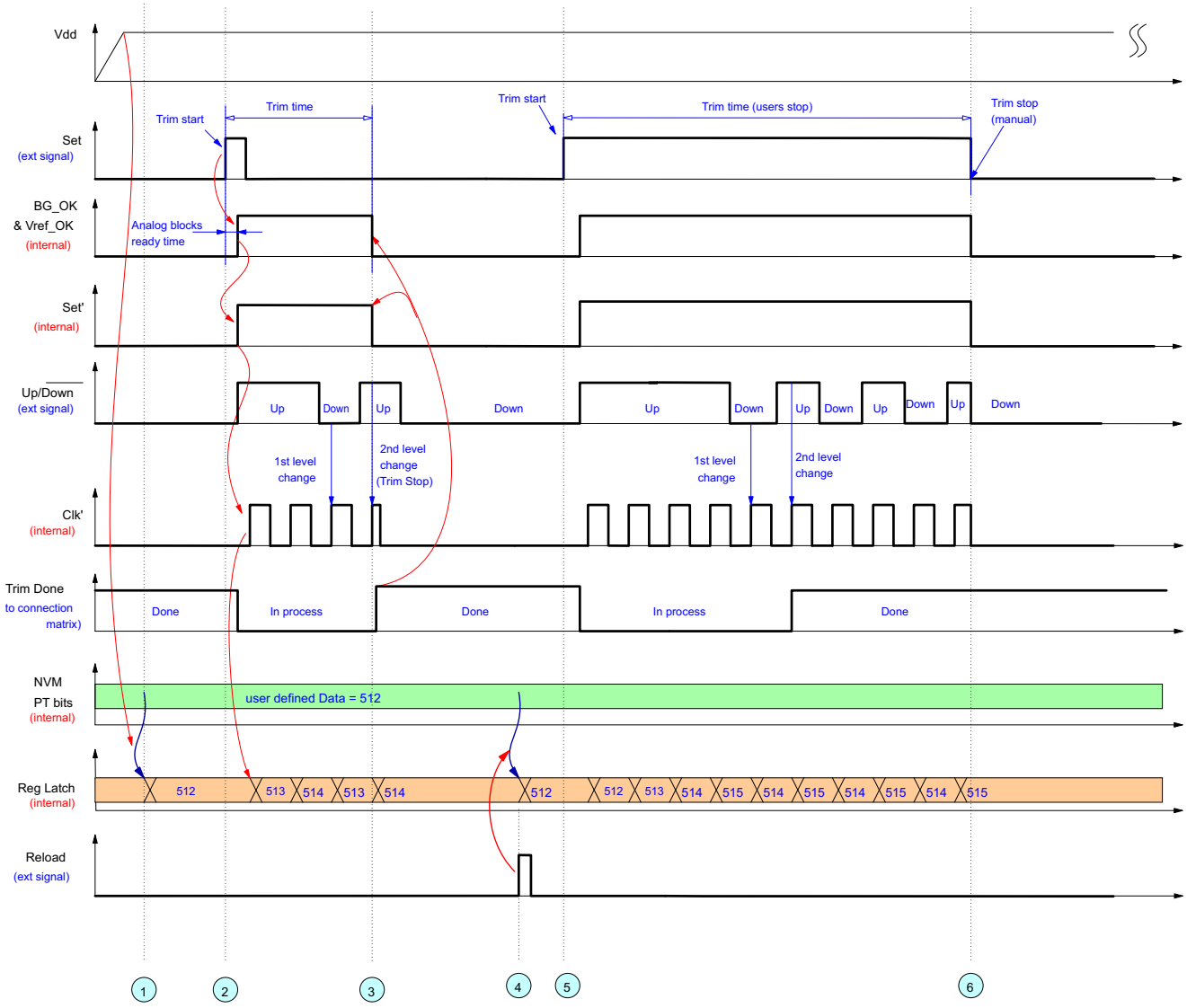


Figure 177. Example of Auto-Trim Process for a Single Rheostat

The key events of the Auto-Trim process are the following (see Figure 177):

1. During the startup event the SLG47004 loads the rheostat value from NVM to Internal Counter. In this example this value is 512.

2. The Trim process starts with a rising edge on Set input. This Set signal is latched until the end of the Auto-Trim process. The Set signal will enable the Chopper ACMP and the V_{REF}, if they were not enabled earlier. After a ready signal from analog blocks (BG_OK and V_{REF}_OK), the clock pulses for the internal counter are enabled. The counter starts to count up or down depending on the level at the Up/Down input. If user selected the “Internal Clock” option for Clock input, these clock pulses are generated automatically during trim time. Each rising edge of the Clock pulse changes the value of the counter and, consequently, the value of the rheostat.

3. There are three stop conditions for the Auto-Trim process:
   a. A subsequent change on Up/Down input at the moment of rising edge on Clock input.
   b. The value of the rheostat reaches its maximum (1023).
   c. The value of the rheostat reaches its minimum (0).

If the Set input signal is shorter than the trim time, the Auto-Trim process stops automatically after a stop condition occurs (event 3, Figure 177). However, if a stop condition comes and High logic level holds on the Set input, the rheostat value will be switched near the set point until a Low level on the Set input occurs (event 7, Figure 177). Note that the Idle/Active signal changes its level to High (Auto-Trim is done) even if the user keeps a High logic level at the Set input.

After the end of the Auto-Trim process, Chopper ACMP powers down and its output goes to a Low logic level.

4. After a rising edge at the “Reload” signal, the value from NVM is copied to the rheostat Internal Counter overwriting current rheostat settings.

5. During this event user starts Auto-Trim process, but holds High logic level at Set input for a time longer than Auto-Trim process.

6. A “Program” signal comes. The “Program” command is latched and will be executed at the end of the Auto-Trim process.

7. The Auto-Trim process stops when the signal at the Set input goes to Low level. Note that a logic High level at the Set input was held longer than the time that was needed for the Auto-Trim process.At the end of the Auto-Trim process, the SLG47004 starts the NVM self-programming routine to copy the rheostat value from Reg LATCH to MPT NVM.

Figure 178 shows a similar Auto-Trim example. The only difference is that the user defined clock source as “External clock” from connection matrix. The clock pulses are present at the Clock input all the time, but have effect (rheostat value changes) during Trim time only. The stop condition for this case is the following: PT block reaches boundary value of 1023 and the logic level at change Set input is Low.

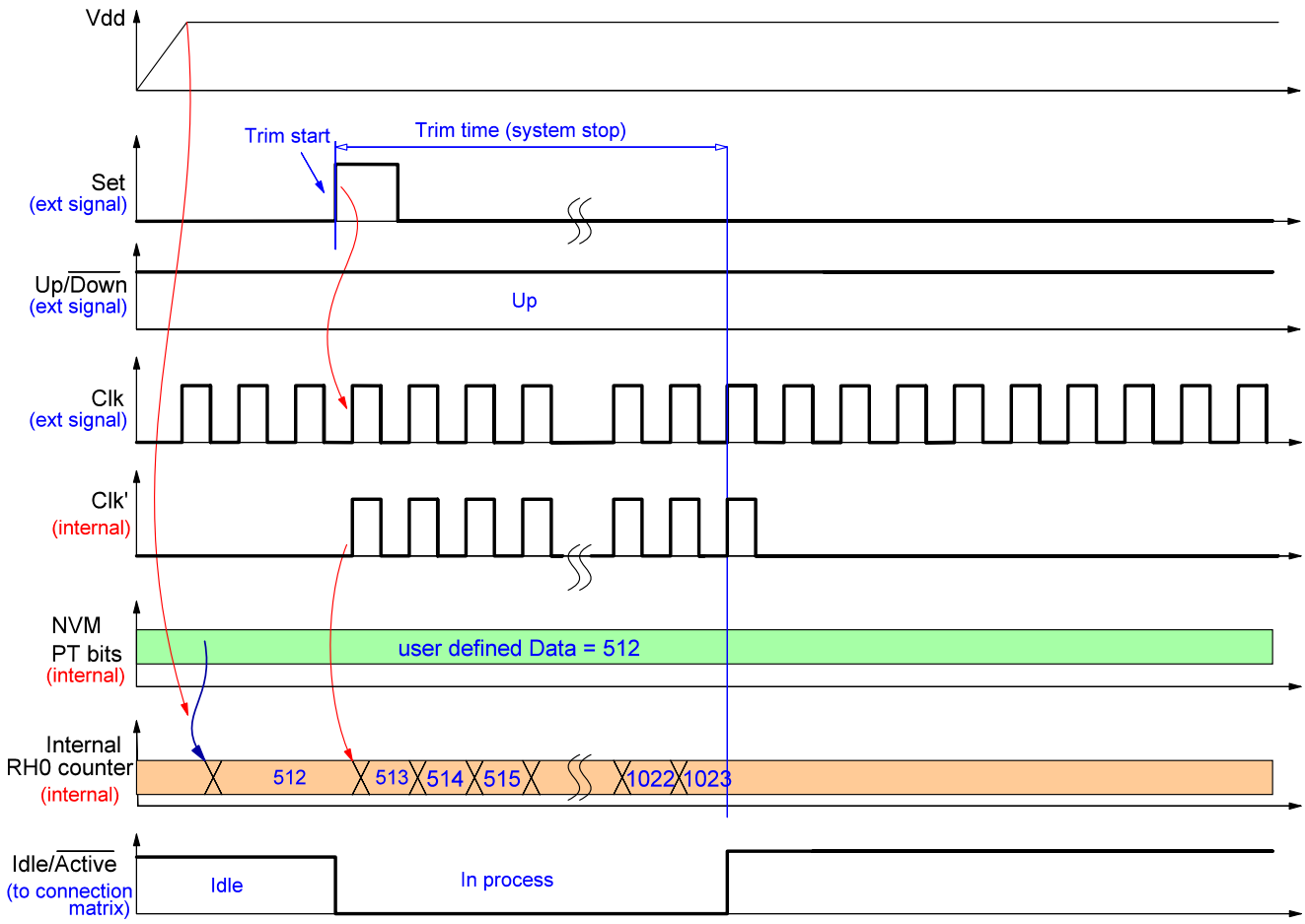


Figure 178. Example of Auto-Trim Process with External Clock Signal

Figure 179 shows Auto-Trim process flow for two rheostats.

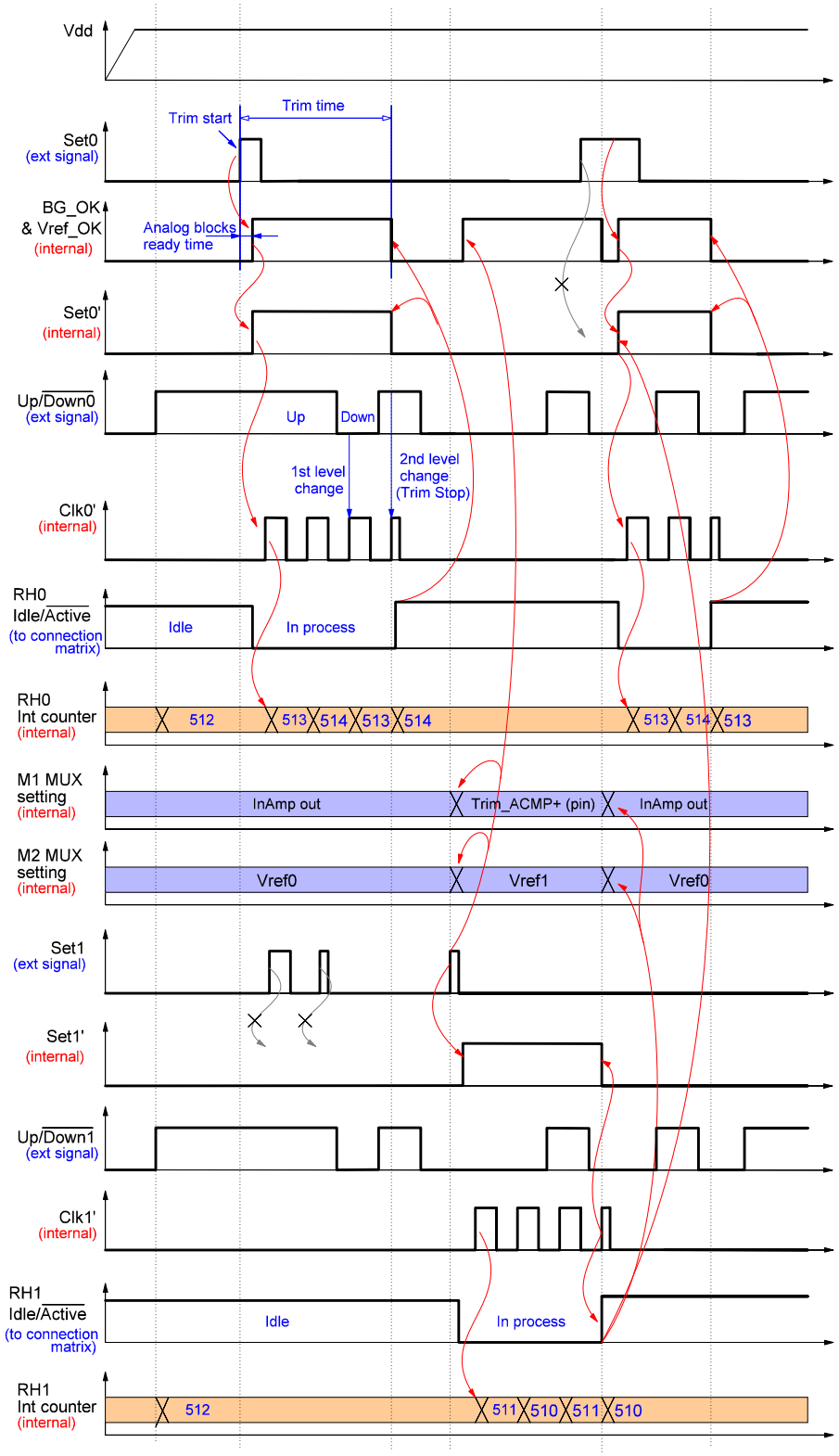


Figure 179. Example of Auto-Trim Process for Two Rheostats

12.4.2 I²C Controlled Trimming Process with Auto-Trim Option Enabled

It's possible to start the Auto-Trim process via I²C interface. In this case the user must configure the SLG47004 PT macrocell as described in section 12.4.1 Trimming Process with Auto-Trim Option Enabled. To start the Auto-Trim process via I²C interface the user can use I²C virtual inputs.

Also, an external I2C controller device can force the SLG47004 to reload the rheostat value from NVM ("Reload" command) or to copy rheostat value to NVM ("Program" command) using I2C virtual inputs.

See Figure 180 for an example of the Auto-Trim process under external I²C controller control.

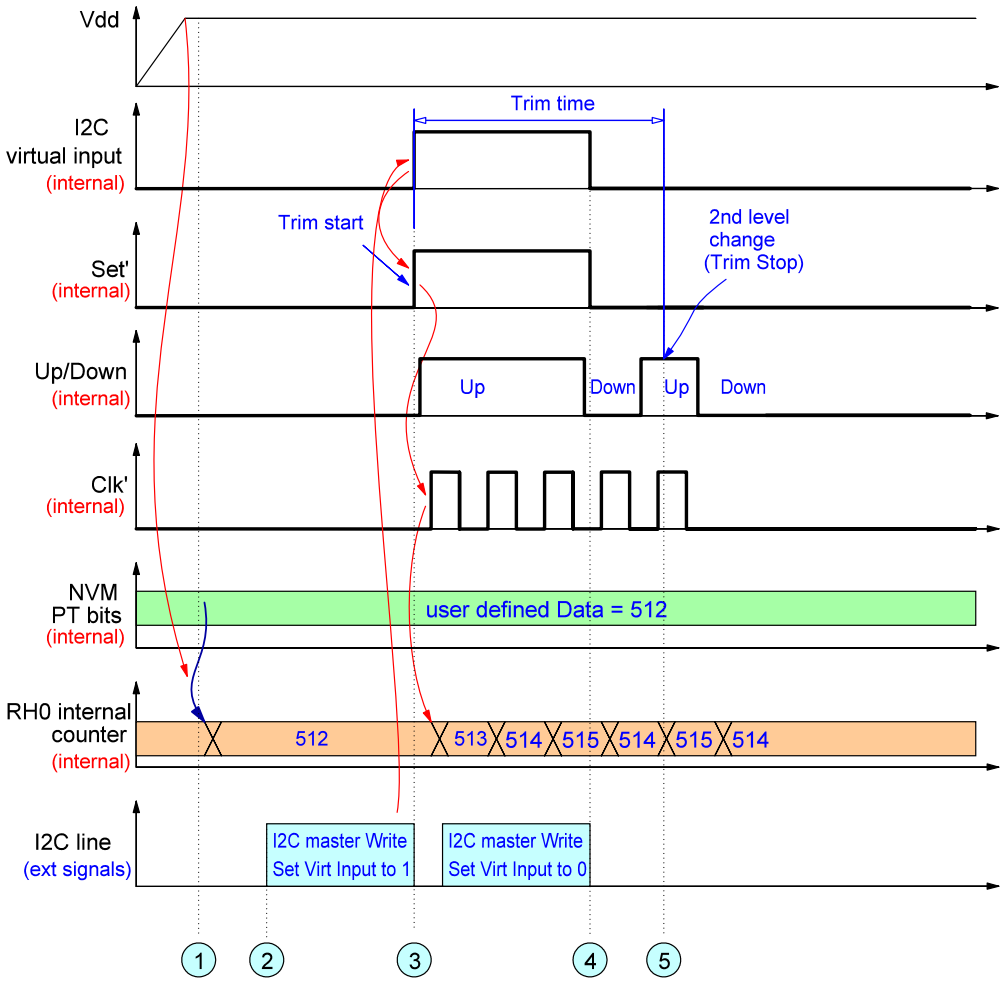


Figure 180. Example of Auto-Trim Process via I²C

The key events of the Auto-Trim process under external I²C controller control are as follows:

1. During the startup event the SLG47004 loads the rheostat value from the NVM to the Internal Counter. In the example this value is 512.

2. I²C controller sends the message to set High one of the I²C virtual inputs that is connected with Set input of the PT macrocell.

3. After the I²C message is received and processed, the I²C virtual input and the Set input will be at a High logic level. The Auto-Trim process begins.

4. I²C controller clears the virtual input and, consequently, the Set input. The Auto-Trim process goes on until a trim stop condition occurs.

5. The Auto-Trim process ends. The stop condition in this example is a 2nd change on Up/Down input at the moment of rising edge on the Clock input and Low level at the Set input.

12.4.3 Changing Rheostat Value Directly via I²C

The user can perform their own trim algorithm setting the rheostat value directly via I²C interface. In the example below, a microcontroller uses a user defined trim algorithm to change SLG47004's rheostat via I²C interface (Figure 181). Note that during Auto-Trim process SLG47004 will return nACK, if controller tries to get access (both read and write) to rheostats registers via I²C.

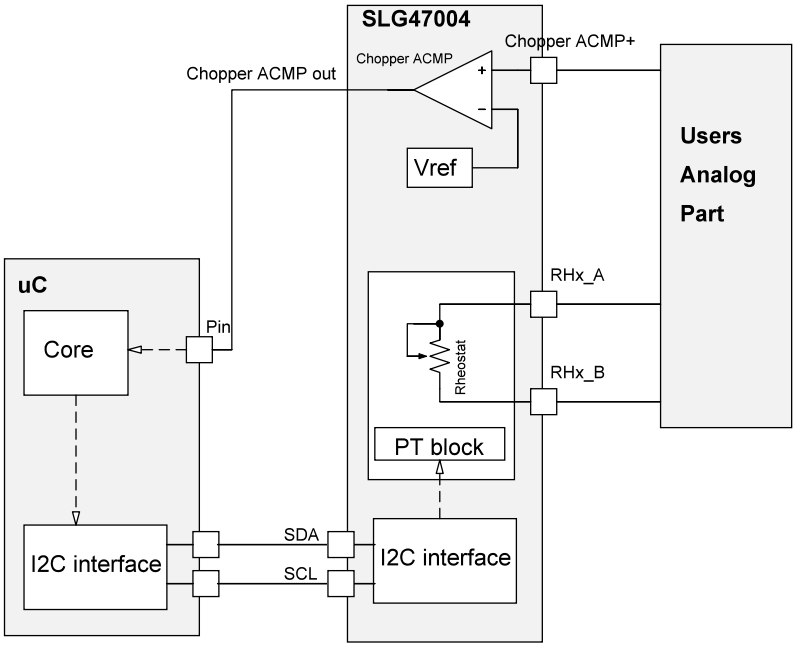


Figure 181. Example of Hardware Configuration

Note that the PT Registers are allowed to read and write via communication interface, if not protected.

The preliminary configuration of system shown in Figure 181 is the following:

- Auto_Cal _Dis_RHx bit is set to 1 (disable Auto-Trim mode).
- M1 MUX (registers [875:872])) is configured to work with user system voltage feedback (pin Chop_ACMP+).
- M2 MUX is configured to work with SLG47004 programmable V_{REF}. Note that M2 MUX is simplified symbol of Chopper ACMP reference selection blocks (see section 9.3 Chopper Analog Comparator).
- Chopper ACMP is powered up from connection matrix. Chopper ACMP out is connected to output pin.
- No Clock source for PT block.

The example of a system trim via I²C is shown in the figure below. In this example the I²C controller uses a simple approximation algorithm for reaching the set point. Every next step the rheostat code is changed by ±(Previous rheostat code step value/2). The sign depends on the Chopper ACMP output. The algorithm steps are as follows:

1. Set rheostat code to 1024/2 = 512.
2. Wait until the system settles down and check if Chopper ACMP output = 1, then Next_rheostat_code = 512 + (512/2). If Chopper ACMP output = 0, then Next_rheostat_code = 512 - (512/2).
3. Repeat previous step until Next_rheostat_code = Prev_rheostat_code ± 1.

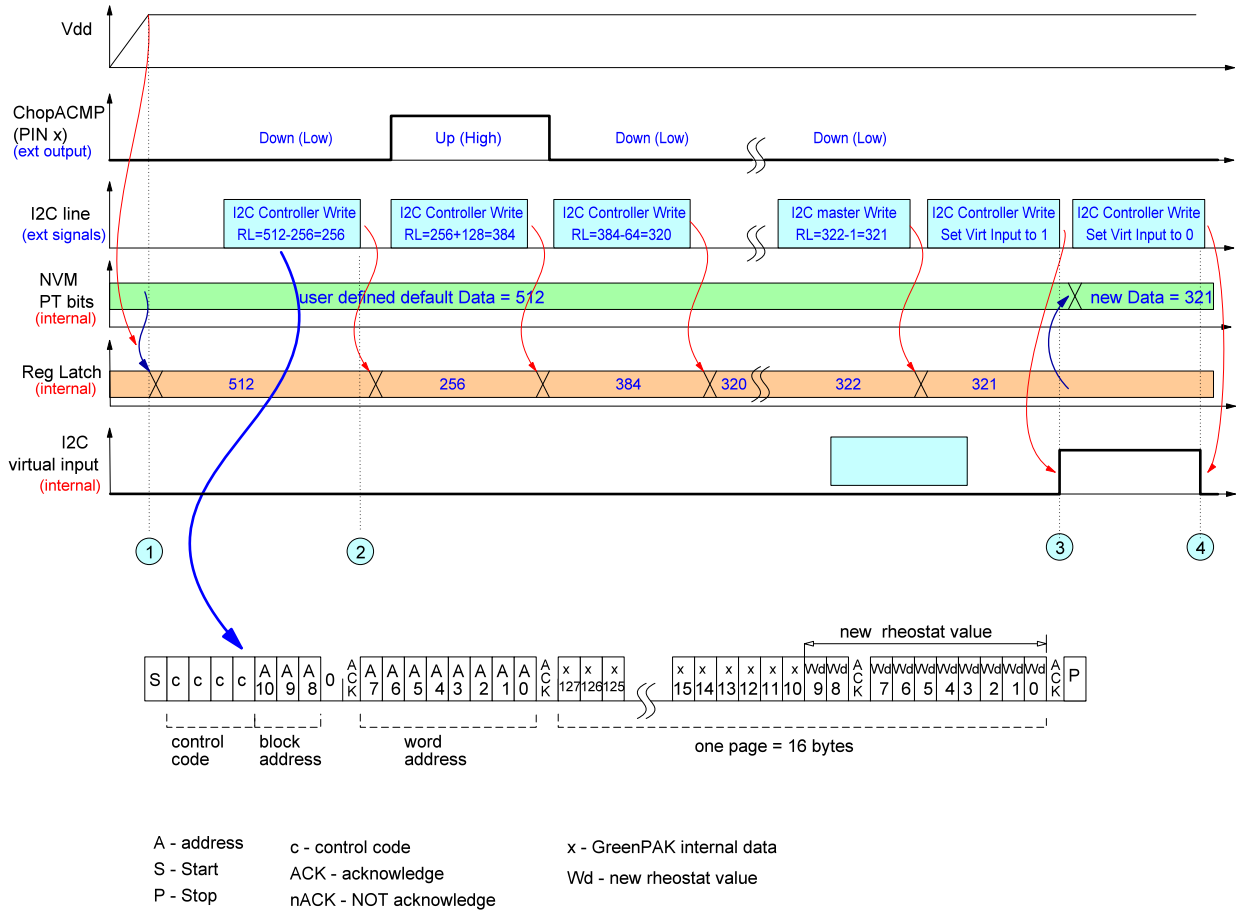


Figure 182. Example of User Specific Trimming Process under I²C Controller Control

The key events of a user specific trimming process under I²C controller control are as follows:

1. During the startup event the SLG47004 loads the rheostat value from NVM to Internal Counter. In the example this value is 512.

2. I²C controller writes a new value to the Rheostat's Internal Counter according to Chopper ACMP output. Note that the minimum time for changing the rheostat code depends on the time response of the user system.

3. After the trim process is completed, the I²C controller sets the I²C virtual input to logic "1". This input is connected to the "Program" signal of the PT macrocell. The rising edge on this input starts the NVM self-programming routine.

4. The I²C controller clears the I²C virtual input.

Additionally, the I²C Controller macrocell can use internal resources such as an ADC to read the system data, find the error, and then adjust the Rheostat value. Also, it is possible to change the Rheostat value for different conditions. For example, the I²C Controller macrocell can change the Rheostat value based on the temperature change to reduce the system error.

12.5 Using Chopper ACMP

When the Auto-Trim Function is disabled, the Chopper comparator can be used as a standalone analog comparator. Inputs of the Chopper ACMP are selected by the M1 and M2 analog MUXs. Output of the Chopper ACMP can be optionally inverted by reg [882]. This comparator output is the input [55] of the connection matrix. In

case of a disabled Auto-Trim Function, the power up source for the Chopper ACMP comes from connection matrix. Please refer to section 9. Analog Comparators for more details.

12.6 Digital Rheostats Typical Performance

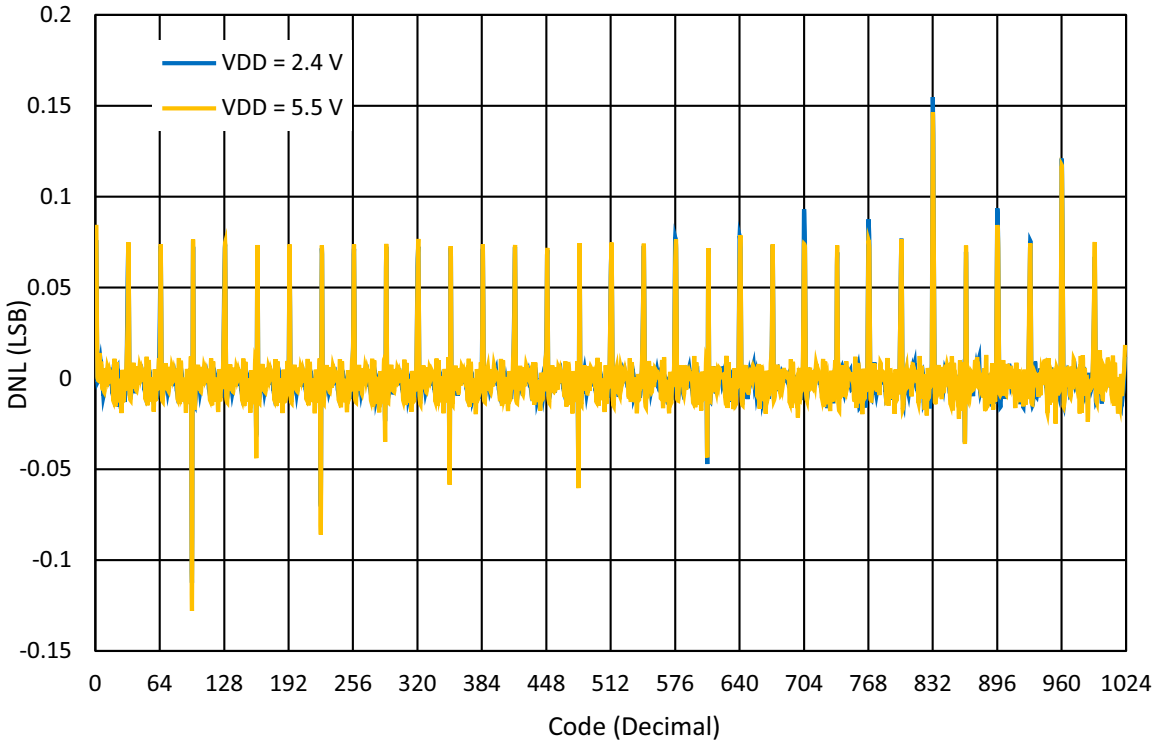


Figure 183. DNL vs. Digital Code, Rheostat Mode (V_{AB} = 1 V) at T_A = 25 °C

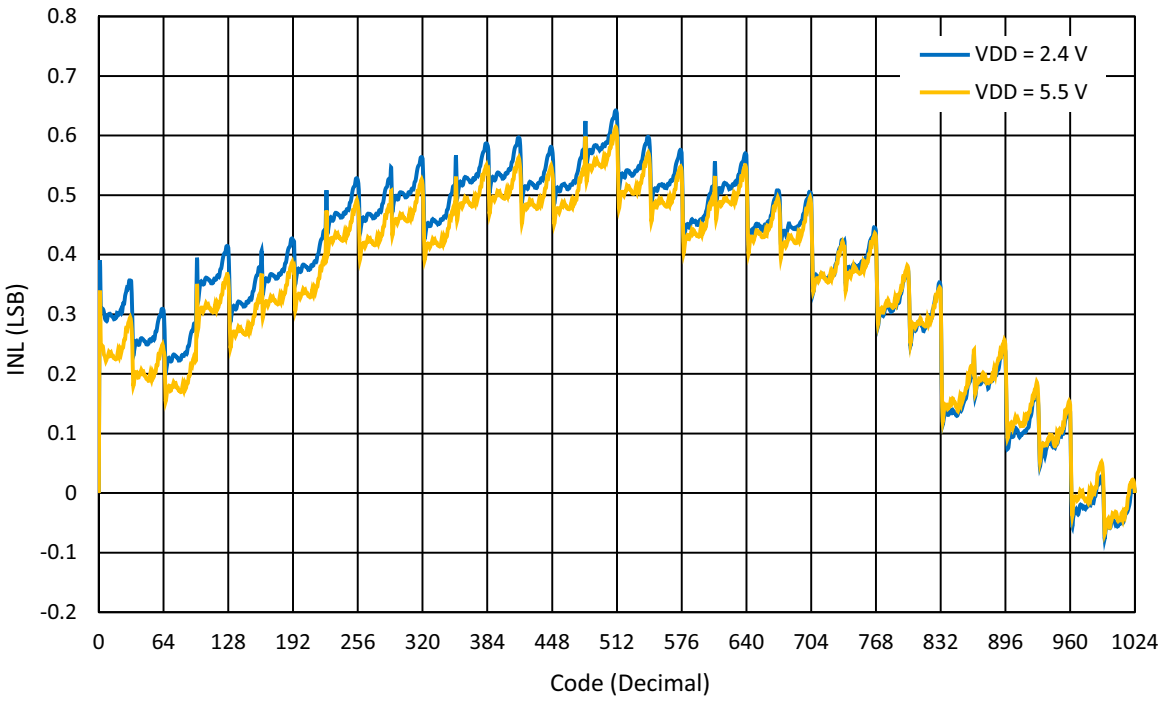


Figure 184. INL vs. Digital Code, Rheostat Mode (V_{AB} = 1 V) at T_A = 25 °C

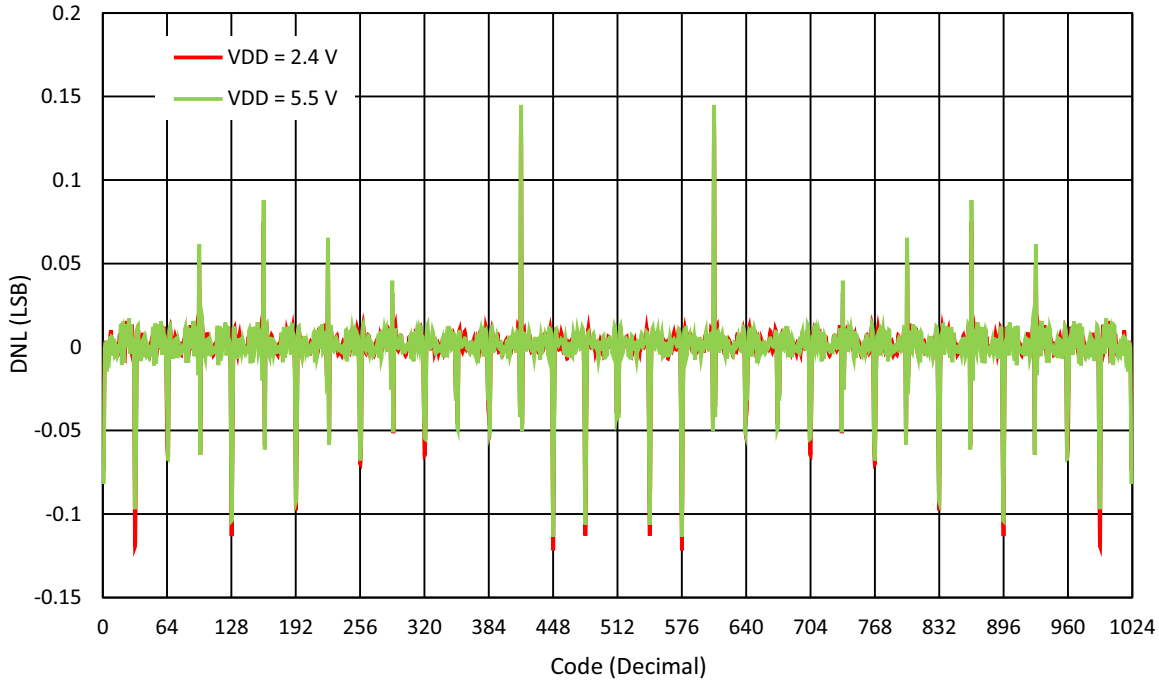


Figure 185. DNL vs. Digital Code, Potentiometer Mode (V_{AB} = 1 V) at T_A = 25 °C

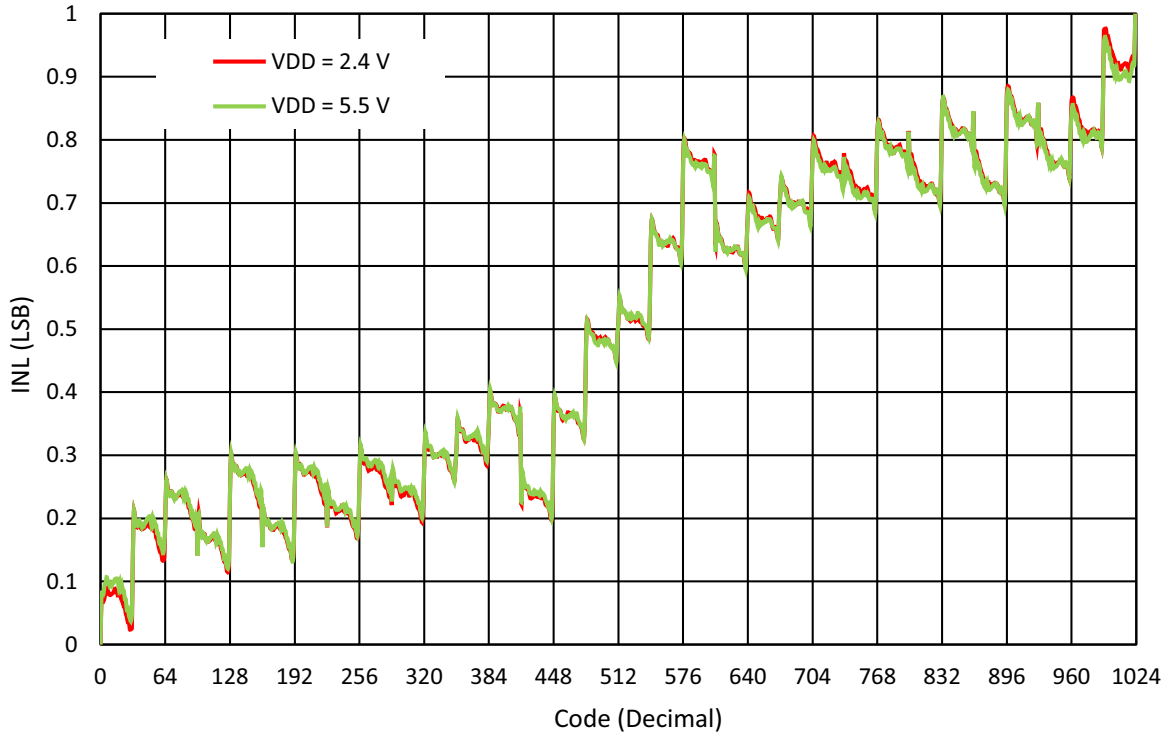


Figure 186. INL vs. Digital Code, Potentiometer Mode (V_{AB} = 1 V) at T_A = 25 °C

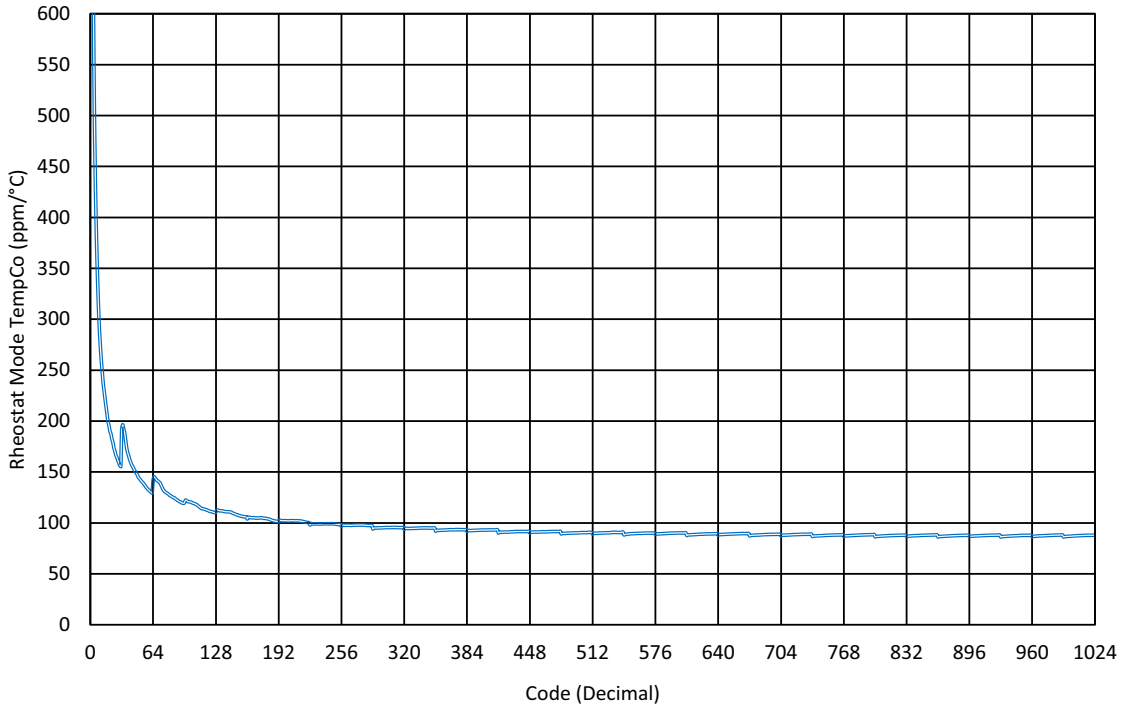


Figure 187. $(\Delta R_{AB}/R_{AB})/\Delta T_A$ Rheostat Mode TempCo

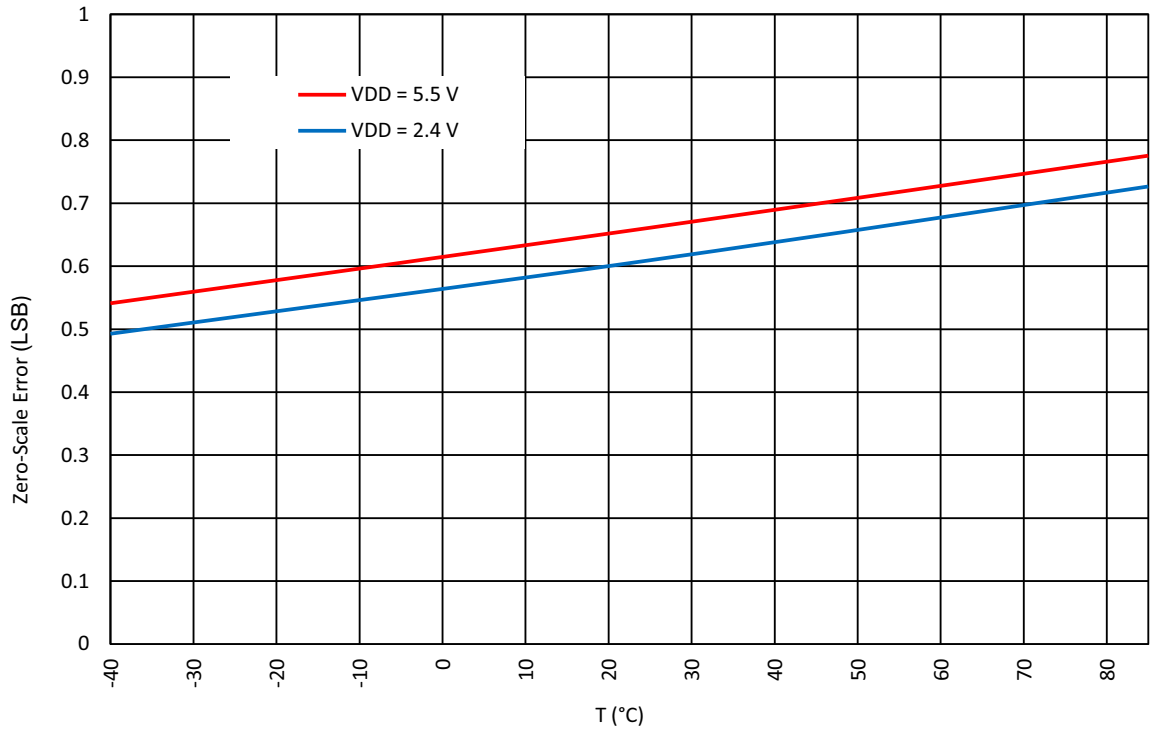


Figure 188. RHx Zero Scale Error vs. Temperature (V_{IN} = 1 V)

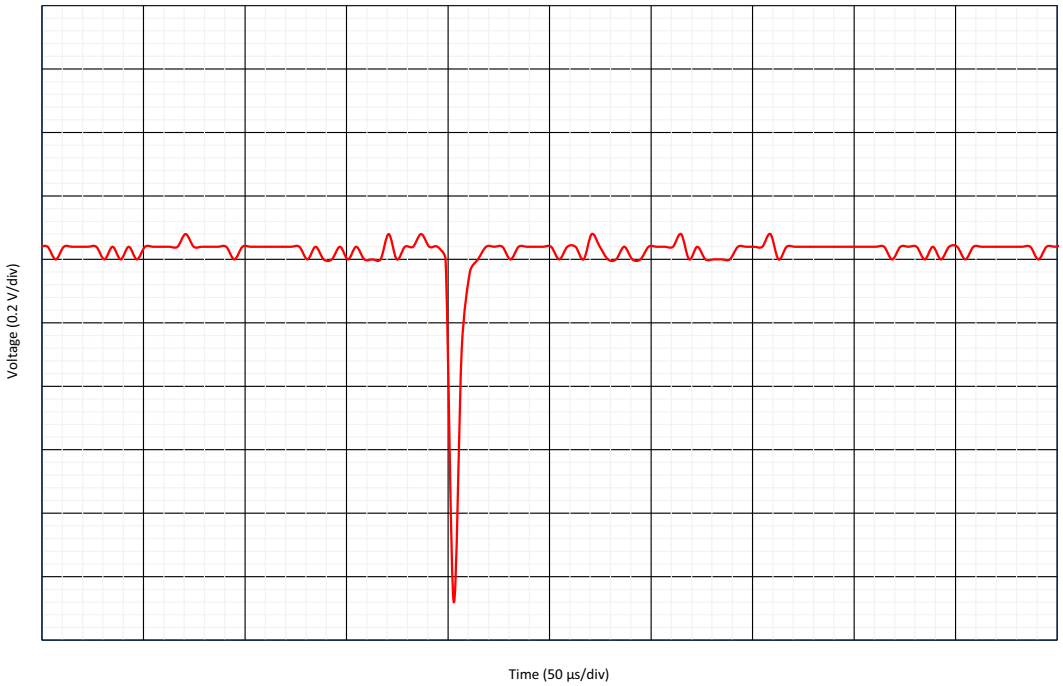


Figure 189. Transition Glitch in Worst Case (Code = 511 to Code = 512)

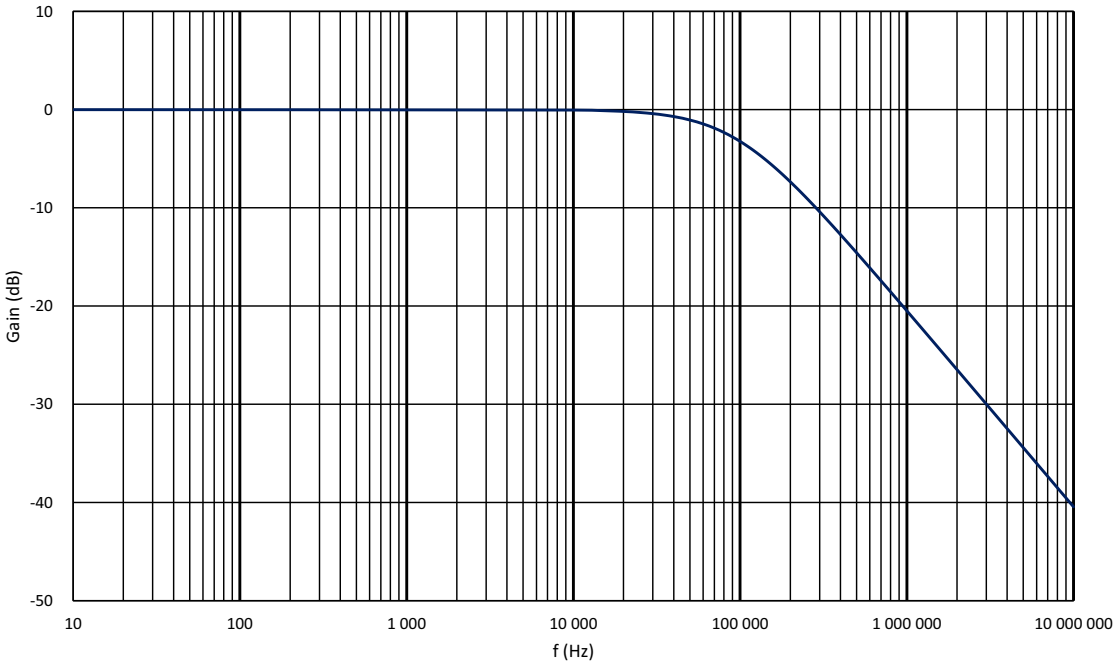


Figure 190. Gain vs. Frequency (Code = 512) at T_A = 25 °C, V_{DDA} = 5 V

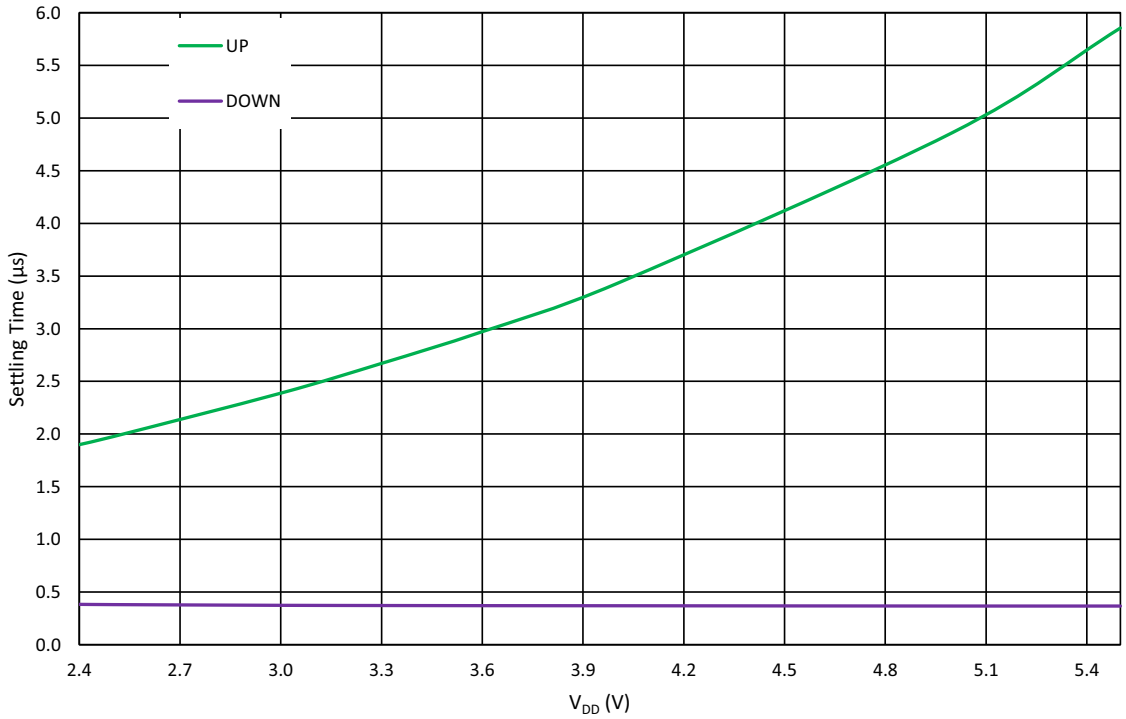


Figure 191. RHx Settling Time vs. V_{DD} at I_{LOAD} = 1 mA, T_A = 25 °C

13. Programmable Delay/Edge Detector

The SLG47004 has a programmable time delay logic cell available, that can generate a delay that is selectable from one of four timings (time 2) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay, as well as glitch rejection during the delay period. See Figure 193 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

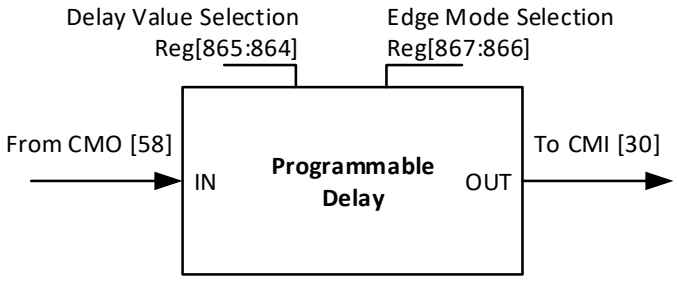


Figure 192. Programmable Delay

13.1 Programmable Delay Timing Diagram - Edge Detector Output

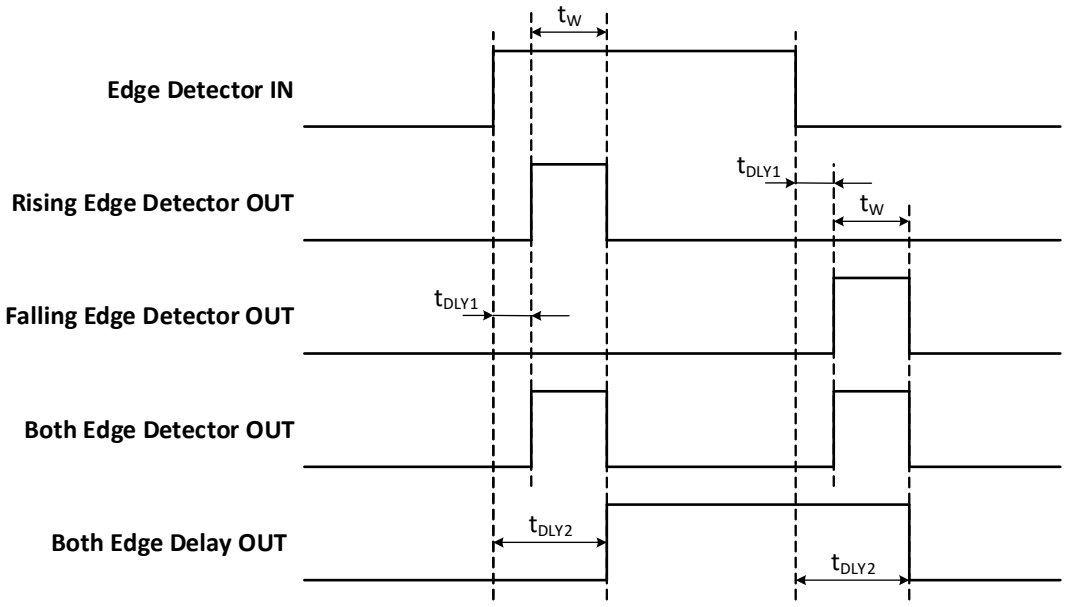


Figure 193. Edge Detector Output

Please refer to section 3.7.2 Programmable Delay Expected Typical Delays and Widths.

14. Additional Logic Function. Deglitch Filter

The SLG47004 has one Deglitch Filter macrocell with inverter function that is connected directly to the Connection matrix inputs and outputs. In addition, this macrocell can be configured as an Edge Detector, with the following settings:

- Rising Edge Detector
- Falling Edge Detector
- Both Edge Detector
- Both Edge Delay.

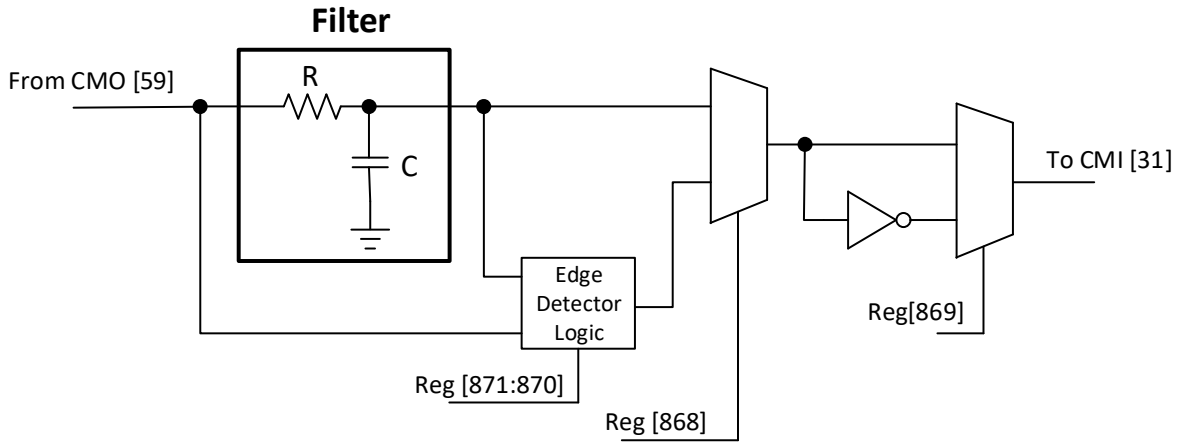


Figure 194. Deglitch Filter or Edge Detector

15. Voltage Reference

15.1 Voltage Reference Overview

The SLG47004 has a Voltage Reference (V_{REF}) Macrocell to provide reference to analog comparators and operational amplifiers. The macrocell also has the option to output reference voltages on external pins (see Table 2). $V_{REF}0$ and $V_{REF}1$ share output buffers with Temperature sensor. Note that user can use any of output buffers, but Temperature sensor is calibrated for $V_{REF}1$ output buffer. See Table 35 for the available selections for each analog comparator. Also, see Figure 195, Figure 196, and Figure 197, which show the reference output structure.

Also there is a high drive voltage reference macrocell called HD Buffer. The purpose of this macrocell is to provide stable voltage to the relatively high-power load (please refer to section 3.11 HD Buffer Specifications). HD Buffer has shared voltage reference source with the Op Amp0 V_{REF}. User can select output voltage in the range from $V_{DD}/64$ to V_{DD} with a step $V_{DD}/64$, or output voltage in a range from 32 mV to 2.048 V with a step 32 mV (see Figure 197).

Note that Chopper ACMP will automatically enable HD Buffer if HD Buffer is selected as a source for Chopper ACMP In-signal (reg [946] = 0) and Chopper ACMP is powered up.

15.2 V_{REF} Selection Table

Table 35. V_{REF} Selection Table

SEL [5:0]	V_{REF} [V]	SEL [5:0]	V_{REF} [V]
0	0.032	33	1.088
1	0.064	34	1.12
2	0.096	35	1.152
3	0.128	36	1.184
4	0.16	37	1.216
5	0.192	38	1.248
6	0.224	39	1.28
7	0.256	40	1.312
8	0.288	41	1.344
9	0.32	42	1.376
10	0.352	43	1.408
11	0.384	44	1.44
12	0.416	45	1.472
13	0.448	46	1.504
14	0.48	47	1.536
15	0.512	48	1.568
16	0.544	49	1.6
17	0.576	50	1.632
18	0.608	51	1.664
19	0.64	52	1.696
20	0.672	53	1.728
21	0.704	54	1.76
22	0.736	55	1.792
23	0.768	56	1.824
24	0.8	57	1.856

Table 35. V_{REF} Selection Table (Cont.)

SEL [5:0]	V_{REF} [V]	SEL [5:0]	V_{REF} [V]
25	0.832	58	1.888
26	0.864	59	1.92
27	0.896	60	1.952
28	0.928	61	1.984
29	0.96	62	2.016
30	0.992	63	2.048
31	1.024	64	External
32	1.056	-	-

15.3 V_{REF} Block Diagram

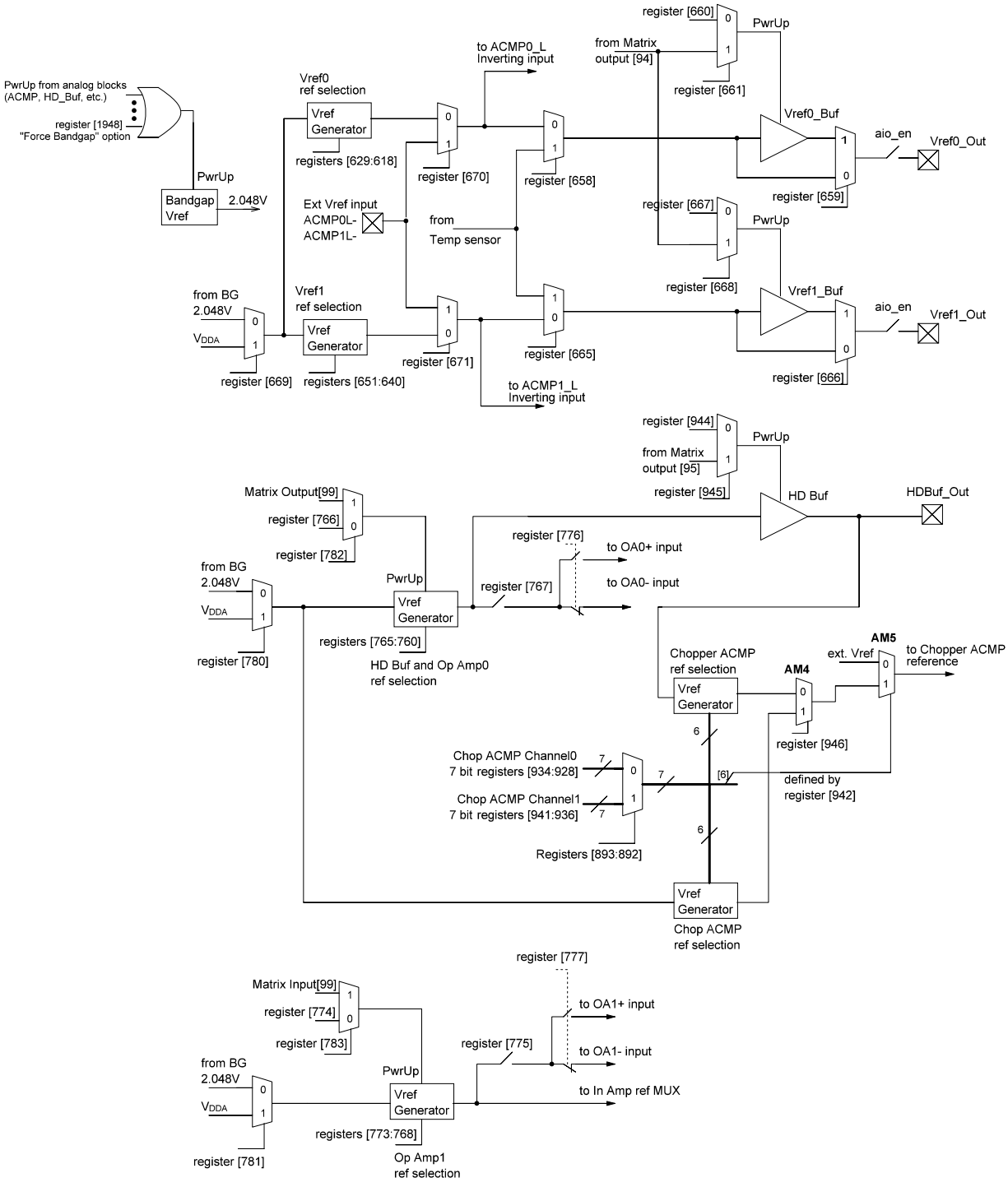


Figure 195. Generalized V_{REF} Structure

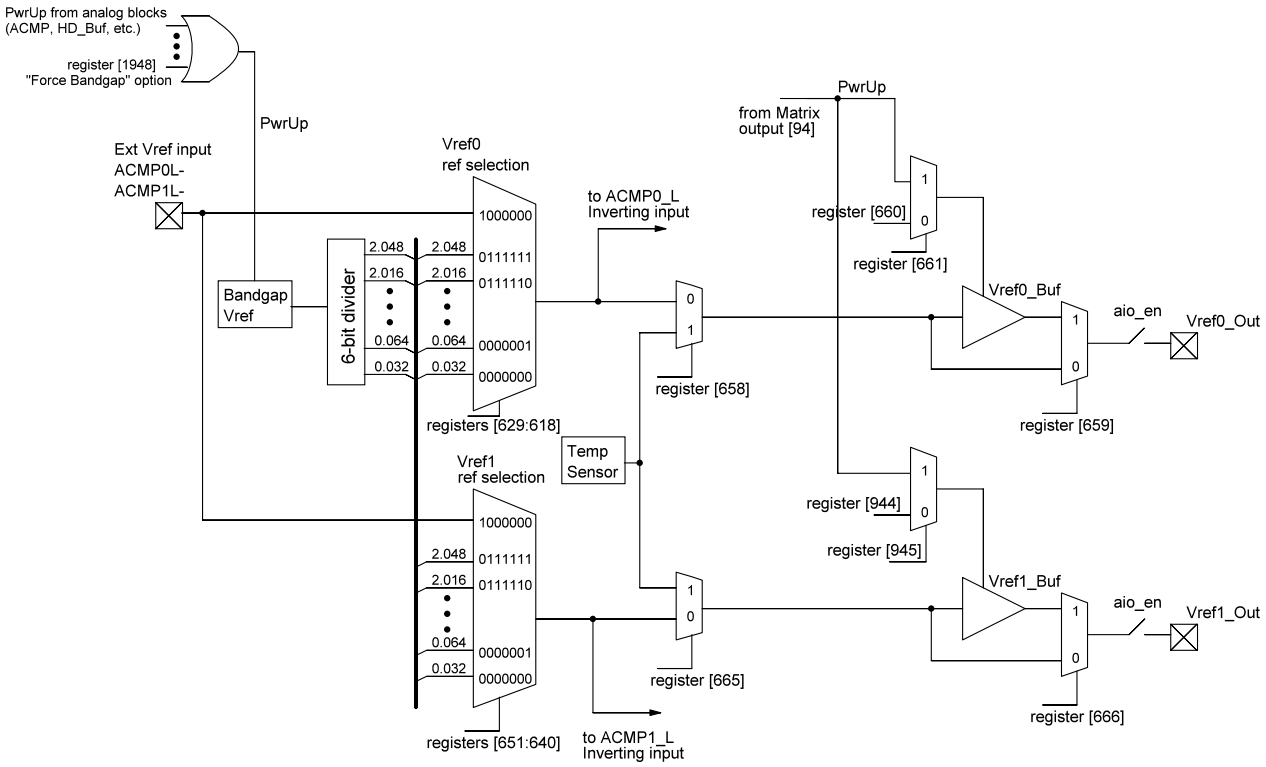


Figure 196. ACMP0L, ACMP1L Voltage Reference Block Diagram

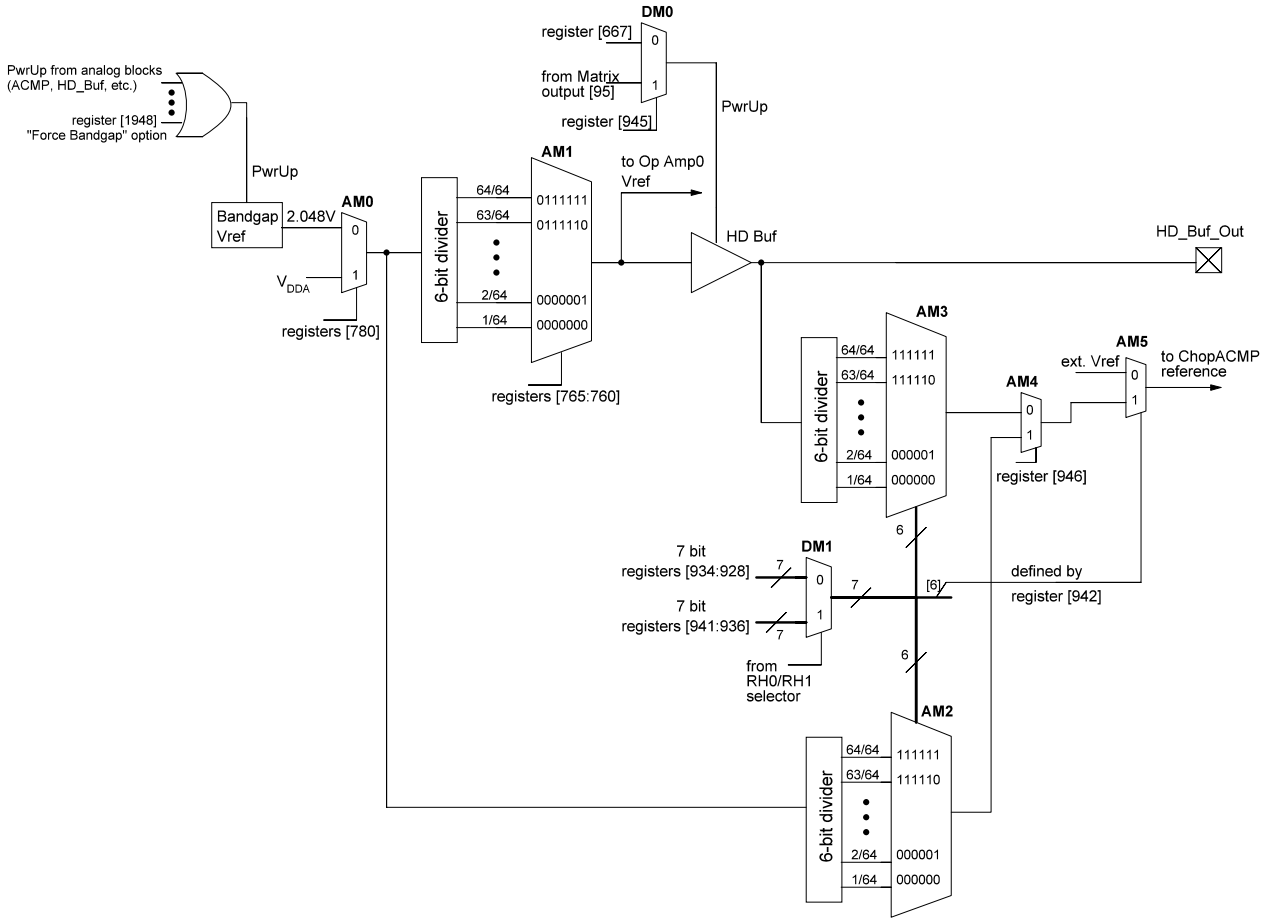


Figure 197. HD Buffer and Chopper ACMP Reference Block Diagram

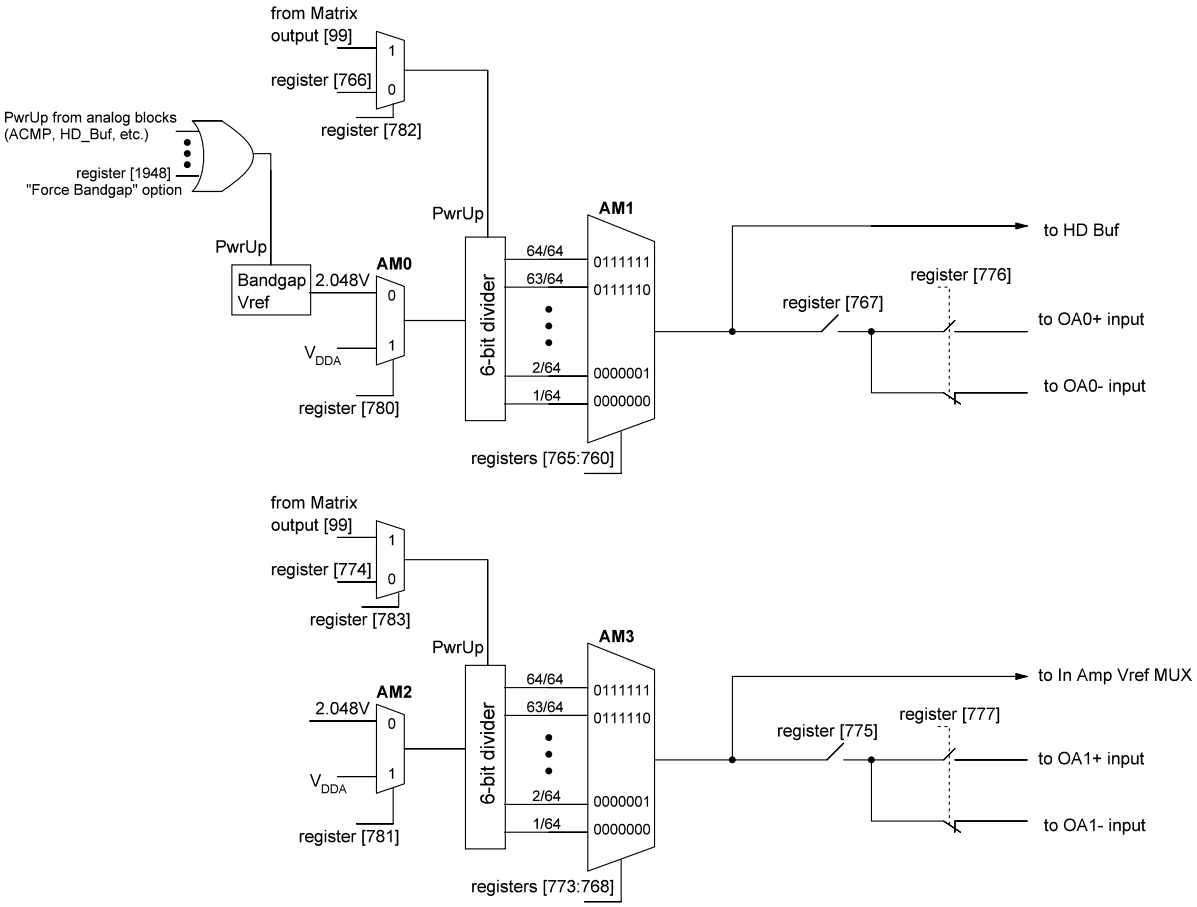


Figure 198. Operational Amplifiers Voltage Reference Block Diagram

15.4 Voltage Reference Typical Performance

Note: It is not recommended to use V_{REF} connected to external pin without buffer.

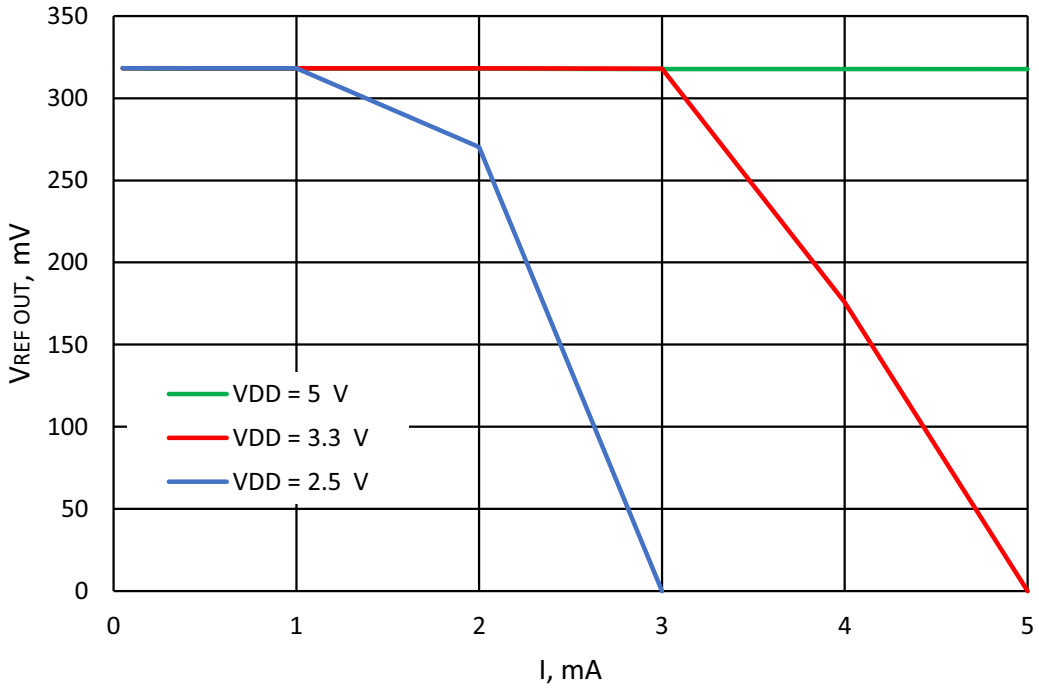


Figure 199. Typical Load Regulation, V_{REF} = 320 mV, T = -40 °C to +85 °C, Buffer - Enable

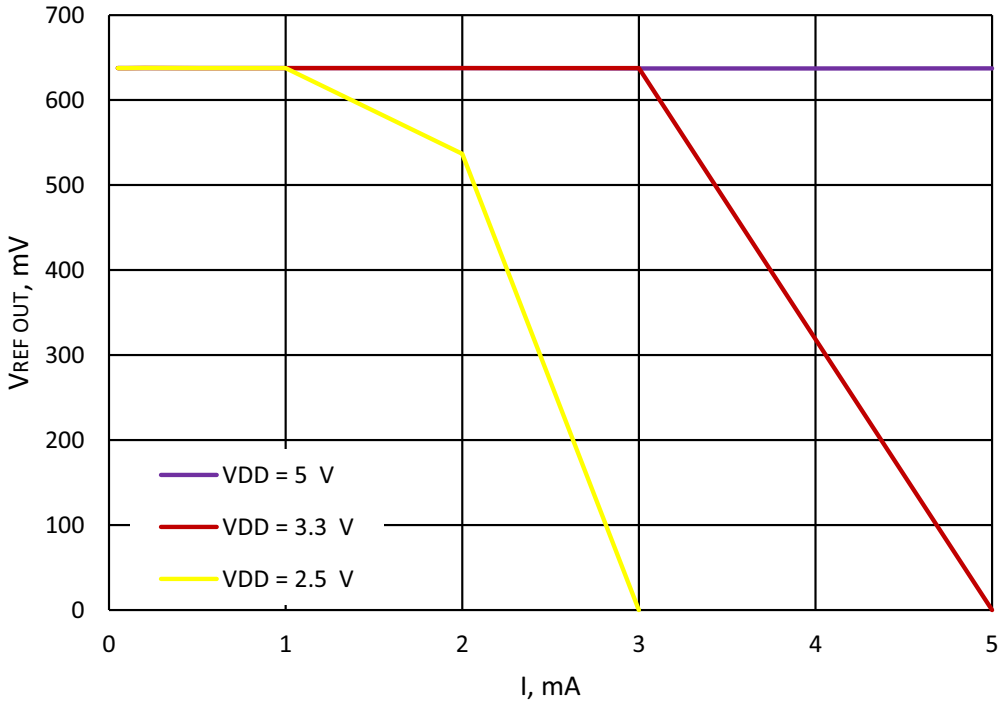


Figure 200. Typical Load Regulation, V_{REF} = 640 mV, T = -40 °C to +85 °C, Buffer - Enable

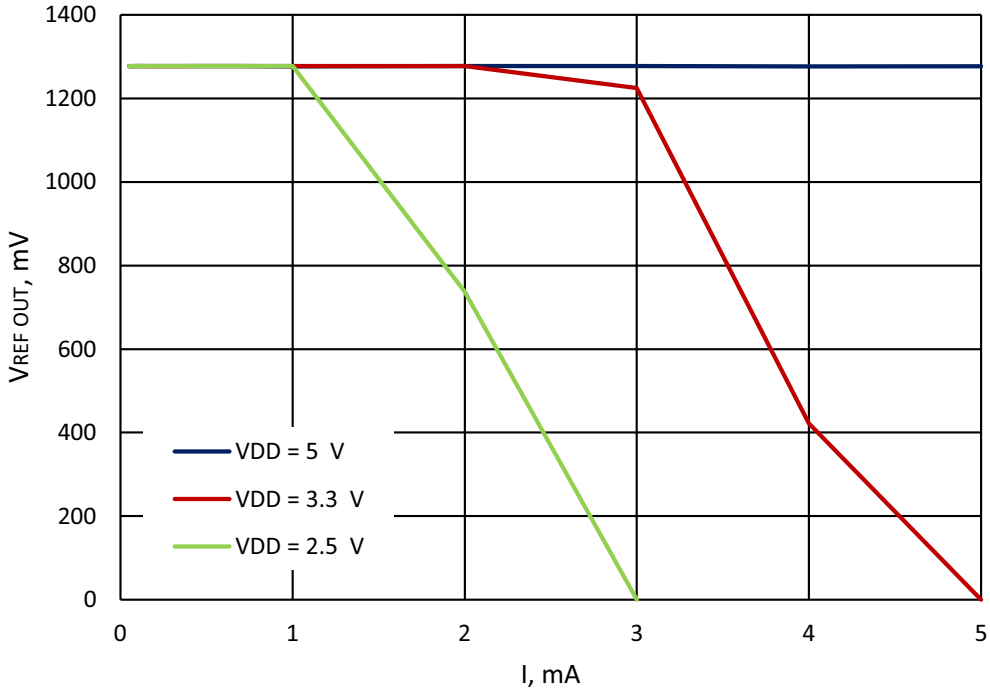


Figure 201. Typical Load Regulation, V_{REF} = 1280 mV, T = -40 °C to +85 °C, Buffer - Enable

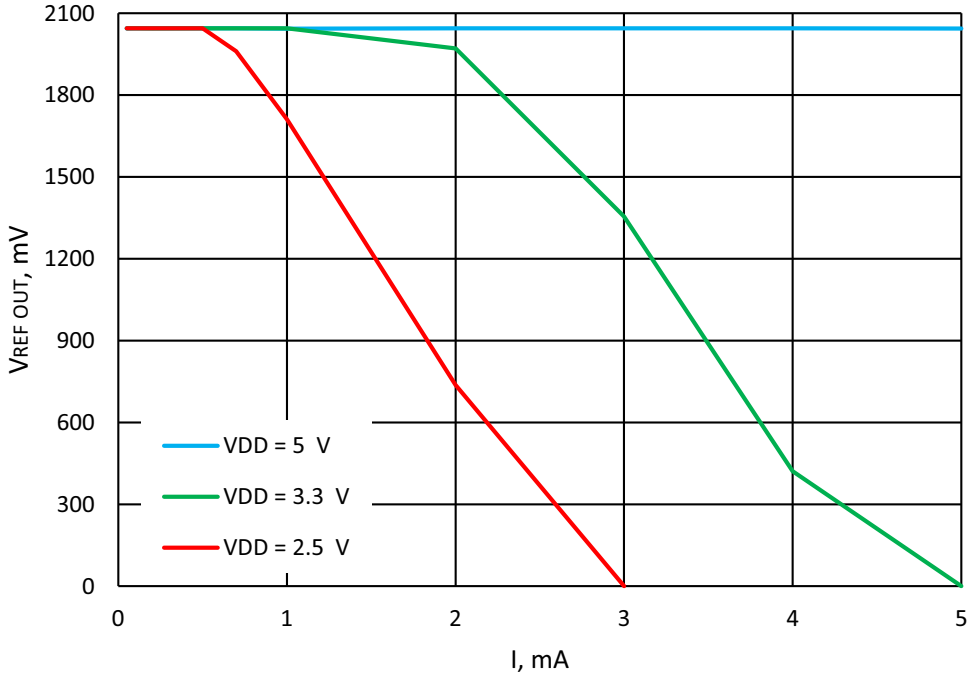


Figure 202. Typical Load Regulation, V_{REF} = 2048 mV, T = -40 °C to +85 °C, Buffer - Enable

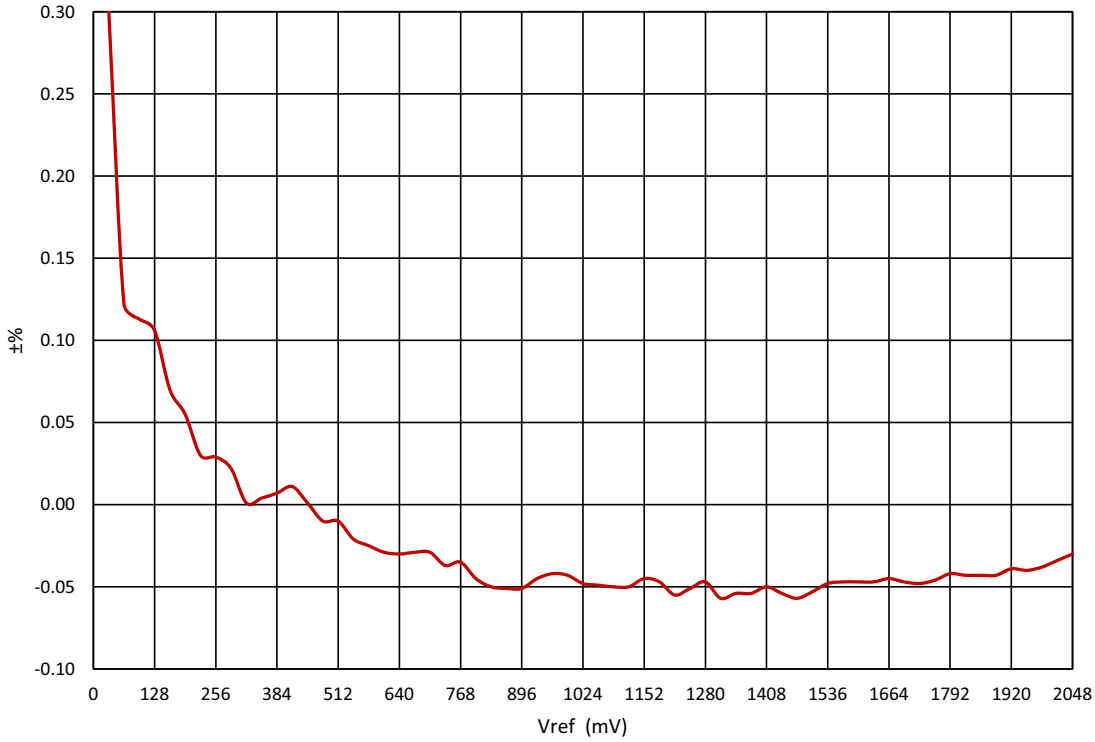


Figure 203. Typical Input Offset Voltage vs. V_{REF} at V_{DD} = 2.4 V to 5.5 V, T_A = 25 °C, Buffer Disabled

.

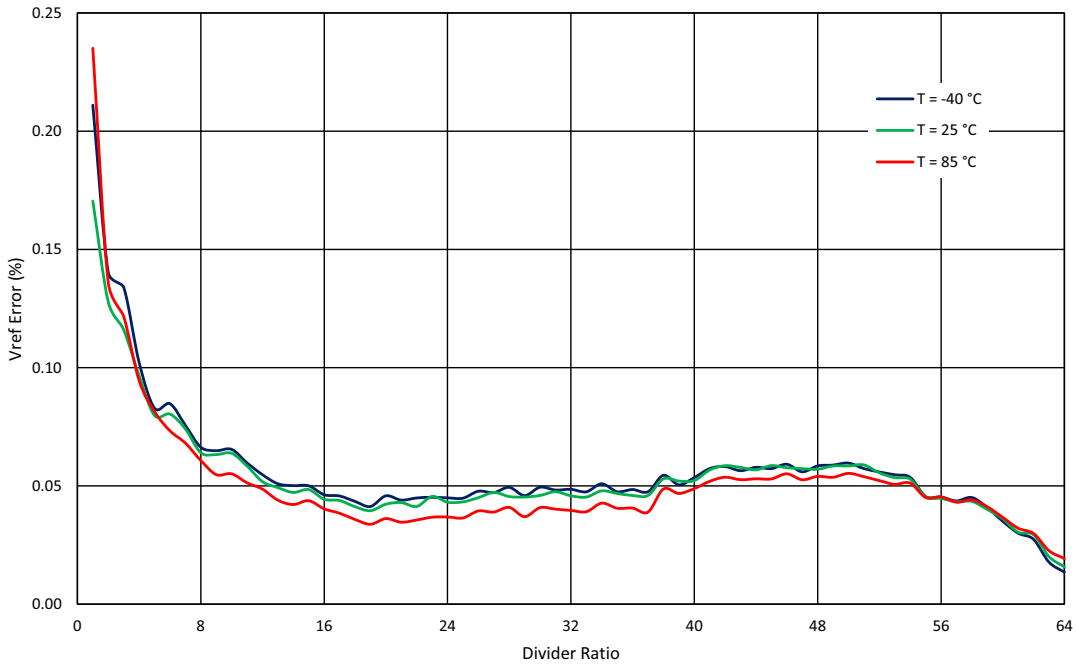


Figure 204. Op Ampx V_{REF} Divider Accuracy at V_{DD} = 3.3 V

15.5 HD Buffer Typical Performance

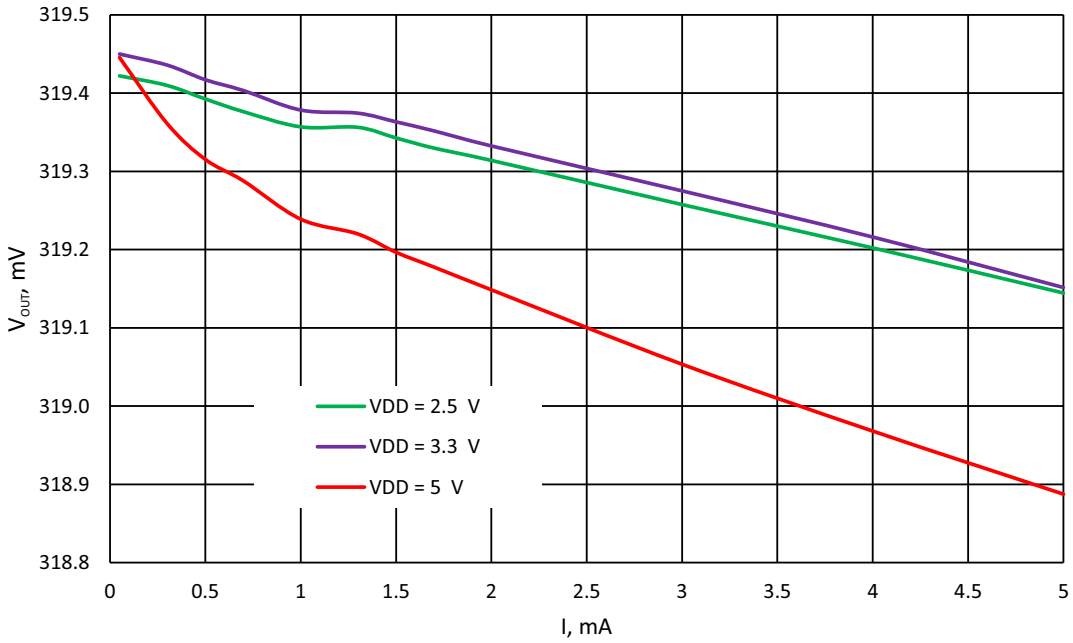


Figure 205. HD Buffer Typical Load Regulation, V_{REF} = 320 mV, T = -40 °C to +85 °C

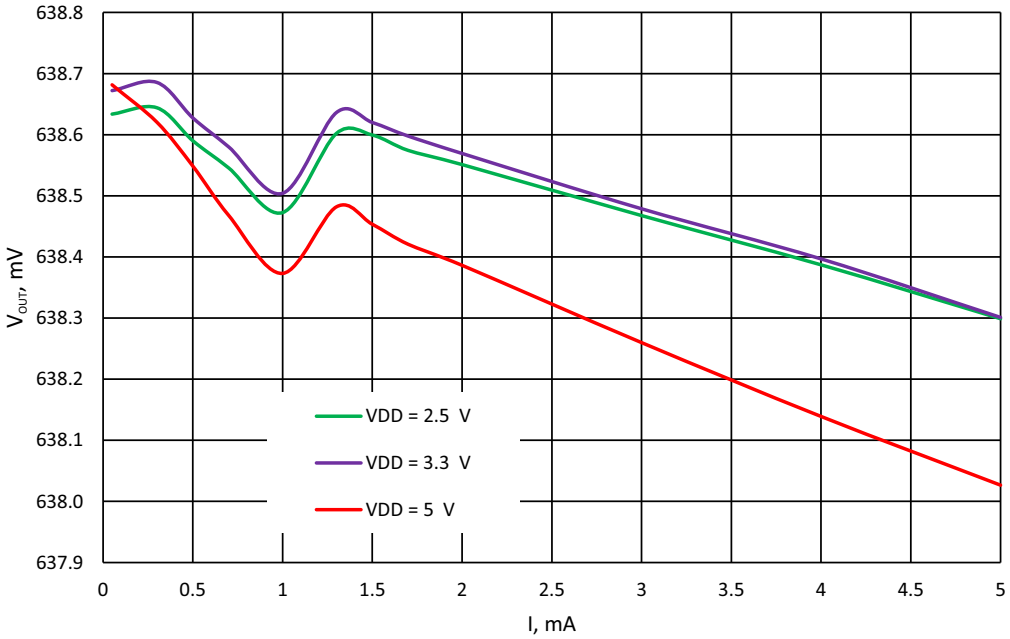


Figure 206. HD Buffer Typical Load Regulation, V_{REF} = 640 mV, T = -40 °C to +85 °C

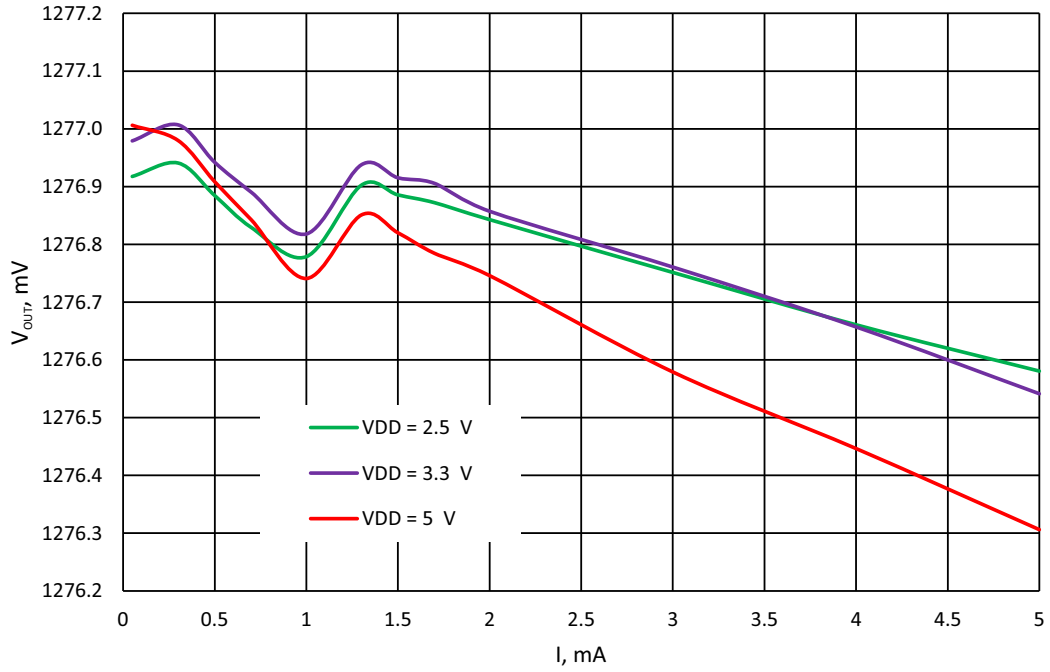


Figure 207. HD Buffer Typical Load Regulation, V_{REF} = 1280 mV, T = -40 °C to +85 °C

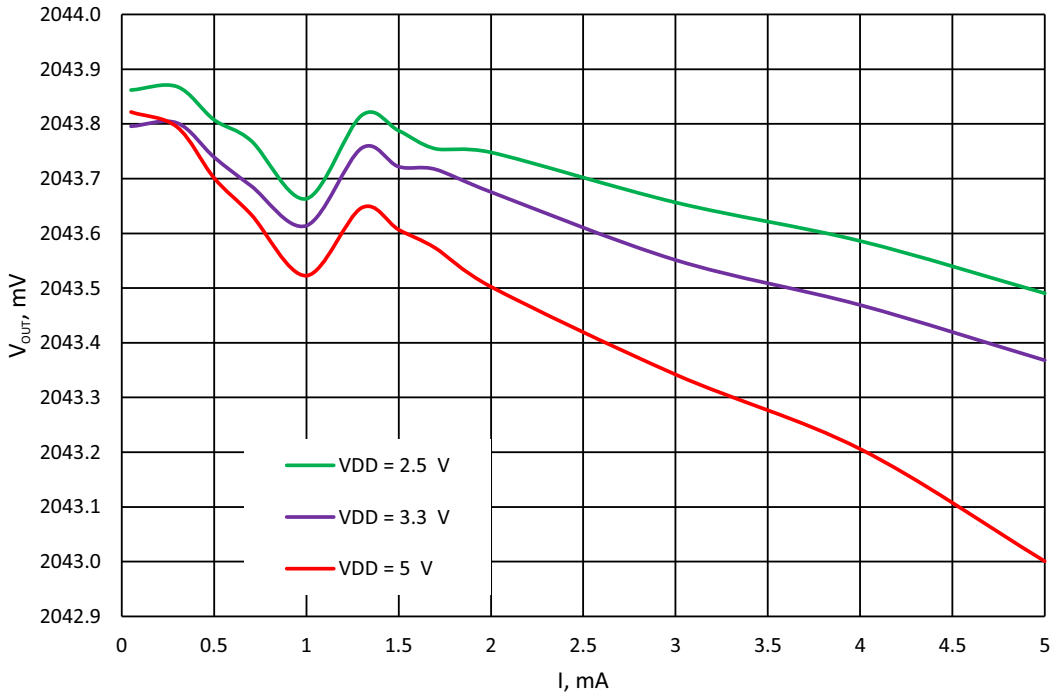


Figure 208. HD Buffer Typical Load Regulation, V_{REF} = 2048 mV, T = -40 °C to +85 °C

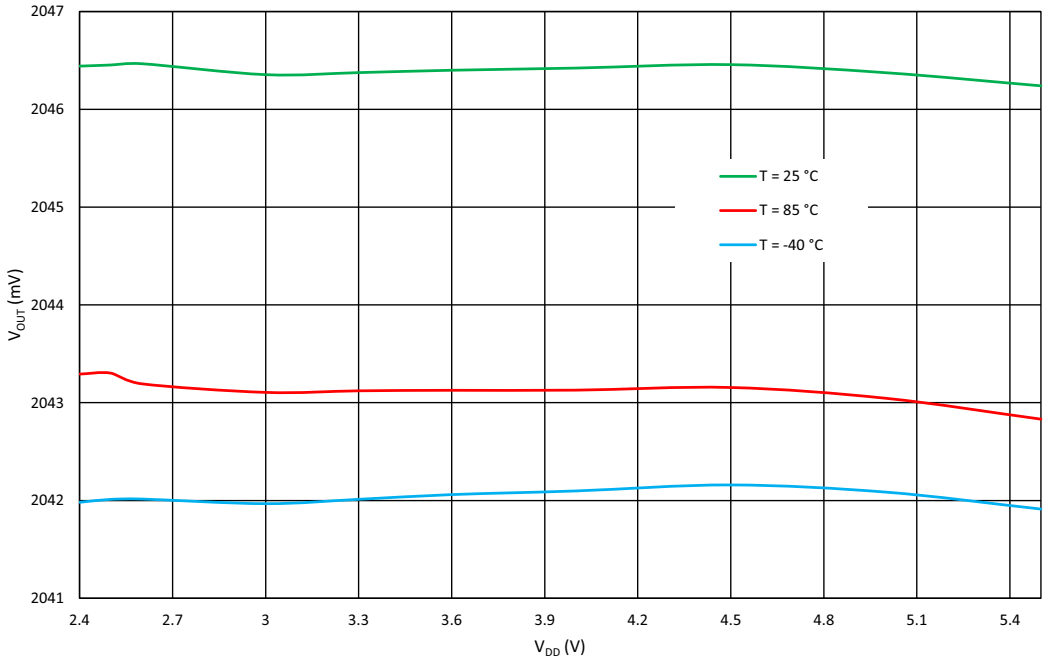


Figure 209. HD Buffer Typical Line Regulation, I_{LOAD} = 5 mA

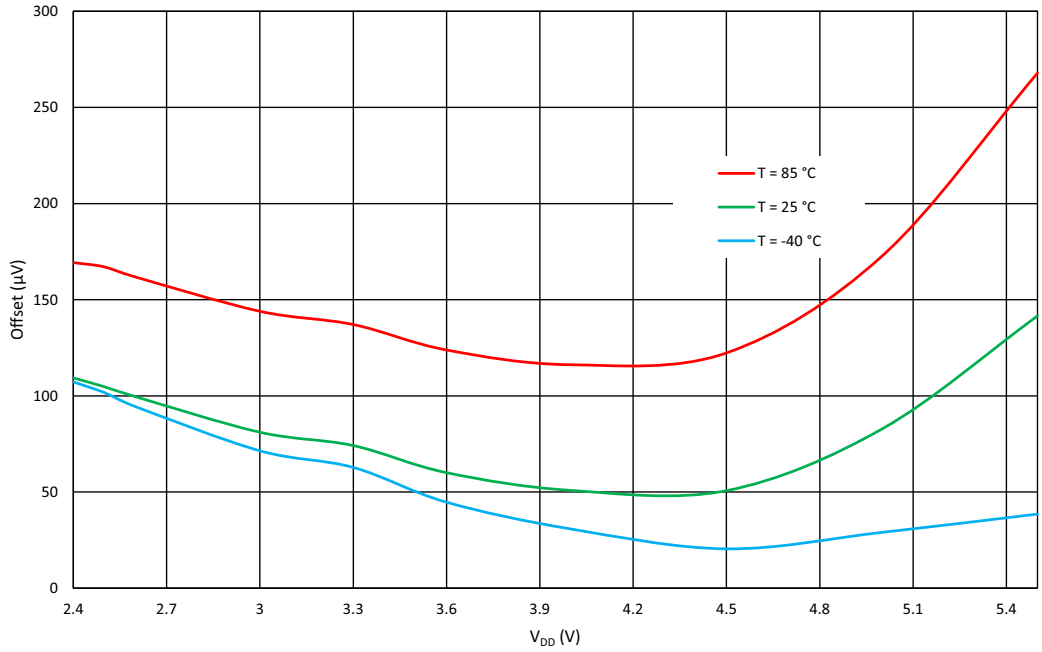


Figure 210. HD Buffer Offset vs. V_{DD}

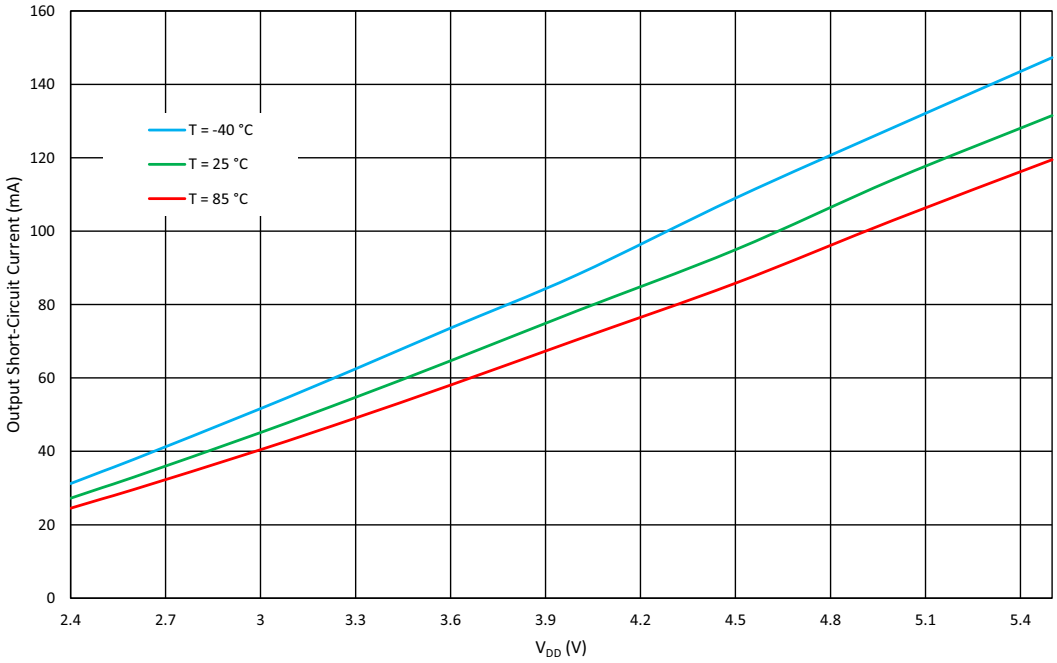


Figure 211. HD Buffer Output Short-Circuit Current vs. V_{DD}

16. Clocking

16.1 OSC General Description

The SLG47004 has three internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz)
- Oscillator1 (2.048 MHz)
- Oscillator2 (25 MHz).

There are two divider stages for each oscillator that give the user flexibility for introducing clock signals to connection matrix, as well as various other Macrocells. The pre-divider (first stage) for Oscillator allows the selection of /1, /2, /4, or /8 to divide down frequency from the fundamental. The second stage divider has an input of frequency from the pre-divider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24, or /64 on Connection Matrix Input lines [52], [53], and [54]. Please see Figure 215 for more details on the SLG47004 clock scheme.

Oscillator2 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by reg [713]. This function is recommended to use when analog blocks are used along with the Oscillator.

The Matrix Power-down/Force On function allows switching off or force on the oscillator using an external pin. The Matrix Power-down/Force On (Connection Matrix Output [91], [92], [93]) signal has the highest priority. The OSC operates according to the Table 36.

It is highly recommended to force the bandgap on when OSC1 or OSC2 are used in the project.

Table 36. Oscillator Operation Mode Configuration Settings

POR	External Clock Selection	Signal from Connection Matrix	Register: Power-Down or Force On by Matrix Input	Register: Auto Power-On or Force On	OSC Enable Signal from CNT/DLY Macrocells	OSC Operation Mode
0	X	X	X	X	X	OFF
1	1	X	X	X	X	Internal OSC is OFF, logic is ON
1	0	1	0	X	X	OFF
1	0	1	1	X	X	ON
1	0	0	X	1	X	ON
1	0	0	X	0	CNT/DLY requires OSC	ON
1	0	0	X	0	CNT/DLY does not require OSC	OFF

[1] The OSC will run only when any macrocell that uses OSC is powered on.

16.2 Oscillator0 (2.048 kHz)

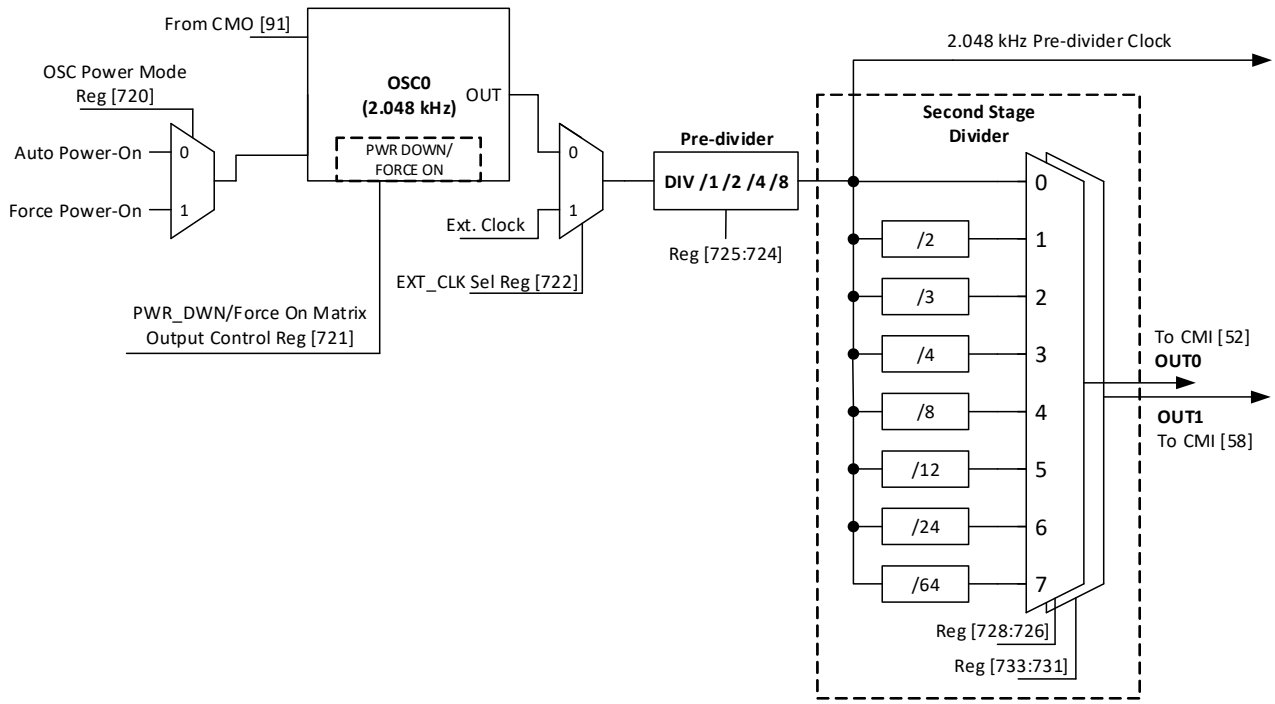


Figure 212. Oscillator0 Block Diagram

16.3 Oscillator1 (2.048 MHz)

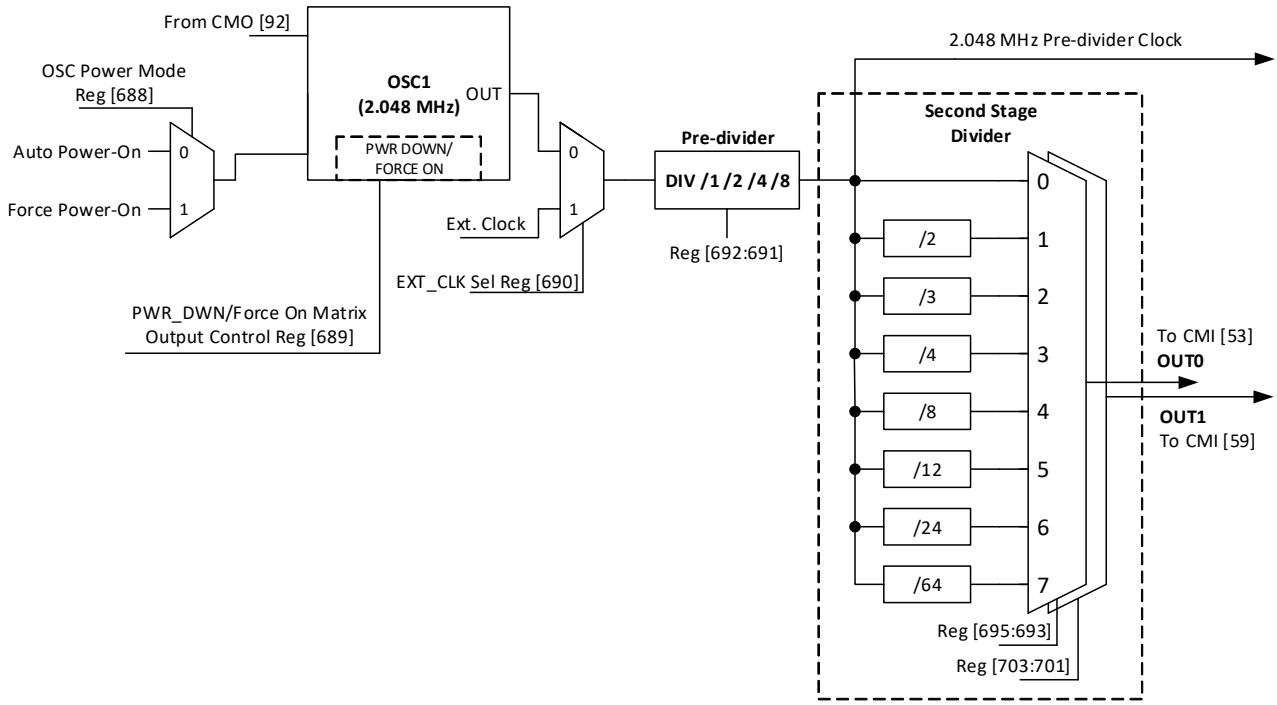


Figure 213. Oscillator1 Block Diagram

16.4 Oscillator2 (25 MHz)

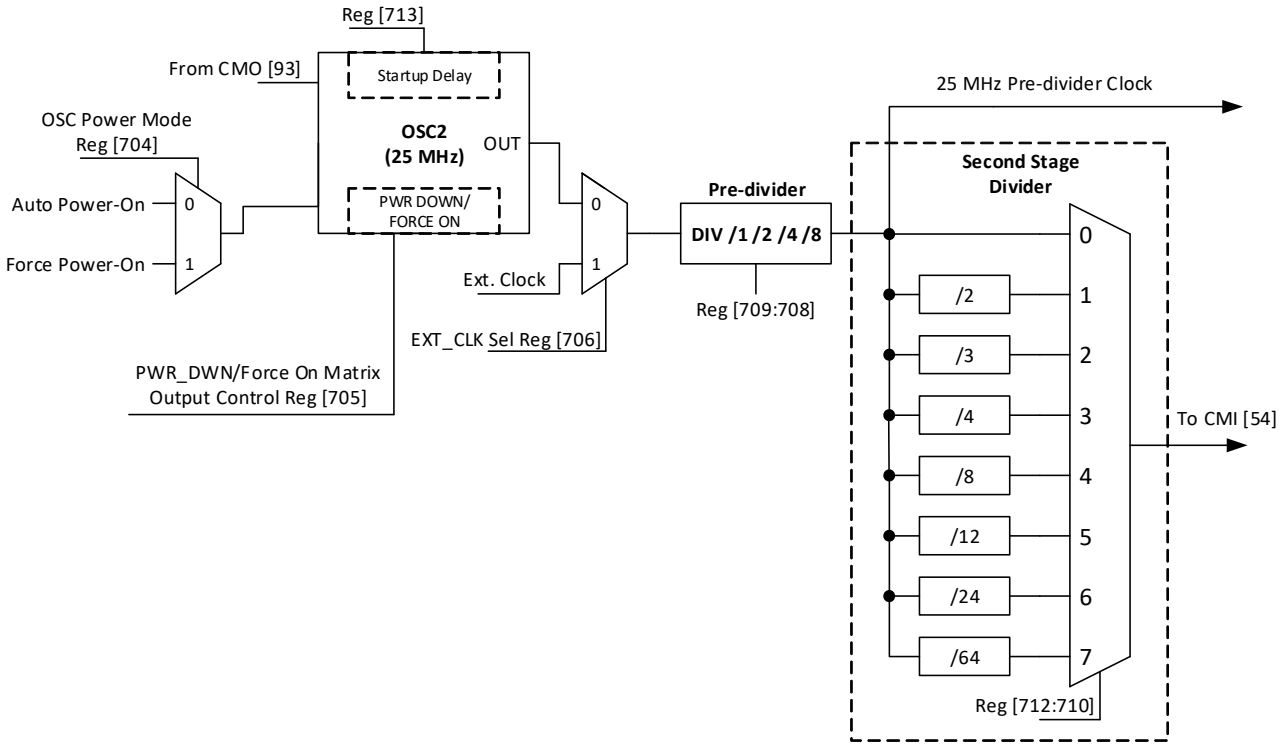


Figure 214. Oscillator2 Block Diagram

16.5 CNT/DLY Clock Scheme

Each CNT/DLY within Multi-Function macrocell has its own additional clock divider connected to oscillators pre-divider. Available dividers are:

- OSC0/1, OSC0/8, OSC0/64, OSC0/512, OSC0/4096, OSC0/32768, OSC0/262144
- OSC1/1, OSC1/8, OSC1/64, OSC1/512
- OSC2/1, OSC2/4

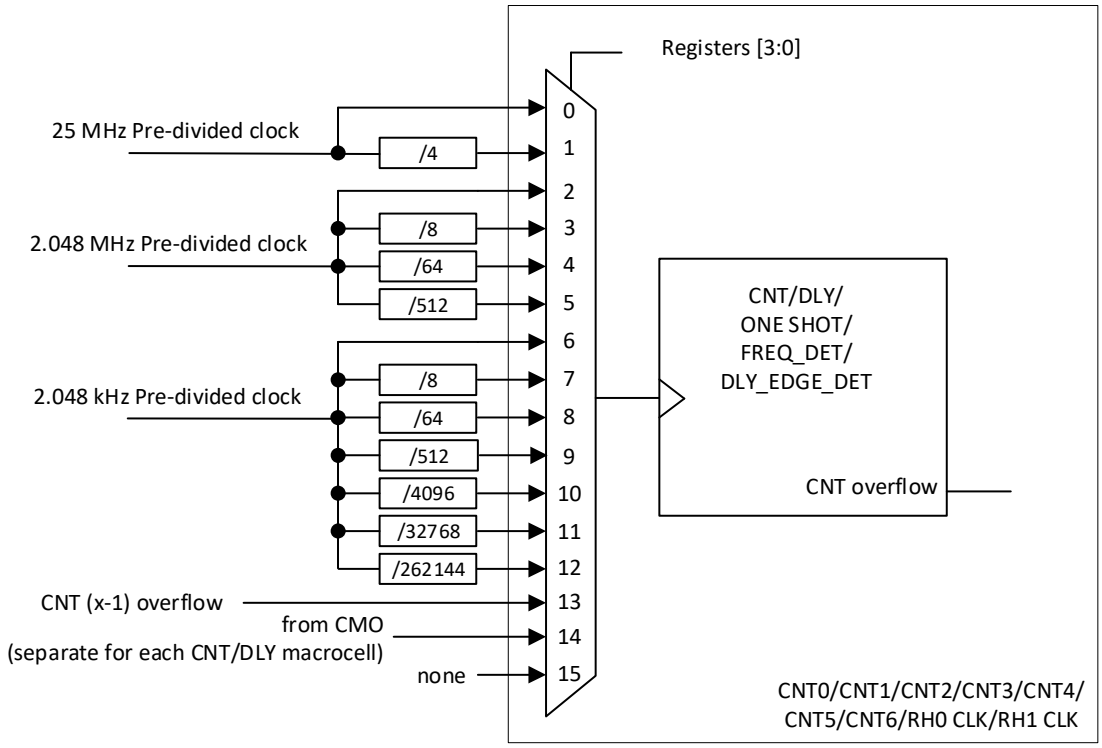


Figure 215. Clock Scheme

16.6 External Clocking

The SLG47004 supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

16.6.1 IO10 Source for Oscillator0 (2.048 kHz)

When reg [722] is set to 1, an external clocking signal on IO0 will be routed in place of the internal oscillator derived 2.048 kHz clock source. See Figure 212. The high and low limits for frequency that can be selected are 0 MHz and 10 MHz.

16.6.2 IO1 Source for Oscillator1 (2.048 MHz)

When reg [690] is set to 1, an external clocking signal on IO1 will be routed in place of the internal oscillator derived 2.048 MHz clock source. See Figure 213. The high and low limits for frequency that can be selected are 0 MHz and 10 MHz.

16.6.3 IO2 Source for Oscillator2 (25 MHz)

When reg [706] is set to 1, an external clocking signal on IO2 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 214. The external frequency range is 0 MHz to 20 MHz at V_{DD} = 2.4 V, 0 MHz to 30 MHz at V_{DD} = 3.3 V, 0 MHz to 50 MHz at V_{DD} = 5.0 V. When an external clock is selected for OSC2, the oscillator's output signal will be inverted with respect to the IO2 input signal.

16.7 Oscillators Power-On Delay

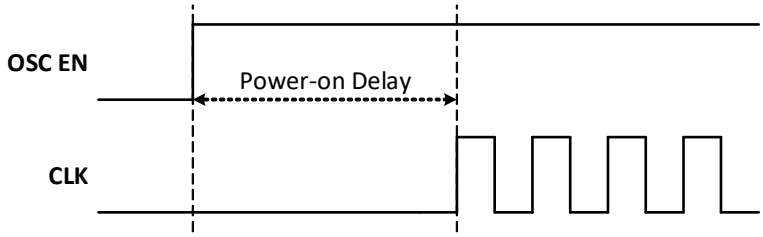


Figure 216. Oscillator Startup Diagram

Note 1: OSC power mode: “Auto Power-On”.
Note 2: OSC enable” signal appears when any macrocell that uses OSC is powered on.

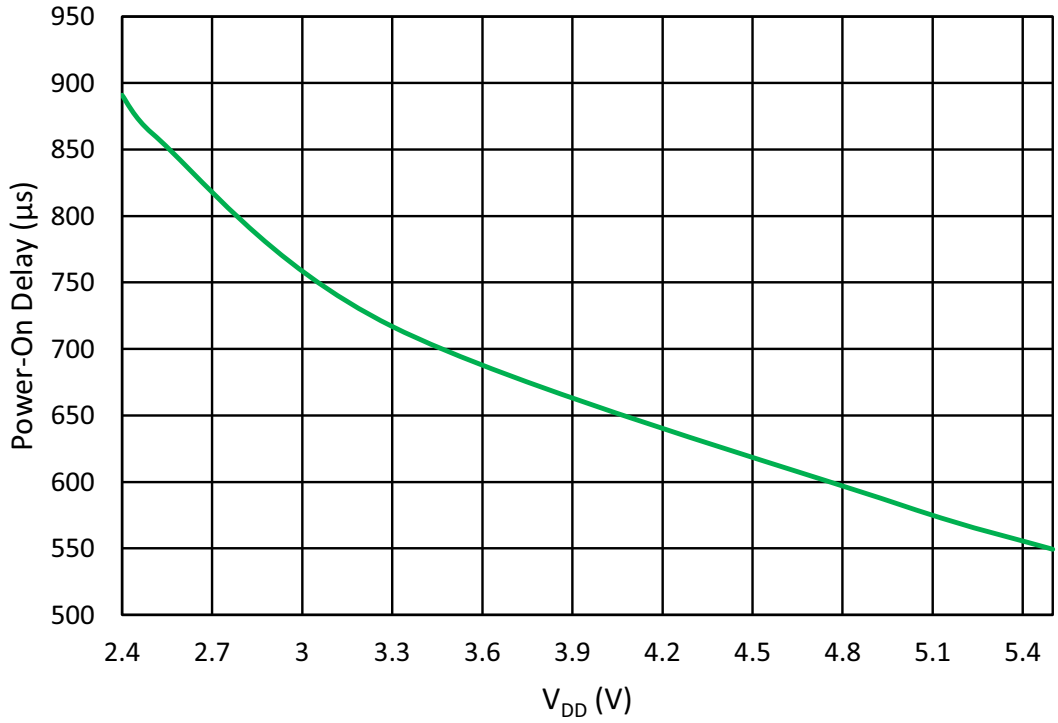


Figure 217. OSC0 Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC0 = 2.048 kHz

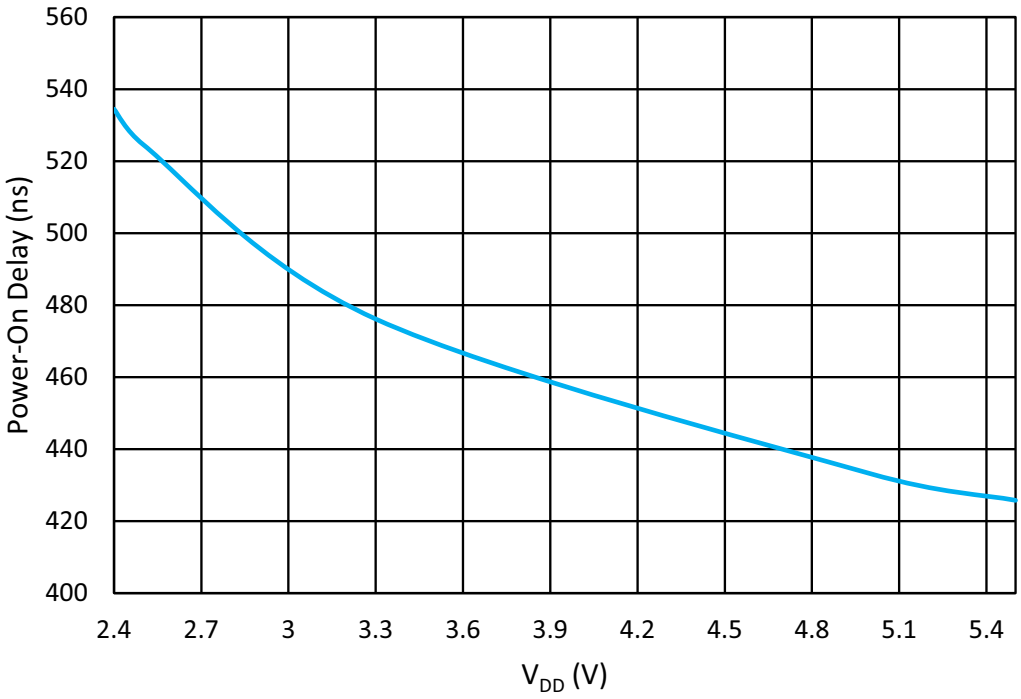


Figure 218. OSC1 Oscillator Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC1 = 2.048 MHz

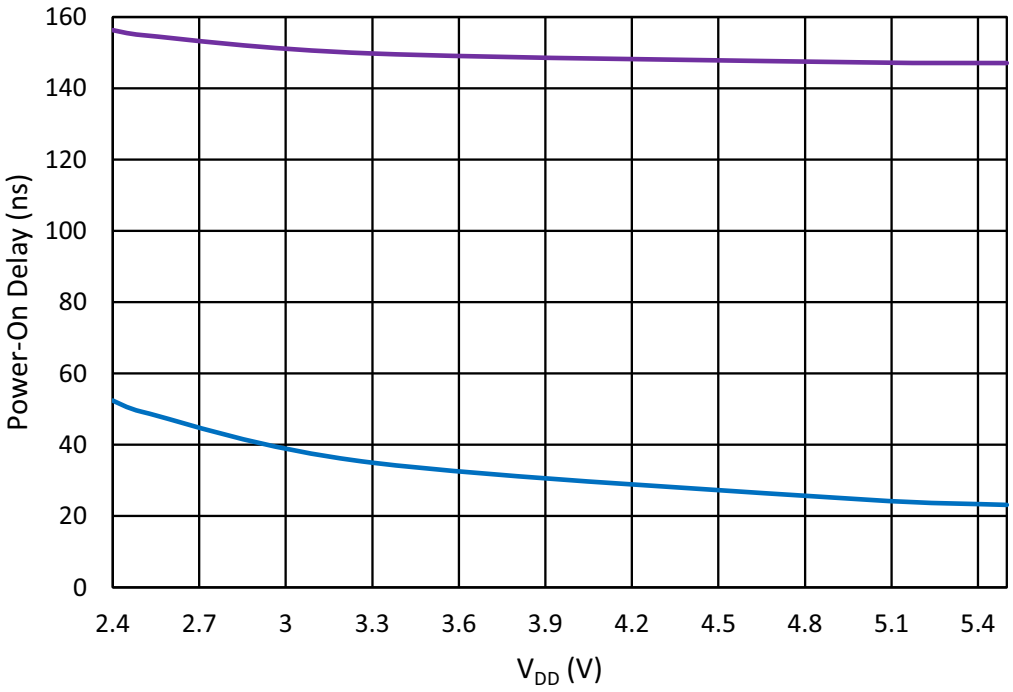


Figure 219. OSC2 Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC2 = 25 MHz

16.8 Oscillators Accuracy

Note: OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

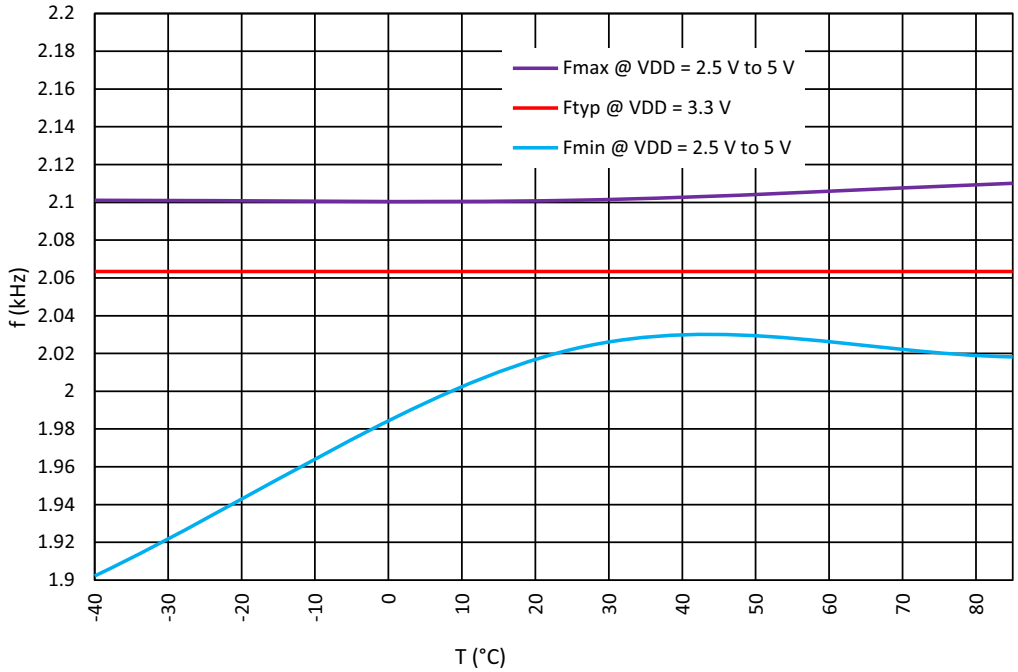


Figure 220. OSC0 Frequency vs. Temperature, OSC0 = 2.048 kHz

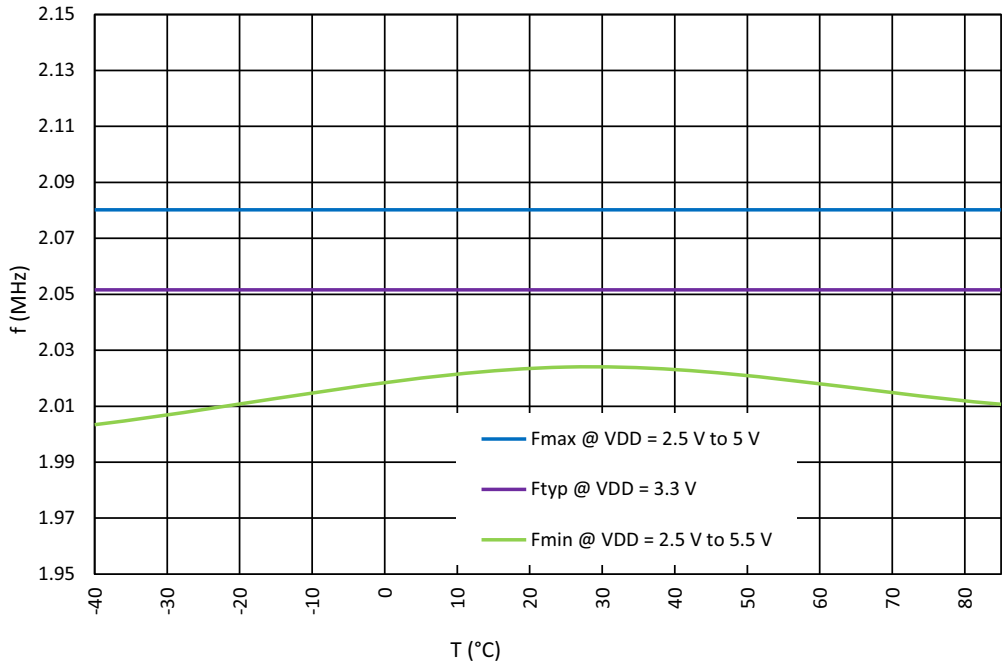


Figure 221. OSC1 Frequency vs. Temperature, OSC1 = 2.048 MHz

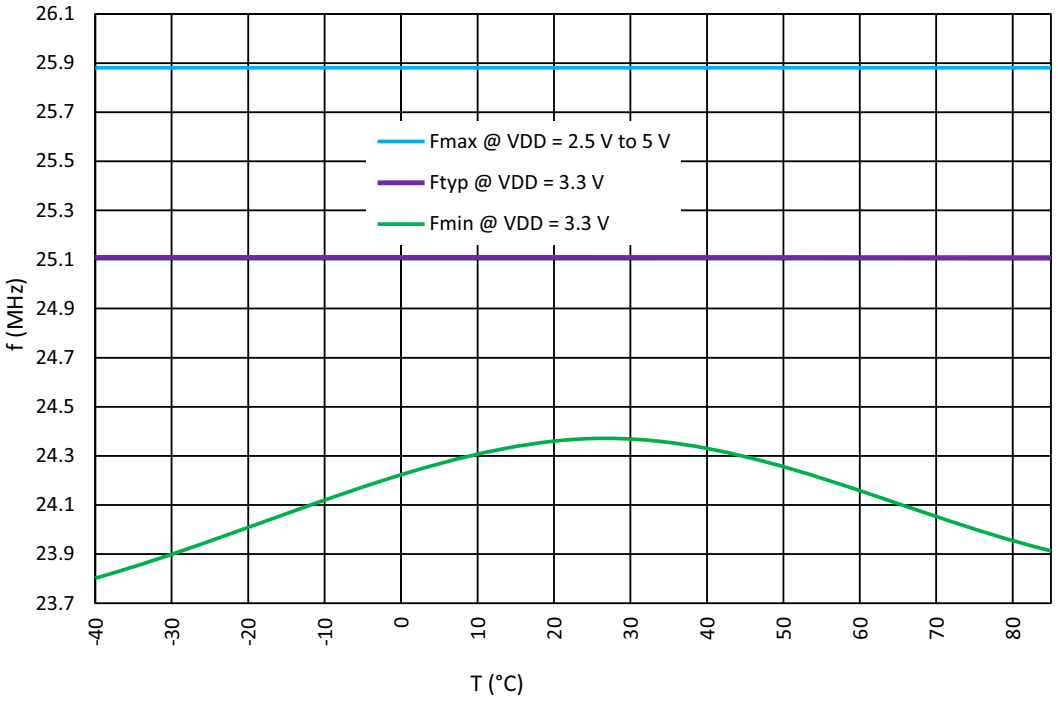


Figure 222. OSC2 Frequency vs. Temperature, OSC2 = 25 MHz

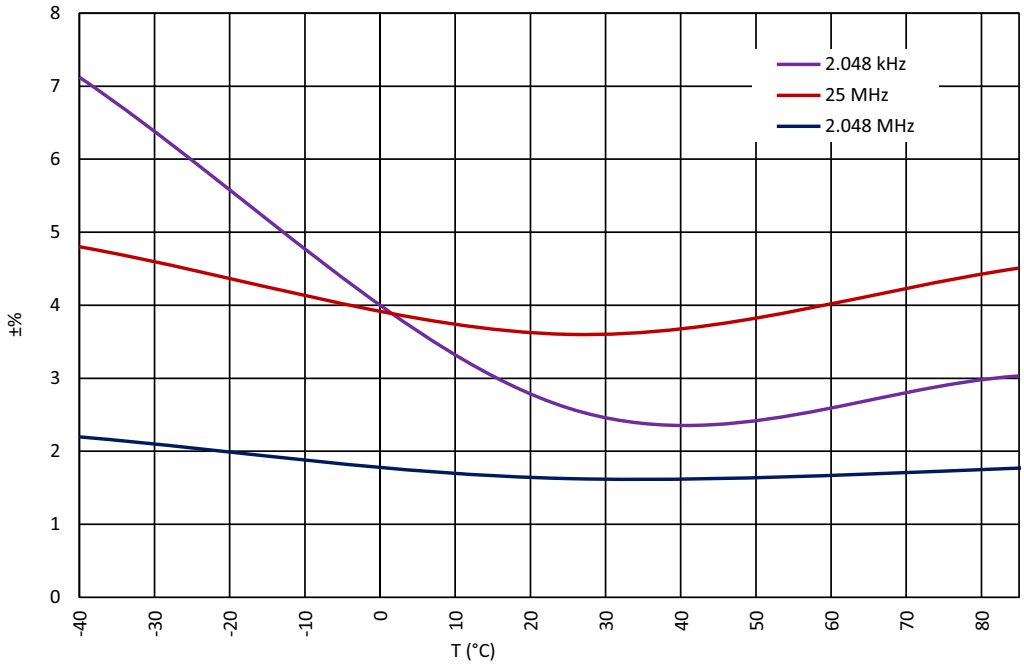


Figure 223. Oscillators Total Error vs. Temperature at V_{DD} = 2.4 V to 5.5 V

Note: For more information see section 3.8 Oscillator Specifications.

16.9 Oscillators Settling Time

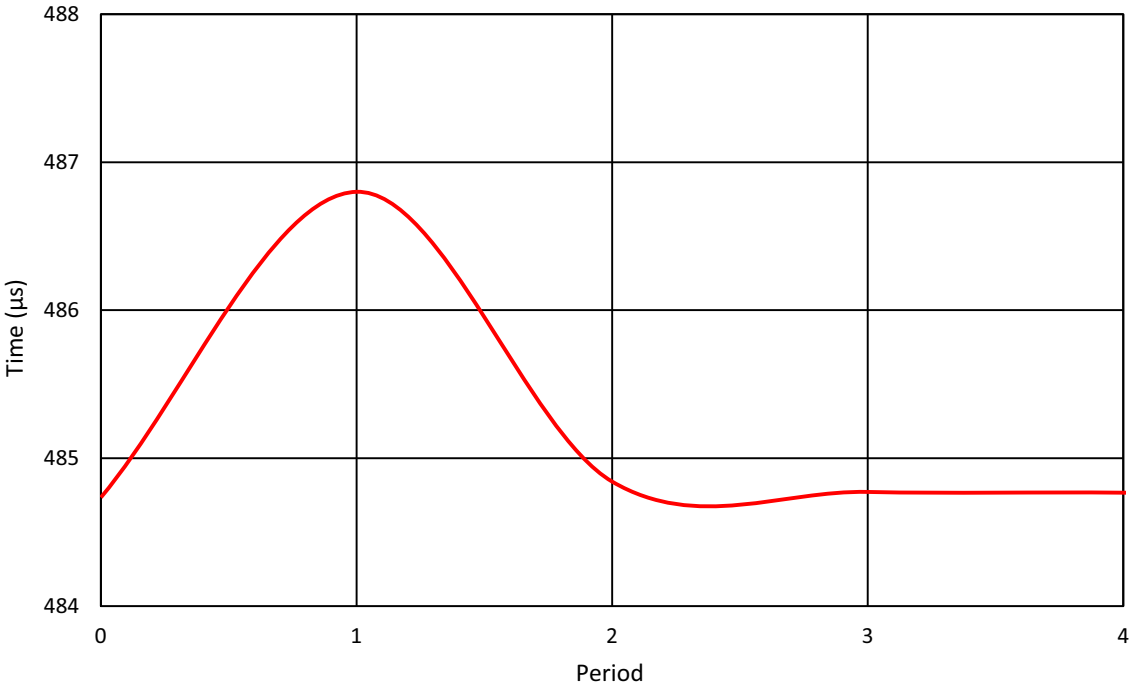


Figure 224. Oscillator0 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC0 = 2 kHz

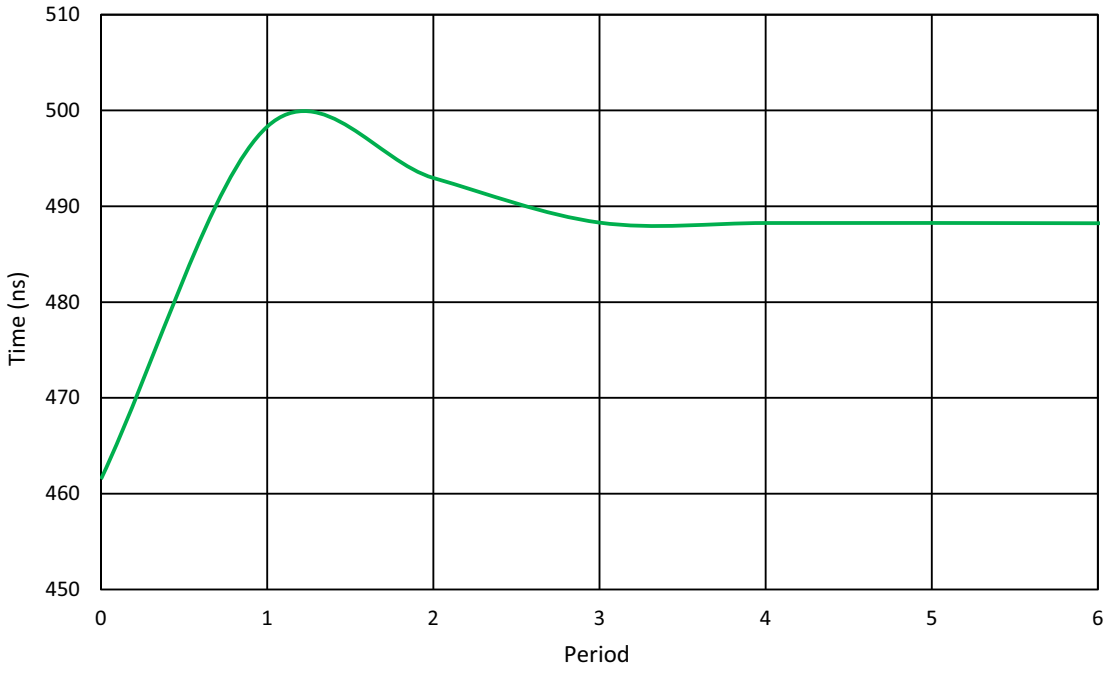


Figure 225. Oscillator1 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC1 = 2 MHz

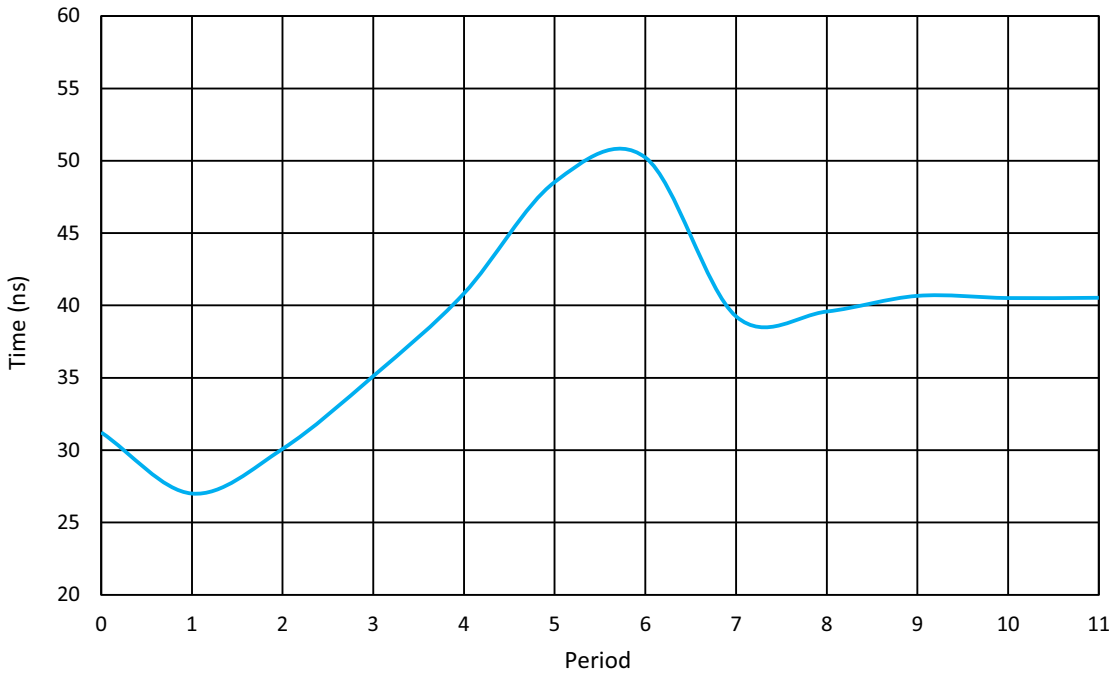


Figure 226. Oscillator2 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC2 = 25 MHz (Normal Start)

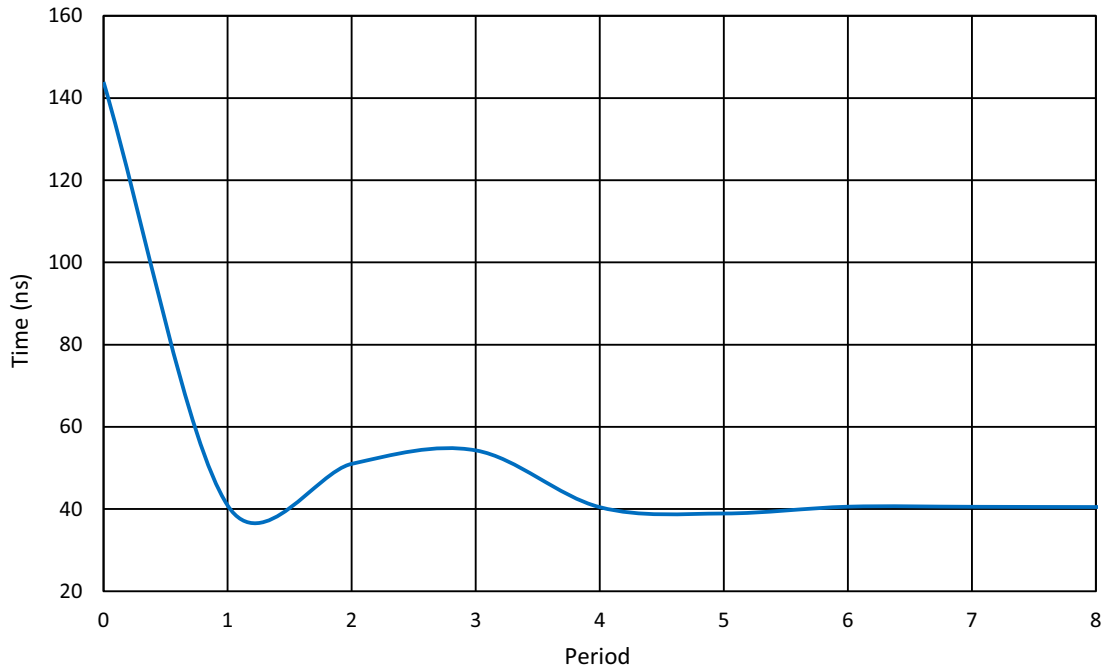


Figure 227. Oscillator2 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC2 = 25 MHz (Start with Delay)

16.10 Oscillators Current Consumption

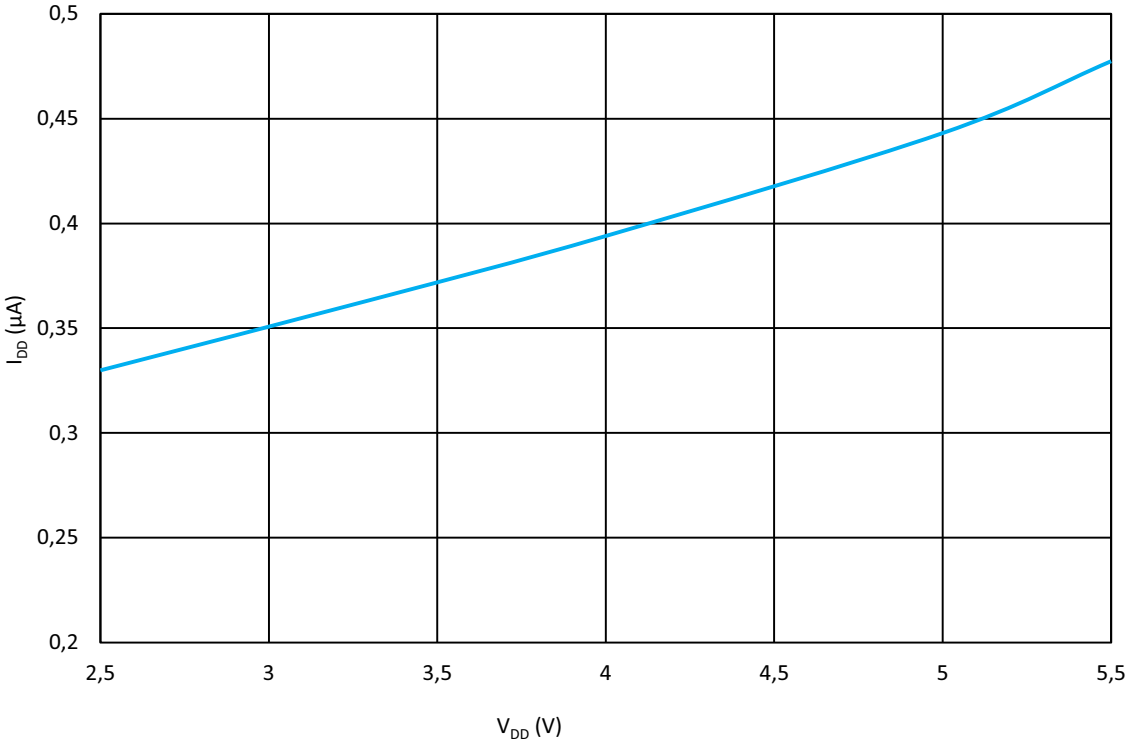


Figure 228. OSC0 Current Consumption vs. V_{DD} at T = -40 °C to +85 °C (All Pre-Dividers)

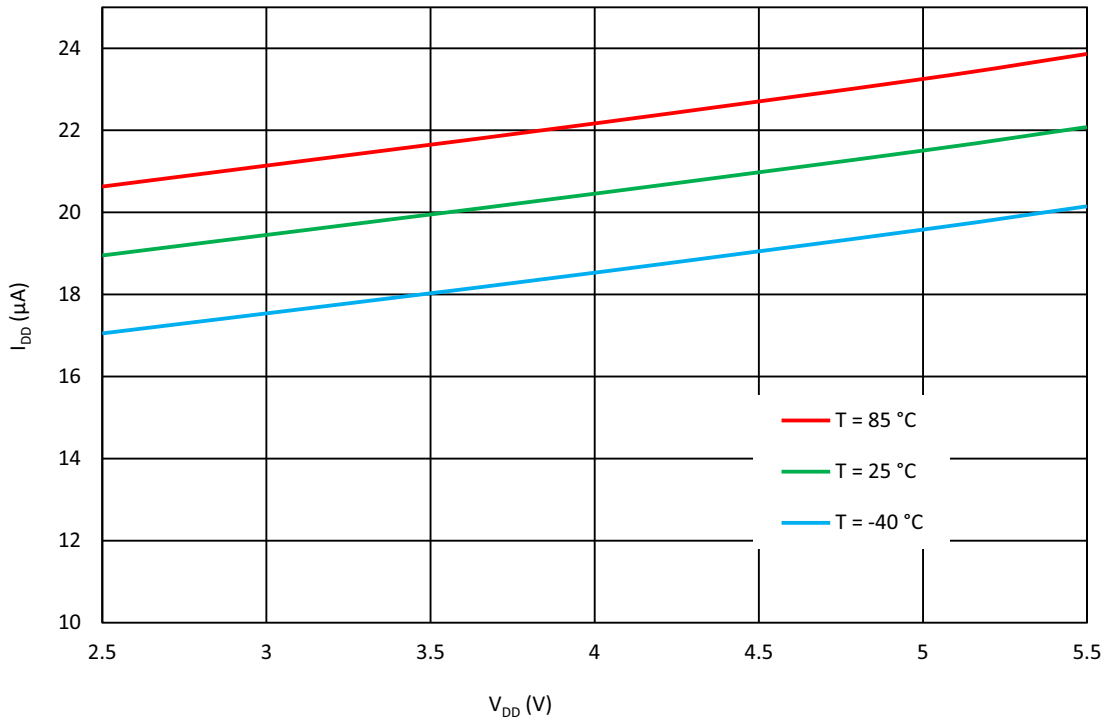


Figure 229. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 1)

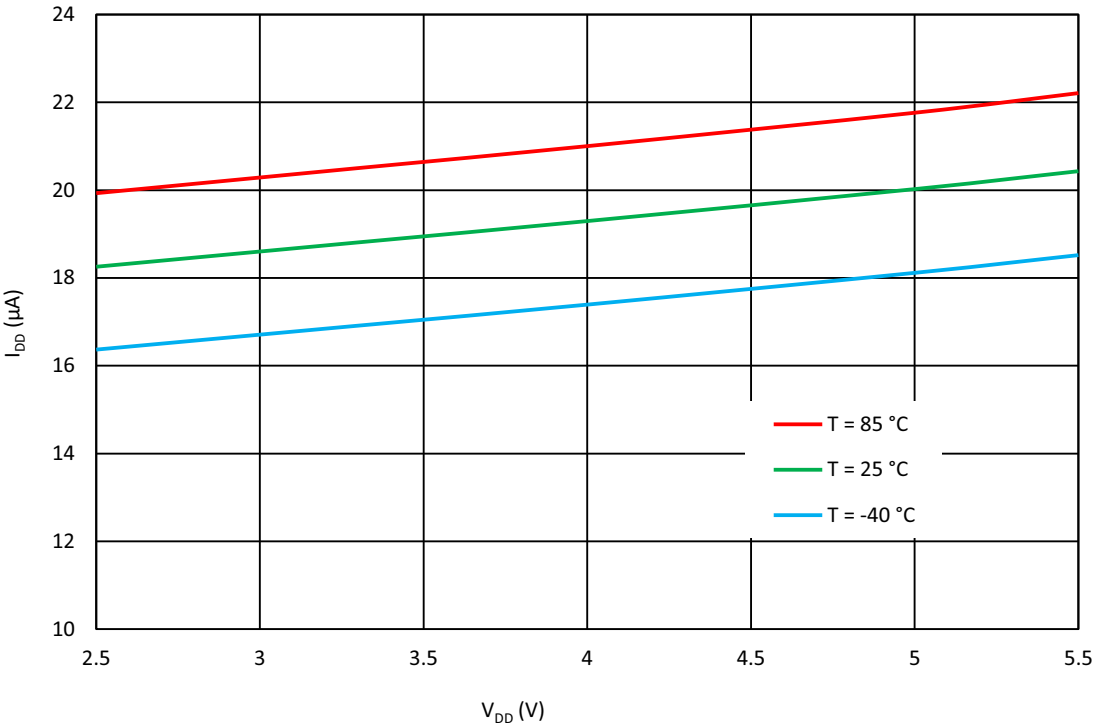


Figure 230. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 4)

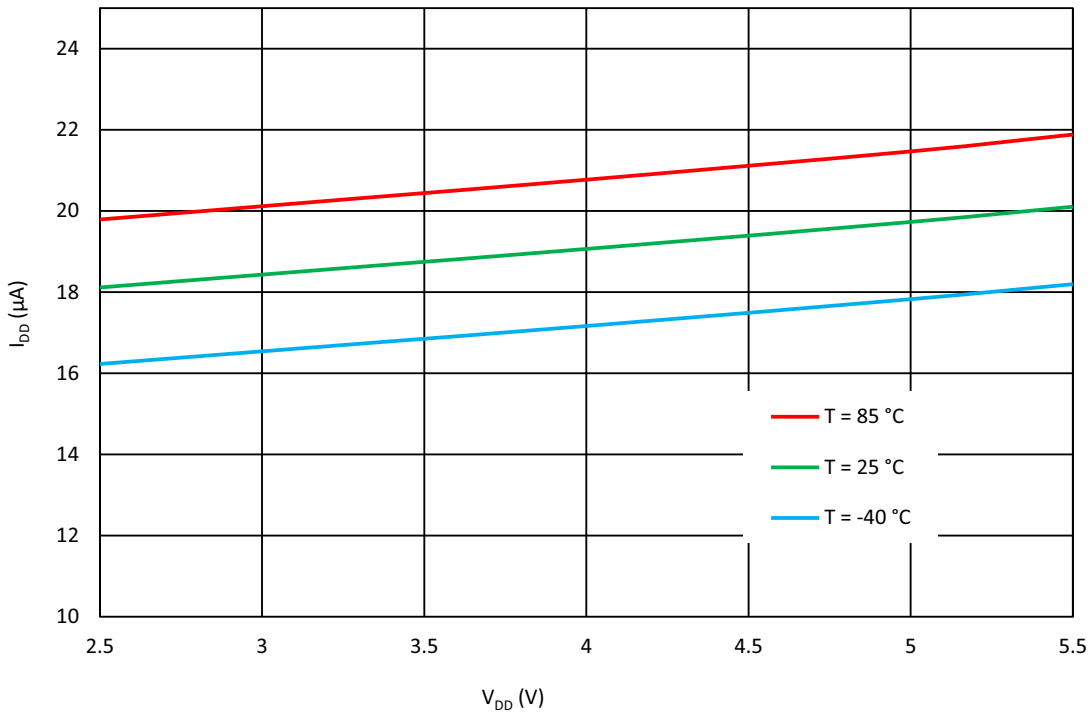


Figure 231. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 8)

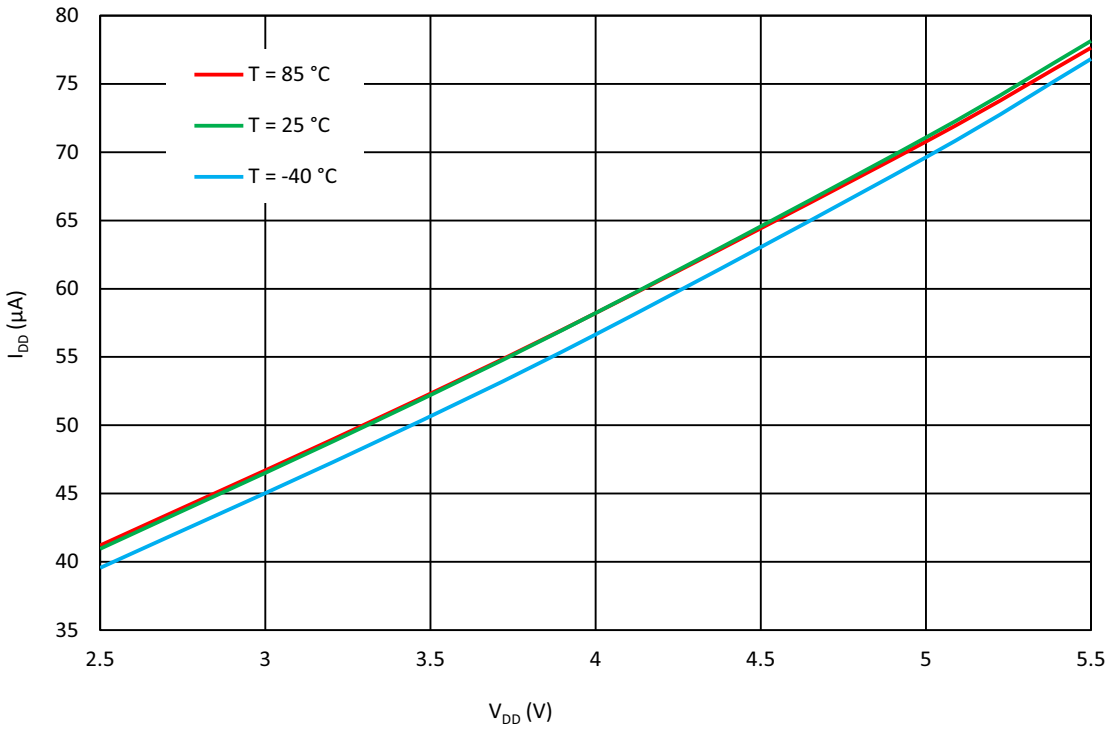


Figure 232. OSC2 Current Consumption vs. V_{DD} (Pre-Divider = 1)

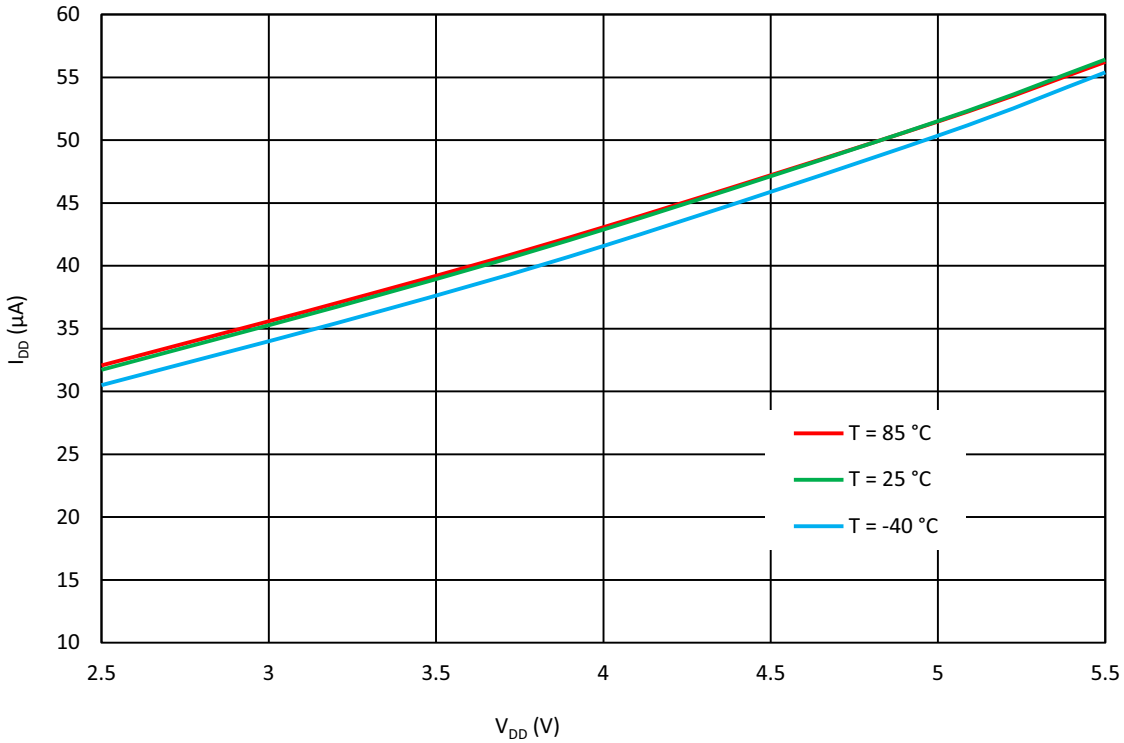


Figure 233. OSC2 Current Consumption vs. V_{DD} (Pre-Divider = 4)