



# FDB2614

## 200V N-Channel PowerTrench MOSFET

### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

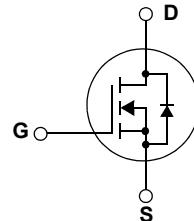
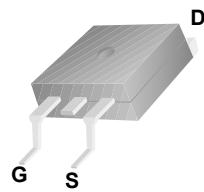


### Application

- PDP application

### Description

- 62A, 200V,  $R_{DS(on)} = 22.9\text{m}\Omega$  @ $V_{GS} = 10\text{ V}$
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(on)}$
- High power and current handling capability



### Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain-Source Voltage	200	V
$V_{GS}$	Gate-Source Voltage	$\pm 30$	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	62 39.3	A A
$I_{DM}$	Drain Current - Pulsed	(Note 1)	see Figure 9
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	145
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	4.5
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	260 2.1	W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\*Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	Min.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.48	$^\circ\text{C}/\text{W}$
$R_{\theta JA}^*$	Thermal Resistance, Junction-to-Ambient*	--	40	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C}/\text{W}$

\*When mounted on the minimum pad size recommended (PCB Mount)

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB2614	FDB2614	D <sup>2</sup> -PAK	330mm	24mm	800

## Electrical Characteristics

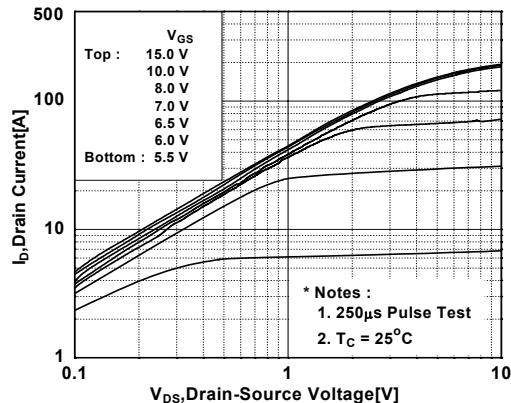
$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>Off Characteristics</b>							
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}} = 0\text{V}$ , $I_D = 250\mu\text{A}$ , $T_J = 25^\circ\text{C}$	200	--	--	V	
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.2	--	$^\circ\text{C}$	
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{\text{DS}} = 200\text{V}$ , $V_{\text{GS}} = 0\text{V}$ $V_{\text{DS}} = 200\text{V}$ , $V_{\text{GS}} = 0\text{V}$ , $T_J = 125^\circ\text{C}$	--	--	1 500	$\mu\text{A}$ $\mu\text{A}$	
$I_{\text{GSSF}}$	Gate-Body Leakage Current, Forward	$V_{\text{GS}} = 30\text{V}$ , $V_{\text{DS}} = 0\text{V}$	--	--	100	nA	
$I_{\text{GSSR}}$	Gate-Body Leakage Current, Reverse	$V_{\text{GS}} = -30\text{V}$ , $V_{\text{DS}} = 0\text{V}$	--	--	-100	nA	
<b>On Characteristics</b>							
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = 250\mu\text{A}$	3.0	4.0	5.0	V	
$R_{\text{DS(on)}}$	Static Drain-Source On-Resistance	$V_{\text{GS}} = 10\text{V}$ , $I_D = 31\text{A}$	--	22.9	27	$\text{m}\Omega$	
$g_{\text{FS}}$	Forward Transconductance	$V_{\text{DS}} = 10\text{V}$ , $I_D = 31\text{A}$	(Note 4)	72	--	S	
<b>Dynamic Characteristics</b>							
$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}} = 25\text{V}$ , $V_{\text{GS}} = 0\text{V}$ $f = 1.0\text{MHz}$	--	5435	7230	pF	
$C_{\text{oss}}$	Output Capacitance		--	505	675	pF	
$C_{\text{rss}}$	Reverse Transfer Capacitance		--	110	165	pF	
<b>Switching Characteristics</b>							
$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}} = 100\text{V}$ , $I_D = 62\text{A}$ $V_{\text{GS}} = 10\text{V}$ , $R_{\text{GEN}} = 25\Omega$	--	77	165	ns	
$t_r$	Turn-On Rise Time		--	284	560	ns	
$t_{\text{d(off)}}$	Turn-Off Delay Time		--	103	220	ns	
$t_f$	Turn-Off Fall Time		--	162	335	ns	
$Q_g$	Total Gate Charge	$V_{\text{DS}} = 100\text{V}$ , $I_D = 62\text{A}$ $V_{\text{GS}} = 10\text{V}$	--	76	99	nC	
$Q_{\text{gs}}$	Gate-Source Charge		--	35	--	nC	
$Q_{\text{gd}}$	Gate-Drain Charge		(Note 4, 5)	--	18	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>							
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		--	--	62	A	
$I_{\text{SM}}$	Maximum Pulsed Drain-Source Diode Forward Current		--	--	186	A	
$V_{\text{SD}}$	Drain-Source Diode Forward Voltage	$V_{\text{GS}} = 0\text{V}$ , $I_S = 62\text{A}$	--	--	1.2	V	
$t_{\text{rr}}$	Reverse Recovery Time	$V_{\text{GS}} = 0\text{V}$ , $I_S = 62\text{A}$ $dI/dt = 100\text{A}/\mu\text{s}$	--	145	--	ns	
$Q_{\text{rr}}$	Reverse Recovery Charge		(Note 4)	--	0.81	--	$\mu\text{C}$

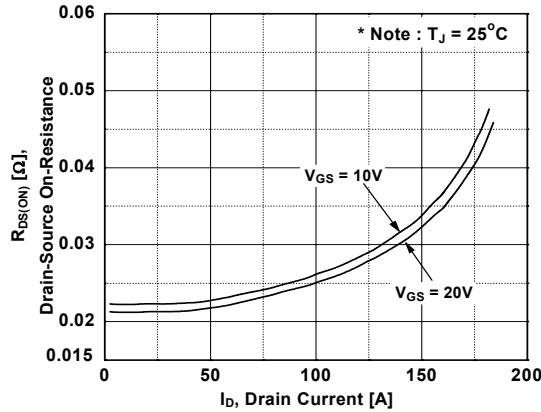
### Notes:

- Repetitive Rating: Pulse width limited by maximum junction temperature
- $L = 1\text{mH}$ ,  $I_{\text{AS}} = 17\text{A}$ ,  $V_{\text{DD}} = 50\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
- $I_{\text{SD}} \leq 62\text{A}$ ,  $dI/dt \leq 100\text{A}/\mu\text{s}$ ,  $V_{\text{DD}} \leq \text{BV}_{\text{DSS}}$ , Starting  $T_J = 25^\circ\text{C}$
- Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$
- Essentially Independent of Operating Temperature Typical Characteristics

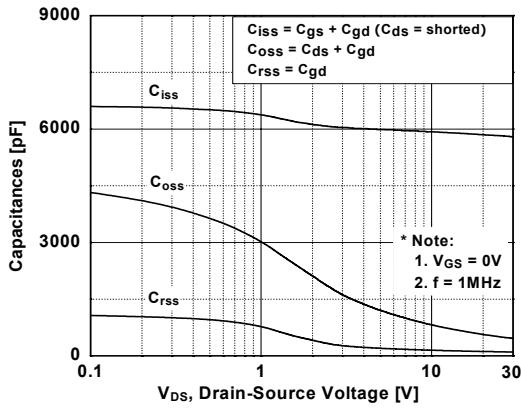
**Figure 1. On-Region Characteristics**



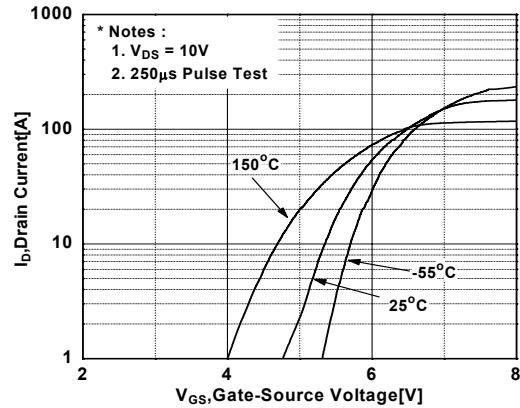
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



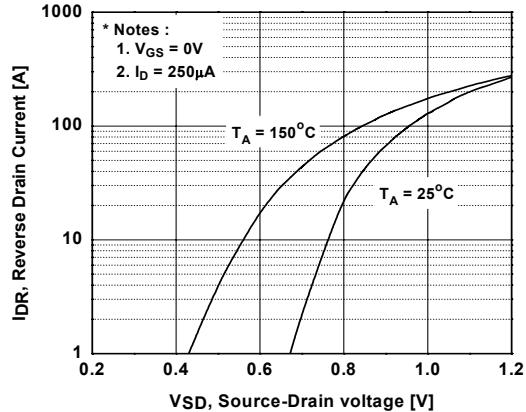
**Figure 5. Capacitance Characteristics**



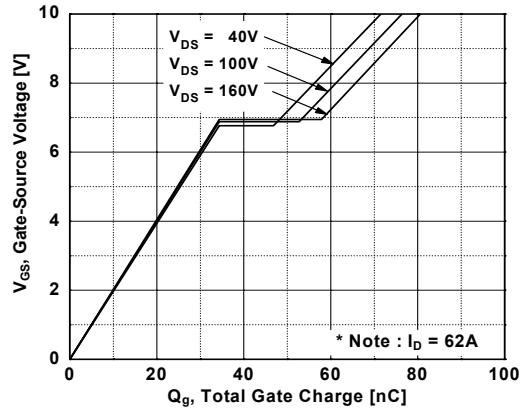
**Figure 2. Transfer Characteristics**



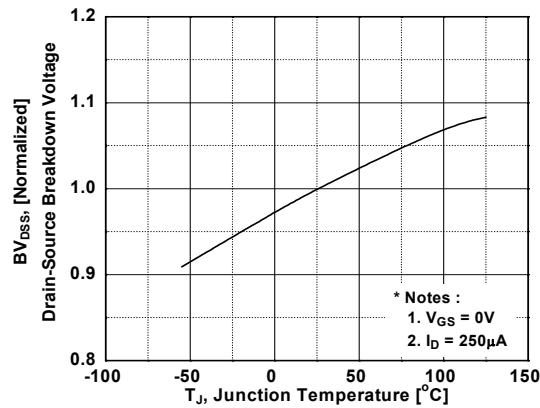
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



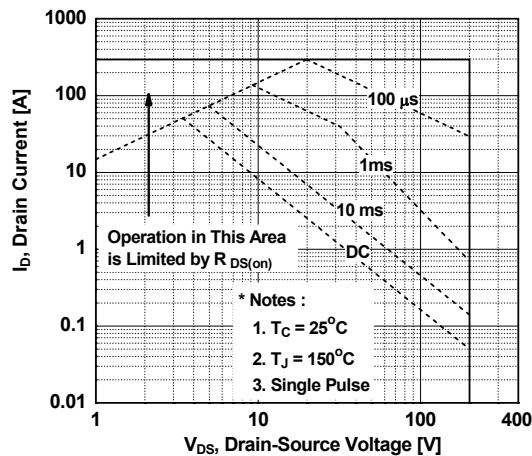
**Figure 6. Gate Charge Characteristics**



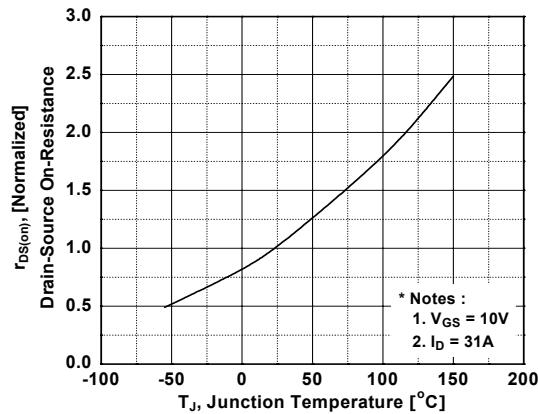
**Figure 7. Breakdown Voltage Variation vs. Temperature**



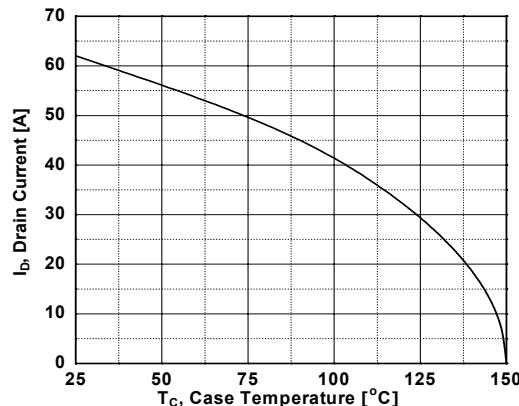
**Figure 9. Maximum Safe Operating Area**



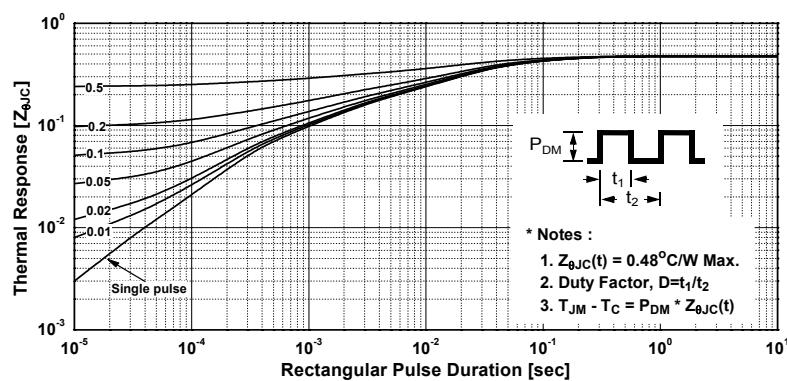
**Figure 8. On-Resistance Variation vs. Temperature**



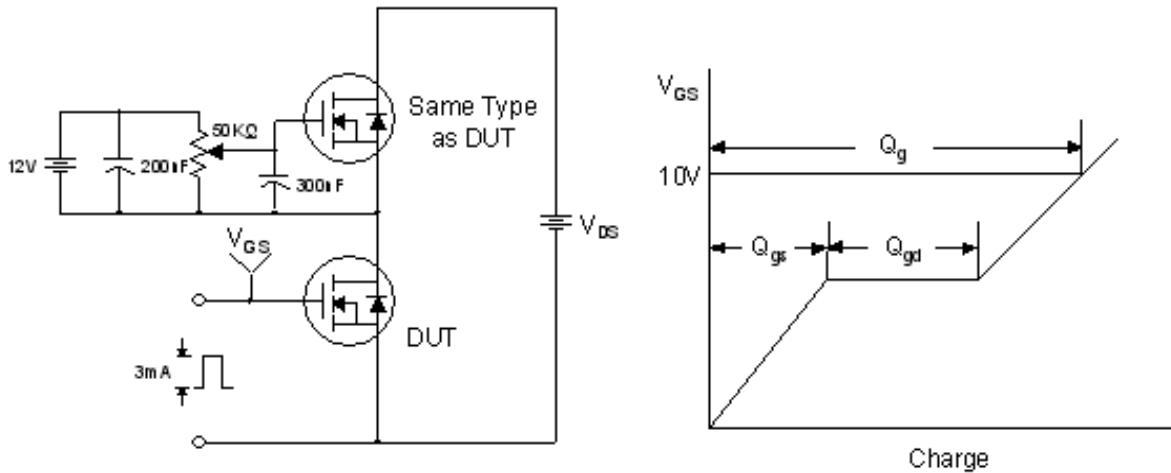
**Figure 10. Maximum Drain Current vs. Case Temperature**



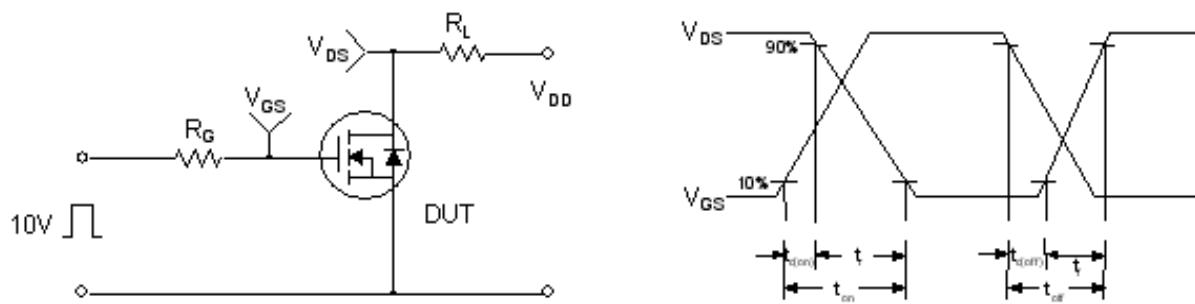
**Figure 11. Transient Thermal Response Curve**



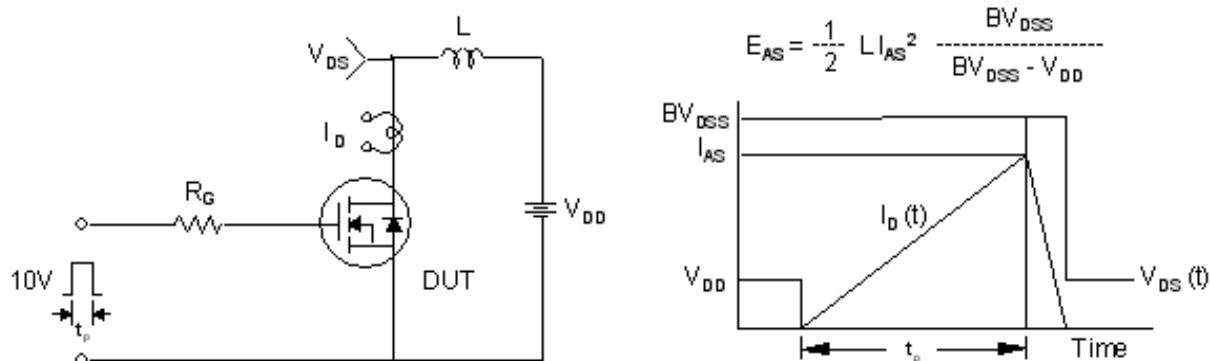
Gate Charge Test Circuit & Waveform



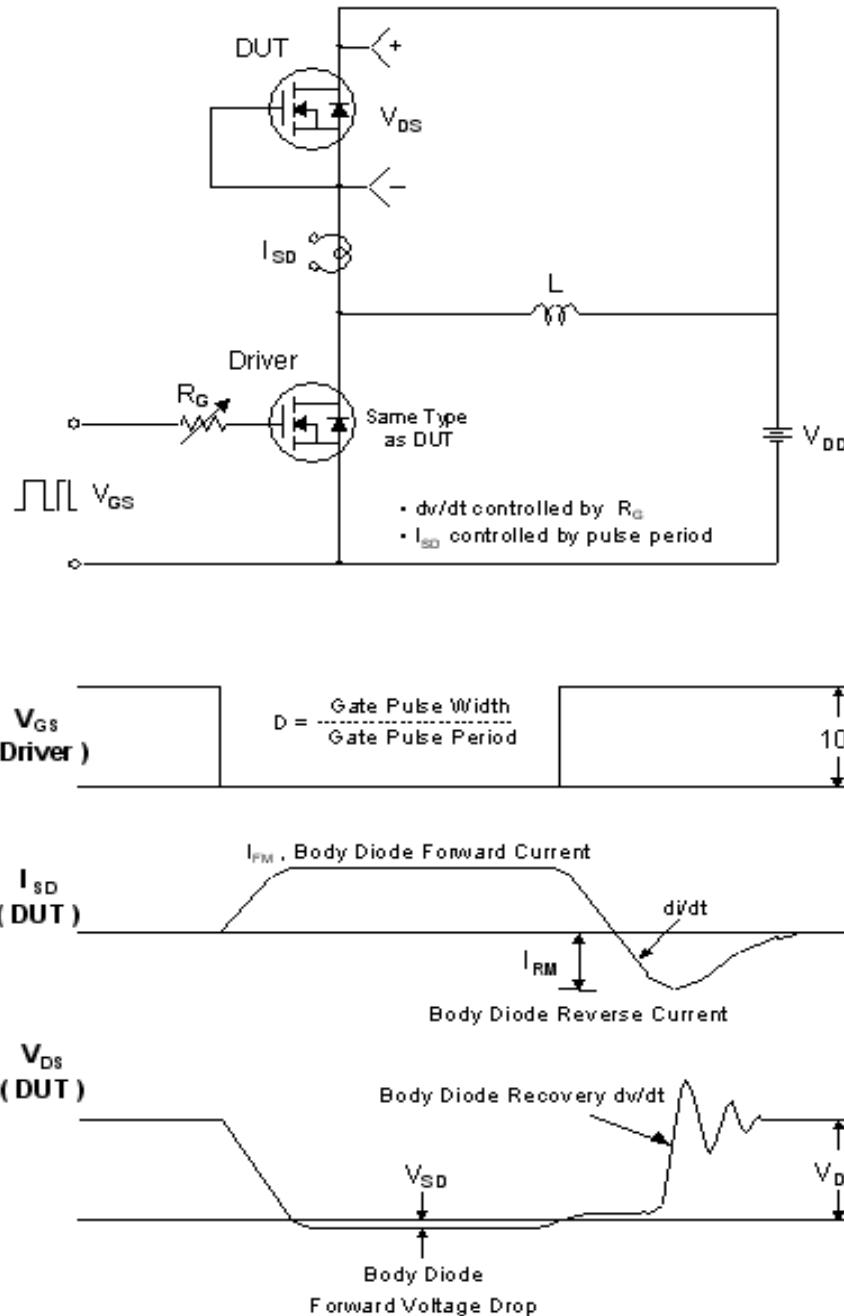
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

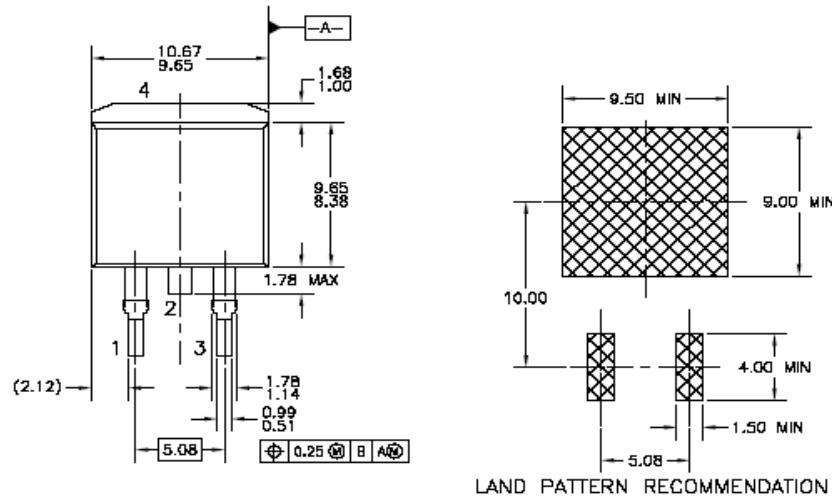


Peak Diode Recovery dv/dt Test Circuit & Waveforms

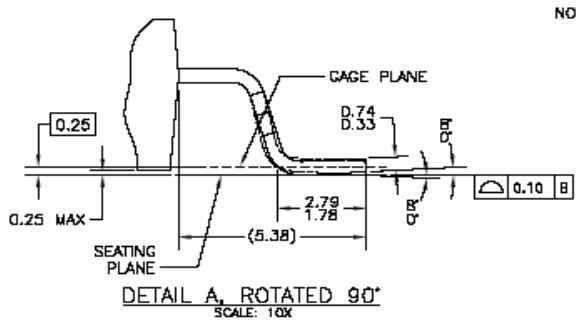
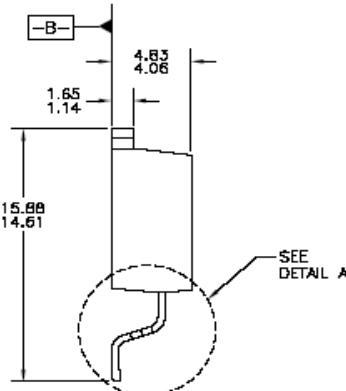
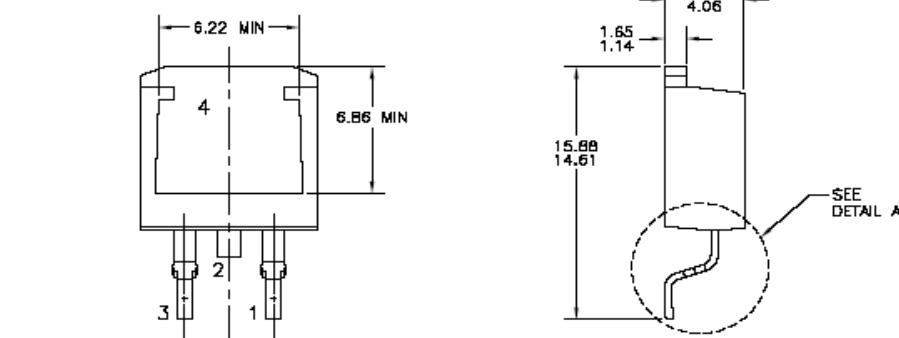


## Package Demensions

### D2-PAK



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) REFERENCE JEDEC, TO-263, ISSUE D, VARIATION AB, DATED JULY 2003.
  - C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1982.
  - D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
  - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

TO263AD2REVD

Dimensions in Millimeters

Ultrafast Recovery Power Rectifier

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE™	FACT Quiet Series™	OCX™	SILENT SWITCHER®	UniFET™
ActiveArray™	GlobalOptoisolator™	OCXPro™	SMART START™	UltraFET®
Bottomless™	GTO™	OPTOLOGIC®	SPM™	VCX™
Build it Now™	HiSeC™	OPTOPLANAR™	Stealth™	Wire™
CoolFET™	I <sup>2</sup> C™	PACMAN™	SuperFET™	
CROSSVOLT™	i-Lo™	POP™	SuperSOT™-3	
DOME™	ImpliedDisconnect™	Power820417™	SuperSOT™-6	
EcoSPARK™	IntelliMAX™	PowerEdge™	SuperSOT™-8	
E <sup>2</sup> CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSign™	LittleFET™	PowerTrench®	TCM™	
FACT™	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
FRFET™	MSX™	RapidConfigure™	TinyLogic®	
	MSXPro™	RapidConnect™	TINYOPTO™	
Across the board. Around the world.™		μSerDes™	TruTranslation™	
The Power Franchise®		ScalarPump™	UHC™	
Programmable Active Droop™				

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I20