ModelSim SE

ModelSim SE is a tool for simulation and verification for Verilog, VHDL and system Verilog. All the designs are compiled into the library and the user start the new design simulation in ModelSim by creating a library which is called work. Work is the default library name used by the compiler. Once the working library is created the next step is to compile the design units into it. The created library of ModelSim is compatible with all the platforms which means you can simulate your design in any platform.

Mentor Graphics was the first to combine single kernel simulator (SKS) technology with a unified debug environment for Verilog, VHDL, and SystemC. The combination of industry-leading, native SKS performance with the best integrated debug and analysis environment make ModelSim the simulator of choice for both ASIC and FPGA designs. The bes standards and platform support in the industry make it easy to adopt in the majority of process and tool flows.

Features:
- Unified mixed language simulation engine for ease of use and performance
- Native support of Verilog, SystemVerilog for design, VHDL, and SystemC for effective verification of sophisticated design environments
- Fast time-to-debug, easy to use, multi-language debug environment
- Advanced code coverage and analysis tools for fast time to coverage closure
- Interactive and Post-Sim Debug available so same debug environment used for both
- Powerful Waveform compare for easy analysis of differences and bugs
- Unified Coverage Database with complete interactive and HTML reporting and processing for understanding and debugging coverage throughout your project
- Coupled with HDL Designer and HDL Author for complete design creation, project management and visualization capabilities