

AC/DC Drivers

Quasi-Resonant Control DC/DC converter IC

BM1Q104FJ

General

The quasi-resonant controller typed AC/DC converter IC "BM1Q104FJ" provides an optimum system for all products that include an electrical outlet. The quasi-resonant operation enables soft switching and helps to keep EMI low. As MOSFET for switching and current detection resistors are external devices, a higher degree of design freedom is achieved.

IC builds in HV starter circuit that tolerates high voltage, it contributes to low consumption power and high speed start. Because IC consumption current is very low and burst operation in light load, the stand-by power is very low.

IC controls to switch bottom numbers in response to loads. And IC builds in harsh sound prevention function of transformer in burst operation.

Because IC builds-in soft-start, burst mode, over current limiter which is cycle-by-cycle, over load protection, over voltage protection, CS open protection and so on, IC provides safety.

Features

- Quasi-resonant method
- Built-in 650V tolerate start circuit
- Low consumption power in light load
- Bottom skip control
- Sound of transformer reduction function
- Harsh sound prevention of transformer function
- VCC pin : under voltage protection
- Over-current protection (cycle-by-cycle)
- OUT pin : H voltage 12.5V clamp
- Soft start
- ZT trigger mask function
- ZT Over voltage protection
- FB Over Load protection [Auto-restart]
- CS pin open protection [Auto-restart]

Package

SOP-J8 6.00mm×4.90mm×1.65mm pitch:1.27mm
(Typ) (Typ) (Max) (Typ)



Key Specifications

- Operating Power Supply Voltage Range:
- VCC : 14.0V to 30.0V
VH : to 600V
- Operating Current: Normal : 0.60mA (Typ)
Burst : 0.37mA(Typ)
- Operate temperature range: -40 to +85deg

Applications

Printer, Copy machine, AC adapter, etc

Application Circuit

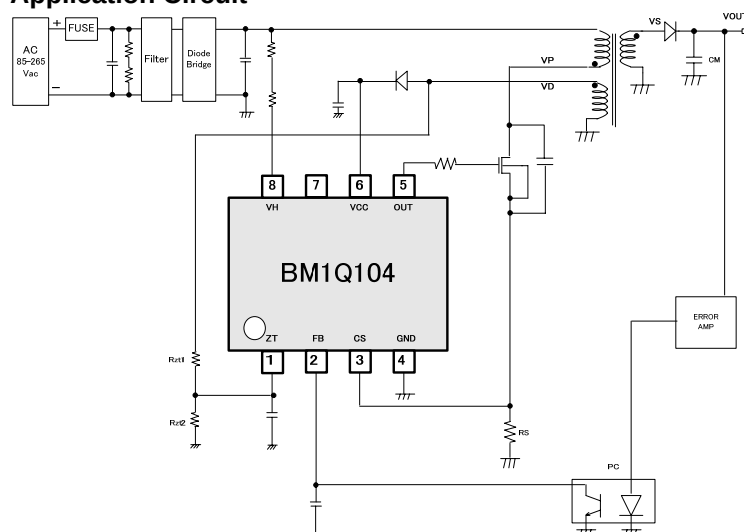


Figure 1. Application Circuit

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit	Condition
voltage range 1	Vmax1	-0.3 ~ 30	V	VCC
voltage range 2	Vmax2	-0.3 ~ 6.5	V	CS, FB
voltage range 3	Vmax3	-0.3 ~ 15	V	OUT
voltage range 4	Vmax4	-0.3 ~ 650	V	VH
OUT pin output peak current	I _{OUT}	±0.50	A	
ZT pin current	I _{SZT}	±3.00	mA	
Allowable dissipation	Pd	0.68 (Note1)	W	
Operating temperature range	T _{opr}	-40 ~ +85	°C	
Max junction temperature	T _{jmax}	150	°C	
Storage temperature range	T _{str}	-55 ~ +150	°C	

(Note 1) When mounted (on 70 mm × 70 mm, 1.6 mm thick, glass epoxy on single-layer substrate).
Reduce to 5.4 mW/°C when Ta = 25°C or above.

Operating Conditions (Ta=25°C)

Parameter	Symbol	Rating	Unit	Conditions
Power supply voltage range 1	VCC	14.0~30.0	V	VCC
Power supply voltage range 2	VH	80~600	V	VH
Power supply voltage range 3	VZT	~7.0	V	ZT
Transformer resonant time	TRT	0.5 ~ 4.0	us	

Electrical Characteristics (Unless otherwise noted, Ta = 25°C, VCC = 15 V)

Parameter	Symbol	Specifications			Unit	Conditions
		MIN	TYP	MAX		
[Circuit current]						
Circuit current (OFF)	I _{OFF}	-	16	50	uA	VCC=12V (VCCUVLO active)
Circuit current (ON)1	I _{ON1}	-	600	1000	uA	FB=2.0V (Switching operation)
Circuit current (ON)2	I _{ON2}	-	370	500	uA	FB=0.3V (Switching OFF)
Circuit current (LATCH)	I _{LATCH}	-	250	400	uA	FB:OPEN In Latch stop state
[VH pin Starter]						
VH Start current1	I _{START1}	0.40	0.70	1.00	mA	VCC=0V
VH Start current2	I _{START2}	1.00	3.00	6.00	mA	VCC=10V
VH OFF current	I _{START3}	-	10	20	uA	Released VCCUVLO VH pin current
VH start current switched voltage	V _{SC}	0.400	0.800	1.400	V	VCC pin
[VCC pin protection]						
VCC UVLO voltage1	V _{UVLO1}	12.50	13.50	14.50	V	VCC rise
VCC UVLO voltage2	V _{UVLO2}	7.20	8.20	9.20	V	VCC fall
VCC UVLO hysteresis	V _{UVLO3}	-	5.30	-	V	V _{UVLO3} = V _{UVLO1} -V _{UVLO2}
VCC charge start voltage	V _{CHG1}	7.70	8.70	9.70	V	Starter circuit
VCC charge end voltage	V _{CHG2}	12.00	13.00	14.00	V	Stop voltage from V _{CHG1}
Latch released voltage	V _{LATCH}	-	V _{UVLO2} -0.50	-	V	
Latch mask time	T _{LATCH}	50	100	200	us	
[OUT pin]						
OUT pin H voltage	V _{OUTH}	10.5	12.5	14.5	V	IO=-20mA VCC=15V
OUT pin L voltage	V _{OUTL}	-	-	0.30	V	IO=+20mA
OUT pin Pull-down resistor	R _{PDOUT}	75	100	125	kΩ	

Electrical Characteristics (Unless otherwise noted, Ta = 25°C, VCC = 15 V)

Parameter	Symbol	Specifications			Unit	Conditions
		MIN	TYP	MAX		
[DC/DC converter unit (Turn-off)]						
Pull-up resistor of FB pin1	RFB1	22.5	30.0	37.5	kΩ	
Pull-up resistor of FB pin2	RFB2	RFB1 × 0.783	RFB1 × 0.833	RFB1 × 0.883	kΩ	In burst operation
CS over current voltage 1A	V _{lim1A}	0.475	0.500	0.525	V	FB=3.2V
CS over current voltage 2A	V _{lim2A}	0.015	0.050	0.085	V	FB=0.3V
Voltage gain1 (ΔVFB/ΔVCS)	AV _{CS1}	5.40	6.00	6.60	V/V	
FB Burst voltage	V _{BURST}	0.25	0.30	0.35	V	
Max burst frequency	FOSCB	3.2	4.0	4.8	kHz	
FB pull-up resistor changed voltage	V _{BSTCH}	V _{BURST} × 1.20	V _{BURST} × 1.33	V _{BURST} × 1.42	V	
CS Leading Edge Blanking time	T _{LEB}	-	0.25	-	us	
Turn-off time	T _{OFF}	-	0.25	-	us	When applied pulse
Minimum ON width	T _{min}	-	0.50	-	us	T _{LEB} + T _{OFF}
Maximum ON width	T _{max}	30.0	39.0	50.7	us	
[DC/DC converter unit (Turn on)]						
On – Off time switched Bottom count						
On Off time switched bottom12	T _{1BTM12}	8.10	9.00	9.90	us	Bottom 1 →2
On Off time switched bottom23	T _{1BTM23}	7.20	8.00	8.80	us	Bottom 2 →3
On Off time switched bottom34	T _{1BTM34}	6.13	7.00	7.88	us	Bottom 3 →4
On Off time switched bottom45	T _{1BTM45}	5.25	6.00	6.75	us	Bottom 4 →5
On Off time switched bottom21	T _{1BTM21}	12.60	14.00	15.40	us	Bottom 2 →1
On Off time switched bottom32	T _{1BTM32}	10.53	11.70	12.87	us	Bottom 3 →2
On Off time switched bottom43	T _{1BTM43}	9.00	10.00	11.00	us	Bottom 4 →3
On Off time switched bottom54	T _{1BTM54}	7.74	8.60	9.46	us	Bottom 5 →4
ZT comparator voltage1	V _{ZT1}	60	100	140	mV	ZT fall
ZT comparator voltage2	V _{ZT2}	120	200	280	mV	ZT rise
ZT comparator hysteresis	V _{ZTHYS}	-	100	-	mV	
ZT trigger mask time	T _{ZTMASK}	1.0	2.0	3.0	us	OUT H ->L prevent noise
ZT Timeout	T _{ZTOUT}	10.5	15.0	19.5	us	Count from last bottom
[DC/DC Protection]						
Soft start time	T _{SS}	2.80	4.00	5.20	ms	
CS pull-up resistor	R _{CS}	0.70	1.00	1.30	MΩ	
FB OLP voltage a	V _{FOLP1A}	3.20	3.40	3.60	V	FBOLP detect (FB rise)
FB OLP voltage b	V _{FOLP1B}	-	V _{FOLP1A} × 0.94	-	V	FBOLP detect (FB fall)
FB OLP delay timer	T _{FOLP}	44.8	64.0	83.2	ms	
FBOLP stop timer	T _{OLPST}	358	512	666	ms	
ZT OVP voltage	V _{ZTL}	3.325	3.500	3.675	V	

*3 Because RFB1 and RFB2 are reacted, RFB1 is always larger than RFB2.

*4 Because VBURST and VBSTCH are reacted, VBURST is always smaller than VBSTCH.

Pin Layout

Table 1 input-output PIN function

NO.	Pin Name	I/O	Function	ESD Diode	
				VCC	GND
1	ZT	I	Zero current detect pin	-	○
2	FB	I	Feedback signal input pin	○	○
3	CS	I	Primary current sensing pin	○	○
4	GND	I/O	GND pin	○	-
5	OUT	O	External MOS drive pin	○	○
6	VCC	I/O	Power supply pin	-	○
7	N.C.	-	Non Connection	-	-
8	VH	I	Starter circuit pin	-	○

External Dimensions

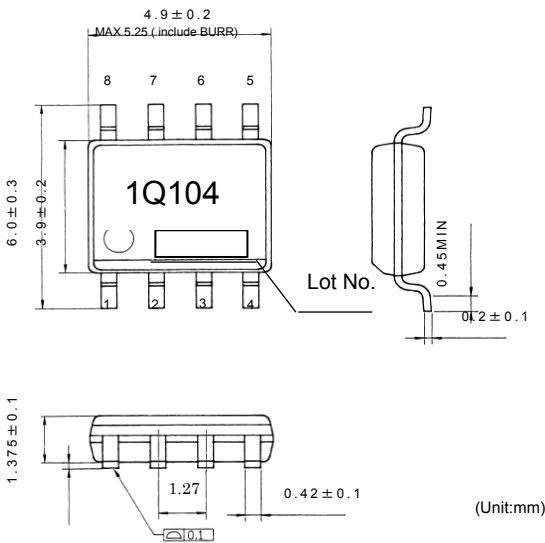


Figure 2. SOP-J8 External Dimensions

I/O Equivalent Circuit Diagram

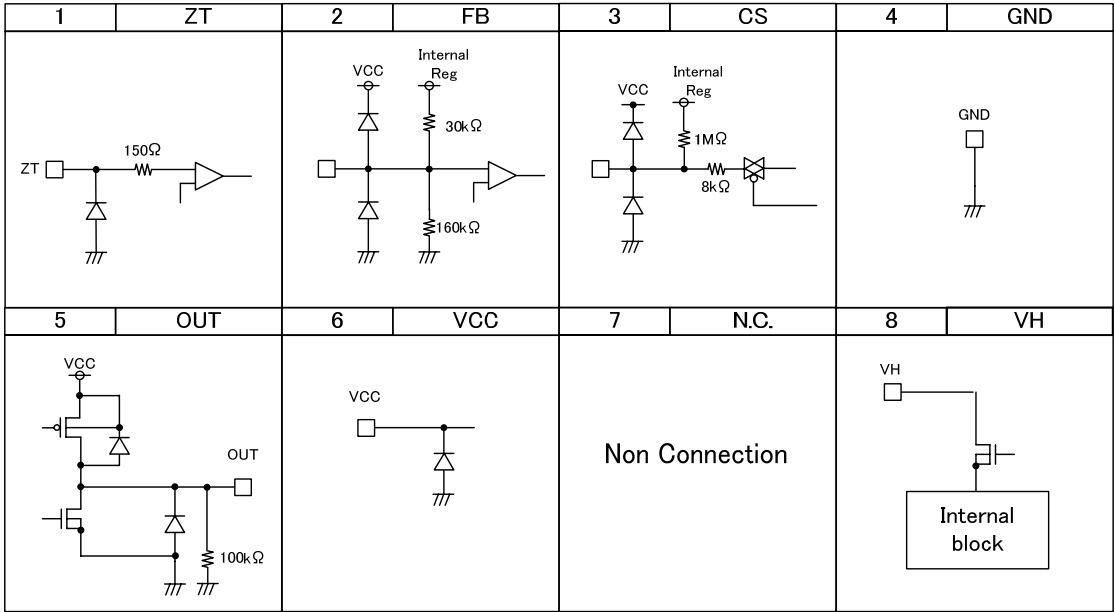


Figure 3. I/O Equivalent Circuit Diagram

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Description of Each Blocks

1. Starter circuit VH pin (8pin)

IC builds in Start circuit (tolerates 650V) to VH pin (8pin). It enables to be low standby power and high speed start. After starting IC, consumption current is decided by idling current I_{START3} (typ=10uA) only from VH pin(8pin). The start time is changed by capacitor value of VCC pin(6pin). Reference values of start time are shown in Figure 7.

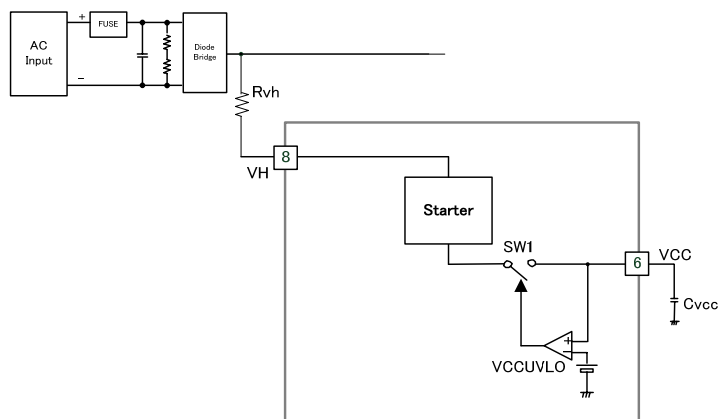


Figure 5. Starter Block

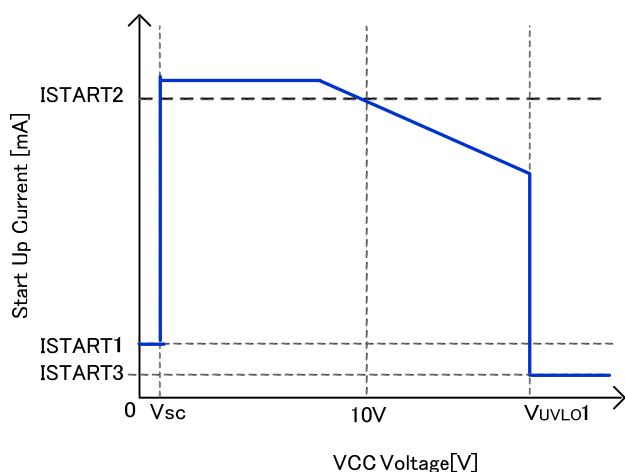


Figure 6. Start Up Current – VCC voltage

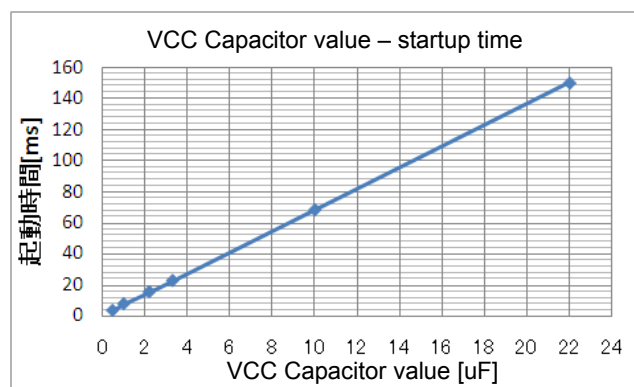


Figure 7. Start Up Time (example)

*Start up current is flowed from VH pin (8Pin).

ex) power consumption of starter circuit only

$$V_{ac}=100V \quad \text{Power}=100V \times \sqrt{2} \times 10\mu A = 1.41mW$$

$$V_{ac}=240V \quad \text{Power}=240V \times \sqrt{2} \times 10\mu A = 3.38mW$$

2. Start sequence (Soft start, light load operation, Auto recovery of over load protection)

IC start sequences are shown in Figure 8. About each detail, explain in each section.

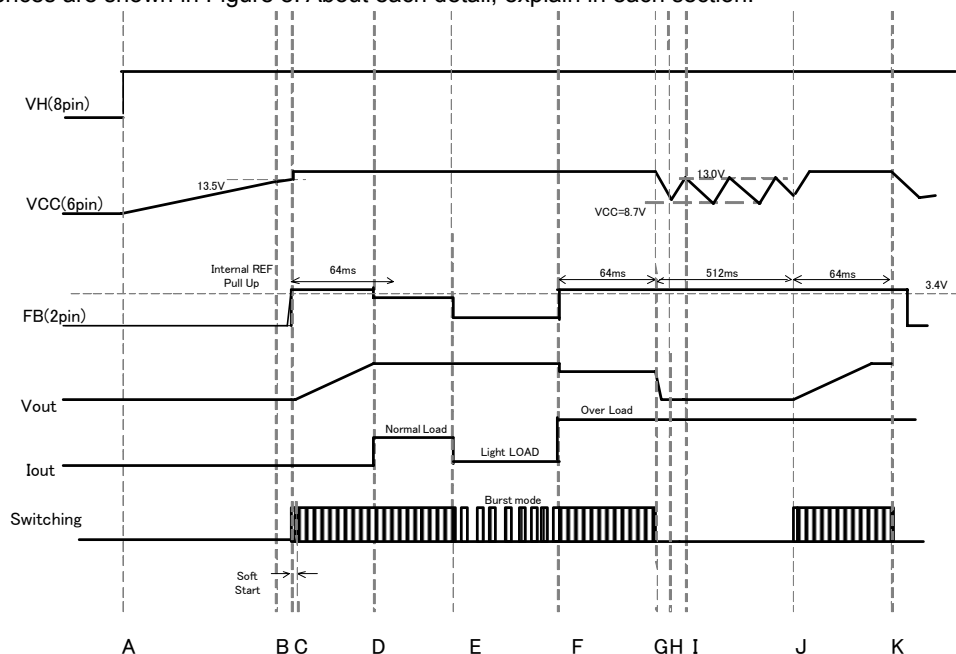


Figure 8. Start sequence time chart

A: Input voltage from AC voltage is supplied to VH pin(8pin).

B: VCC (6pin) voltage is rise. When $V_{CC} > V_{UVLO1}$ (typ=13.5V), IC starts to operate. In case of protection function is no active, IC starts to switching operation.

Then, VCC pin voltage is dropped in cause of VCC (6pin) consumption current. In case of $V_{CC} < V_{CHG1}$ (typ=8.7V), starter circuit operates, IC starts to charge VCC pin.

After starting of charge, IC continues to charge until $V_{CC} > V_{CHG1}$ (typ=13.0V).

C: There is a soft start function that regulates the CS peak voltage level at to prevent a rise in voltage and current redundantly.

D: When the switching operation starts, "VOUT" which is secondary output voltage rises.

After start switching operation, the output voltage is necessary to set to be stable within the T_{FOLP} (typ=64ms) period

E: The burst operation is operated to keep power consumption down in light load.

F: When it is heavy load, FB pin voltage(2pin) is larger than V_{FOLP1A} (typ=3.4V), because output voltage is down.

G: When the FB pin(2pin) voltage keeps V_{FOLP1A} (typ=3.4V) or above for T_{FOLP} (64ms typ), the switching operation is stopped by the over load protection for T_{OLPST} (typ=512ms).

When the FB pin(2pin) voltage does not keep V_{FOLP1B} (typ=3.2V) or above for T_{FOLP} (64ms typ), the timer of T_{FOLP} (typ=64ms) is reset.

H: When VCC voltage (6pin) is less V_{CHG1} (typ=8.7V), starter circuit starts to charge VCC pin(6pin) to operate starter circuit.

I: When VCC voltage (6pin) is above V_{CHG2} (typ =13.0V), starter circuit stops to charge VCC pin(6pin).

J: The same as F.

K: The same as G.

3. VCC pin (6pin) protection function

IC is built in VCC UVLO (Under Voltage Protection) function and VCC charge function.

VCC UVLO function is the protection when VCC (6pin) voltage is low.

VCC UVLO function is for preventing MOSFET for switching from destroying when VCC pin voltage is low.

VCC charge function is for settling secondary output voltage in VCC pin voltage low, as starter circuit charge VCC pin from VH line.

(1) VCC UVLO

VCC UVLO is auto recovery typed protection that has voltage hysteresis,

In Figure 9, it is shown the operation.

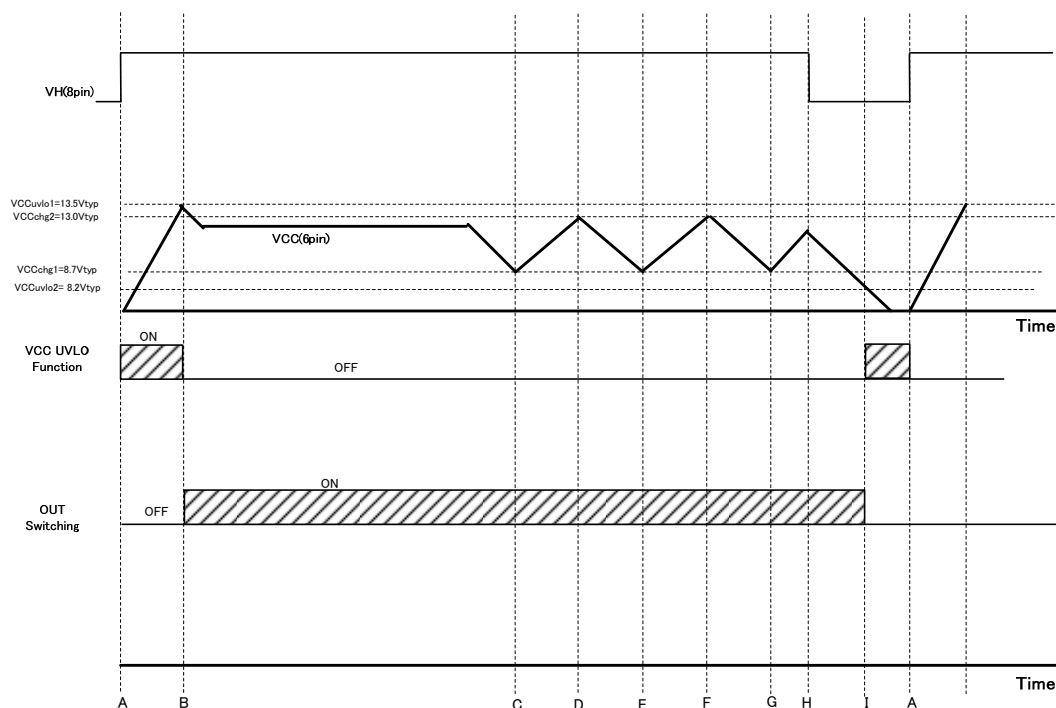


Figure 9. VCC UVLO Timing chart

A: VH (8pin) pin voltage is applied, VCC (6pin) voltage starts rising.

B: When VCC pin (6pin) voltage $> V_{UVLO1}$, the VCC UVLO function is released and DC/DC operation starts.

C: VCC (6pin) voltage $< V_{CHG1}$, VCC charge function operates and the VCC (6pin) voltage rises.

D: VCC (6pin) voltage $> V_{CHG2}$, VCC charge function stops.

E: The same as C.

F: The same as D.

G: The same as C.

H: High voltage line "VH" is down.

I: VCC $< V_{UVLO2}$, VCC UVLO function is operated.

(2)VCC charge function

Once VCC (6pin) pin voltage $> V_{UVLO1}$, IC start to operate. After that, when VCC pin voltage $< V_{CHG1}$, VCC charge function is active. Then starter circuit operates charge from VH line to VCC (6pin). A malfunction for start-up does not occur. The operation is shown to Figure 10.

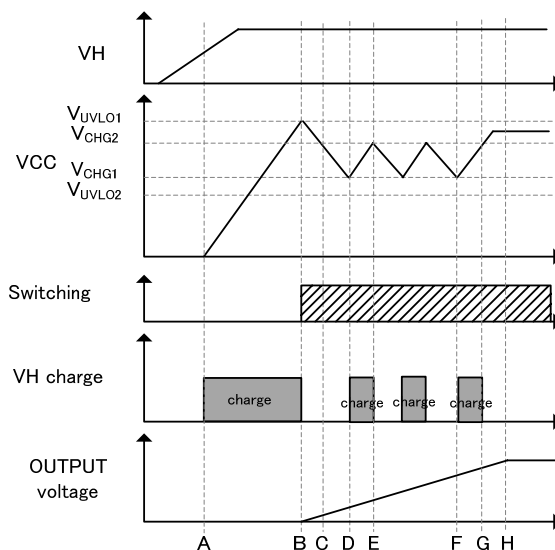


Figure 10. VCC pin charge operation

- A: As VH pin voltage (8pin) is rising, IC is started to charge to VCC(6pin) by VCC charge function.
- B: When VCC pin (6pin) voltage $> V_{UVLO1}$, VCC UVLO function is released, VCC charge function is stopped, DC/DC operation starts.
- C: VCC (6pin) voltage drops on starting because OUTPUT voltage is low.
- D: VCC (6pin) voltage $< V_{CHG1}$, VCC pin(6pin) voltage rises to start by VH charge.
- E: VCC (6pin) voltage $> V_{CHG2}$, VCC charge stops.
- F: VCC (6pin) voltage $< V_{CHG1}$, VCC pin (6pin) voltage rises to restart by VH charge.
- G: VCC (6pin) voltage $> V_{CHG2}$, VCC charge function stops.
- H: OUTPUT voltage is stable. Then, VCC pin (6pin) voltage is stable for charging from the auxiliary coil to VCC pin(6pin).

Care) As VCC pin voltage range must be set over V_{CHG2} (Max=14.0V), the auxiliary winding is set.

4. DC/DC driver

BM1Q104FJ operates on PFM (Pulse Frequency Modulation) mode method.

By monitoring FB pin(2pin) and ZT pin (1pin), CS pin(3pin), the IC supply optimum system for quasi-resonant operation. The IC controls ON width (Turn Off) of external MOSFET by FB pin(2pin) and CS pin(3pin). The IC controls OFF width (Turn ON) of external MOSFET by ZT pin (1pin). The detail is shown below. (Refer to Figure 11.)

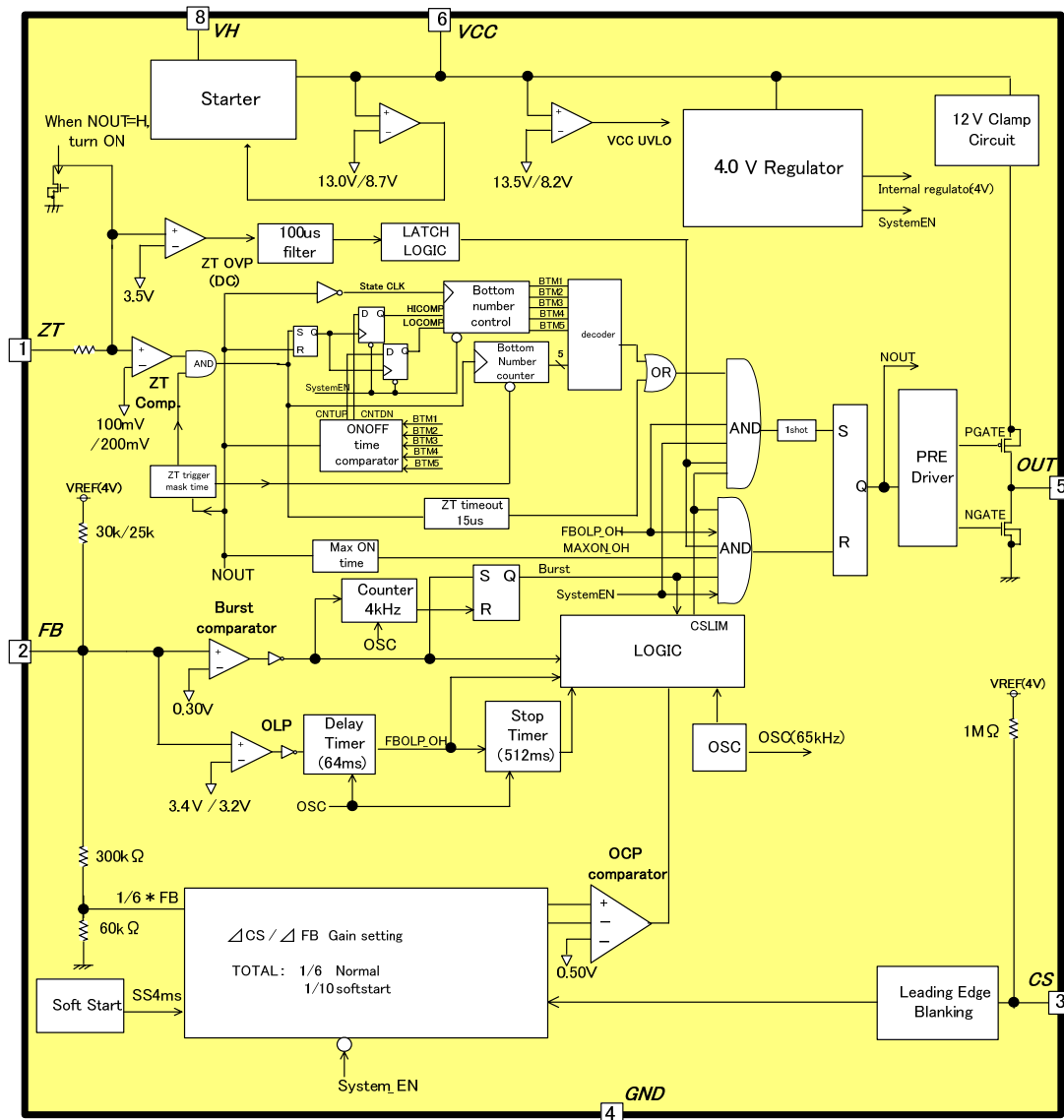


Figure 11. DC/DC Operation Block

(1) Determination of ON width (Turn OFF)

The ON width is controlled by FB pin(2pin), CS pin(3pin).

As FB voltage divided by AV_{CS1} (typ=6) and CS pin voltage are compared, the IC decides ON width.

CS comparator level is changed lineally to be shown in Figure 12.

CS (3pin) is built in over current limiter circuit per pulse. IC set over current limiter level by FB (2pin) voltage.

•FB voltage < 0.3V : Burst operation.

•0.3V < FB voltage < 3.4V : $\angle CS/FB$ gain = $1/AV_{CS1}$ (typ=6) = 1/6 operation

•3.4V < FB voltage : Over load operation (To detect over load state, IC is stopped switching)

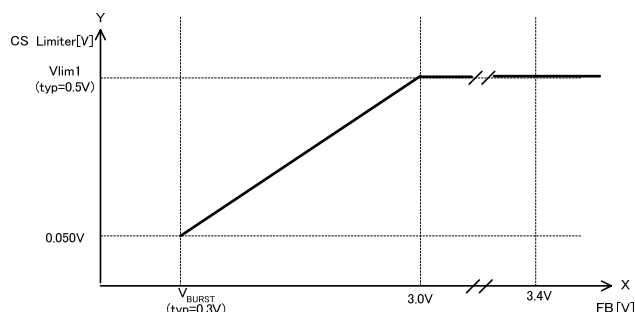


Figure 12. FB pin voltage - over current limiter characteristics
[gain=1/6 setting]

When soft-start operation is done, CS over current protection voltage is adjusted over current detection level. Vlim1 on soft-start are changed to show below.

Table2 Over current detection voltage Detail

Softstart	Vlim1
start ~4ms	0.300V(60%)
4ms~	0.500V(100%)

(2) LEB (Leading Edge Blanking) function

When a MOSFET for switching is turned ON, surge current occurs in cause of capacitance or rush current.

Therefore, CS (3pin) voltage rises temporarily, and over current limiter circuit may miss detections.

To prevent miss detections, the IC builds in Leading edge blanking function which mask CS detection for

T_{LEB} (typ=250ns) from switching OUT pin(5pin) from L to H. This blanking function enables to reduce noise filter of CS pin(3pin).

(3) Determination of OFF width (Turn on)

OFF width is controlled at the ZT pin.

When switching is OFF, the power stored in the primary-side winding is supplied to the secondary-side output capacitor. When the power had supplied, there is no more current flowing to the secondary side output capacitor, the drain pin voltage of switching MOSFET drops. After that, resonant operation starts. Consequently, the voltage on the auxiliary winding also starts it.

ZT pin voltage was applied the voltage resistance-divided by Rzt1 and Rzt2.

When ZT pin voltage level drops to V_{ZT1} (typ=100mV) or below, IC detects it as the bottom of resonant. When bottom count is up to certain count, MOSFET is turned ON by the ZT comparator. Since zero current detection time is adjusted at Czt, Rzt1 and Rzt2 of the ZT pin in Figure 4.

Additionally, a ZT trigger mask function (described in section 4-6) and a ZT timeout function (described in section 4-7) are built in ZT pin. It shows about certain bottom count below.

It explains below about constant bottom numbers.

The IC changes a bottom number in response of loads. The bottom number is decided by a charge and discharge time.

The charge and discharge waveform is shown in Figure 13. The charge and discharge time – bottom numbers are shown in table-3. The bottom number for charge and discharge time and switching example for loads are shown in Figure 14.

Switching frequency = $1 / \{ \text{charge and discharge time} + (\text{Bottom count} - 1) \times \text{resonant time} + 1/2 \times \text{resonant time} \}$

Resonant time = $2 \times \pi \times \sqrt{L_p \times C_{ds}}$

* L_p : primary inductance value, C_{ds} : Capacitance of MOSFET between drain and source.

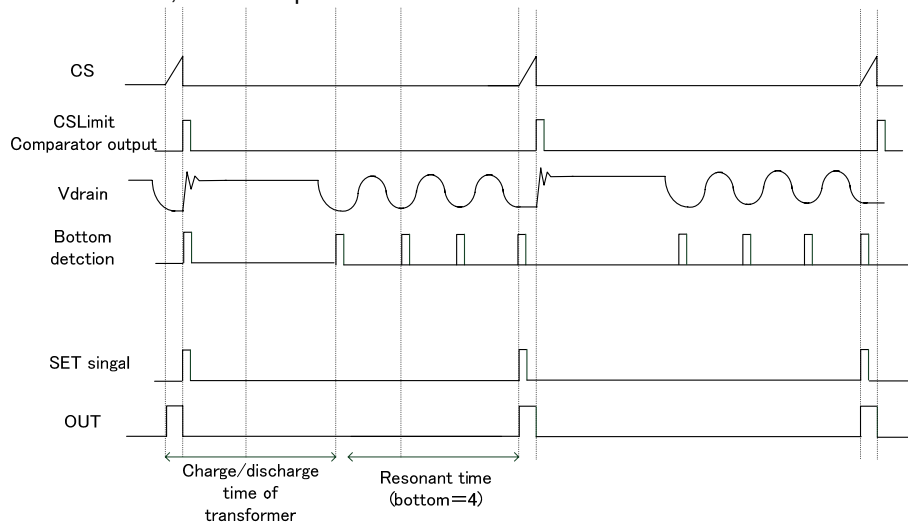


Figure 13. charge/discharge time of transformer- Bottom time

Table 3-1 Bottom count – ON OFF width table (Load increasing)

Bottom	Charge/discharge time[us]
5	~ 8.6
4	8.6 ~ 10.0
3	10.0 ~ 11.7
2	11.7 ~ 14.0
1	14.0 ~

Table 3-2 Bottom count – ON OFF width table (Load decreasing)

Bottom	Charge/discharge time[us]
1	~ 9.0
2	8.0 ~ 9.0
3	7.0 ~ 8.0
4	6.0 ~ 7.0
5	~ 6.0

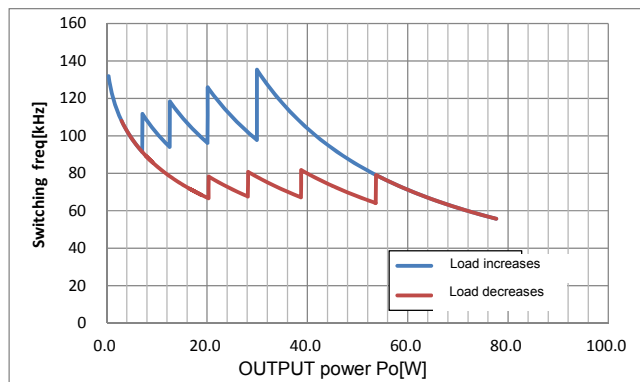


Figure 14-1. Output power–Switching frequency

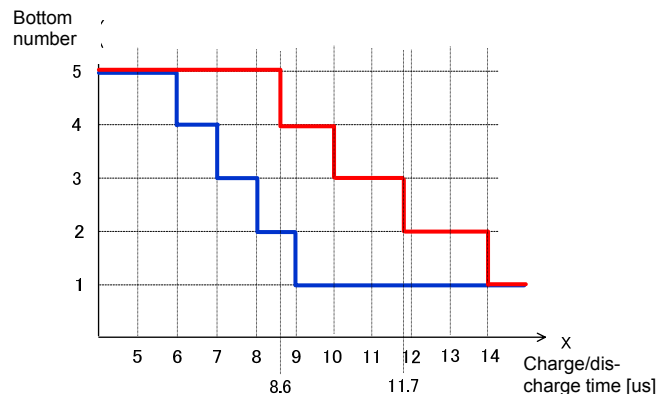


Figure 14-2. Charge/discharge time–bottom number

(4) A harsh sound reduction function in burst operation

When FB pin voltage(2pin) is lower than $V_{BURST}(typ=0.3V)$, IC stops switching for burst operation. IC built in a harsh sound reduction function to reduce harsh sound of transformer (10kHz ~ 20kHz) in burst operation. The burst frequency is not operated ranged from 10kHz to 20kHz. The operation is shown in Figure 15. By the function, the base frequency spectrum is not from 10kHz to 20kHz. For that, harsh sound is reduced. The operation is shown in Figure 15. about burst frequency.

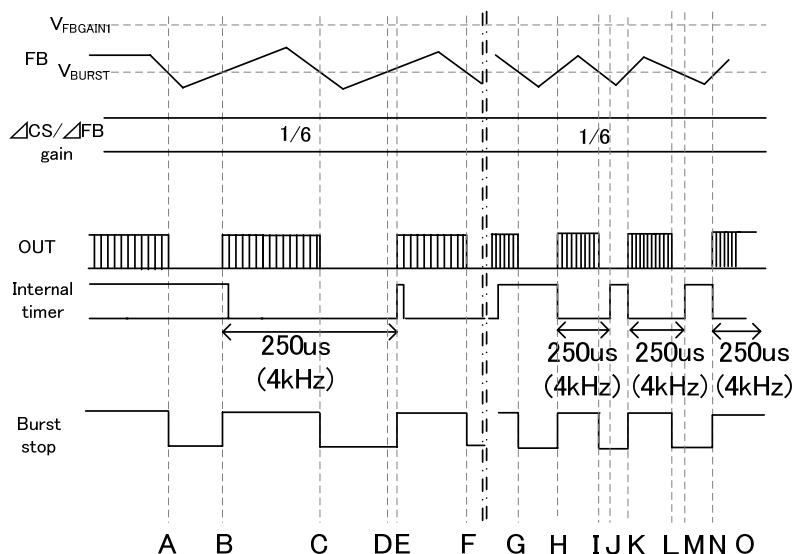


Figure 15. Switching waveform in burst operation

- A: Because the output load is light, FB pin voltage drops. When FB pin voltage $< V_{BURST}(typ=0.3V)$, IC stops switching operation.
 B: IC starts switching because the FB pin voltage $> V_{BURST}(typ=0.3V)$ after 250us(4kHz) from start switching.
 C: When FB pin voltage $< V_{BURST}(typ=0.3V)$, IC stops switching.
 D: FB pin voltage $> V_{BURST}(typ=0.3V)$. Because it does not pass 250us($F=4kHz$) from B period, IC does not operate switching.
 E: Because it passes 250us from previous burst-start, IC starts switching.
 F: When FB pin voltage $< V_{BURST}(typ=0.3V)$, IC stops switching.
 G: When FB pin voltage $< V_{BURST}(typ=0.3V)$, IC stops switching.
 H: After it past 250us from previous switching start, FB pin voltage rises $V_{BURST}(typ=0.3V)$, IC starts switching.
 I: IC stops switching because $FB < V_{BURST}(typ=0.3V)$.
 J: Though it past 250us from H, IC does not operate switching for FB voltage $< V_{BURST}(typ=0.3V)$.
 K: IC starts switching operation to be FB pin voltage $> V_{BURST}(typ=0.3V)$.
 L: IC stops switching operation to be FB pin voltage $< V_{BURST}(typ=0.3V)$.
 M: Though it past 250us from K, IC does not operate switching for FB voltage $< V_{BURST}(typ=0.3V)$.
 N: IC starts switching operation because $FB \text{ pin} > V_{BURST}(typ=0.3V)$.

When harsh sound reduction function operates, the burst frequency is operated in Figure 16.

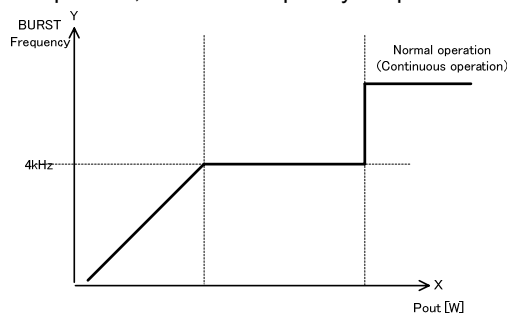


Figure 16. Burst frequency operation

(5) Gain up function in burst operation

When FB pin is lower than $V_{BURST}(typ=0.3V)$, IC stops switching operation by burst function. IC builds in gain up function for preventing harsh sound of transformer and reducing output voltage ripple. The function operates that FB pin pull-up resistor is switched between $R_{FB1}(typ=30k\Omega)$ and $R_{FB2}(typ=25k\Omega)$.

Because IC is changed the DC/DC gain, when DC/DC application oscillates in burst operation released, FB pin capacitor may be larger. By the function, FB voltage speed is faster near load of burst operation. When FB pin voltage is larger than $V_{BSTCH}(typ=0.4V)$, the gain up function is released. Figure 17. shows the operation.

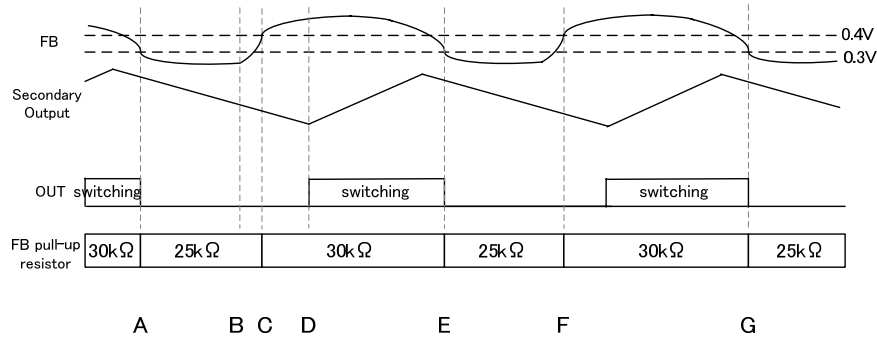


Figure 17. Gain up function in burst operation waveform

- A: The load is light. When FB pin voltage is lower than $V_{BURST}(typ=0.3V)$, IC stops switching operation. Then FB pin pull-up resistor changes from $R_{FB1}(typ=30k\Omega)$ to $R_{FB2}(typ=25k\Omega)$.
- B: Because the output voltage is lower than regulation voltage, FB pin voltage rises.
- C: When FB voltage is larger than $V_{BSTCH}(typ=0.4V)$, FB pull-up resistor changes from $R_{FB2}(typ=25k\Omega)$ to $R_{FB1}(typ=30k\Omega)$, the gain up function is released.
- D: After harsh sound reduction function is released, IC starts switching operation.
- E: The load is light. When FB pin voltage is lower than $V_{BURST}(typ=0.3V)$, IC stops switching operation. Then FB pin pull-up resistor changes from $R_{FB1}(typ=30k\Omega)$ to $R_{FB2}(typ=25k\Omega)$.
- F: When FB voltage is larger than $V_{BSTCH}(typ=0.4V)$, FB pull-up resistor changes from $R_{FB2}(typ=25k\Omega)$ to $R_{FB1}(typ=30k\Omega)$, the gain up function is released.

(6) ZT trigger mask function (Figure 18.)

When MOSFET turns from ON to OFF, turn off noise may occur at the ZT pin.

Then, the ZT comparator and ZTOVP comparator are masked for the $T_{ZTMASK}(typ=2.0\mu s)$ time to prevent ZT comparator miss-detection.

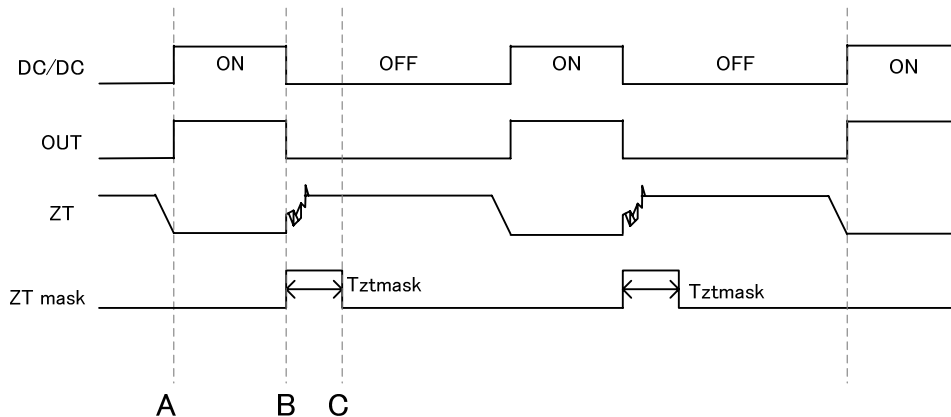


Figure 18. ZT trigger mask function waveform

- A: DCDC OFF=> ON
- B: DCDC ON=> OFF
- C: IC masks ZT pin action for $T_{ZTMASK}(typ=2.0\mu s)$ to occur the noise at ZT pin.

(7) ZT timeout function (Figure 19.)

After ZT comparator detects bottom, when ZT pin does not detect next bottom within T_{ZTOUT} (typ = 15 μ s), IC turns on MOSFET by force.

When secondary output voltage is low such as start-up, the voltage on the auxiliary winding "VA" is also low. Then ZT pin (1pin) voltage is low than V_{ZT2} (typ = 200mV). In that case, the function is operated.

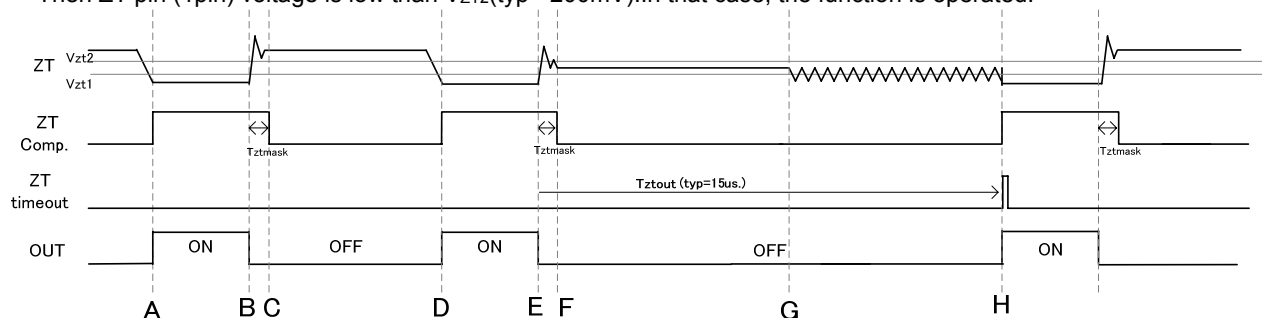


Figure 19. ZT timeout function

- A: $ZT < V_{ZT1}$, IC turns ON operation to detect bottom.
 B: DC/DC ON $\Rightarrow$ OFF. For the state of $ZT > V_{ZT2}$ (typ = 200mV), the timeout function is no operation.
 C: Because the surge noise occurs to ZT pin, IC does not have no operation ZT comparator for T_{ZTMASK} time.
 D: $ZT < V_{ZT1}$, IC turns ON to detect bottom.
 E: DC/DC ON $\Rightarrow$ OFF. Then $ZT < V_{ZT2}$.
 F: For $ZT < V_{ZT2}$, the timeout function starts to operate at the time.
 G: The timeout operation continues for $ZT < V_{ZT2}$.
 H: Since ZT pin voltage is lower than V_{ZT1} for T_{ZTOUT} , IC turns ON by force by timeout function.

5. Soft start sequence

Normally, when AC voltage is applied, a large current flows. Then secondary output voltage and current is occurred overshoot.

For preventing it, IC built in soft-start function.

When VCC pin(6pin) voltage is lower than V_{UVLO2} (typ = 8.2V), IC is reset. After that, when AC voltage is applied, IC operates soft-start.

The soft start operation is shown below: (Please refer to (4-1) turn off item.)

- start $\sim$ 4.0ms $\Rightarrow$ Set CS limiter to 60% of normal operation.
- 4.0ms $\sim$ $\Rightarrow$ normal operation.

6. ZT pin (1pin) OVP (Over Voltage Protection)

OVP function is built at ZT pin(1pin). The protection method is latched type.

IC built in T_{LATCH} (typ = 100 μ s) timer to prevent ZT OVP from miss-detecting at noise.

7. CS (3pin) open protection

IC builds in CS pin(3pin) open protection to prevent OUT pin from changing to H by noise when CS pin(3pin) is OPEN.

When CS pin(3pin) is open, IC stops switching operation by the function. (This is auto-recovery)

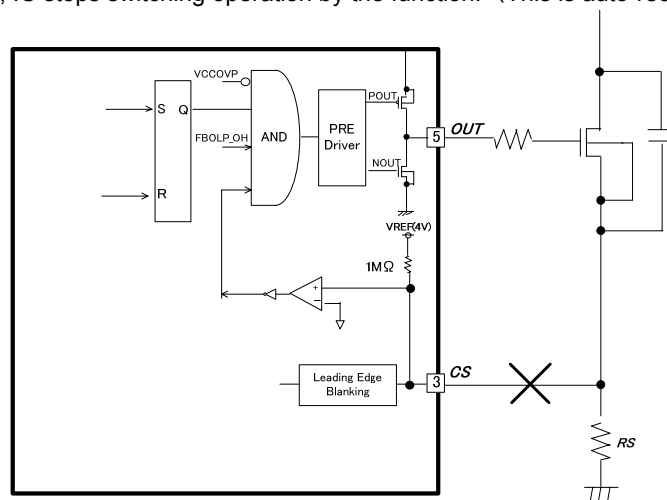


Figure 20. CS open protection

8. OUTPUT Over Load protection (FB OLP comparator)

When secondary output is over load, IC detects it at FB pin(2pin), and IC stops switching operation.

Because secondary photo-coupler is not flown current in OLP state, FB (2pin) voltage is up in Figure 4. circuit.

When the state continues for T_{FOLP} (typ=64ms), IC detects over load state, IC stops switching operation. After FB (2pin) voltage is over V_{FOLP1A} (typ=3.4V), when FB pin(2pin) voltage is lower than V_{FOLP1B} (typ=3.2V) within T_{FOLP} (typ =64ms), over load protection timer is reset. Then IC does not stop switching operation.

In start-up, because FB pin(2pin) is connected to a pull-up resistor to internal voltage, FB (2pin) voltage starts to operate in the state which is more than V_{FOLP1A} (typ =3.4V).

For that, secondary output voltage has to be set within T_{FOLP} (typ =64ms) from starts-up.

When detecting over load, IC stops switching operation for T_{OLPST} (typ =512ms). After that, IC is auto-recovery operation.

In stopping switching operation, though VCC (6pin) voltage is not charged from auxiliary coil side, IC operates re-charge function from starter circuit. For that, VCC (6pin) voltage keeps VCC pin voltage > V_{UVLO2} .

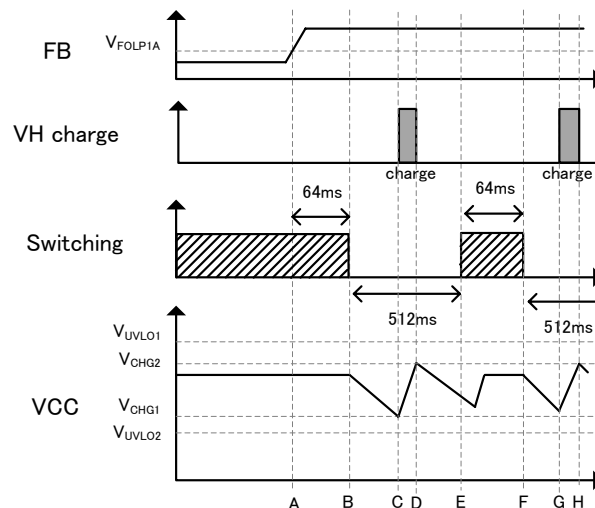


Figure 21. Over load protection : Auto-recovery

A: When FB voltage is over V_{FOLP1A} (typ=3.4V), FBOLP comparator detects over load.

B: When the state A continues for T_{FOLP} (typ=64ms), IC stops switching by over load protection.

C: During stopping switching by over load protection, VCC (6pin) voltage drops. When VCC (6pin) voltage is lower than V_{CHG1} , VCC re-charge function operates. Then VCC (6pin) voltage is up.

D: When VCC (6pin) voltage is higher than V_{CHG2} by re-charge function, VCC recharge function is stopped.

E: When it takes for T_{OLPST} (typ =512ms) from B, IC starts switching with soft-start.

F: When over load state continues, FB (2pin) voltage is over V_{FOLP1A} . When it passes for T_{FOLP} (typ=64ms) from E, IC stops switching by over load protection.

G: During stopping switching by over load protection, VCC (6pin) voltage drops. When VCC (6pin) voltage is lower than V_{CHG1} , VCC re-charge function operate, VCC (6pin) voltage is up.

H: When VCC (6pin) voltage is higher than V_{CHG2} by re-charge function, VCC recharge function is stopped.

9. OUT(5pin) clamp function

H level of OUT (5pin) is clamped to V_{OUTH} (typ=12.5V) by the purpose which protects external MOSFET

It prevents gate destruction of MOSFET of rising VCC (6pin) voltage. (It refers to Figure 22.)

OUT pin(5pin) is connected to pull-down R_{PDOUT} (typ=100k Ω).

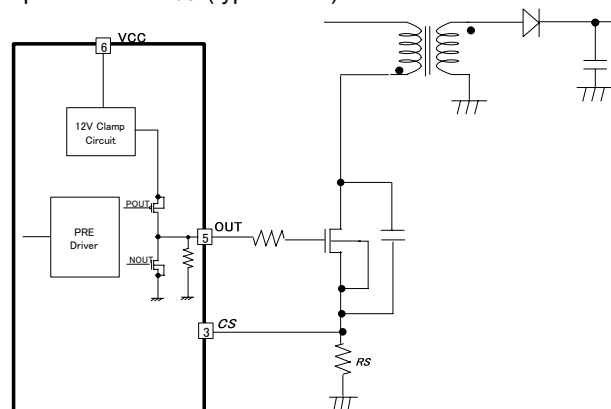


Figure 22. OUT (5pin) construction

Operation mode of protection circuit

Operation mode of protection functions are shown in table-4.

Table-4 Operation mode of protection circuit

Item	protection mode
VCC Under Voltage Locked Out	Self-restart
FB Over Load Protection	Self-restart(64ms delay, 512ms stop)
CS Open Protection	Self-restart
ZT Over Voltage Protection	Latch stop(With 100us timer)
VCC Charge Protection	Self-restart

Thermal loss

The thermal design should set operation for the following conditions.

(Since the temperature shown in Figure-23 is the guaranteed temperature, be sure to take a margin into account.)

1. The ambient temperature "Ta" must be 85°C or less.
2. The IC's loss must be within the allowable dissipation Pd.

The thermal abatement characteristics are as follows.

(PCB: 70 mm × 70 mm × 1.6 mm, mounted on glass epoxy substrate)

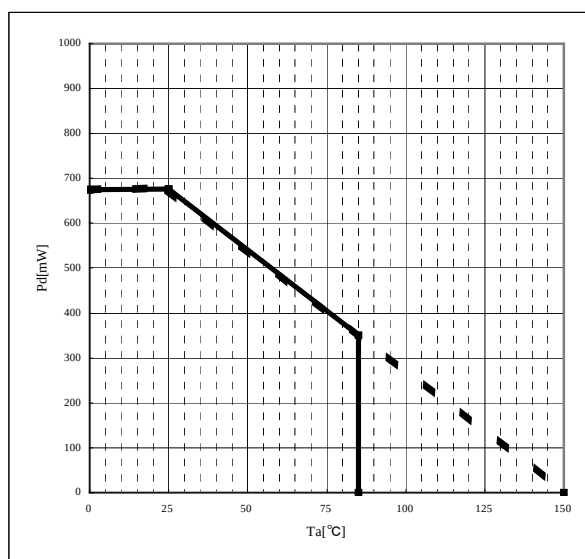


Figure 23. SOP-J8 Thermal Abatement Characteristics

●Reference Data (This is a reference data. For that, it is not guaranteed.)

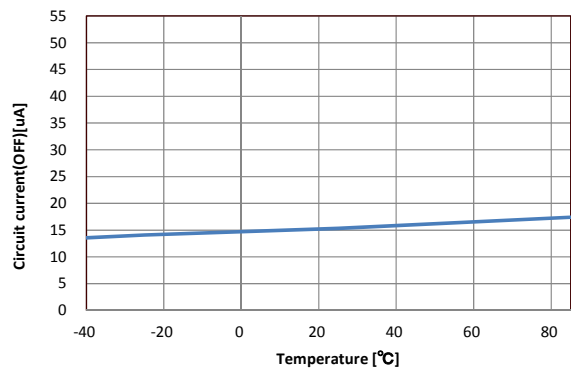


Figure 24 Circuit current(OFF) vs Temperature

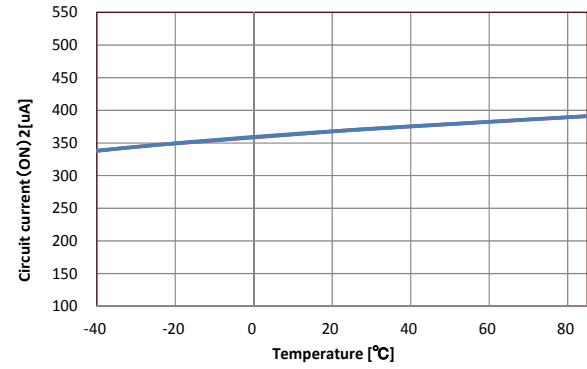


Figure 25 Circuit current(ON)2 vs Temperature

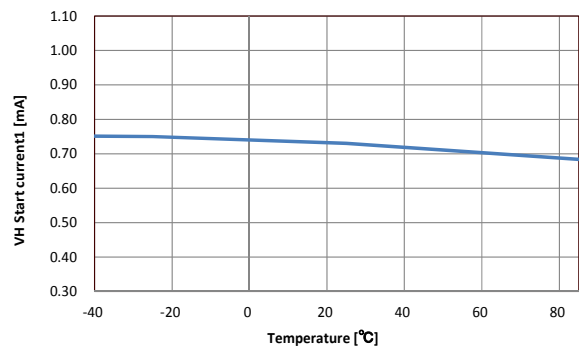


Figure 26 VH start current1 vs Temperature

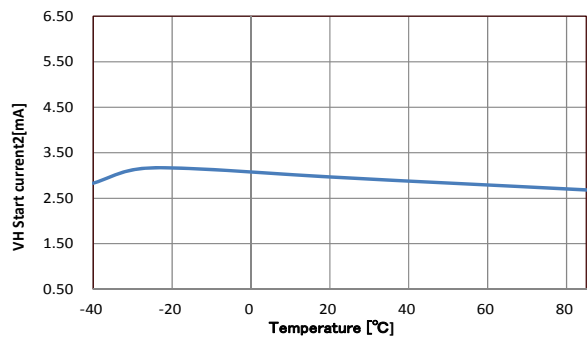


Figure 27 VH start current2 vs Temperature

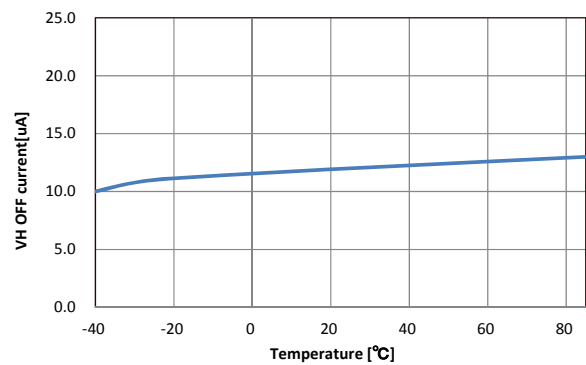


Figure 28 VH OFF current vs Temperature

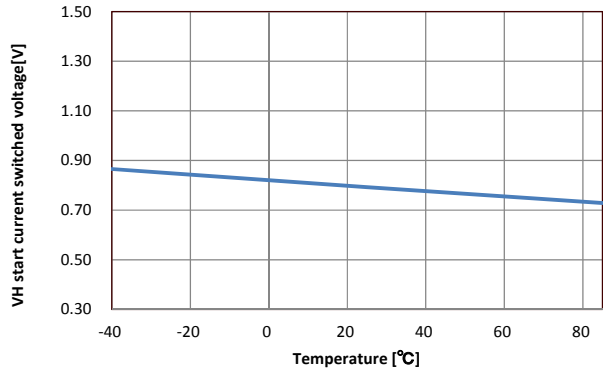


Figure 29 VH start switched voltage vs Temperature

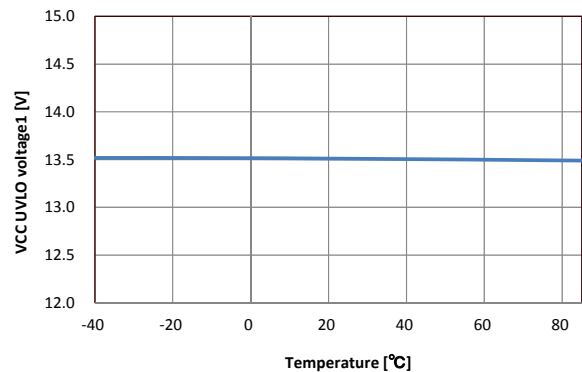


Figure 30 VCC UVLO voltage1 vs Temperature

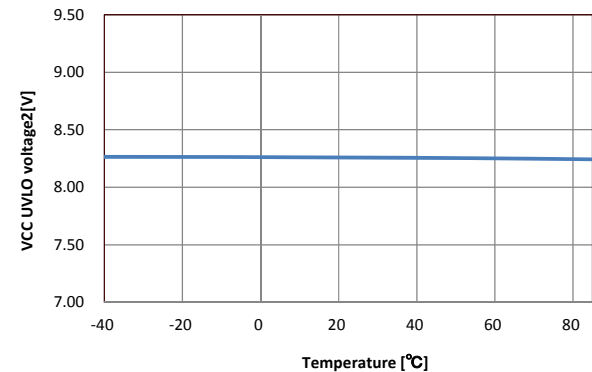


Figure 31 VCC UVLO voltage 2 vs Temperature

●Reference Data (This is a reference data. For that, it is not guaranteed.)

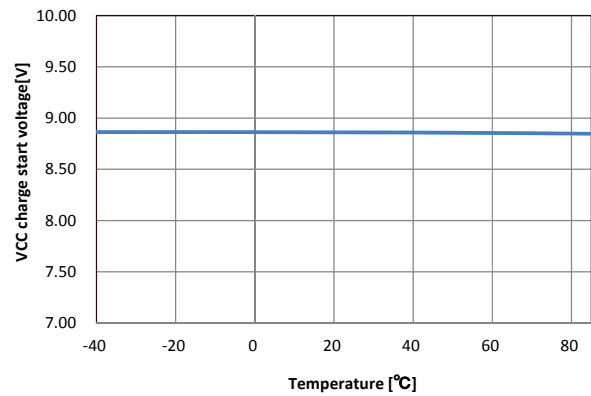


Figure 32 VCC charge start voltage vs Temperature

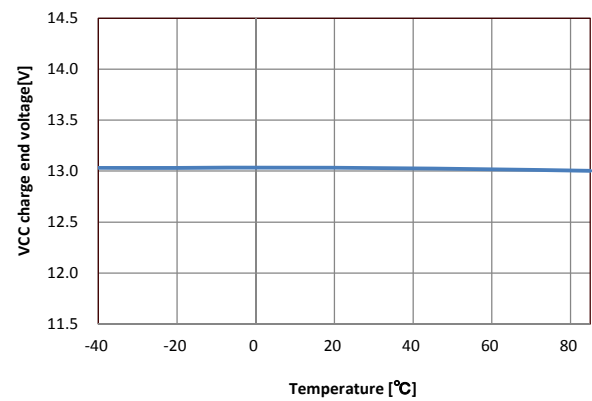


Figure 33 VCC charge end voltage vs Temperature

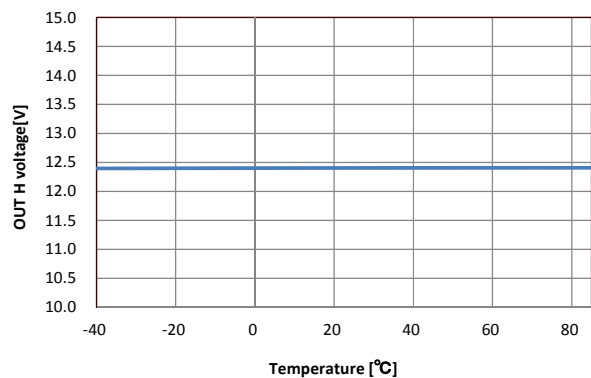


Figure 34 OUT H voltage vs Temperature

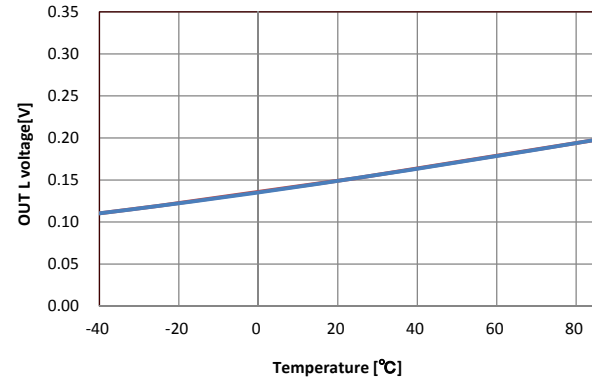


Figure 35 OUT L voltage vs Temperature

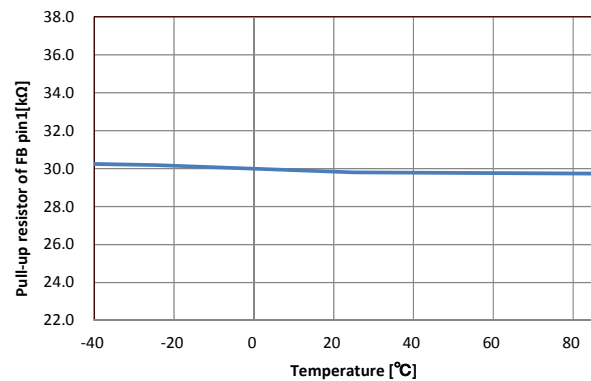


Figure 36 Pull-up resistor of FB pin 1 vs Temperature

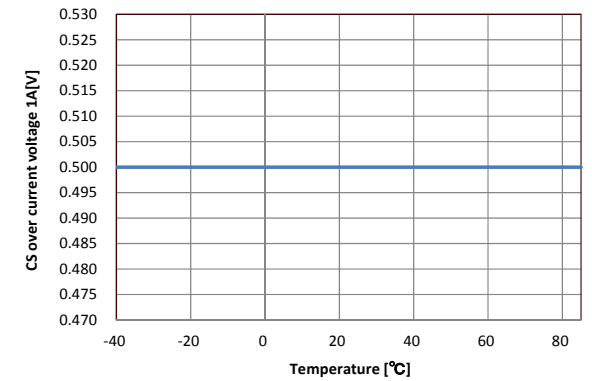


Figure 37 CS over current voltage 1A vs Temperature

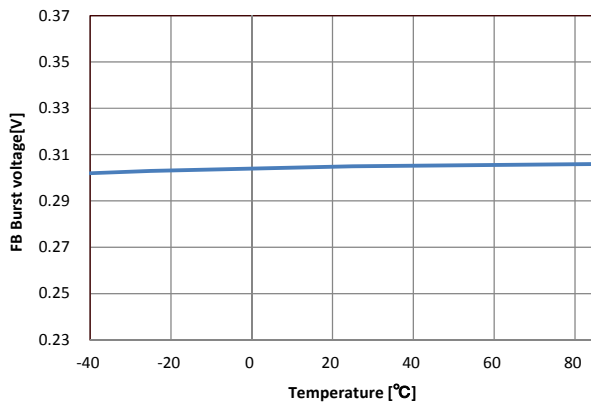


Figure 38 FB Burst voltage vs Temperature

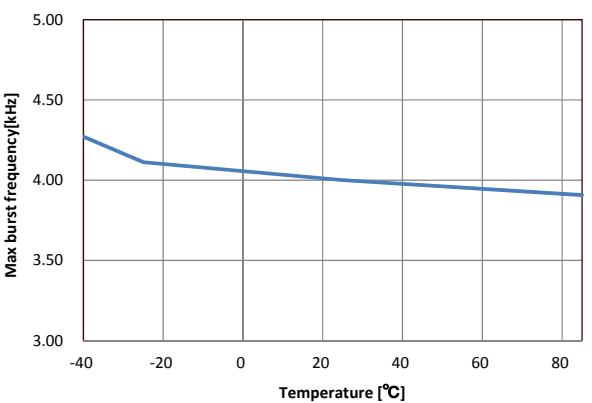


Figure 39 Max burst frequency vs Temperature

●Reference Data (This is a reference data. For that, it is not guaranteed.)

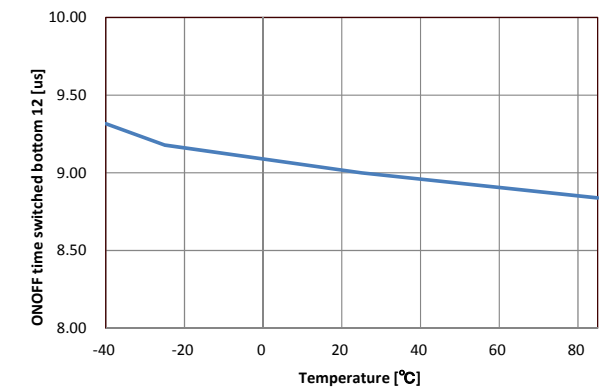


Figure 40 ONOFF time switched bottom 12 vs Temperature

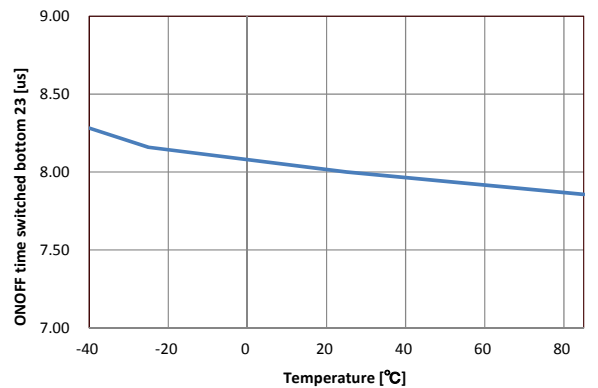


Figure 41 ONOFF time switched bottom 23 vs Temperature

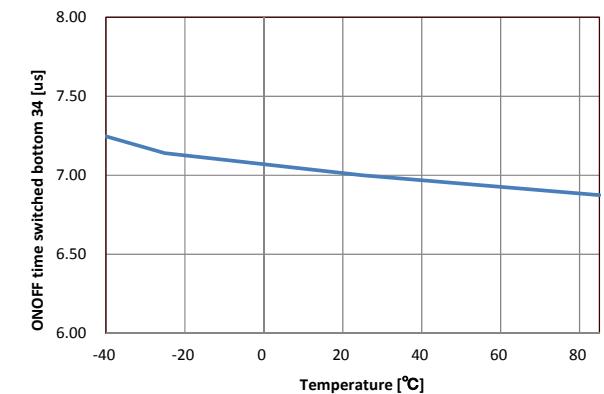


Figure 42 ONOFF time switched bottom 34 vs Temperature

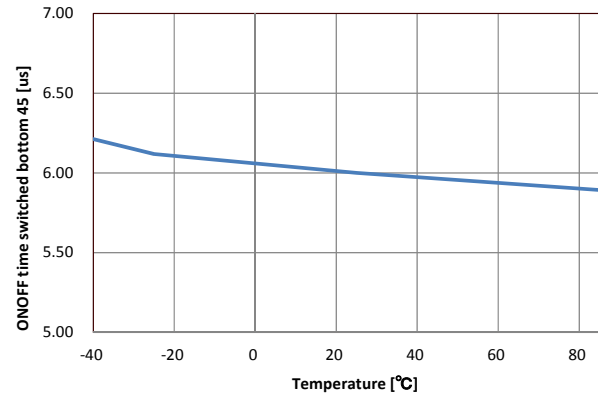


Figure 43 ONOFF time switched bottom 45 vs Temperature

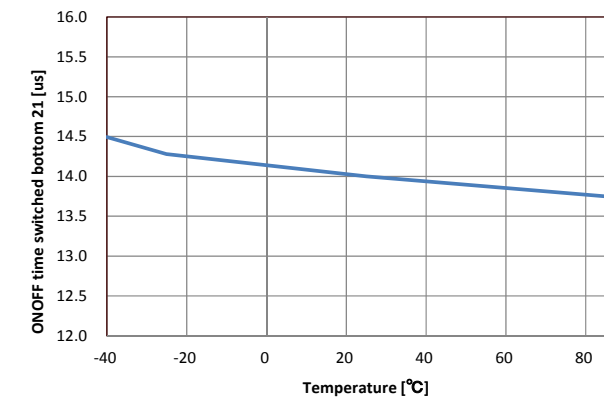


Figure 44 ONOFF time switched bottom 21 vs Temperature

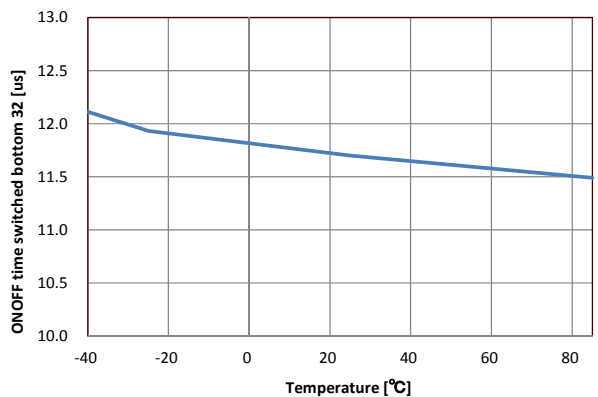


Figure 45 ONOFF time switched bottom 32 vs Temperature

●Reference Data (This is a reference data. For that, it is not guaranteed.)

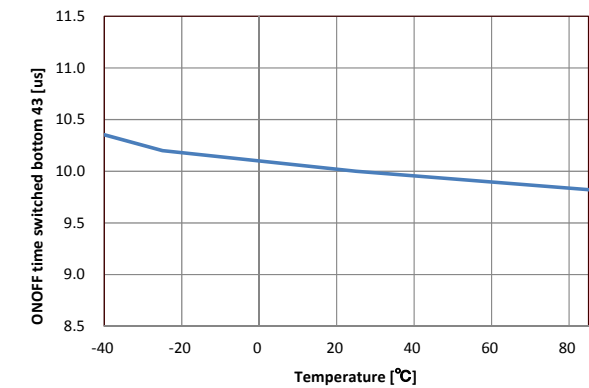


Figure 46 ONOFF time switched bottom 43 vs Temperature

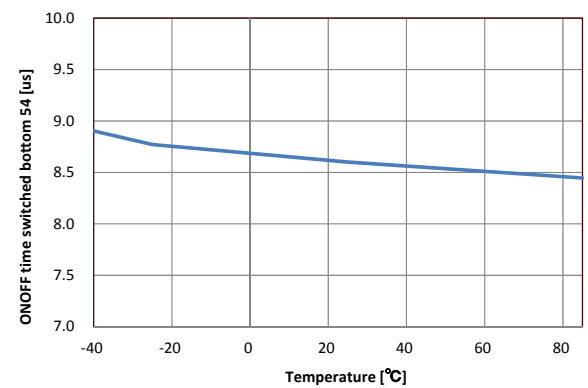


Figure 47 ONOFF time switched bottom 54 vs Temperature

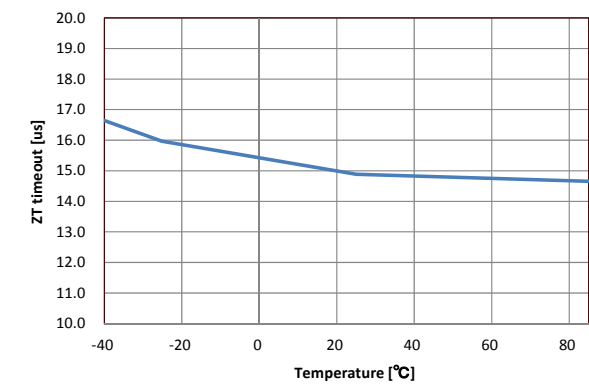


Figure 48 ZT timeout vs Temperature

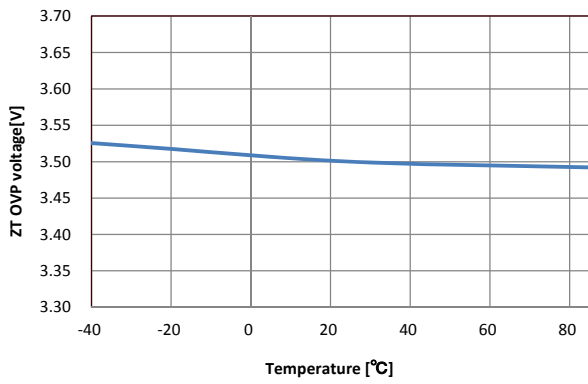


Figure 49 ZT OVP voltage vs Temperature

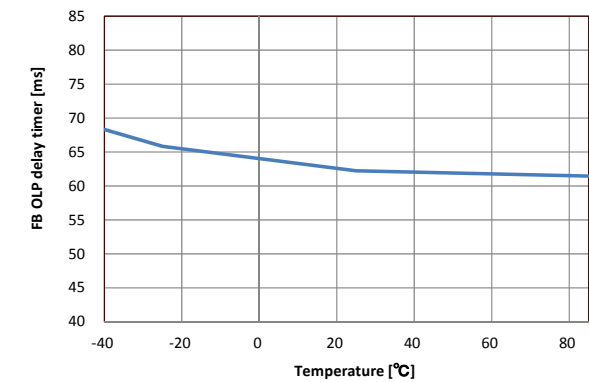


Figure 50 FBOLP delay timer vs Temperature

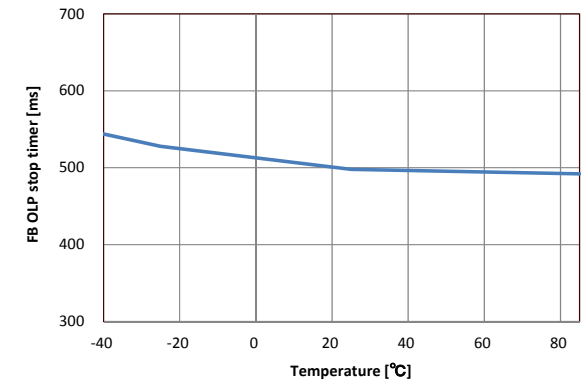


Figure 51 FBOLP stop timer vs Temperature

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Rush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

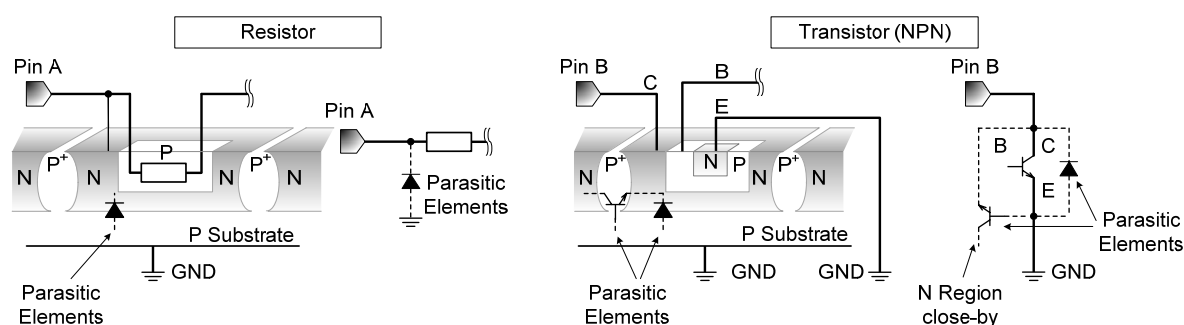


Figure 52. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Status of this document

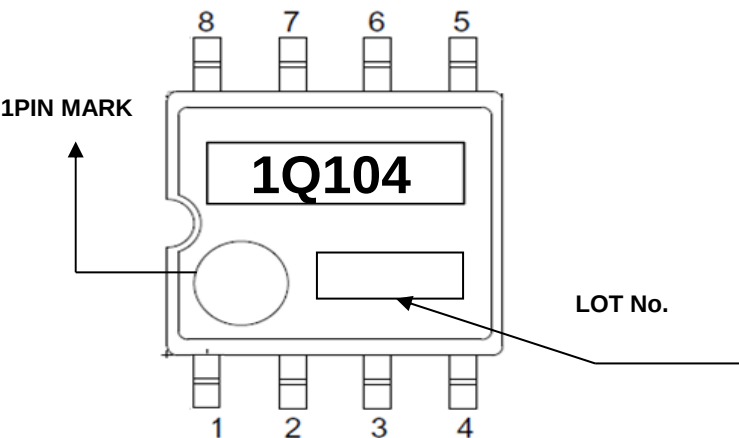
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority

Ordering Information

B M 1 Q 1 0 4 F J								-	E 2	
Part Number				Package FJ:SOP-J8					Packaging and forming specification E2: Embossed tape and reel	

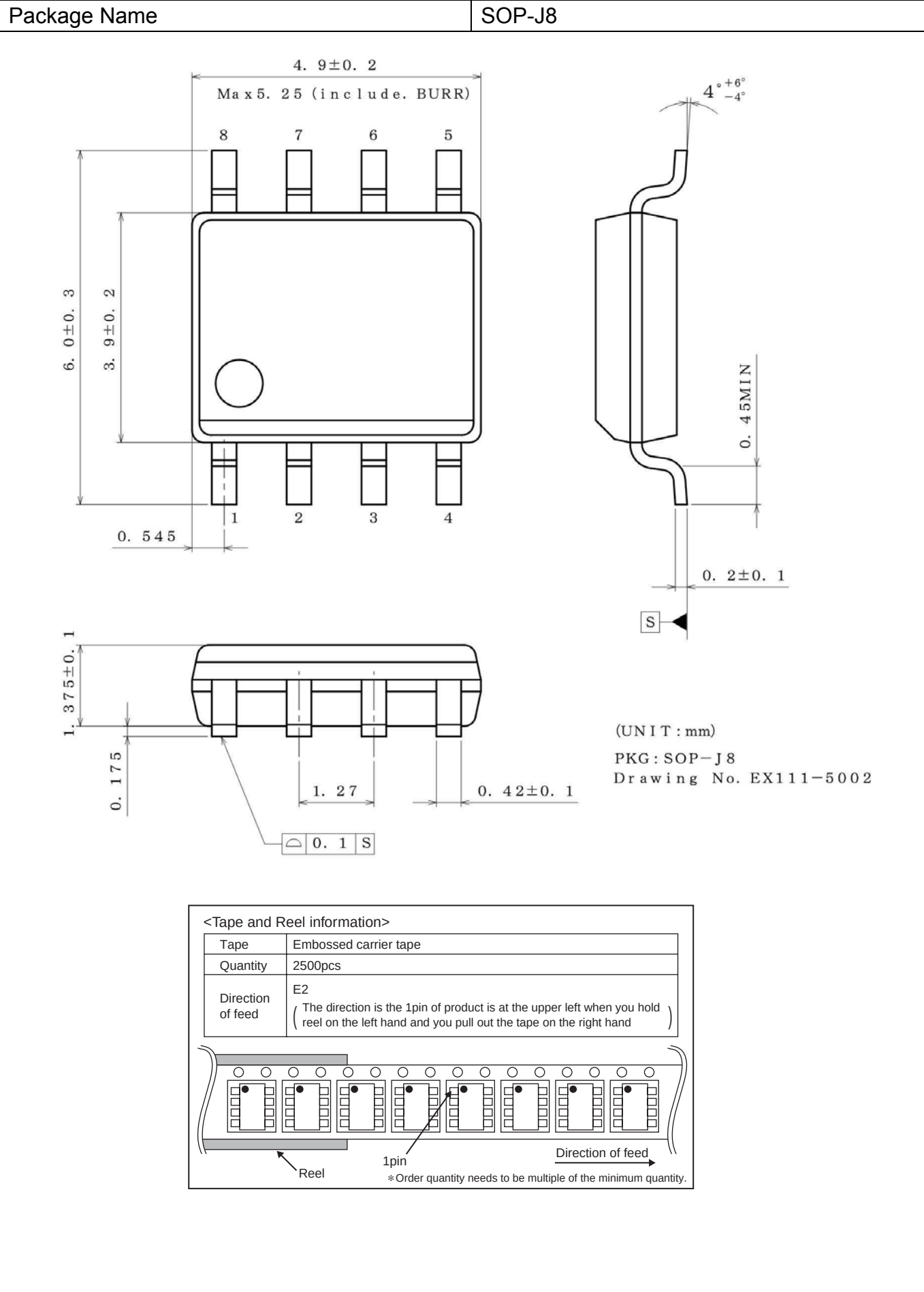
Marking Diagrams



Line-up

形名 (BM1Q10XFJ)
BM1Q104FJ

Physical Dimension, Tape and Reel Information



Revision History

Date	Revision	Changes
2014.3.31	001	New preparation
2014.5.20	001	New registration
2017.7.5	002	P-1, P-2 Change recommended VCC voltage range, P-9 And add note.
2017.7.13	002	Electrical Characteristics Add Icc(OFF),

Notice

Precaution on using ROHM Products

- Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

- ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
 - Installation of protection circuits or other protective devices to improve system safety
 - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
- Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc. prior to use, must be necessary:
 - Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
 - Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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General Precaution

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BM1Q104FJ - Web Page

Part Number	BM1Q104FJ
Package	SOP-J8
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes