# F2933 Datasheet

*High Reliability SP2T RF Switch* *50 MHz to 8000 MHz*

## General Description

The F2933 is a high reliability, low insertion loss, 50 Ω SP2T absorptive RF switch designed for a multitude of wireless and other RF applications. This device covers a broad frequency range from 50 MHz to 8000 MHz. In addition to providing low insertion loss, the F2933 also delivers high linearity and high isolation performance while providing a 50 Ω termination to the unused RF input port.

The F2933 uses a single positive supply voltage of 2.7 V to 5.5 V supporting three states using either 3.3 V or 1.8 V control logic.

## Competitive Advantage

The F2933 provides the following advantages

- ✓ Insertion Loss = 0.79 dB*
- ✓ RFX to RFC Isolation = 67 dB*
- ✓ IIP3 = +64 dBm*
- ✓ Active Port Operating Power Handling = 34 dBm
- ✓ Term Port Operating Power Handling = 27 dBm
- ✓ Extended Temperature Range = -40°C to 105°C

* 2 GHz

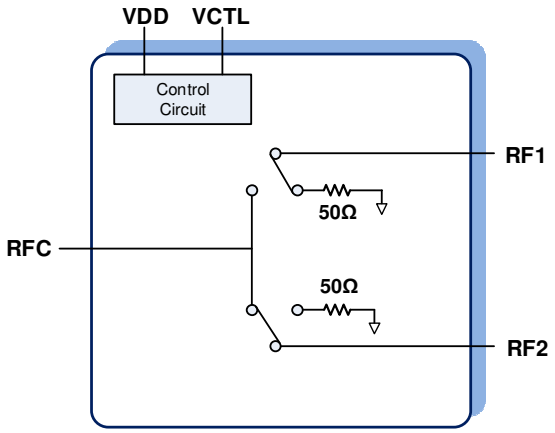
## Applications

- Base Station 2G, 3G, 4G
- Portable Wireless
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems, JTRS radios
- RFID handheld and portable readers
- Test / ATE Equipment

## Features

- High Isolation:
  - 70 dB @ 1 GHz
  - 67 dB @ 2 GHz
  - 65 dB @ 3 GHz
  - 66 dB @ 4 GHz
- High Linearity:
  - IIP2 of 111 dBm
  - IIP3 of 64 dBm @ 2 GHz
- Wide Single Positive Supply Voltage Range
- 3.3 V and 1.8 V compatible control logic
- Operating temperature -40 °C to +105 °C
- 4 mm x 4 mm 16 pin QFN package

## Functional Block Diagram




## Ordering Information

**F2933NBGP8**

Tape & Reel

Green

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## ABSOLUTE MAXIMUM RATINGS

| Parameter / Condition | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ to GND | | $V_{DD}$ | -0.3 | +6.0 | V |
| VCTL to GND | | $V_{logic}$ | -0.3 | Lower of 3.6, $V_{DD}$+0.3 | V |
| RF1, RF2, RFC to GND | | $V_{RF}$ | -0.3 | +0.3 | V |
| RF Input Power [1] | RF1 or RF2 as an input (Connected to RFC) | $P_{RF12}$ | | 36 | dBm |
| | RFC as an input (Connected to RF1 or RF2) | $P_{RFC}$ | | 36 | |
| | RF1 or RF2 as input (Terminated states) | $P_{RF12_TERM}$ | | 30 | |
| Maximum Junction Temperature | | $T_{Jmax}$ | | +140 | °C |
| Storage Temperature Range | | $T_{ST}$ | -65 | +150 | °C |
| Lead Temperature (soldering, 10s) | | $T_{LEAD}$ | | +260 | °C |
| ESD Voltage– HBM (Per JESD22-A114) | | $V_{ESDHBM}$ | | Class 2 (2000V) | |
| ESD Voltage – CDM (Per JESD22-C101) | | $V_{ESDCDM}$ | | Class C3 (1000V) | |

Note 1: $V_{DD}$ = 2.7 V to 5.5 V, 50 MHz ≤ $F_{RF}$ ≤ 8000 MHz, Tc= 105 ºC, $Z_S$ = $Z_L$ = 50 ohms.
Note 2: Each port.

*Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

| | |
|---|---|
| $\theta_{JA}$ (Junction – Ambient) | 60 °C/W |
| $\theta_{JC}$ (Junction – Case) The Case is defined as the exposed paddle | 3.9 °C/W |
| Moisture Sensitivity Rating (Per J-STD-020) | MSL1 |

## F2933 Recommended Operating Conditions

| Parameter | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | | 2.7 | | 5.5 | V |
| Operating Temp Range | $T_{CASE}$ | Exposed Paddle Temperature | | -40 | | +105 | $^{O}C$ |
| RF Frequency Range | $F_{RF}$ | | | 50 | | 8000 | MHz |
| RF Continuous Input CW Power (Non-Switched) [1] | $P_{RF}$ | RFC connected to RF1 or RF2[2] | $T_C$ = 85 ºC | | | 34 | dBm |
| | | | $T_C$ = 105 ºC | | | 34 | |
| | | RF1/ RF2 Input Terminated State[3,4] | $T_C$ = 85 ºC | | | 27 | |
| | | | $T_C$ = 105 ºC | | | 27 | |
| RF Continuous Input Power (RF Hot Switching CW) [1] | $P_{RFSW}$ | RFC Input, switching between RF1 and RF2 | $T_C$ = 85 ºC | | | 30 | dBm |
| | | | $T_C$ = 105 ºC | | | 30 | |
| | | RF1 or RF2 as input, switched between RFC and Term. | $T_C$ = 85 ºC | | | 27 | |
| | | | $T_C$ = 105 ºC | | | 27 | |
| RF1/2 Port Impedance | $Z_{RFx}$ | | | | 50 | | Ω |
| RFC Port Impedance | $Z_{RFC}$ | | | | 50 | | |

Note 1: Levels based on: $V_{DD}$ = 3.1 V to 5.5 V, 50 MHz ≤ $F_{RF}$ ≤ 8000 MHz, $Z_S$ = $Z_L$ = 50 ohms. See Figure 1 for power handling derating vs. RF frequency.
Note 2: Input could be: RFC, RF1, or RF2 (applied to only one input).
Note 3: Any RF1 / RF2 termination state. Power level specified is for each port.
Note 4: Power level specified is for each port.

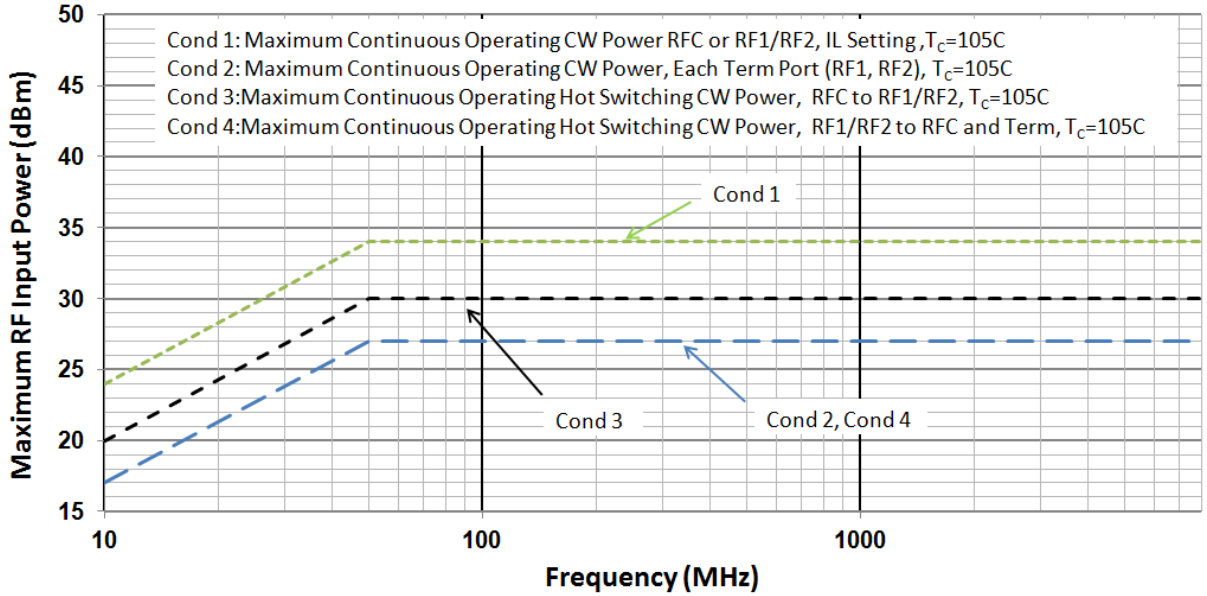



**Figure 1: Maximum RF Input Operating Power vs. RF Frequency**

## F2933 SPECIFICATION

Typical Application Circuit, $V_{DD}$ = 5.0 V, $T_C$ = +25 °C, $F_{RF}$ = 2000 MHz, Driven Port = RF1 or RF2, input power = 10 dBm, $Z_S$ = $Z_L$ = 50 ohms, PCB board trace and connector losses are de-embedded unless otherwise noted.

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Logic Input High Threshold | $V_{IH}$ | | ***1.1*** | | ***Lower of (3.6, $V_{DD}$)*** | V |
| Logic Input Low Threshold | $V_{IL}$ | | -0.3 | | ***0.6*** | V |
| Logic Current | $I_{IH}$, $I_{IL}$ | For each control pin | ***-1*** | | ***+1*** | µA |
| DC Current | $I_{DD}$ | $V_{DD}$ =3.3 V | | 200 | ***260*** [1] | µA |
| | | $V_{DD}$ =5.0 V | | 260 | ***325*** | |
| Insertion Loss RFC to RF1 / RF2 | IL | 50 MHz | | 0.68 | | dB |
| | | 1 GHz | | 0.73 | | |
| | | 2 GHz | | 0.79 | ***1.1*** | |
| | | 3 GHz | | 0.82 | | |
| | | 4 GHz | | 0.93 | | |
| | | 6 GHz | | 1.06 | | |
| | | 8 GHz | | 1.6 | | |
| Isolation RFC to RF1 / RF2 | ISOC | 50 MHz | 77[2] | 79 | | dB |
| | | 1 GHz | 68 | 70 | | |
| | | 2 GHz | 63 | 67 | | |
| | | 3 GHz | 62 | 65 | | |
| | | 4 GHz | 60 | 66 | | |
| | | 6 GHz | 53 | 63 | | |
| | | 8 GHz | | 45 | | |
| Isolation RF1 to RF2 | ISOX | 50 MHz | | 86 | | dB |
| | | 1 GHz | | 64 | | |
| | | 2 GHz | | 58 | | |
| | | 3 GHz | | 54 | | |
| | | 4 GHz | | 51 | | |
| | | 6 GHz | | 45 | | |
| | | 8 GHz | | 37 | | |
| Return Loss RFC, RF1, RF2 | $RF_{RL}$ | 50 MHz | | 25 | | dB |
| | | 1 GHz | | 25 | | |
| | | 2 GHz | | 23 | | |
| | | 3 GHz | | 24 | | |
| | | 4 GHz | | 20 | | |
| | | 6 GHz | | 18 | | |
| | | 8 GHz | | 14 | | |
| Return Loss RF1, RF2 Terminated | $RF_{RLTERM}$ | 50 MHz | | 40 | | dB |
| | | 1 GHz | | 31 | | |
| | | 2 GHz | | 35 | | |
| | | 3 GHz | | 23 | | |
| | | 4 GHz | | 17 | | |
| | | 6 GHz | | 19 | | |
| | | 8 GHz | | 22 | | |

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.

## F2933 SPECIFICATION (CONT.)

Typical Application Circuit, $V_{DD}$ = 5.0 V, $T_C$ = +25 °C, $F_{RF}$ = 2000 MHz, Driven Port = RF1 or RF2, input power = 10 dBm, $Z_S$ = $Z_L$ = 50 ohms, PCB board trace and connector losses are de-embedded unless otherwise noted.

| Parameter | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Input 1dB Compression[3] | $ICP_{1dB}$ | 50 MHz | | | 33.2 | | dBm |
| | | 1 GHz | | | 35.5 | | |
| | | 2 GHz | | | 36.5 | | |
| | | 3 GHz | | | 36.1 | | |
| | | 4 GHz | | | 35.3 | | |
| Input 0.1dB Compression[3] | $ICP_{0.1dB}$ | $V_{DD}$ = 5.0 V | 50 MHz | | 30.4 | | dBm |
| | | | 2 GHz | | 32.3 | | |
| | | | 3 GHz | | 32.6 | | |
| | | | 4 GHz | | 32.2 | | |
| | | $V_{DD}$ = 3.1 V | 50 MHz | | 30.1 | | |
| | | | 2 GHz | | 32.1 | | |
| | | | 3 GHz | | 32.6 | | |
| | | | 4 GHz | | 32.1 | | |
| Input IP2 | IIP2 | $F_{RF1}$ = 2000 MHz, $F_{RF2}$ = 1990 MHz<br>$RF_{IN}$ = RF1 or RF2<br>$P_{IN}$ = +20 dBm / tone<br>$F_{IP2}$ =$F_{RF1}$ + $F_{RF2}$ | | | 111 | | dBm |
| Input IP3 | IIP3 | RF Input = RF1 or RF2<br>$P_{IN}$ = +15 dBm/tone<br>Δ F = 1 MHz | 50 MHz | | 58 | | dBm |
| | | | 1 GHz | | 64 | | |
| | | | 2 GHz | | 64 | | |
| | | | 2.5 GHz | | 63.4 | | |
| | | | 4 GHz | | 63.6 | | |
| Non-RF Driven Spurious[4] | | At any RF port when externally terminated into 50 Ω | | | -114 | | dBm |
| Switching Time[5] | $T_{SW}$ | 50% control to 90% RF | | | 210 | | ns |
| | | 50% control to 10% RF | | | 115 | | |
| | | 50% control to RF settled to within +/- 0.1 dB of I.L. value | | | 225 | | |
| Maximum Switching Rate[6] | $SW_{RATE}$ | | | | 25 | | kHz |
| Maximum Video Feed-through on RF Ports | $VID_{FT}$ | 5 MHz to 1000 MHz<br>Measured with 20 ns risetime,<br>0 to 3.3 V control pulse | | | 12 | | $mV_{pp}$ |

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: The input 1 dB compression point is a linearity figure of merit. Refer to the Recommended Operating Conditions section for the specified maximum operating power levels.
Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 5.2 MHz.
Note 5: $F_{RF}$ = 1 GHz.
Note 6: Minimum time required between switching of states = 1/ (Maximum Switching Rate).

## Control Mode

### Table 1 - Switch Control Truth Table

| VCTL | RFC to RF1 | RFC to RF2 |
|---|---|---|
| 0 | ON | OFF |
| 1 | OFF | ON |

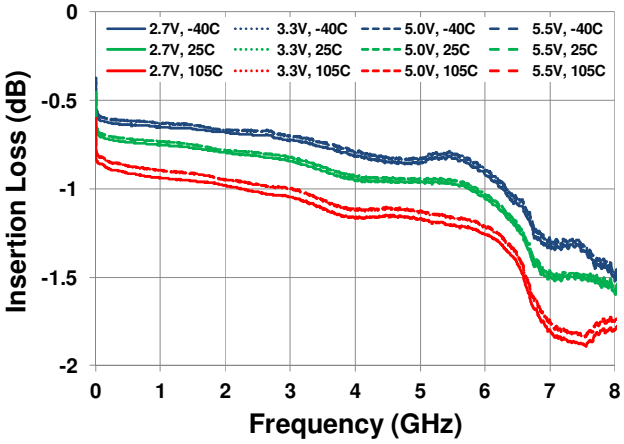
## TYPICAL OPERATING CONDITIONS (TOC)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

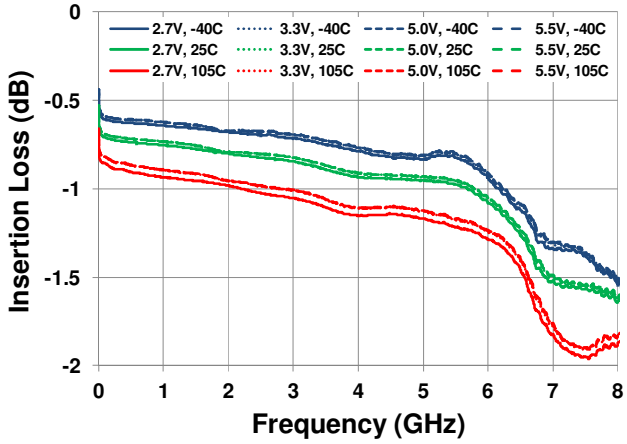
- **$V_{DD}$= 3.3 V**
- **$T_C$ = +25 °C ($T_C$ = Temperature of Exposed Paddle)**
- **$F_{RF}$ = 2000 MHz**
- **$Z_S$ = $Z_L$ = 50 Ω**
- **$P_{IN}$ = +10 dBm for all small signal tests.**
- **$P_{IN}$ = +15 dBm/tone applied to RF1 or RF2 port for two tone linearity tests.**
- **Two tone frequency spacing = 1 MHz.**
- **RF1 or RF2 is the driven RF port and RFC is the output port.**
- **All unused RF ports terminated into 50 ohms.**
- **For Insertion Loss and Isolation plots, RF trace and connector losses are de-embedded (see EVKIT Board and Connector loss plot).**
- **Plots for Isolation and Insertion Loss over temperature and voltage are for a typical path. For performance of a specific path, refer to the online S-Parameter file.**

## TYPICAL OPERATING CONDITIONS (- 1 -)

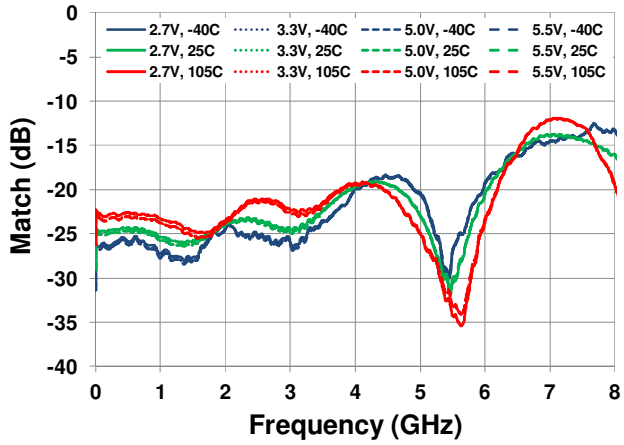
### RF1 to RFC Insertion Loss



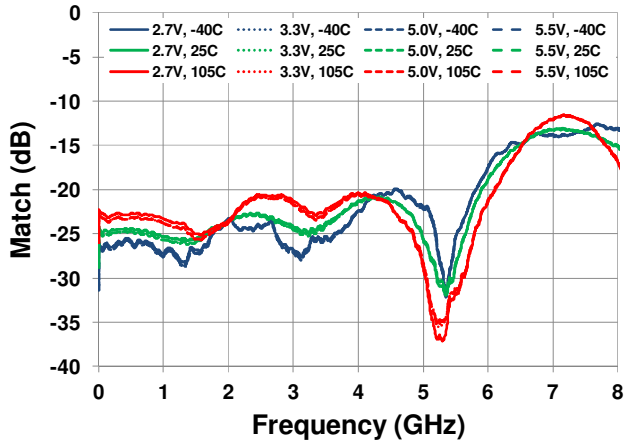

### RF2 to RFC Insertion Loss



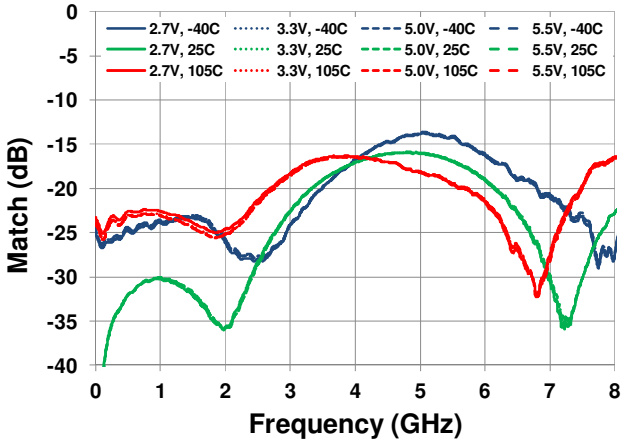

### RF1 Port Match [On State]



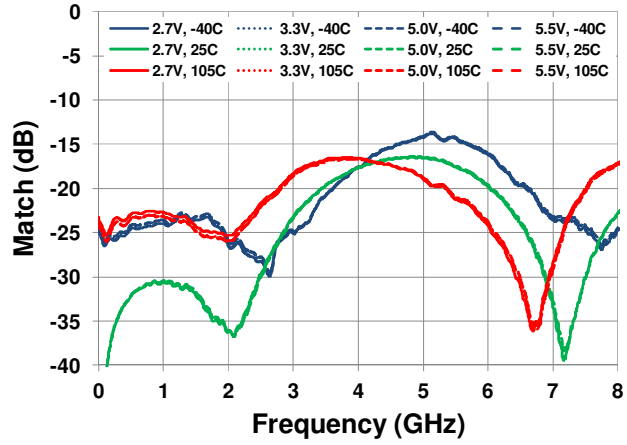

### RF2 Port Match [On State]




### RF1 Port Match [Terminated State]

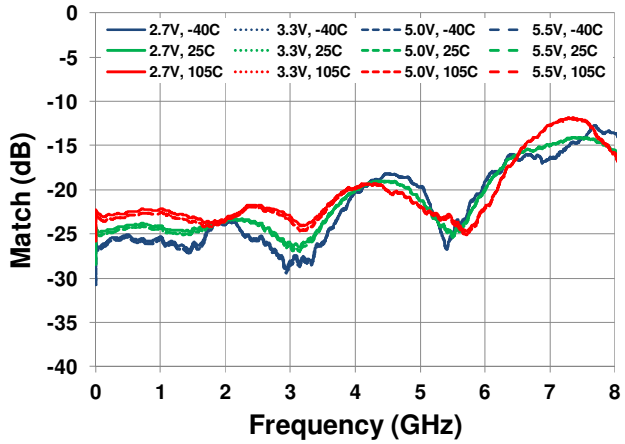



### RF2 Port Match [Terminated State]

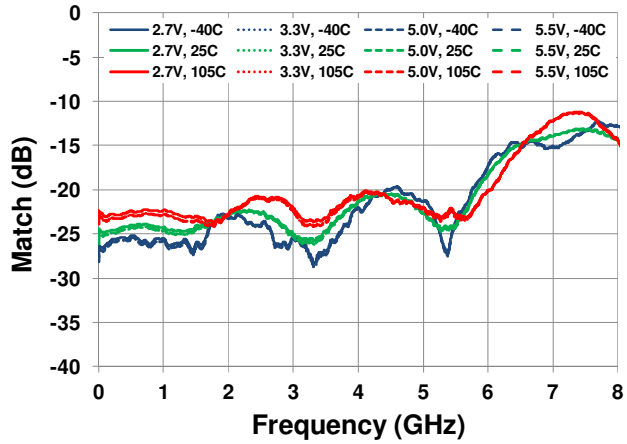


## TYPICAL OPERATING CONDITIONS (- 2 -)

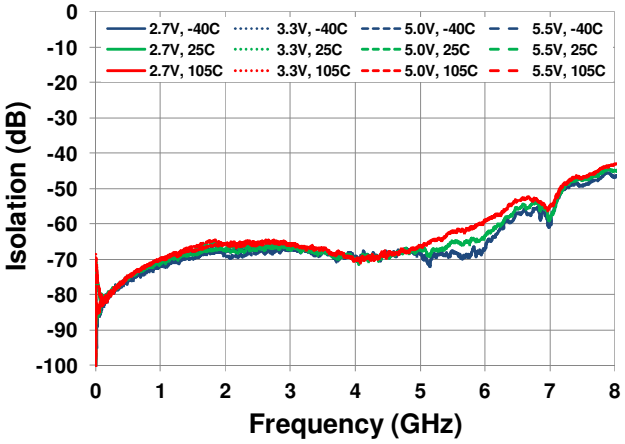
### RFC Port Match [RF1 On State]



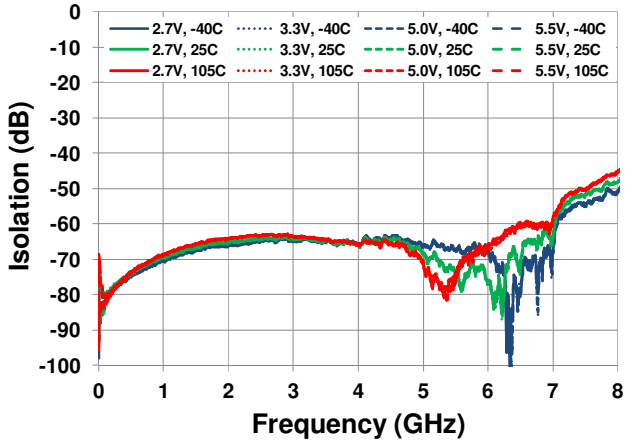

### RFC Port Match [RF2 On State]



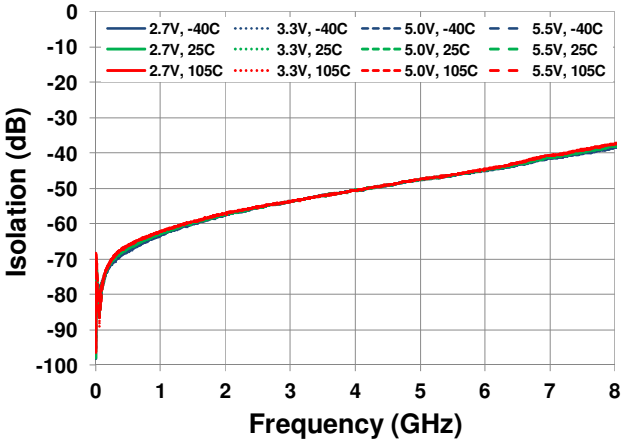

### RF1 to RFC Isolation [RF2 On State]



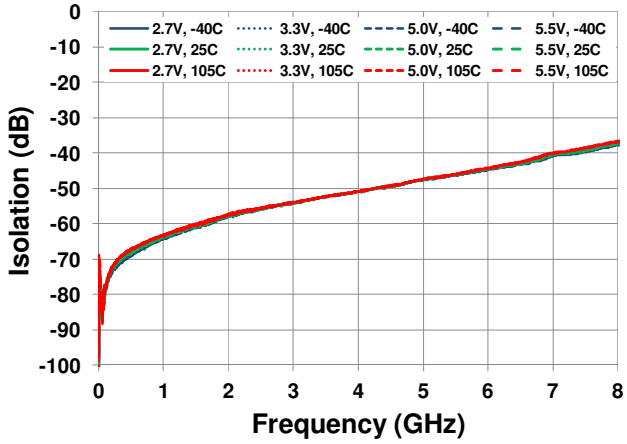

### RF2 to RFC Isolation [RF1 On State]




### RF1 to RF2 Isolation [RF1 On State]

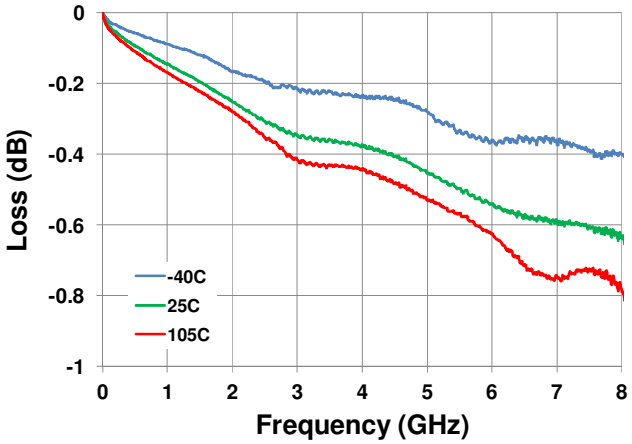



### RF2 to RF1 Isolation [RF2 On State]

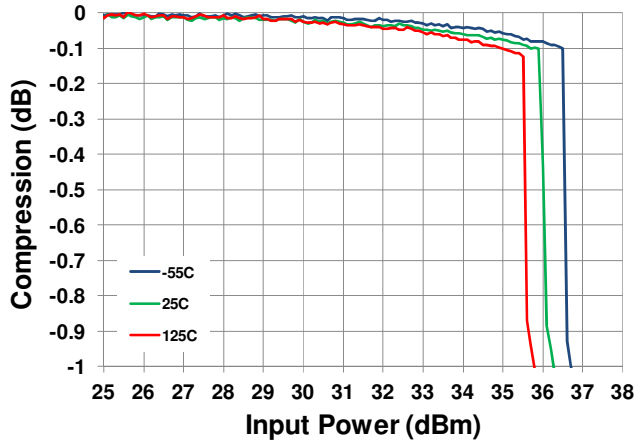


## TYPICAL OPERATING CONDITIONS (- 3 -)

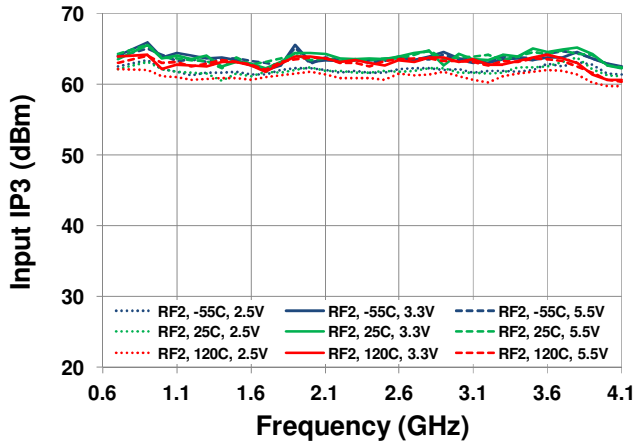
**EVKIT PCB and Connector Thru Loss**



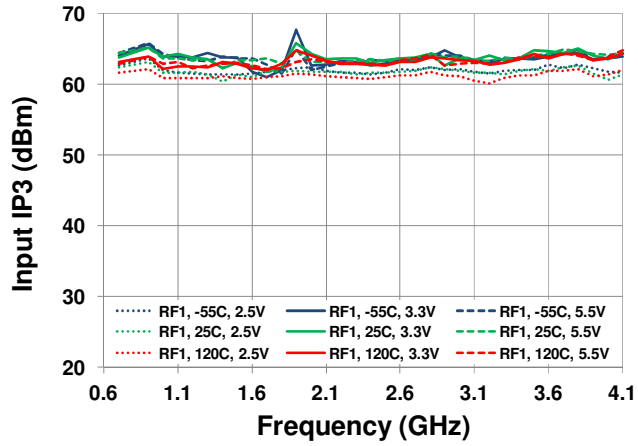

**Input P1dB [1GHz] [$T_C$ operating = -40C to 105C]**




**Input IP3 RF1 Port [$T_C$ operating = -40C to 105C]**



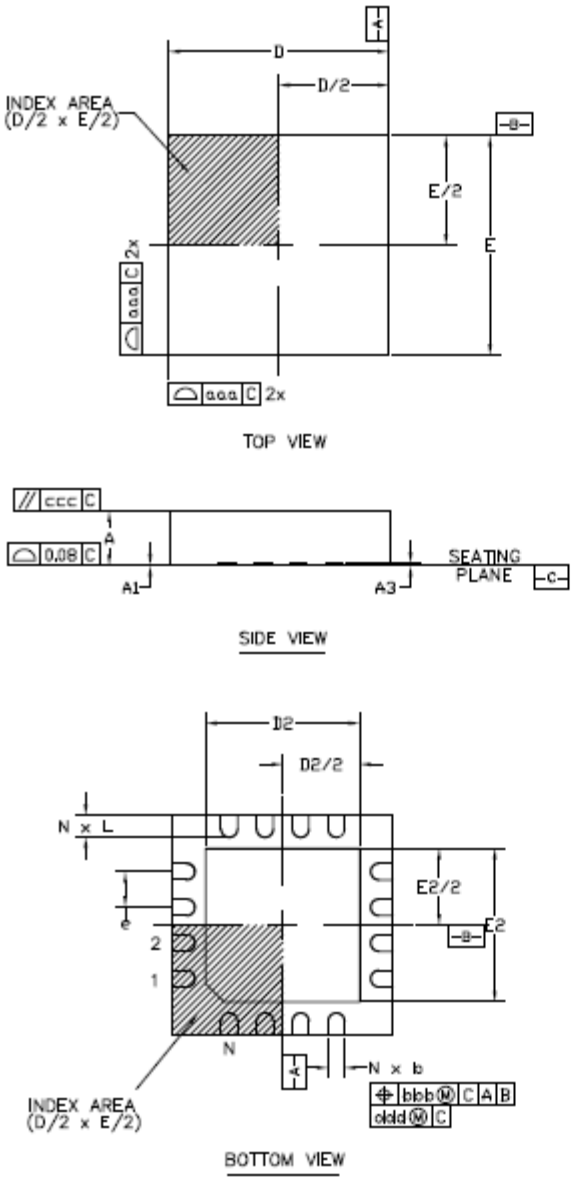

**Input IP3 RF2 Port [$T_C$ operating = -40C to 105C]**



## PACKAGE DRAWING

(4 mm x 4 mm 16-pin QFN), NBG16

**Note: The F2933 uses EPAD Option P2 and Lead Option Z2**




| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.02 ref | | |
| b | 0.25 | 0.30 | 0.35 |
| D | 4.0 | | |
| E | 4.0 | | |
| e | 0.65 | | |
| N | 16 | | |
| ND | 4 | | |
| NE | 4 | | |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |

EPAD OPTION:

| | P2 | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| D2 | 2.55 | 2.70 | 2.80 |
| E2 | 2.55 | 2.70 | 2.80 |

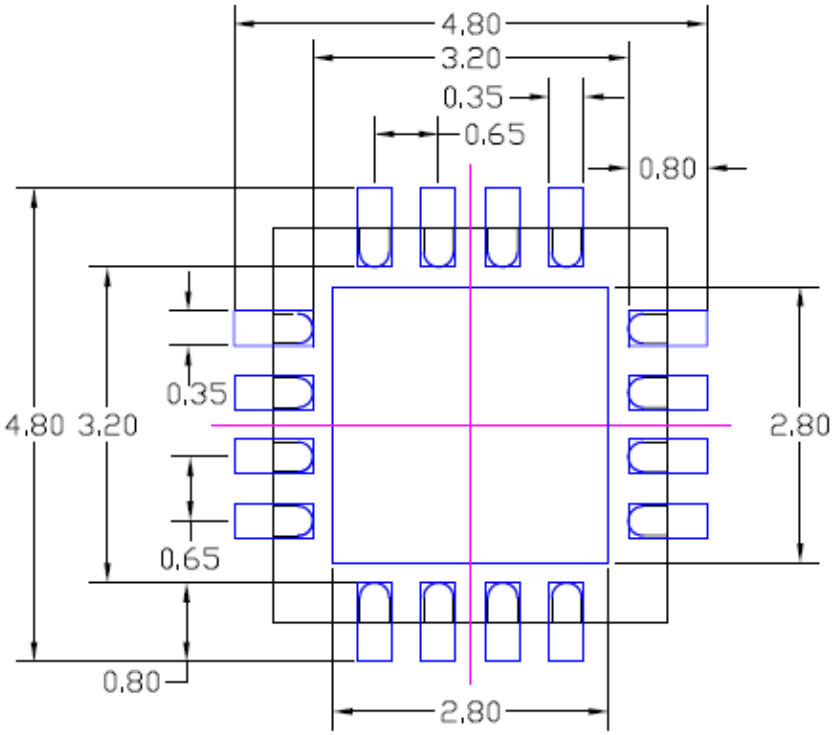
LEAD OPTION:

| | Z2 | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| L | 0.30 | 0.40 | 0.50 |

NOTES:

1. All dimensions in mm.
2. The dimension and tolerancing meet ASME Y–14.5M–1994.

## LAND PATTERN DIMENSION



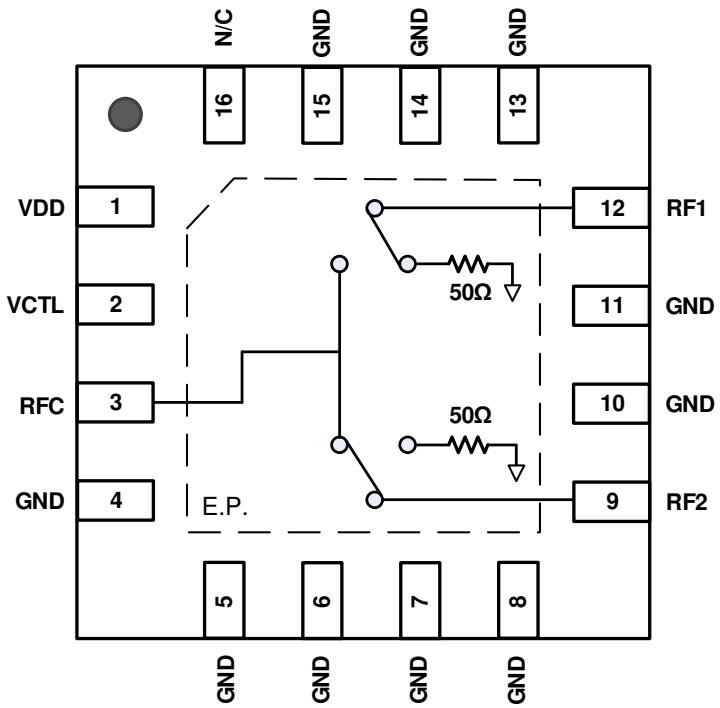

P2/Z2 OPTION

RECOMMENDED LAND PATTERN DIMENSION

NOTE:

1) ALL dimensions are in mm, Angles in degrees.
2) Top down view, as view on PCB.
3) Land Pattern in BLUE.NSMD Land Pattern Assumed
4) Land Pattern Recommendation as per IPC-7351B generic requirement for surface mount design and Land Pattern.

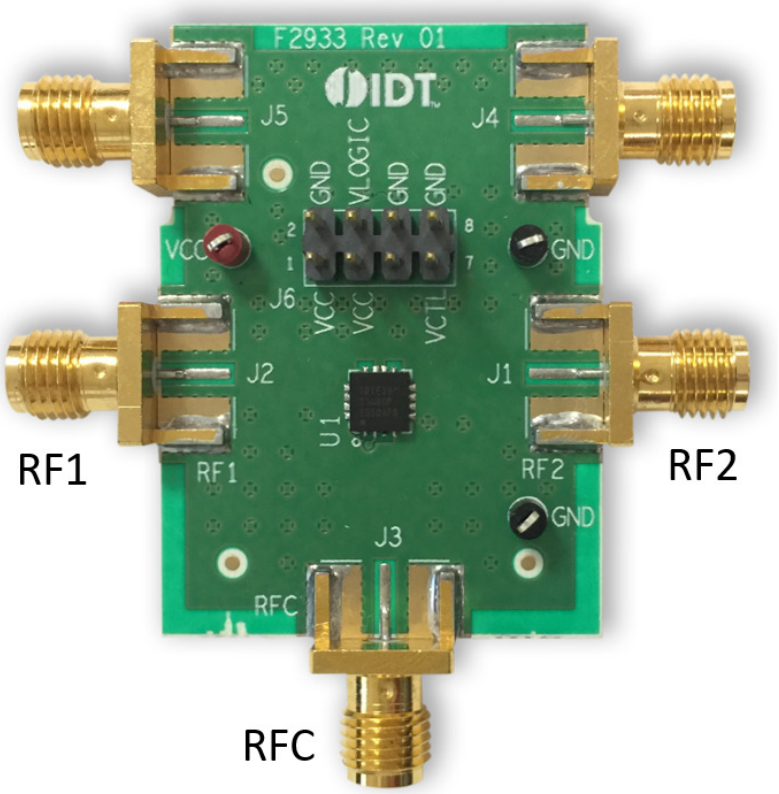
## PIN DIAGRAM



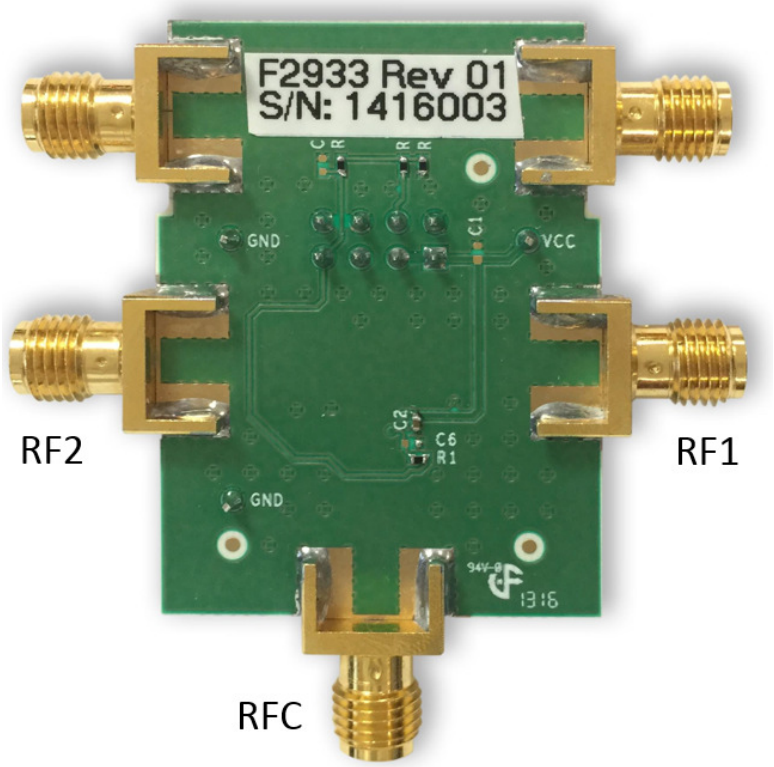

## PIN DESCRIPTION

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | VDD | Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin. |
| 2 | VCTL | Logic control pin. See Table 1. |
| 3 | RFC | RF Common Port. Matched to 50 Ω when one of the 2 RF ports is selected. If this pin is not 0 V DC, then an external coupling capacitor must be used. |
| 4, 5, 6, 7, 8, 10, 11, 13, 14, 15, 16 | GND | Ground. Also, internally connected to the ground paddle. Ground this pin as close to the device as possible. |
| 9 | RF2 | RF2 Port. Matched to 50 Ω. If this pin is not 0 V DC, then an external coupling capacitor must be used. |
| 12 | RF1 | RF1 Port. Matched to 50 Ω. If this pin is not 0 V DC, then an external coupling capacitor must be used. |
| 17 | — EP | Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device and into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance. |

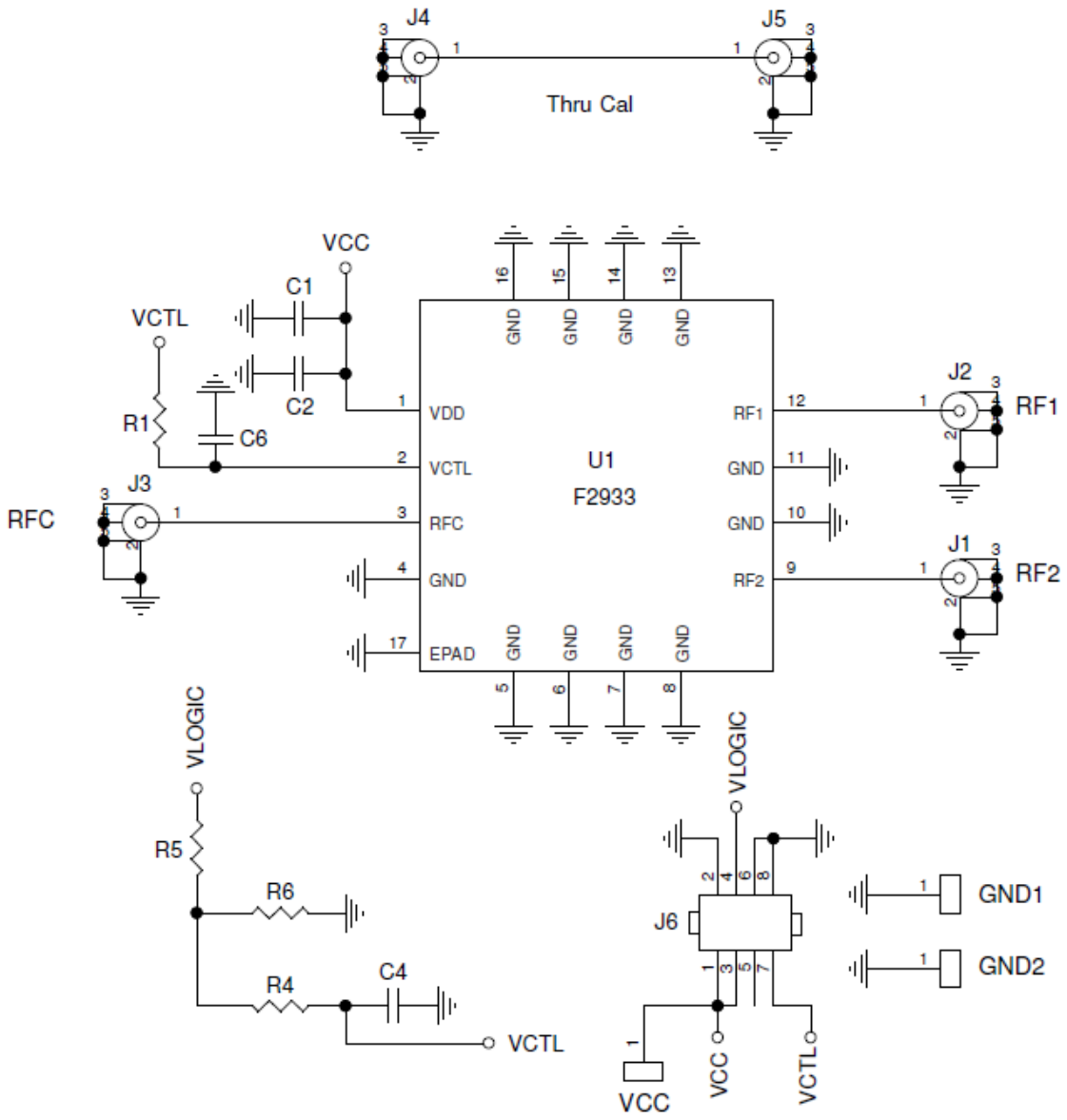
## EvKit Picture (Top)




## EvKit Picture (Bottom)



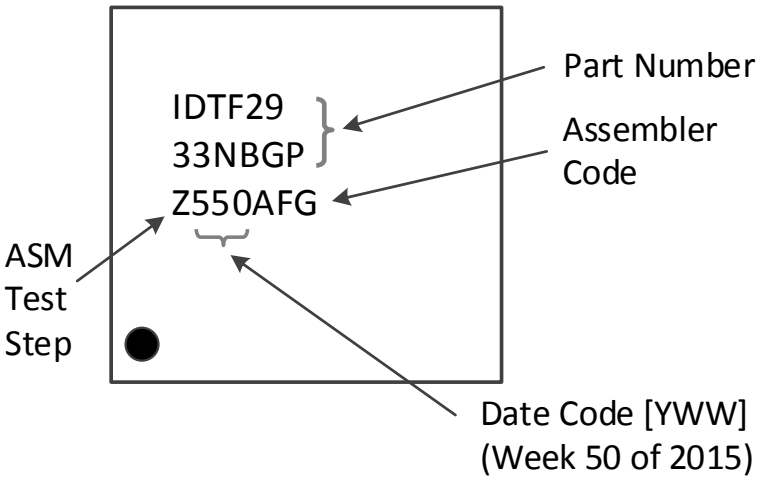
## EVKIT / APPLICATIONS CIRCUIT



## EVKIT BOM

| Part Reference | QTY | DESCRIPTION | Mfr. Part # | Mfr. |
|---|---|---|---|---|
| C1 | 0 | Not Installed (0402) | | |
| C2 | 1 | 0.1 µF ±10%, 16V, X7R, Ceramic Capacitor (0402) | GRM155R71C104K | Murata |
| C4, C6 | 0 | Not Installed (0402) | | |
| R1 | 1 | 100 Ω ±1%, 1/10W, Resistor (0402) | ERJ-2RKF1000X | Panasonic |
| R4 | 1 | 100k Ω ±1%, 1/10W, Resistor (0402) | ERJ-2RKF1003X | Panasonic |
| R5 | 1 | 15k Ω ±1%, 1/10W, Resistor (0402) | ERJ-2RKF1502X | Panasonic |
| R6 | 1 | 18k Ω ±1%, 1/10W, Resistor (0402) | ERJ-2RKF1802X | Panasonic |
| J1 – J5 | 5 | SMA Edge Launch (0.375 inch pitch ground tabs) | 142-0701-851 | Emerson Johnson |
| J6 | 1 | CONN HEADER VERT 4x2 POS GOLD | 67997-108HLF | FCI |
| U1 | 1 | SP2T Switch 4 mm x 4 mm QFN16-EP | F2933NBGP | IDT |
| VCC | 1 | Test Point Loop (Red) | 5000 | Keystone Electronics |
| GND1, GND2 | 2 | Test Point Loop (Black) | 5001 | Keystone Electronics |
| | 1 | Printed Circuit Board | F2933 EVKIT REV 1 | IDT |

## TOP MARKINGS



## APPLICATIONS INFORMATION

### Default Start-up

There is no internal pull-up or pull-down resistor on the VCTL pin.

### Logic Control

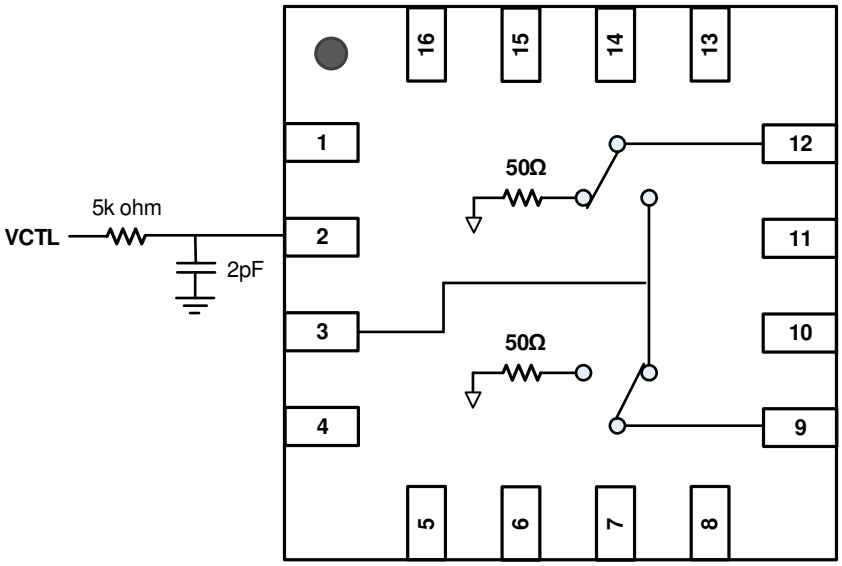
The VCTL pin is used to set the state of the SP2T switch (see Table 1).

### Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1 V / 20 µs. In addition, all control pins should remain at 0 V (+/-0.3 V) while the supply voltage ramps or while it returns to zero.

### Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit is recommended at the input of control pin 2 (VCTL). See figure below.



# EVKIT OPERATION

## External Supply Setup

Set up a VCC power supply in the voltage range of 2.7 V to 5.5 V and disable the power supply output.

## Logic Control Setup

### Using the EVKIT to manually set the control logic:

On connector J6 connect a 2-pin shunt from pin 3 (VCC) to pin 4 (VLOGIC). This connection provides the VCC voltage supply to the Eval Board logic control pull up network. Resistors R5 and R6 form a voltage divider to set the Vhigh level over the 2.7 V to 5.5 V VCC range for manual logic control.

Connector J6 has one logic input pin: VCTL (pin 7). See Table 1 for Logic Truth Table. With the pullup network enabled (as noted above) this pin can be left open to provide a logic high through pull up resistor R4. To set a logic low for VCTL connect a 2-pin shunt on J6 from pin 7 (VCTL) to pin 8 (GND).

Note that when using the on board R5 / R6 voltage divider the current draw from the VCC supply will be higher by approximately VCC / 33k Ω.

### Using external control logic:

Pins 3, 4, 5, 6, and 8 of J6 should have no external connection. External logic control is applied to J6 pin 7 (VCTL). See Table 1 for Logic Truth Table.

## Turn on Procedure

Setup the supplies and Eval Board as noted in the **External Supply Setup** and **Logic Control Setup** sections above.

Connect the preset disabled VCC power supply to the red VCC loop and ground to GND1 or GND2.

Enable the VCC supply.

Set the desired logic setting using J6 pin 7 (VCTL) to achieve the desired Table 1 setting. Note that external control logic should not be applied without VCC being present.

## Turn off Procedure

If using external control logic for VCTL then set it to a logic low.

Disable the VCC supply.

## Revision History Sheet

| Rev | Date | Page | Description of Change |
|---|---|---|---|
| O | 2016-May-04 | | Initial Release |

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