SiI1292 MHL Bridge and HDMI Monitor Receiver

Data Brief

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General Description

The SiI1292 MHL Bridge and HDMI Monitor Receiver facilitates the design of low-pin count, low-power mobile-to-standard HDMI®-interoperable applications. The Silicon Image Mobile High-definition Link (MHL™) technology carries formatted video and audio from compatible transmitters, using only 3 signal lines, power, and ground (5 pins total) compared to the 19 pins required for the standard High Definition Multimedia Interface (HDMI).

As an MHL bridge, the SiI1292 device supports a single MHL input to provide MHL capability in computer or multimedia display devices.

Additionally, the SiI1292 receiver can be configured to support HDMI input and supporting all HDMI compliant transmitters in the market at resolutions up to 1080p60 12-bit color.

The HDMI core of the SiI1292 device uses the latest generation Transition Minimized Differential Signaling (TMDS™) core technology. With this solution, HD camcorders, digital still cameras, and personal mobile devices can connect to a large installed base of HDMI TVs.

Features

- The MHL input function of the bridge receives data over a single differential pair instead of four pairs
- A single-wire control bus supports all sideband signaling for DDC, Remote Control, and Hot Plug Detect (HPD)
- The bridge converts data received in the MHL format to standard HDMI, and supports all resolutions ranging from 25 MHz to 75 MHz
- HDMI receiver mode supports all resolutions between 25–225 MHz including 1080p60 12-bit Deep Color

The combined transmitter and bridge implements a total A/V interface solution with the following features:

- I^2C interface for configuration by local microcontroller
- Built-in adaptive equalizer for long cable support on HDMI
- HDMI and DVI 1.0 transmitter compatibility
- Low power 1.2 V core
- 40-pin QFN, 6 mm x 6 mm body size
- Extended commercial temperature range (–20 C to +85 °C).

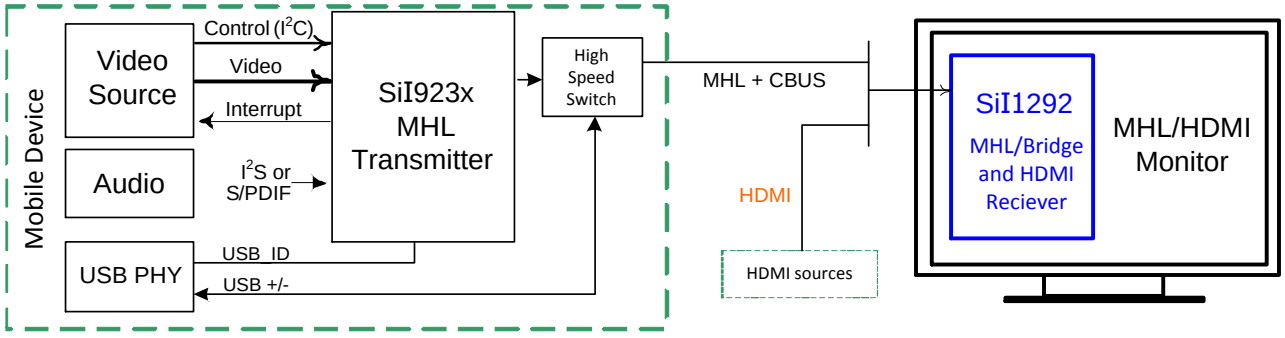
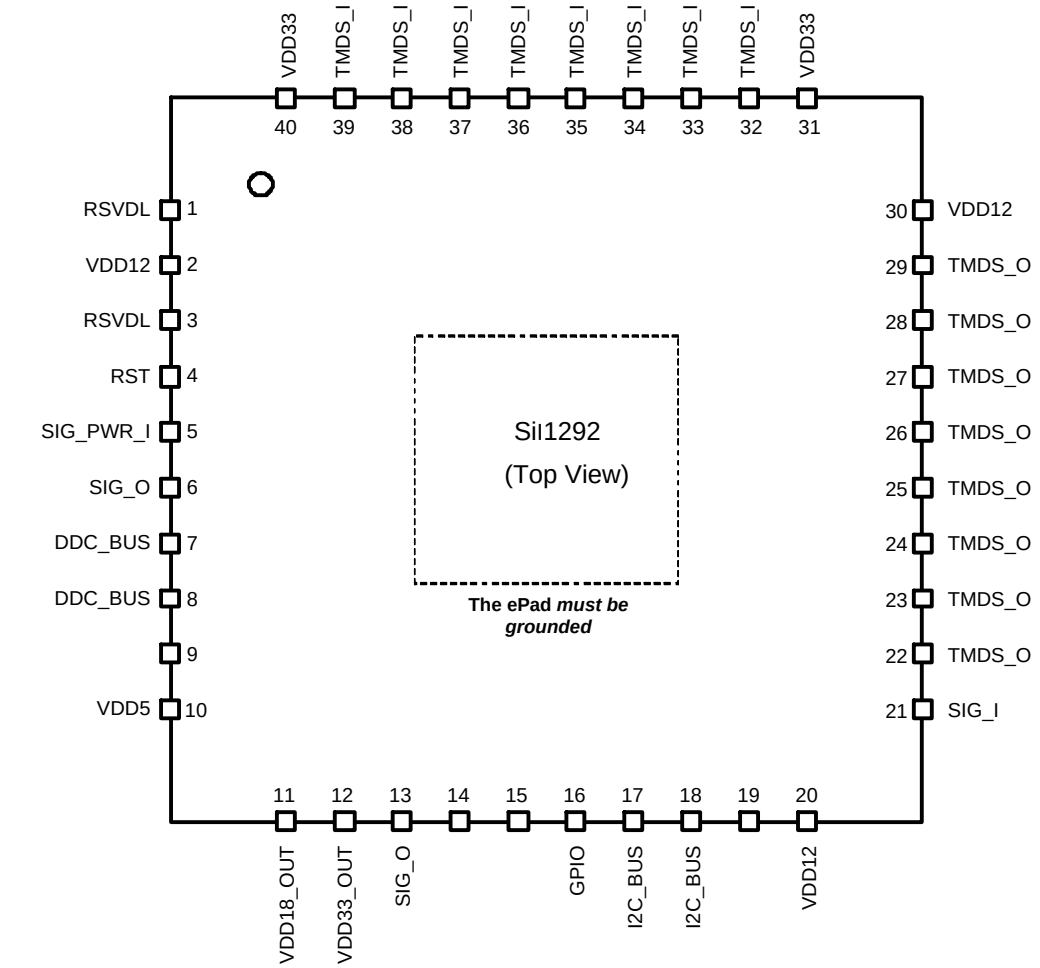


Figure 1. Typical Application as an MHL/HDMI Monitor Input Switch

Pin Mapping

Figure 2 shows the pin assignments of theSiI1292 receiver. Pin names are generalized by type for this document. The list below the diagram describes the purpose of each type. The package is 40-pin QFN with ePad.



TMDS_I -- TMDS Input
TMDS_O -- TMDS Output
DDC_BUS -- DDC Bus, OD, 5 V Tolerant
SIG_PWR_I -- Internal Power Supply Control Signal
SIG_I/O -- Signal Input/Output, 5 V Tolerant
RST -- Active LOW reset

GPIO -- GPIO Pin, 5 V tolerant
I2C_BUS -- I^2C Bus
CTRL_SIG_I/O -- Control Signal I/O
SIG_I -- Signal Input, 5 V tolerant
SIG_O -- Signal Output, 5 V tolerant, open drain
RSVDL -- Reserved pin, tie LOW

Figure 2. Pin Mapping

Packaging

ePad Requirements

The SiI1292 chip is packaged in a 40-pin QFN package with an Exposed Pad™ (ePad™), used both for electrical connectivity and for improved thermal transfer characteristics. The ePad dimensions are shown on the following page. Soldering of the ePad is ***required*** to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground.

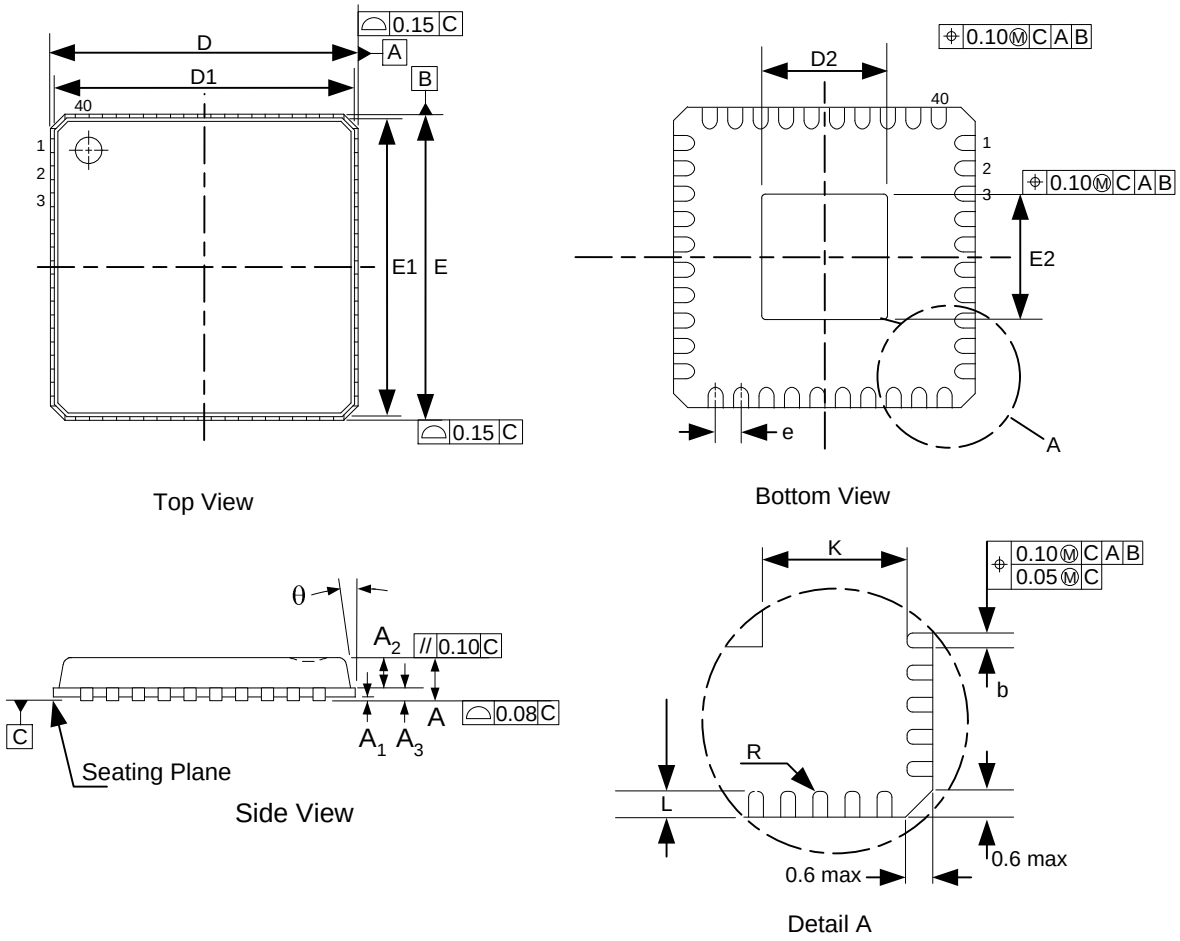
Note: The ePad must be soldered to the PCB ground. Provide a landing area on the PCB with dimensions and location corresponding to the ePad within the footprint of the package. The size of this landing area can be larger than the ePad on the package but should be at least the same as the maximum size of exposed pad of the package (2.50 mm x 2.50 mm). If any circuit traces are within the area of the maximum size of the ePad, the trace may short to the pad if the package has a pad with the maximum dimensions.

The thermal land area on the PCB can use thermal vias to improve heat removal from the package. These thermal vias can double as ground connections, attaching internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, Silicon Image recommends the diameter of vias set within 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel be plated with 1-ounce copper to plug the via. This is desirable to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off is also a consideration. For a nominal stand-off of approximately 0.1 mm (see dimension A1), the stencil thickness of 5 mils to 8 mils provide a good solder joint between the ePad and the thermal land.

Package Dimensions

Package drawings are not to scale.



JEDEC Package Code MO-220

Item	Description	Min	Typ	Max
A	Thickness	0.80	0.85	0.90
A_1	Stand-off	0.00	0.02	0.05
A_2	Body thickness	0.60	0.65	0.70
A_3	Base thickness		0.20 REF	
D	Body size	5.90	6.00	6.10
E	Body size	5.90	6.00	6.10
D_1	Footprint		5.75 BSC	
E_1	Footprint		5.75 BSC	

Item	Description	Min	Typ	Max
D_2	ePad size	2.35	2.50	2.65
E_2	ePad size	2.35	2.50	2.65
b	Plated lead width	0.18	0.23	0.30
e	Lead pitch		0.50 BSC	
L	Lead foot length	0.30	0.40	0.50
θ	Mold angle	0°	—	12°
R	Lead tip radius	0.09	—	—
K	Lead to ePad clearance	0.20	—	—

Figure 3. 40-pin QFN Package Diagram

Marking Specification

Marking drawing is not to scale.

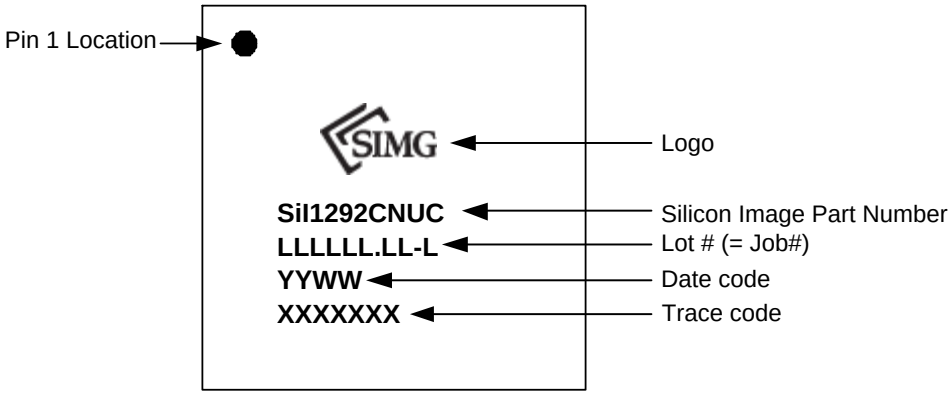


Figure 4. Marking Diagram

Ordering Information

Production Device Type	Device Number
Universal	SiI1292CNUC

The universal package can be used in lead-free and ordinary process lines.

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1060 E. Arques Avenue
Sunnyvale, CA 94085
T 408.616.4000 F 408.830.9530
www.siliconimage.com