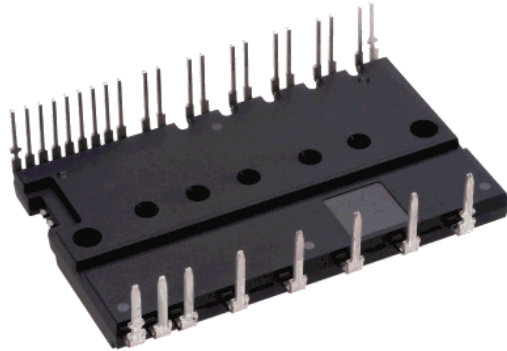


< DIIPM >

PSS10S73FT

TRANSFER MOLDING TYPE
INSULATED TYPE

OUTLINE



MAIN FUNCTION AND RATINGS

- 3 phase DC/AC inverter
- 1200V / 10A (CSTBT)
- N-side IGBT open emitter
- Built-in bootstrap diodes with current limiting resistor

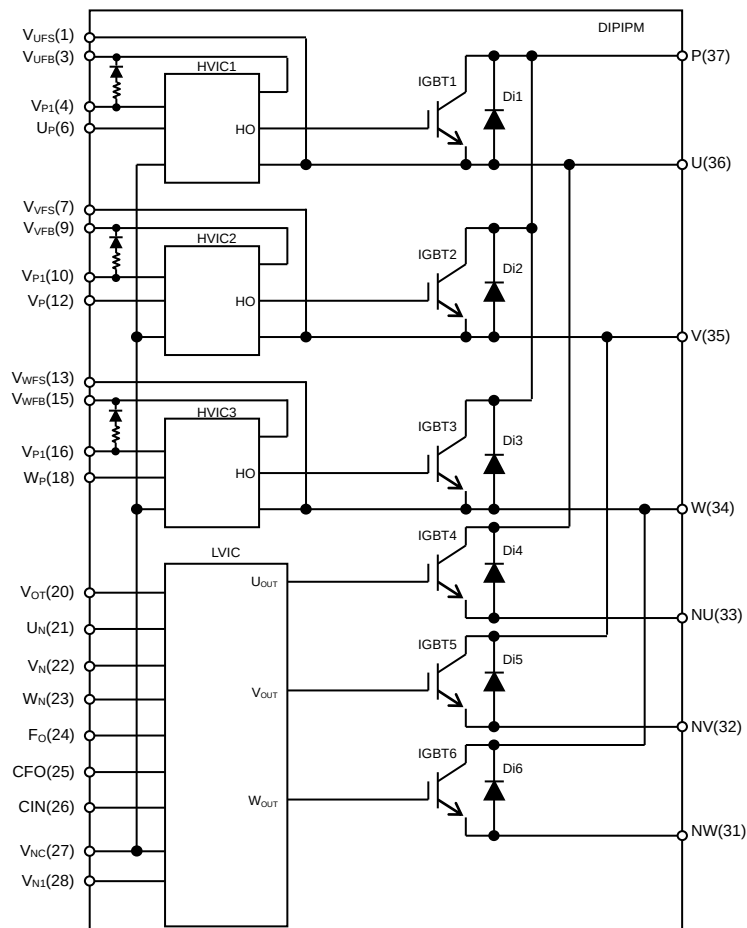
APPLICATION

- AC 400Vrms(DC voltage:800V or below) class
low power motor control

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC),
- Fault signaling : Corresponding to SC fault (N-side IGBT), UV fault (N-side supply)
- Temperature output : Outputting LVIC temperature by analog signal
- Input interface : 3, 5V line, Schmitt trigger receiver circuit (High Active)
- UL Recognized : UL1557 File E323585

INTERNAL CIRCUIT



MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	900	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU, NV, NW	1000	V
V_{CES}	Collector-emitter voltage		1200	V
$\pm I_C$	Each IGBT collector current	$T_C = 25^\circ\text{C}$ (Note 1)	10	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_C = 25^\circ\text{C}$, less than 1ms	20	A
T_{jop}	Operation junction temperature	Continuous operation (Note 2)	-30~+150	$^\circ\text{C}$
T_{jmax}	Maximum junction temperature	Temporally operation (e.g. overload)	175	$^\circ\text{C}$

Note 1: Pulse width and period are limited due to junction temperature.

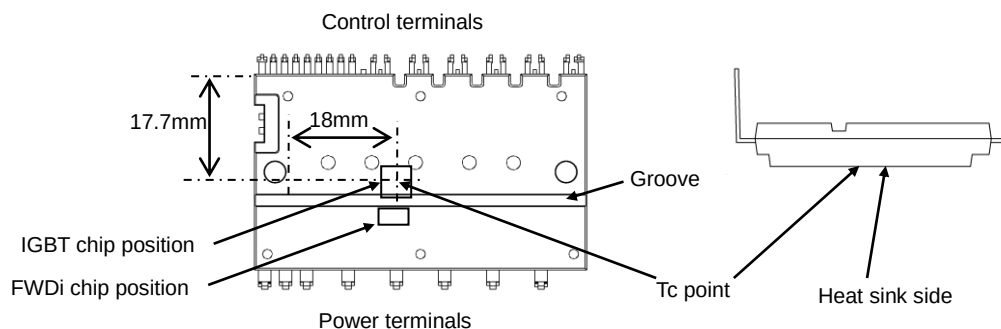
Note 2: The maximum junction temperature rating of built-in power chips is 175°C ($@T_C \leq 125^\circ\text{C}$). However, to ensure safe operation of DIIPM, the average junction temperature should be limited to $T_j(\text{Ave}) \leq 150^\circ\text{C}$ ($@T_C \leq 125^\circ\text{C}$).

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between $V_{P1}-V_{NC}$, $V_{N1}-V_{NC}$	20	V
V_{DB}	Control supply voltage	Applied between $V_{UFB}-V_{UFS}$, $V_{VFB}-V_{VFS}$, $V_{WFB}-V_{WFS}$	20	V
V_{IN}	Input voltage	Applied between U_P , V_P , W_P , U_N , V_N , W_N-V_{NC}	-0.5~ $V_D+0.5$	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~ $V_D+0.5$	V
I_{FO}	Fault output current	Sink current at F_O terminal	5	mA
V_{SC}	Current sensing input voltage	Applied between $CIN-V_{NC}$	-0.5~ $V_D+0.5$	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(Prot)}$	Self protection supply voltage limit (Short circuit protection capability)	$V_D = 13.5\sim 16.5\text{V}$, Inverter Part $T_j = 150^\circ\text{C}$, non-repetitive, less than 2 μs	800	V
T_C	Module case operation temperature	Measurement point of T_C is provided in Fig.1	-30~+125	$^\circ\text{C}$
T_{stg}	Storage temperature		-40~+125	$^\circ\text{C}$
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	V_{rms}

Fig. 1: T_C MEASUREMENT POINT**THERMAL RESISTANCE**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(i-c)Q}$	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	-	-	1.50	K/W
$R_{th(i-c)F}$		Inverter FWDi part (per 1/6 module)	-	-	1.80	K/W

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about $+100\mu\text{m}\sim +200\mu\text{m}$ on the contacting surface of DIIPM and heat sink. The contacting thermal resistance between DIIPM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.3K/W (per 1/6 module, grease thickness: 20 μm , thermal conductivity: 1.0W/m $\cdot$ k).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D=V_{DB} = 15\text{V}$, $I_C = 10\text{A}$, $V_{IN} = 5\text{V}$	-	1.50	2.20	V
V_{EC}	FWDi forward voltage	$V_{IN} = 0\text{V}$, $-I_C = 10\text{A}$	-	1.90	2.40	V
t_{on}	Switching times	$V_{CC} = 600\text{V}$, $V_D = V_{DB} = 15\text{V}$ $I_C = 10\text{A}$, $T_J = 25^\circ\text{C}$, $V_{IN} = 0 \leftrightarrow 5\text{V}$ Inductive Load (upper-lower arm)	0.85	1.50	2.20	μs
$t_{c(on)}$			-	0.30	0.60	μs
t_{off}			-	1.60	2.00	μs
$t_{c(off)}$			-	0.25	0.50	μs
t_{rr}			-	0.40	-	μs
I_{CES}	Collector-emitter cut-off current	$V_{CE} = V_{CES}$	-	-	1	mA

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
I_D	Circuit current	Total of $V_{P1}-V_{NC}$, $V_{N1}-V_{NC}$	$V_D=15\text{V}$, $V_{IN}=0\text{V}$	-	-	5.60
			$V_D=15\text{V}$, $V_{IN}=5\text{V}$	-	-	5.60
I_{DB}		Each part of $V_{UFB}-V_{UFS}$, $V_{VFB}-V_{VFS}$, $V_{WFB}-V_{WFS}$	$V_D=V_{DB}=15\text{V}$, $V_{IN}=0\text{V}$	-	-	0.55
			$V_D=V_{DB}=15\text{V}$, $V_{IN}=5\text{V}$	-	-	0.55
$V_{SC(ref)}$	Short circuit trip level	$V_D = 15\text{V}$ (Note 4)	0.450	0.480	0.510	V
UV_{DBt}	P-side Control supply under-voltage protection(UV)	Trip level	10.0	-	12.0	V
UV_{DBr}		Reset level	10.5	-	12.5	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)	Trip level	10.3	-	12.5	V
UV_{Dr}		Reset level	10.8	-	13.0	V
V_{OT}	Temperature Output	LVIC Temperature= 85°C , Pull down R= $5.1\text{k}\Omega$ (Note 5)	2.51	2.64	2.76	V
V_{FOH}	Fault output voltage	$V_{SC} = 0\text{V}$, F_O terminal pulled up to 5V by $10\text{k}\Omega$	4.9	-	-	V
V_{FOL}		$V_{SC} = 1\text{V}$, $I_{FO} = 1\text{mA}$	-	-	0.95	V
t_{FO}	Fault output pulse width	$C_{FO}=22\text{nF}$ (Note 6)	1.6	2.4	-	ms
I_{IN}	Input current	$V_{IN} = 5\text{V}$	0.70	1.00	1.50	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P , V_P , W_P , U_N , V_N , W_N-V_{NC}	-	-	2.60	V
$V_{th(off)}$	OFF threshold voltage		0.80	-	-	
V_F	Bootstrap Di forward voltage	$I_F=10\text{mA}$ including voltage drop by limiting resistor (Note 7)	0.5	0.9	1.3	V
R	Built-in limiting resistance	Included in bootstrap Di	16	20	24	Ω

Note 4 : SC protection works only for N-side IGBT. Please select the external shunt resistance such that the SC trip-level is less than 2.0 times of the current rating.

5 : DIPIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM. Temperature of LVIC vs. VOT output characteristics is described in Fig. 3. These minimum and maximum curves are based on theoretical designed value excluding LVIC temperature= 85°C limits.

6 : Fault signal F_O outputs when SC or UV protection works. F_O pulse width is different for each protection modes. At SC failure, F_O pulse width is a fixed width which is specified by the capacitor connected to C_{FO} terminal. ($C_{FO}=9.1 \times 10^{-6} \times t_{FO}$ [F]), but at UV failure, F_O outputs continuously until recovering from UV state. (But minimum F_O pulse width is the specified time by C_{FO} .)

7 : The characteristics of bootstrap Di is described in Fig.2.

Fig. 2 Characteristics of bootstrap Di V_F - I_F curve (@ $T_a=25^\circ\text{C}$) including voltage drop by limiting resistor (Right chart is enlarged chart.)

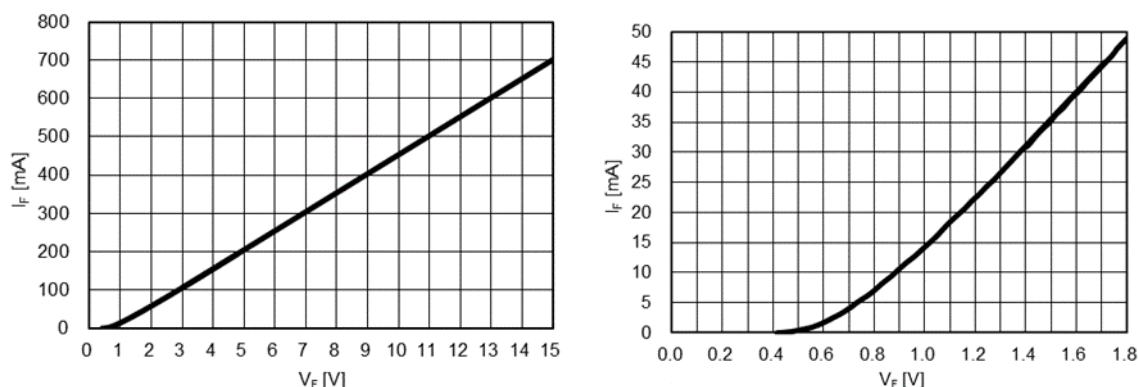
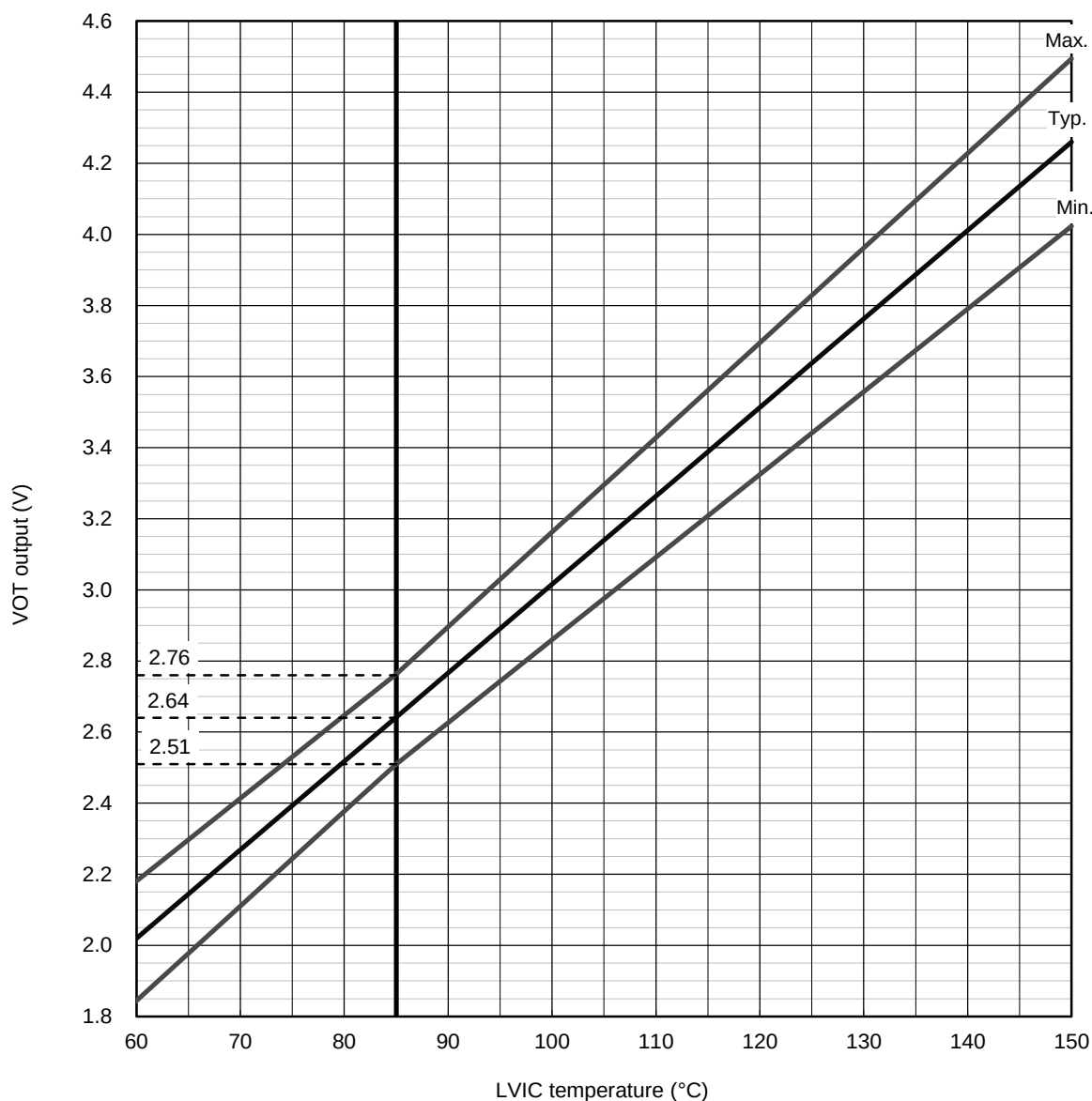
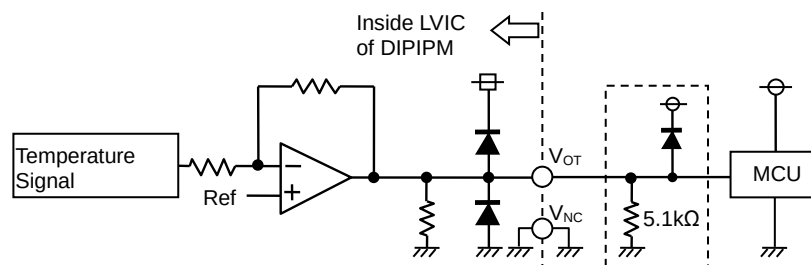


Fig. 3 Temperature of LVIC vs. V_{OT} output characteristicsFig. 4 V_{OT} output circuit

- (1) It is recommended to insert 5.1kΩ pull down resistor for getting linear output characteristics at low temperature below room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC} (control GND), the extra circuit current, which is calculated approximately by V_{OT} output voltage divided by pull down resistance, flows as LVIC circuit current continuously. In the case of using V_{OT} for detecting high temperature over room temperature only, it is unnecessary to insert the pull down resistor.
- (2) In the case of using V_{OT} with low voltage controller like 3.3V MCU, V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and V_{OT} output for preventing over voltage destruction.
- (3) In the case of not using V_{OT} , leave V_{OT} output NC (No Connection).

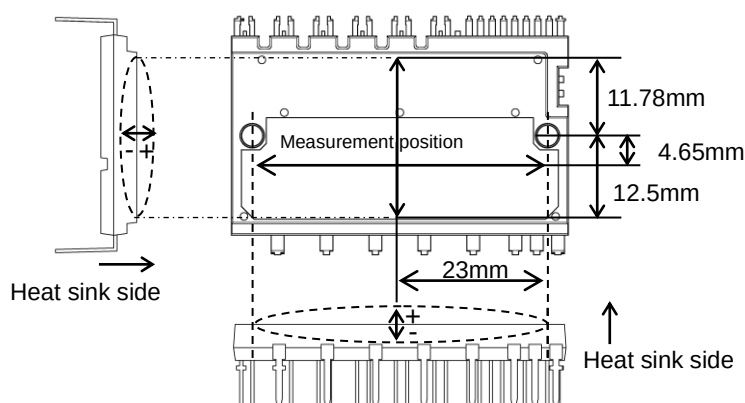
Refer the application note for this product about the usage of V_{OT} .

PSS10S73FT
TRANSFER MOLDING TYPE
INSULATED TYPE
MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Reference	Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 8)	JEITA-ED-4701 402 method II	0.59	0.78	0.98	N·m
Terminal strength pull	Load 10N	JEITA-ED-4701 401 method I	10	-	-	s
Terminal strength bending	Load 5N, 90deg. Bend	JEITA-ED-4701 401 method III	2	-	-	times
Weight		-	-	21	-	g
Heat radiation part flatness	(Note 9)	-	-50	-	100	μm

Note 8: Plain washers (ISO 7089~7094) are recommended.

Note 9: Measurement positions of heat radiation part flatness are as below.

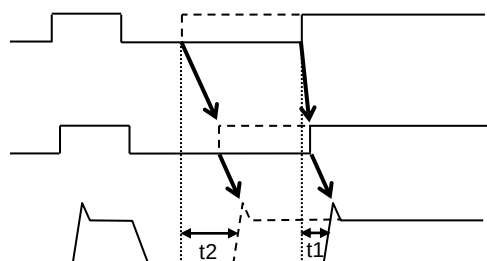
**RECOMMENDED OPERATION CONDITIONS**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	350	600	800	V
V_D	Control supply voltage	Applied between V_{P1} - V_{NC} , V_{N1} - V_{NC}	13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB} - V_{UFS} , V_{VFB} - V_{VFS} , V_{WFB} - V_{WFS}	13.0	15.0	18.5	V
ΔV_D , ΔV_{DB}	Control supply variation		-1	-	+1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal	2.0	-	-	μs
f_{PWM}	PWM input frequency	$T_C \leq 125^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$	-	-	20	kHz
$P_{WIN(on)}$	Minimum input pulse width	(Note 10)	1.0	-	-	μs
$P_{WIN(off)}$		(Note 11)	2.0	-	-	
V_{NC}	V_{NC} variation	Between V_{NC} -NU, NV, NW (including surge)	-5.0	-	+5.0	V

Note 10: DIIPM might not make response if the input signal pulse width is less than $P_{WIN(on)}$.Note 11: DIIPM might make no response or delayed response (P-side IGBT only) for input pulse width less than $P_{WIN(off)}$. Over rated collector current (I_C) operation, DIIPM might make delayed response even if the input signal pulse width is $P_{WIN(off)}$ or more. The timing charts are described as below.

P Side Control Input

Internal IGBT Gate

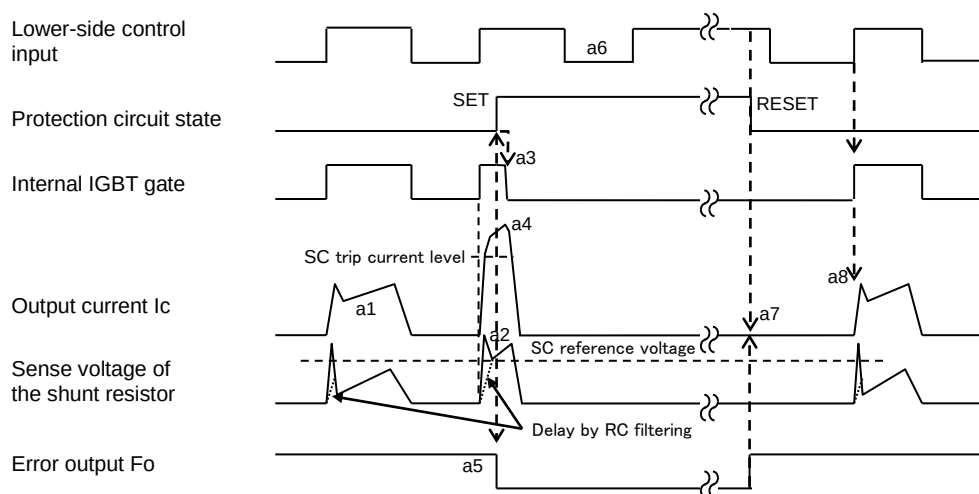
Output Current I_C 

Real line: Normal response; turn on time t_1
 Broken line: Delayed response; turn on time t_2
 (t_1 : Normal switching time)

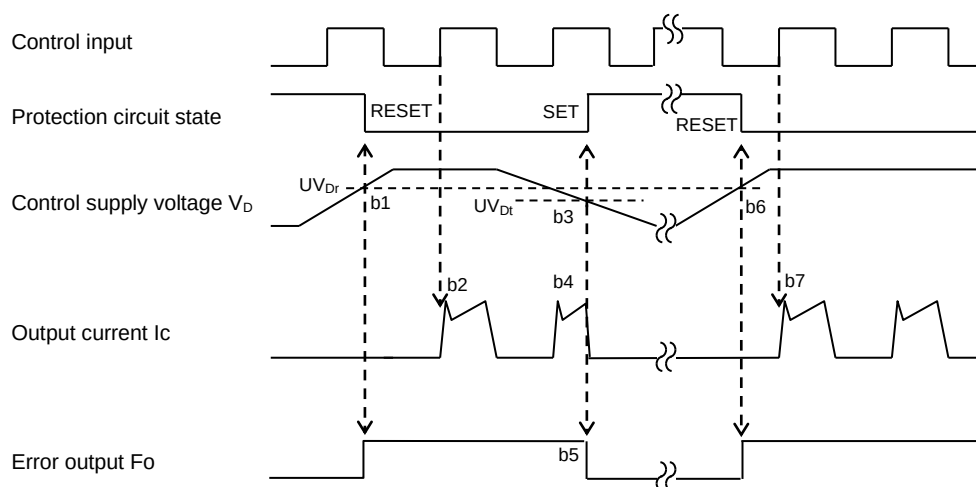
Fig. 5 Timing Charts of The DIIPM Protective Functions

[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

- a1. Normal operation: IGBT ON and outputs current.
- a2. Short circuit current detection (SC trigger)
(It is recommended to set RC time constant 1.5~2.0 μ s so that IGBT shut down within 2.0 μ s when SC.)
- a3. All N-side IGBT's gates are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. F_o outputs. The pulse width of the F_o signal is set by the external capacitor C_{F_o} .
- a6. Input = "L": IGBT OFF
- a7. F_o finishes output, but IGBTs don't turn on until inputting next ON signal (L $\rightarrow$ H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a8. Normal operation: IGBT ON and outputs current.

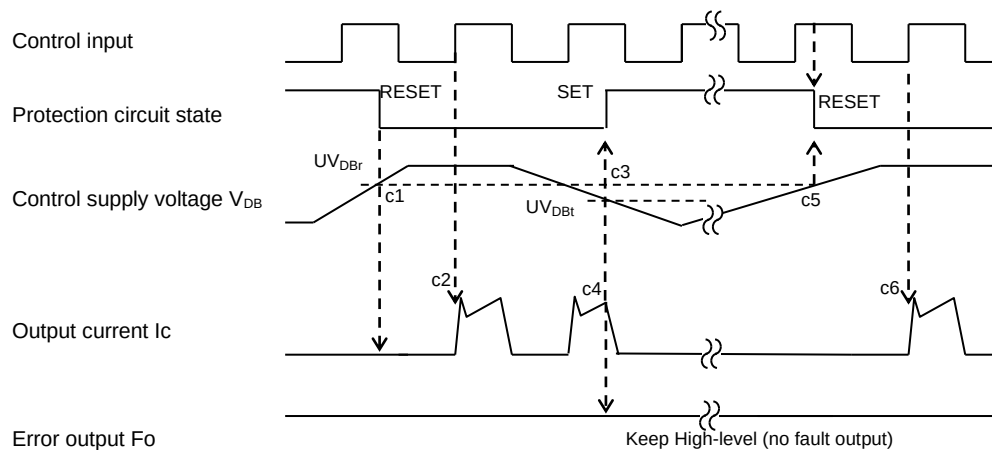
**[B] Under-Voltage Protection (N-side, UV_D)**

- b1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON by next ON signal (L $\rightarrow$ H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- b2. Normal operation: IGBT ON and outputs current.
- b3. V_D level drops to under voltage trip level. (UV_{Dt}).
- b4. All N-side IGBTs turn OFF in spite of control input condition.
- b5. F_o outputs for the period set by the capacitance C_{F_o} , but output is extended during V_D keeps below UV_{Dr} .
- b6. V_D level reaches UV_{Dr} .
- b7. Normal operation: IGBT ON and outputs current.



[C] Under-Voltage Protection (P-side, UV_{DB})

- c1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr} , IGBT turns on by next ON signal (L→H).
- c2. Normal operation: IGBT ON and outputs current.
- c3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
- c4. IGBT of the correspond phase only turns OFF in spite of control input signal level, but there is no F_o signal output.
- c5. V_{DB} level reaches UV_{DBr} .
- c6. Normal operation: IGBT ON and outputs current.



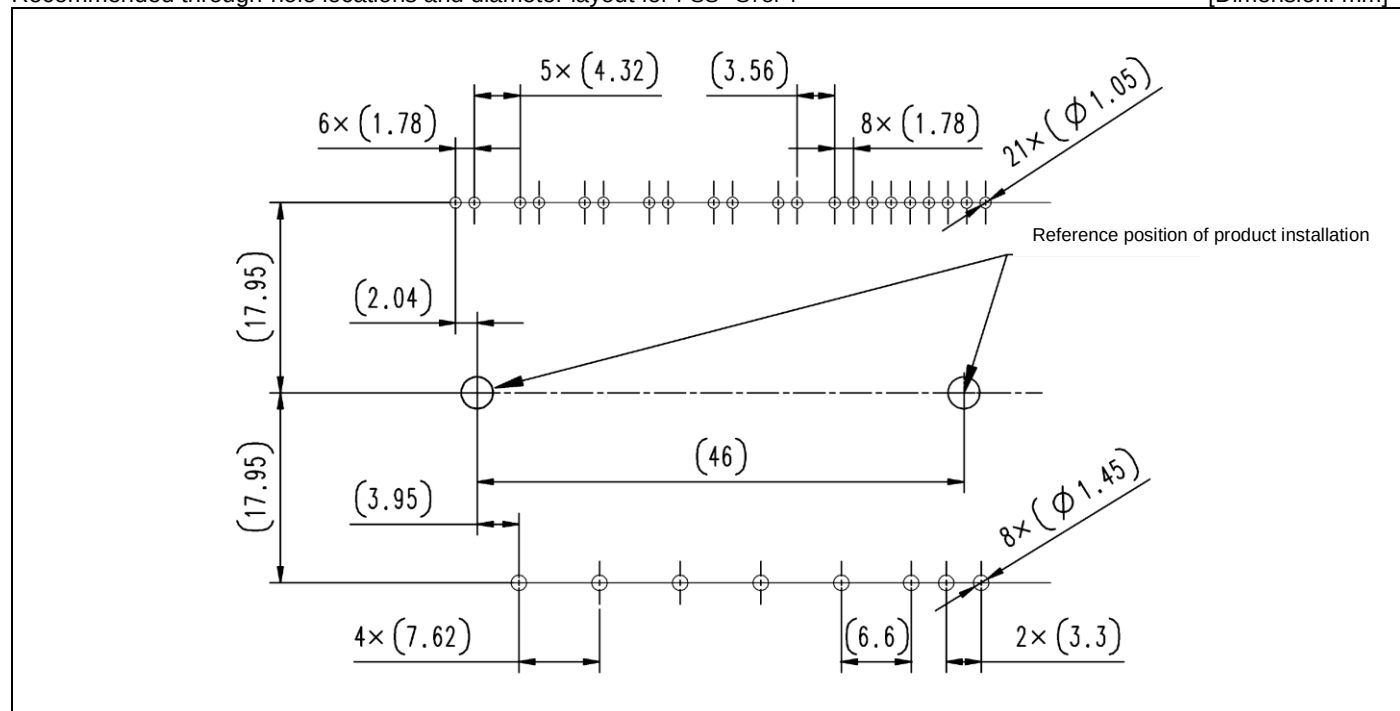
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PSS10S73FTTRANSFER MOLDING TYPE
INSULATED TYPE

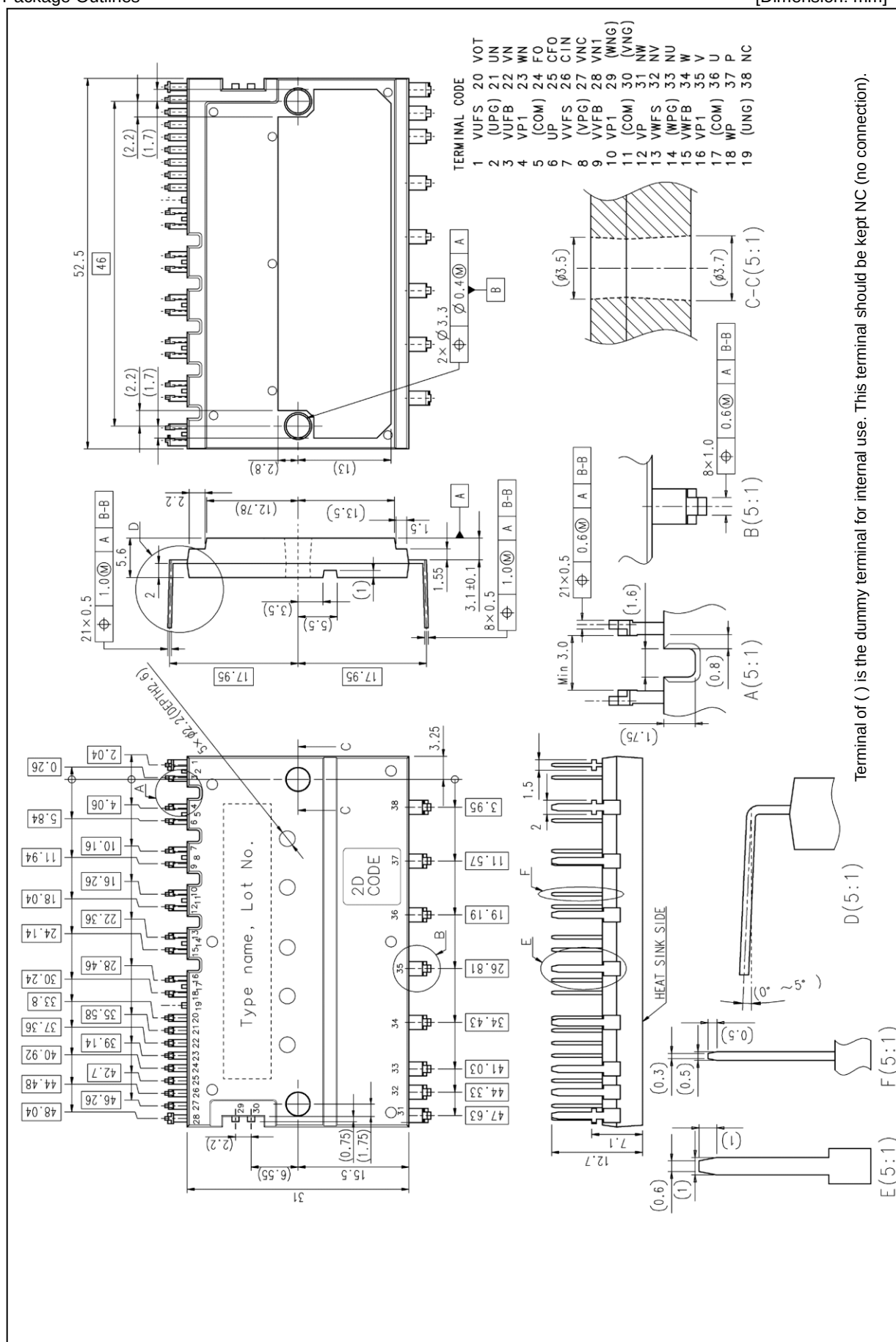
Fig. 10 (Reference Figure) PCB Through-hole Pattern

Recommended through-hole locations and diameter layout for PSS**S73FT

[Dimension: mm]



[Dimension: mm]



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