Electrically Programmable Analog Circuit

Design Handbook

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1996

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Introduction to EPAC

About IMP

IMP, Inc. was founded in 1981, as International Microelectronic Products, Inc. to design, develop and manufacture cell-based, CMOS, application-specific custom ICs (ASICs). It was a pioneer in this segment of the business, being one of the first vendors to employ advanced computer aided engineering (CAE) software and an extensive library of pre-characterized cells. IMP was also one of the first suppliers to integrate mixed analog and digital functions onto the same chip.

Today, IMP's primary focus is to deliver value to its customers through innovative, high-integration, proprietary analog and mixed-signal ICs developed with the core analog process and design competencies created in the custom arena. IMP is a technology leader in the field of analog signal processing techniques for communications, computer and control applications. The company is one of the largest suppliers of highly integrated programmable filters and read-channels for removable media storage peripherals, including the popular Iomega Zip™ drive and tape back-up products from the Colorado Memory Systems division of Hewlett-Packard. To reflect this new identity as a proprietary device supplier, the company name was formally changed in 1993 to the abbreviated form of IMP, Inc.

IMP's headquarters, wafer fabrication plant, and test facility are located in San Jose, California. An engineering and product development center is based in Pleasanton, California. Products are sold through a worldwide network of representatives and distributors, including Wyle Laboratories and Digi-Key Corporation in North America. More information on the company and its products is available on the IMP website at ***http://www.impweb.com***.

EPAC Devices

Electrically Programmable Analog Circuit (EPAC™) devices are the analog counterpart of the digital field programmable gate array (FPGA). They extend the familiar benefits of high-levels of integration, low total system cost, user-configurability and fast time-to-market to analog systems designers. The dual EEPROM/SRAM architecture, which permits in-system reconfiguration under the control of an embedded microcontroller, opens up unique new applications taking advantage of adaptive-analog functionality.

Introduced by IMP, Inc. of San Jose, California in 1995, EPAC devices are the first electrically programmable, general-purpose analog integrated circuits (ICs) in the industry. Low-cost, Analog Magic™, Windows PC-based software and hardware development tools allow users to create and program complex, system-level building blocks on their desktops. Previously this process required expert knowledge and weeks of tedious iterative design effort using multiple low-density IC packages and discrete components. Using EPAC devices and design tools, the design of complex analog circuits can now be accomplished in a few hours by engineers with limited analog experience.

EPAC Devices in the News

IMP EPAC™ devices and Analog Magic™ software have been featured in dozens of journals, in many languages, throughout the world. This includes a front cover feature in Electronic Design magazine, selection as Product of the Year by Electronic Products magazine, and a Product Recognition Award by Control Engineering. Quotations from some of these articles are reprinted below.

EPAC Epoch - "EPAC Will Go Down in History ...."

"I predict that we're at the dawn of a new era ..... I think EPAC will go down in history as one of the opening shots of the revolution.

(As a digital designer) I'm always on the lookout for handy gadgets to help bypass analog hassles, and the EPAC certainly fills the bill.

Configuring an EPAC is easy - largely a point and click exercise. Defining the specific attributes of a cell is a simple matter of double clicking on it. Now tell me, isn't mousing around much easier than messing around with a (typical prototype analog circuit design) rat's nest."

Circuit Cellar Ink

Analog Counterparts of FPGAs Ease System Design

"Analog (custom) arrays have ... nearly disappeared. That's because they're expensive and risky. Many chips worked - until they were plugged into systems. ...the need for a low-cost, easy-to-use, *foolproof* analog ASIC became clear. Designers at IMP answered the call."

Electronic Design

Epoch of EPAC: The Start of the Analogue FPGA Era ?

"The EPAC design method ... goes some way towards de-skilling the design of analog circuits by allowing the user to operate at the module level.

... not only can configurations be selected on the fly but also by the host microcontroller in response to system behavior, providing interesting system design possibilities."

Electronic Engineering

New Directions ...

" The device is intended to simplify analog design choices for digital designers. It should appeal to ... the novice wondering why everything oscillates but the oscillator."

Computer Design

Les Circuits Analogiques ..... Enfin Programmables!

(Analog Circuits ..... Finally Programmable!)

"IMP circuits are the analog equivalent to the digital FPGA: they allow programming of the characteristics and application function without needing to understand analog design."

Electronique

EPAC Technology Overview

Abstract

The IMP50E10 is the first analog integrated circuit that can be programmed by the user, even in the field. It is an analog counterpart to a digital FPGA. This paper provides an overview of the technology used in EPAC™ devices. Examples are given of various programmable functions, along with several applications of them to demonstrate the degree of flexibility and ease of design that is achieved.

Overview

Electrically Programmable Analog Circuit (EPAC) technology provides the users of analog circuits with access to an analog counterpart of digital field-programmable gate arrays (FPGA). EPAC devices are analog ICs where functionality, performance characteristics and interconnection are all programmable.

EPAC technology is based on a mixed-signal CMOS process with on-chip SRAM and EEPROM memory. Programming can be performed either off-line or in real-time, which means the user can make changes "on-the-fly" (i.e., in-system programming) while leaving the original EEPROM configuration unchanged. EPAC devices are totally self-contained. They do not require external programming equipment to change any of the configuration settings. The first devices form fully functional analog systems without using additional external components.

EPAC technology raises the analog design task from a tedious and error-prone component level to a functional, or block, level. This is made possible by programmable analog "expert cells," each of which feature a variety of functions and performance characteristics. The EPAC development and debug process is supported by the intuitive Analog Magic™ PC-based development software that utilizes "correct-by-construction" and unique WYSIWYG methodologies.

Using the EPAC Development System, the user builds a circuit on a building-block level by choosing both the functional performance and interconnection of the modules. This approach simplifies and shortens the design task.

Like FPGAs, EPAC devices offer significant benefits over traditional analog design approaches because they address the key needs of today's system developers, such as:

- instant prototyping and reprogramming,
- design on a block level using an intuitive Windows-based design system,
- flexible design implementation due to SRAM and EEPROM technology,
- no NRE for design or redesign,
- minimum inventory and purchase commitment, and
- generalized test programs.

To address cost-effective solutions at large volumes, IMP also offers a sibling product line, MPACs (Mask-Programmable Analog Circuits). Cost reduction in MPACs is achieved by using a simpler process, smaller die size and larger-volume orders.

The following discussion will provide information about process technology, circuit topology and applications.

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The EPAC Architecture: An Expert Cell Approach to Field Programmable Analog Devices

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Abstract

This paper describes the architectural configuration of the Electrically Programmable Analog Circuit (EPAC™), an expert cell approach to meeting the market need for an analog counterpart to the digital FPGA. It provides an overview of the technology and describes the internal operation of the first commercial EPAC devices.

1. Overview

EPAC devices are analog ICs that can be programmed in functionality, interconnect, and performance characteristics. The EPAC device architecture is based on a mixed-signal CMOS process with on-chip SRAM and EEPROM memory to provide user programmability. Programming can be performed either off-line or in real-time. The SRAM components enable in-system functional reconfiguration, while leaving the original EEPROM configuration unchanged.

EPAC technology raises the design task of system analog functions from a tedious and error-prone component level to a functional, or block, level. This is made possible by programmable analog "expert cell" modules each of which feature a variety of functions and performance characteristics. Using a PC-based development system, the user creates a circuit by selecting the functionality of the modules along with their respective performance settings and cell-to-cell interconnections. This approach greatly simplifies and shortens the design for analog circuits.

Programmable analog devices offer significant benefits over traditional analog design approaches because they address key needs of today's system developers, by providing

- High levels of integration
- Instant prototyping and reprogramming
- Design on block level using intuitive design tools
- In-system reconfiguration for use in microcontroller-based systems
- No NRE for design or redesign
- Minimum inventory and purchase commitment
- Generalized test programs.

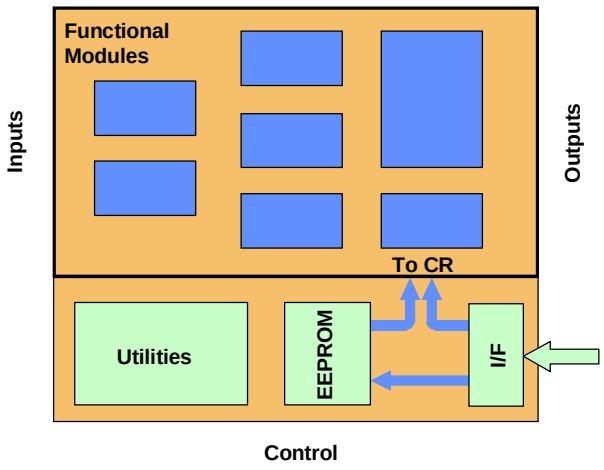
The EPAC architecture also permits straightforward migration of designs to a compatible mask-programmable solution using a simpler process and smaller die size for high-volume applications.

2. EECMOS Process Technology

The first implementation of EPAC technology is based on a 1.2 micron analog EECMOS process. This required adding a self-contained EEPROM process module (including a high-voltage generator) to a proven analog CMOS process without affecting the critical analog performance characteristics. This permits the device design engineers to draw from an existing library of high-performance cells, ranging from very fast circuits to high-precision converters, references, etc. This also ensures that the performance of the modules embedded in EPAC devices are competitive with dedicated ICs, while offering higher degrees of flexibility and functionality.

3. The EPAC Device Framework

EPAC devices are built on framework which incorporates the functional modules together with programming features, debugging aides and reference modules. The key elements of that framework include a serial interface, an EEPROM-memory module, a “utility” section, and a functional section containing programmable analog modules.



The serial programming interface both configures the IC and processes commands, including probing of internal analog or digital signals, readback of configuration data, controls power management and other functions. The readback data can be locked out by setting a security bit. Multiple EPAC devices can be cascaded and programmed in sequence or individually if a microprocessor is available in

the system. Automatic synchronization among multiple devices is provided so that all chips "wake up" in the new configuration simultaneously. No special programmer architectures are required to interface with the chip.

Via the EPAC framework, analog modules can be configured using the on-chip EEPROM memory which acts as “shadow memory” for the SRAM-based configuration register (CR). On powering up, the EEPROM contents are internally downloaded into a CR carrying the data to the appropriate modules. The CR can also be loaded directly from the serial interface such that multiple configurations can be executed without disturbing the contents of the EEPROM. The contents of the CR and the EEPROM can be redefined at any time, even while the chip is in normal operation.

4. Expert Cell Functional Modules

Unlike in FPGAs, where generic logic modules can implement virtually any digital function, analog circuits must be dedicated to address the large variety of specifications, such as input and output voltage and current, frequency range, noise and accuracy requirements. Since each of these specifications require their specific trade-offs (area, cost, power-consumption, features, etc.) it is more challenging to define a programmable analog architecture than a digital FPGA. Even though it is possible to create a rather generic user-programmable array architecture [1-3], the wide range of performance requirements makes it necessary to optimize the “array” for a certain range of applications. As a result, EPAC devices are more dedicated to a certain class of applications and hence offer better performance-functionality trade-offs than general-purpose arrays. The same dedication also simplifies the chip architecture and minimizes circuit overhead and, hence, cost. Examples of the kind of application areas for this approach include general signal conditioning, data communication, data/signal monitoring, process control, etc. Consequently, EPAC devices contain modules that are optimized for use in those application classes.

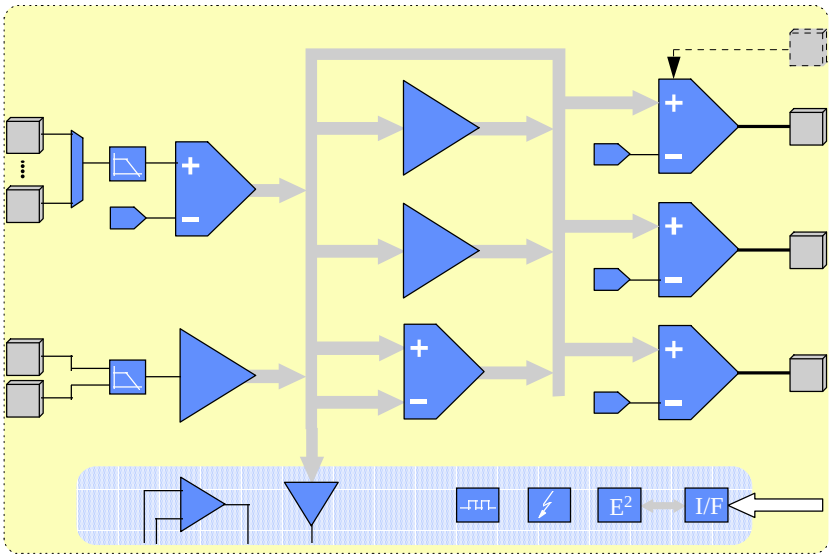
One of the key differences between EPAC devices and FPGAs or other general-purpose analog arrays is that the granularity of the building blocks is quite different. While FPGAs typically provide access to a large number of relatively low-level cells, the EPAC architecture provides high level cells (or “macro” modules). The cells typically include high-level functions such as D/A converters, amplifiers and comparators rather than simple operational amplifiers, resistors, capacitors or other low-level components.

These high-level modules have been given a large number of programmable characteristics. We describe these modules as "expert cells," because they have been developed by an analog IC design expert and given a variety of useful options all of which are guaranteed to work, no matter how they are used. The user does not need to worry about temperature matching, offset cancellation, parasitic coupling, stability, loading effects, gain-bandwidth trade-offs, minimization of power consumption, etc. By contrast, analog arrays following the FPGA paradigm suffer from parasitics introduced by unpredictable routing and signal coupling, and the cells cannot be optimized for special performance requirements (such as low noise) even though they offer the potential for a larger number of implementable functions.

For each EPAC expert cell module, the user can select from a variety of functions and for each function there is a set of parameters to choose from. Within the constraints presented by the development system, the user is free to choose any combination available. Thus, the development process is highly simplified, guaranteed by construction, and because the possible or meaningful routing options can be predetermined, the compilation of configuration and routing data literally takes only seconds.

The figure below shows, for overview purposes, a simplified block diagram of an EPAC device, the IMP50E10, which is targeted at general signal-conditioning applications. The “flow” of the chip is from input modules on the left, through core modules to output modules on the right. The shaded area at the bottom of the block represents the “utility section” which contains the serial interface, memory module, power management, oscillator, probe, and an operational amplifier.

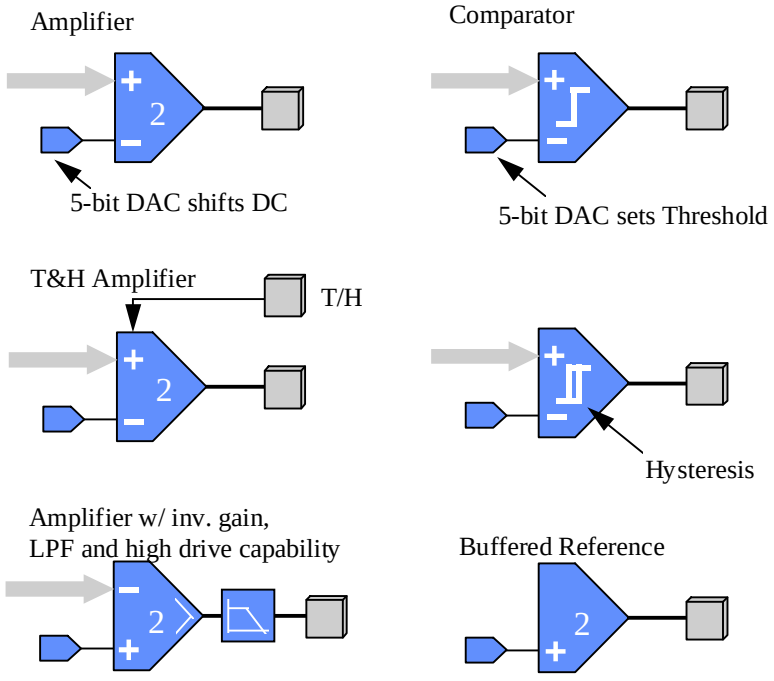
The output module of the IMP50E10 is a good example to show the degree of flexibility which can be designed into an EPAC expert cell module: It can act as an amplifier with reference to ground (e.g., 0 V), or virtual ground (e.g., 2.5 V), with or without a low-pass filter in the signal path. The amplifier can be "free running" or a sample-and-hold type. The module can also act as a comparator with and without



Block Diagram of a User Programmable Analog Signal Conditioning Device

hysteresis. A second input to the module connects to a dedicated 5-bit DAC, letting the user define the trip-point of the comparator. The same DAC input can be used to either drive the amplifier (thus making it a reference module) or provide for DC-shift of the outgoing signal. This output module can operate at a reduced power consumption for slower-speed signals and in its "turbo mode" the output can sink and source higher currents. The module can also be shut off altogether, either selectively while other modules continue to operate, or globally when the entire chip powers down. With all of these combinations, the user doesn't need to worry about component-level detail as this has been already implemented.

Supported by an intuitive development system ("Analog Magic"), the user can select from a menu of functions for each module. Then for each function there is a respective set of characteristics available. In case of the previous output module example each selected function and characteristics results in a different graphical representation on the screen, as shown below.

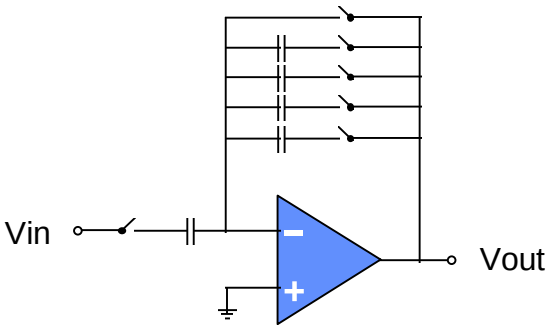


Examples of certain selections made of an output module

5. Module Implementation

Because of the target applications of general-purpose signal conditioning switched-capacitor (SC) technology was chosen as the prime implementation technique for the IMP50E10. SC modules offer advantages of high reproducibility and excellent stability, and these techniques have been in use for many years. The figure below shows the underlying principle of SC circuit modules.

The input capacitor samples an incoming voltage signal



Switched-Capacitor Implementation Concept

while feedback capacitors determine the amount of gain between input and output signal. When "transferring" the charge from input to feedback capacitors, the ratio between them determines the amount of output voltage needed to achieve and complete the transfer. Hence, it is the capacitor ratio and not their absolute value that determines the gain. Since capacitor ratios can be manufactured very precisely, gain matching of 0.1% can be achieved. Furthermore, the gain is not subject to temperature drift as the closely coupled capacitors are affected identically. In fact, most of today's A/D converters use the same principle to achieve 10-16 bit resolution, however trimming is required beyond 10 bits.

The principle drawing shown above is a highly simplified version of the techniques used in the IMP50E10. For example, to increase flexibility and performance all capacitors can be made programmable, multi-phase clocking can enable offset and noise cancellation through "correlated double-sampling", clock rates can be altered to allow for various speed settings, and multiple inputs can be used to sum multiple inputs. In addition, modules can be implemented in fully-differential manner, effectively doubling the feedback circuitry with the substantial benefit of good common-mode rejection and excellent clock-feedthrough cancellation.

Another important benefit of this technique is that it only requires a 5V while input signals can go from rail to rail, and even beyond. On the downside, because SC circuits are clocked, the Nyquist sampling theorem must be considered. Thus, the bandwidth of the incoming signal must be limited, for which there are low-pass filters on chip.

In other application areas where such characteristics are not as interesting different implementation techniques can be chosen. An example would be current mode or traditional continuous-time voltage-mode techniques to achieve higher system bandwidth. A practical application would be data-communication requiring tens of MHz bandwidth. There's no significant limitation to the speed achievable with EPAC

devices, it's merely a trade-off between "overhead" (area, power, functionality) and programmability.

6. Signal Highway Interconnect Approach

One of the unique features of EPAC technology is the user-programmable interconnect among various modules. This allows the user to implement different functions on the same chip. Likewise, on-chip modules can be reused for different purposes automatically without the user even realizing it.

To allow for such capability the output signals of each module are provided to an on-chip "signal highway" to which all other analog modules have access. This "signal highway" is an on-chip bus of balanced and shielded signal wires. Because the underlying architecture is not really a grid-array of a large number of general-purpose cells (like in FPGAs) but rather an assembly of optimized modules, it is possible to predict all possible and meaningful interconnect schemes. Thus, the signal highway can be optimized for 100% routability with lowest crosstalk and minimization of other parasitic effects. This is an important difference to other approaches because the traditional problem of severely limiting the performance by the programmable interconnect network is not present in EPAC devices.

Optimized analog switches are used to form interconnect among modules and to control components internal to the modules. These switches are arranged in clusters to form "highway-connectors" at the appropriate locations. Inside each functional module, analog switches also select component values or ratios, feedback tap-points, change bias conditions, and perform all other analog programming.

New and proprietary circuit techniques had to be developed to overcome the problem of varying loading effects when connecting various modules together. The combined optimization of the signal highway, the interconnect switches, and the modules' input and output stages allow for a totally flexible interconnect scheme which puts no restrictions on the user's configuration.

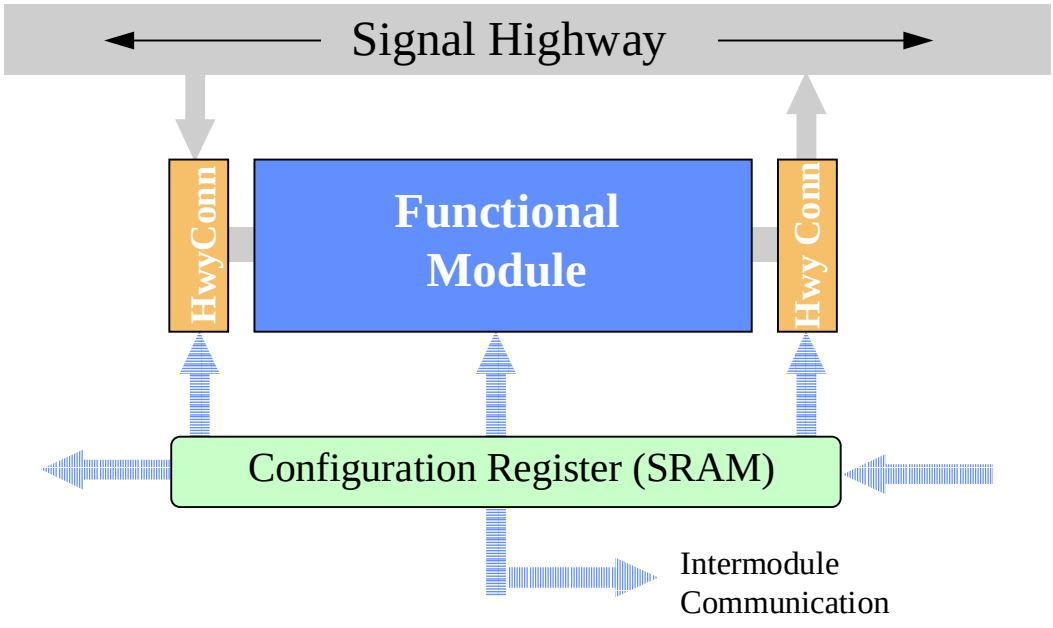
For example, a user may choose to connect all modules in series, to achieve the highest possible signal gain (20,000 V/V, or 86 dB) in case of the IMP50E10. Alternatively, the user may want to run signals independently and concurrently through the chip, probably connecting only one input module to one output module. In another example, the user can switch between four different sets of characteristics within 4 micro-seconds. Or the user can reconfigure the chip including all interconnects for an entirely new configuration within 200 micro-seconds.

7. Design Example and Performance

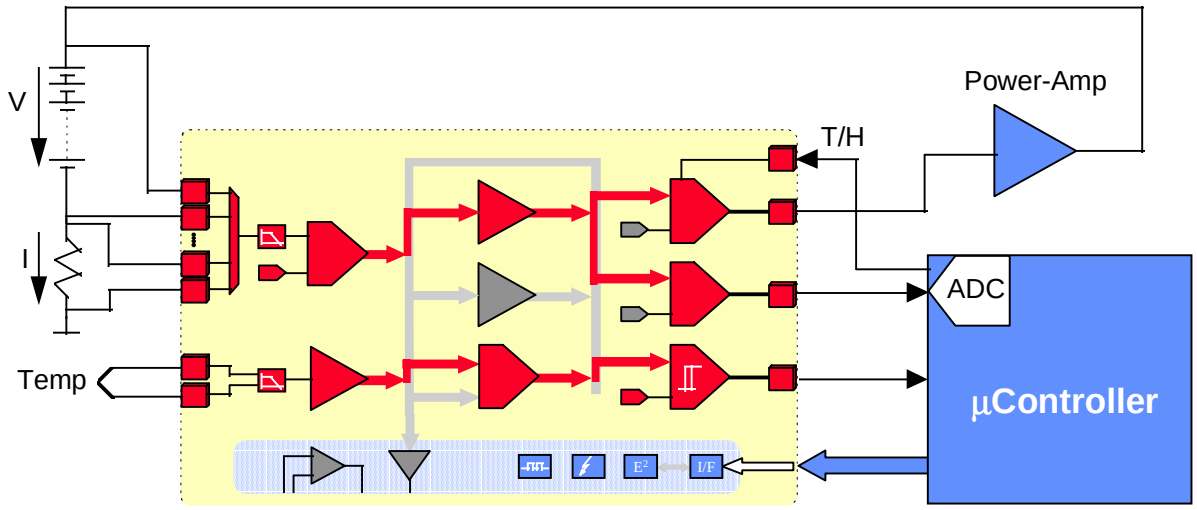
To illustrate the usage of the IMP50E10, the figure on the next page shows an industrial implementation of a multi-sensor analog front end to an A/D converter in a battery-charger application. This implementation was done in conjunction with a micro-controller to allow for in-system reprogramming.

In the example shown, the EPAC device picks up different sensor signals (voltage, current, temperature) and conditions them for later A/D conversion. The temperature signal is derived from a thermocouple although other (and cheaper) sensor could have been used. Unlike the voltage and current signals which are selected through the input multiplexer, the temperature signal enters the chip in a separate channel. Also, unlike the other signals, the temperature signals triggers an on-chip comparator at a programmable trip point, only alerting the microcontroller when the temperature exceeds a critical limit.

Other system-level functions not obvious from the schematic include automatic offset cancellation for chip and



Functional module and its surrounding support modules



Application Example using the IMP50E10

sensor offsets, automatic changes of gain, offset, and filter settings when switching among the different input signals.

The table below summarizes just a few of the many performance characteristics:

Power Supply Voltage	5V +/- 10%
Quiescent supply current	3.8 - 18 mA (configuration dependent)
Sleep-mode current	40 uA
Max. sampling rate	250 kHz
Max. signal bandwidth	125 kHz (Nyquist rate)
Input/output voltage range	0 - 5 V (rail-to-rail)
Gain range and error	1 - 20,000 V/V, 1.2% typ.
Gain drift	30 ppm/^{o}C
Offset before/after Auto-Zero	<10 mV, <100 uV
Offset drift	50 uV/^{o}C
Max. capacitive load	infinite (unconditionally stable)
Noise level, DC-15 kHz	0.4 uV/sqrt(Hz), input referred
Max. output current	40 mA
Max. dynamic range	100 dB
THD	-68 dB

Summary

In this paper we present the expert-cell approach to programmable analog solutions for rapid prototyping and customization of analog integrated circuits. In contrast to general-purpose grid-array cells, the expert-cell approach allows for higher performance, less overhead, and lower cost.

EPAC devices are more tailored to a certain range of applications than digital FPGAs, but they basically offer the same benefits. The high degree of programmability and ease of development, using low-cost PC-based tools, allows the user to implement a complex analog function in minutes.

References

[1] E. Pierzchala et al., "Current-Mode Amplifier/Integrator for a Field-Programmable Analog Array," *ISSCC Digest of Technical Papers*, 1994, San Francisco

[2] E. Lee et al., "A Transconductor-based Field-Programmable Analog Array", *ISSCC Digest of Technical Papers*, 1994, San Francisco

[3] Pilkington, Conf. Proceedings, PLD 1995, London

[4] R. W. Brodersen et al., "MOS Switched-Capacitor Filters," *Proc. IEEE*, Vol. 67, No. 1, Jan. 1979

[5] R. Gregorian et al., "Switched-Capacitor Circuit Design," *Proc. IEEE*, Vol. 71, No. 8, Aug. 1983

[6] E. Habekotte et al. "State of the Art in Analog CMOS Circuit Design," *Proc. IEEE*, Vol. 75, No. 6, June 1987