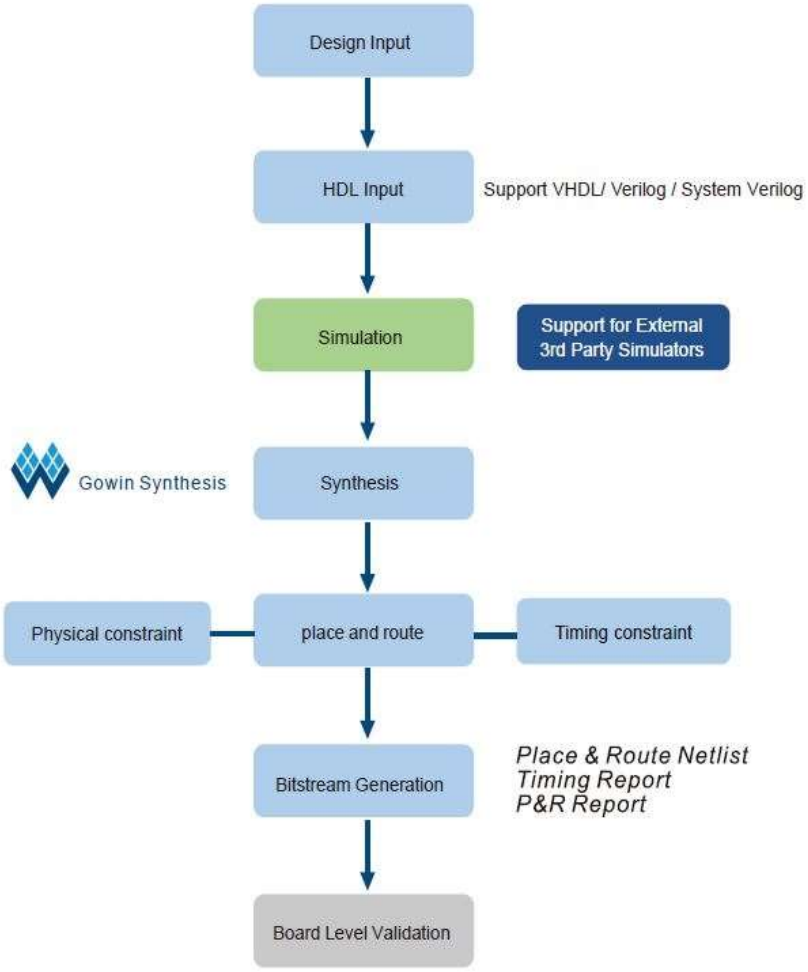
GOWIN EDA

GOWIN EDA (Gowin® EDA) – our easy to use integrated design environment provides design engineers one-stop solution from design entry to verification.

Features:

- Complete GUI based environment from FPGA design entry, code synthesis, place & route, bitsteam generation to download on the GOWIN FPGA on your boards.
- Integrates in-house GowinSynthesis for front end design synthesis
- Supports creating RTL and Post-Synthesis.
    - RTL input files are RTL file complied with Hardware Description
- Language and constraints file that users require;
    - Post-synthesis input files are netlist file generated by user RTL
- Synthesis and constraints files that users require.
- Integrates IP Core Generator
- Online debug tool Gowin Analysis Oscilloscope (GAO) for instant analyze of signal design


Design Input
HDL Input
Support VHDL/ Verilog / System Verilog
Simulation
Support for External
3rd Party Simulators
Gowin Synthesis
Synthesis
Physical constraint
place and route
Timing constraint
Bitstream Generation
Place & Route Netlist
Timing Report
P&R Report
Board Level Validation

GOWIN's official choice in simulation solutions is Metrics Design Automation's DSim. Designers never have to think again about whether they can afford to simulate or whether their simulator is up to the job. Now all GOWIN FPGA designers have a world-class simulator with unlimited resources at their fingertips from a single server to thousands of nodes if they need to finish a large test very quickly. True freedom to design and deliver.