

## DM74ALS174/DM74ALS175 Hex/Quad D Flip-Flops with Clear

### General Description

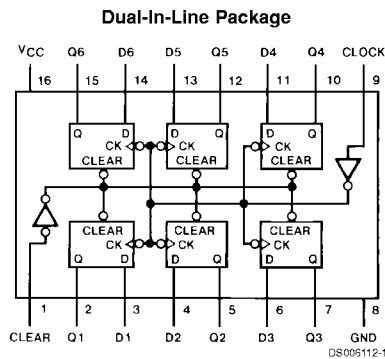
These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. Both have an asynchronous clear input, and the quad (175) version features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

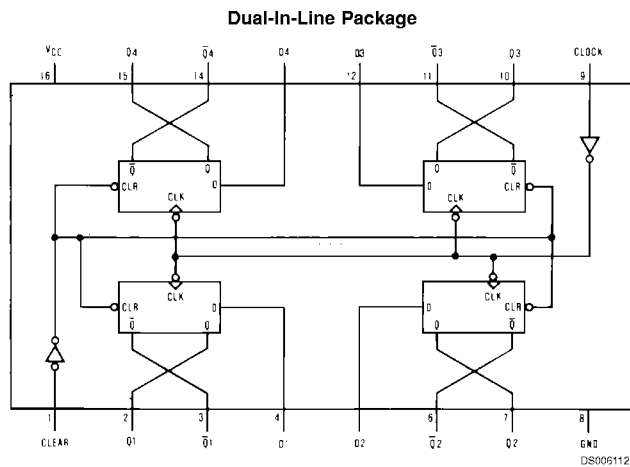
### Features

- Advanced oxide-isolated ion-implanted Schottky TTL process
- Pin and functional compatible with LS family counterpart
- Typical clock frequency maximum is 80 MHz
- Switching performance guaranteed over full temperature and  $V_{CC}$  supply range

### Connection Diagrams



Order Number DM74ALS174M, DM74ALS174N or DM74ALS174SJ  
See Package Number M16A, M16D or N16A



## Function Table

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}^*$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	$Q_0$	$\overline{Q}_0$

H = High Level (steady state)

L = Low Level (steady state)

X = Don't Care

↑ = Transition from Low to High Level

$Q_0$  = the level of Q before the indicated steady-state input conditions were established

\*applies to 74ALS175 only

Order Number **DM74ALS175M, DM74ALS175N or DM74ALS175SJ**

See Package Number **M16A, M16D or N16A**

## Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
DM74ALS	

Storage Temperature Range	-65°C to +150°C
Typical $\theta_{JA}$	
N Package	77.9°C/W
M Package	107.3°C/W

## Recommended Operating Conditions

Symbol	Parameter	DM74ALS174,175			Units
		Min	Nom	Max	
$V_{CC}$	Supply Voltage	4.5	5	5.5	V
$V_{IH}$	High Level Input Voltage	2			V
$V_{IL}$	Low Level Input Voltage			0.8	V
$I_{OH}$	High Level Output Current			-0.4	mA
$I_{OL}$	Low Level Output Current			8	mA
$t_w$	Pulse Width	Clock	10		ns
		High or Low			
		Clear Low	10		
$t_{SETUP}$	Setup Time (Note 2)	Data Input	10 $\uparrow$		ns
		Clear	6 $\uparrow$		
		Inactive State			
$t_{HOLD}$	Data Hold Time (Note 2)	0 $\uparrow$			ns
$f_{CLOCK}$	Clock Frequency	0		50	MHz
$T_A$	Free Air Operating Temperature	0		70	°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** The symbol  $\uparrow$  indicates that the rising edge of the clock is used as reference.

## Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IK}$	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_{IN} = -18 mA$			-1.5	V
$V_{OH}$	High Level Output Voltage	$I_{OH} = -400 \mu A$ $V_{CC} = 4.5V$ to $5.5V$	$V_{CC} - 2$	$V_{CC} - 1.6$		V
$V_{OL}$	Low Level Output Voltage	$V_{CC} = 4.5V$ DM74 $I_{OL} = 8 mA$		0.35	0.5	V
$I_i$	Input Current at Max Input Voltage	$V_{CC} = 5.5V$ , $V_{IN} = 7V$			0.1	mA
$I_{IH}$	High Level Input Current	$V_{CC} = 5.5V$ , $V_{IH} = 2.7V$			20	$\mu A$
$I_{IL}$	Low Level Input Current	$V_{CC} = 5.5V$ , $V_{IN} = 0.4V$			-0.1	mA
$I_o$	Output Drive Current	$V_{CC} = 5.5V$ , $V_o = 2.25V$	-30		-112	mA
$I_{CC}$	Supply Current	$V_{CC} = 5.5V$ Clock = 4.5V Clear = GND D Input = GND	ALS174	11	19	mA
		ALS175	8	14		

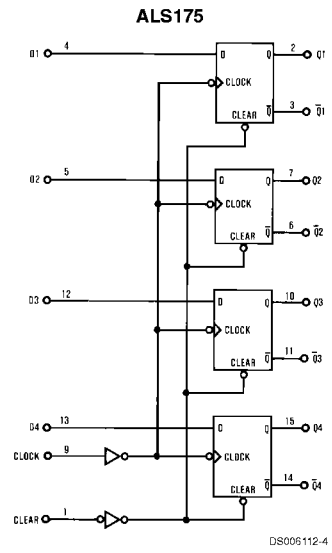
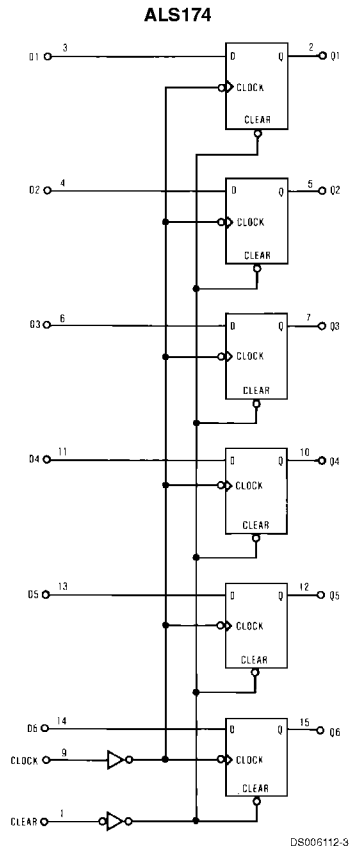
## Switching Characteristics (Note 3)

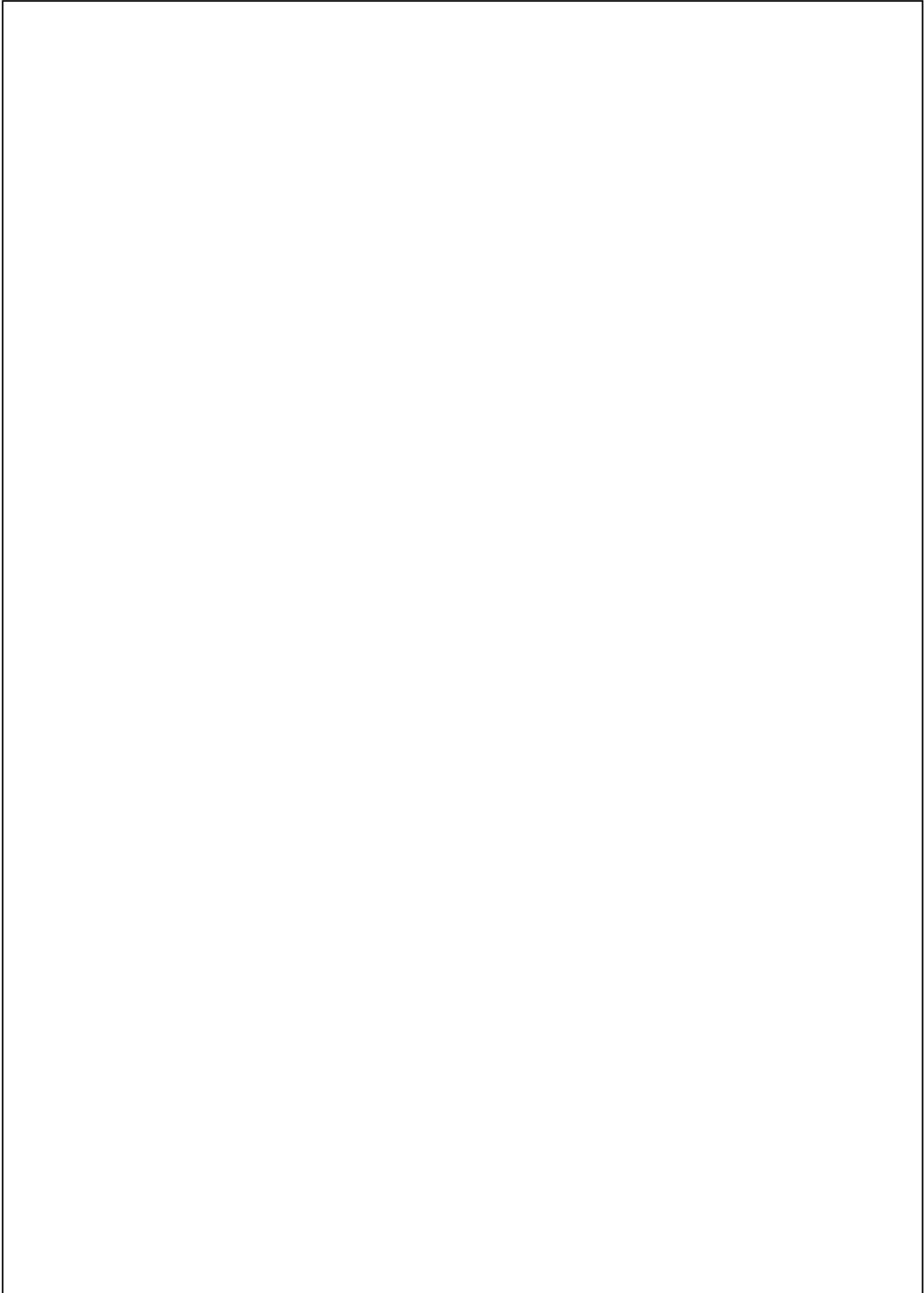
over recommended operating free air temperature range

Symbol	Parameter	Conditions	DM74ALS174, 175		Units
			Min	Max	
$f_{MAX}$	Maximum Clock Frequency	$R_L = 500\Omega$ $C_L = 50\text{ pF}$ $V_{CC} = 4.5\text{V to }5.5\text{V}$	50		MHz
$t_{PLH}$	Propagation Delay Time Low to High Level Output From Clear (175 Only)		5	18	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output From Clear		8	23	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output From Clock		3	15	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output From Clock		5	17	ns

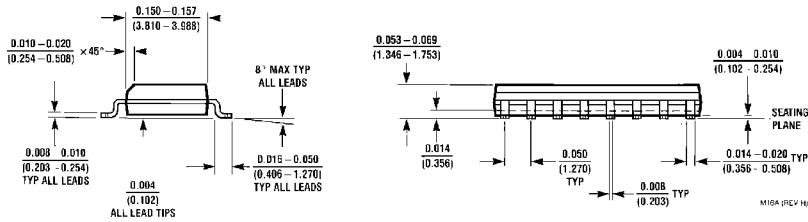
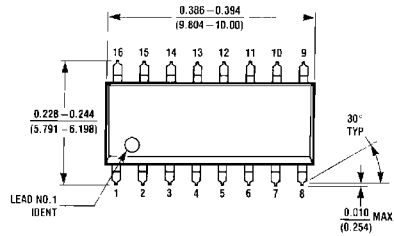
**Note 3:** See Section 1 for test waveforms and output load.

# Logic Diagrams

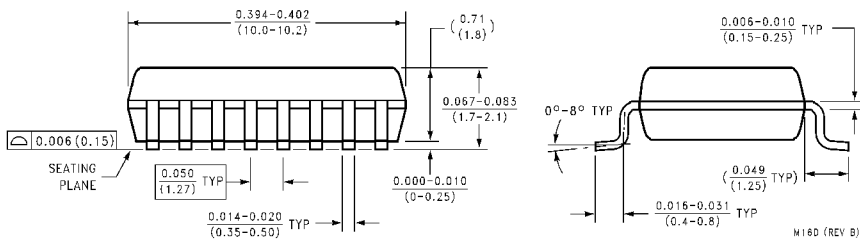
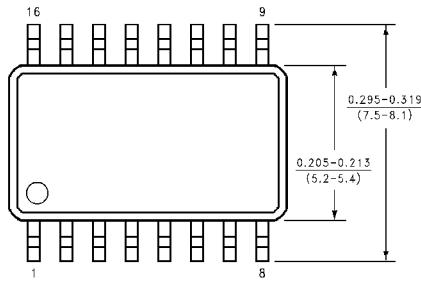




**Physical Dimensions** inches (millimeters) unless otherwise noted

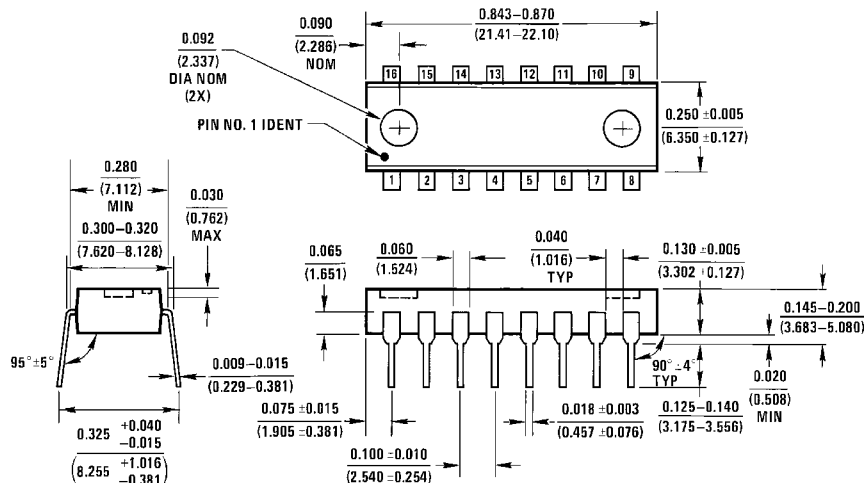


**S.O. Package (M)**  
**Order Number DM74ALS174M or DM74ALS175M**  
**Package Number M16A**



**Small Outline Package (SJ)**  
**Order Number DM74ALS174SJ or DM74ALS175SJ**  
**Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



N16A (REV B)

**Molded Dual-In-Line Package (N)**  
**Order Number DM74ALS174N or DM74ALS175N**  
**Package Number N16A**

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Fairchild Semiconductor Corporation  
 Americas  
 Customer Response Center  
 Tel: 1-888-522-5372

Fairchild Semiconductor Europe  
 Fax: +49 (0) 1 80-530 85 86  
 Email: europe.support@nsc.com  
 Deutsch Tel: +49 (0) 8 141-35-0  
 English Tel: +44 (0) 1 793-85-68-56  
 Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.  
 13th Floor, Straight Block,  
 Ocean Centre, 5 Canton Rd.  
 Tsimshatsui, Kowloon  
 Hong Kong  
 Tel: +852 2737-7200  
 Fax: +852 2314-0061

National Semiconductor Japan Ltd.  
 Tel: 81-3-5620-6175  
 Fax: 81-3-5620-6179

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