SSD2828QN4

Advance Information

MIPI Master Bridge

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Copyright © 2013 **Solomon Systech Limited**

Appendix 1: IC Revision history of SSD2828 Specification

Version	Change Items	Effective Date
1.0	Initial release of Advance Information	16-Oct-12
1.1	- Modify the description of END and CO (Section 8.1.38) - Modify the timing for data latch in RGB timing (Section 14.4)	13-Dec-12
1.2	- Specify the prefix T in RGB timing (Section14.4)	09-Jan-13
1.3	- Modify RGB color arrangement (Table 6-3) - Update power up and power down sequence (Section 15 & Section 16) - Include current consumption of using VDDIO=3.3V (Section 13)	27-Mar-13

CONTENTS

1 GENERAL DESCRIPTION 9

2 FEATURES 10

2.1 REFERENCES 10
2.2 DEFINITIONS 10

3 ORDERING INFORMATION 11

4 BLOCK DIAGRAM 11

5 FUNCTIONAL DESCRIPTION 14

5.1 FUNCTIONAL BLOCKS 14
5.2 CLOCK AND RESET MODULE 14
5.3 EXTERNAL INTERFACE 15
5.4 PROTOCOL CONTROL UNIT (PCU) 15
5.5 PACKET PROCESSING UNIT (PPU) 15
5.6 ERROR CORRECTION CODE/ CYCLIC REDUNDANCY CHECK (ECC/CRC) 16
5.7 LONG AND COMMAND BUFFERS 16
5.8 INTERRUPT SIGNAL 16
5.9 D-PHY CONTROLLER 16
5.10 ANALOG TRANSCEIVER 16
5.11 INTERNAL PLL 17

6 SSD2828QN4 PIN ASSIGNMENT 18

7 PIN DESCRIPTION 20

8 COMMAND TABLE 23

8.1 REGISTER DESCRIPTION 25
8.1.1 Device Identification Register 25
8.1.2 RGB Interface Control Register 1 26
8.1.3 RGB Interface Control Register 2 27
8.1.4 RGB Interface Control Register 3 28
8.1.5 RGB Interface Control Register 4 29
8.1.6 RGB Interface Control Register 5 30
8.1.7 RGB Interface Control Register 6 31
8.1.8 Configuration Register 33
8.1.9 VC Control Register 35
8.1.10 PLL Control Register 36
8.1.11 PLL Configuration Register 37
8.1.12 Clock Control Register 38
8.1.13 Packet Size Control Register 1 39
8.1.14 Packet Size Control Register 2 40
8.1.15 Packet Size Control Register 3 41
8.1.16 Generic Packet Drop Register 42
8.1.17 Operation Control Register 43
8.1.18 Maximum Return Size Register 44
8.1.19 Return Data Count Register 45
8.1.20 ACK Response Status Register 46
8.1.21 Line Control Register 47
8.1.22 Interrupt Control Register 49
8.1.23 Interrupt Status Register 50
8.1.24 Error Status Register 52
8.1.25 Delay Adjustment Register 1 54
8.1.26 Delay Adjustment Register 2 55

8.1.27 Delay Adjustment Register 3 56
8.1.28 Delay Adjustment Register 4 57
8.1.29 Delay Adjustment Register 5 58
8.1.30 Delay Adjustment Register 6 59
8.1.31 HS TX Timer Register 1 60
8.1.32 HS TX Timer Register 2 61
8.1.33 LP RX Timer Register 1 62
8.1.34 LP RX Timer Register 2 63
8.1.35 TE Status Register 64
8.1.36 SPI Read Register 65
8.1.37 PLL Lock Register 66
8.1.38 Test Register 67
8.1.39 TE Count Register 69
8.1.40 Analog Control Register 70
8.1.41 Analog Control Register 2 71
8.1.42 Analog Control Register 3 72
8.1.43 Analog Control Register 4 73
8.1.44 Interrupt Output Control Register 74
8.1.45 RGB Interface Control Register 7 75
8.1.46 Lane Configuration Register 76
8.1.47 Delay Adjustment Register 7 77
8.1.48 Pull Control Register 1 78
8.1.49 Pull Control Register 2 80
8.1.50 Pull Control Register 3 81
8.1.51 CABC Brightness Control Register 1 82
8.1.52 CABC Brightness Control Register 2 83
8.1.53 CABC Brightness Status Register 84
8.1.54 Encoder Control Register 85
8.1.55 Video Sync Delay Register 86
8.1.56 Trimming Register 87
8.1.57 GPIO1 Register 89
8.1.58 GPIO2 Register 91
8.1.59 DLYA01 Register 93
8.1.60 DLYA23 Register 94
8.1.61 DLYB01 Register 95
8.1.62 DLYB23 Register 96
8.1.63 DLYC01 Register 97
8.1.64 DLYC23 Register 98
8.1.65 Analog Control Register 5 99
8.1.66 Read Register 101

9 CONFIGURATION 102

9.1 LANE MANAGEMENT 102
9.2 USE CASES 103
9.2.1 RGB + SPI Interface 103
9.2.2 MIPI DC Characteristics 105
9.2.3 High Speed Clock Transmission 106
9.2.4 Data Lane State Flow 106
9.2.5 High Speed Data Transmission 107
9.2.6 Bi-Directional Data Lane Turnaround 109
9.2.7 Escape Mode 109
9.2.8 Low Power Data Transmission 111
9.2.9 Reset Trigger 112
9.2.10 Tearing Effect 113
9.2.11 Acknowledge 114
9.2.12 Packet Transmission 115
9.2.13 HS Transmission Example 115
9.2.14 General Packet Structure 116
9.2.15 Long Packet Format 116
9.2.16 Short Packet Structure 117

9.2.17 Data Identifier (DI) *117*
9.2.18 Victual Channel Identifier (VC) *118*
9.2.19 Data Type (DT) *118*
9.3 OPERATING MODES 122
9.3.2 State machine operation *135*
9.3.3 D-PHY operation *136*
9.3.4 Analog Transceiver *137*
9.3.5 PLL *137*
9.3.6 Clock Source Example *138*

10 EXTERNAL INTERFACE 139

10.1 SPI INTERFACE 8 BIT 4 WIRE 139
10.2 SPI INTERFACE 8 BIT 3 WIRE 141
10.2.1 3 or 4 wires 8bit SPI read back sequence for 0xFF register which is stored MIPI read back data 143
10.3 SPI INTERFACE 24 BIT 3 WIRE 145
10.3.1 3 wires 24bit SPI read back sequence for 0xFF register which is stored MIPI read back data 147

11 MAXIMUM RATINGS 149

12 RECOMMENDED OPERATING CONDITIONS 150

13 DC CHARACTERISTICS 151

14 AC CHARACTERISTICS 153

14.1 8 BIT 4 WIRE SPI INTERFACE TIMING 154
14.2 8 BIT 3 WIRE SPI INTERFACE TIMING 155
14.3 24 BIT 3 WIRE SPI INTERFACE TIMING 156
14.4 RGB INTERFACE TIMING 157
14.5 RESET TIMING 158
14.6 TX_CLK TIMING 158

15 POWER UP SEQUENCE 159

16 POWER OFF SEQUENCE 160

17 EXAMPLE FOR SYSTEM SLEEP IN AND OUT 161

18 SERIAL LINK DATA ORDER 162

19 PACKAGE INFORMATION 165

19.1 DIMENSION FOR SSD2828QN4 165

TABLES

TABLE 3-1: ORDERING INFORMATION 11
TABLE 6-1: SSD2828QN4 PINOUT DIAGRAM – 68 QFN-EP (TOP VIEW) 18
TABLE 6-2: SSD2828QN4 PIN ASSIGNMENT – 68 QFN-EP (TOP VIEW) 19
TABLE 6-3: SSD2828QN4 RGB DATA ARRANGEMENT 19
TABLE 7-1: MIPI PINS 20
TABLE 7-2: INTERFACE LOGIC PINS 21
TABLE 7-3: MISCELLANEOUS PINS 22
TABLE 8-1: SSD2828 REGISTER SUMMARY 23
TABLE 8-2: DEVICE IDENTIFICATION REGISTER DESCRIPTION 25
TABLE 8-3: RGB INTERFACE CONTROL REGISTER 1 DESCRIPTION 26
TABLE 8-4: RGB INTERFACE CONTROL REGISTER 2 DESCRIPTION 27
TABLE 8-5: RGB INTERFACE CONTROL REGISTER 3 DESCRIPTION 28
TABLE 8-6: RGB INTERFACE CONTROL REGISTER 4 DESCRIPTION 29
TABLE 8-7: RGB INTERFACE CONTROL REGISTER 5 DESCRIPTION 30
TABLE 8-8: RGB INTERFACE CONTROL REGISTER 6 DESCRIPTION 31
TABLE 8-9: CONFIGURATION REGISTER DESCRIPTION 33
TABLE 8-10: VC CONTROL REGISTER DESCRIPTION 35
TABLE 8-11: PLL CONTROL REGISTER DESCRIPTION 36
TABLE 8-12: PLL CONFIGURATION REGISTER DESCRIPTION 37
TABLE 8-13: CLOCK CONTROL REGISTER DESCRIPTION 38
TABLE 8-14: PACKET SIZE CONTROL REGISTER 1 DESCRIPTION 39
TABLE 8-15: PACKET SIZE CONTROL REGISTER 2 DESCRIPTION 40
TABLE 8-16: PACKET SIZE CONTROL REGISTER 3 DESCRIPTION 41
TABLE 8-17: GENERIC PACKET DROP REGISTER DESCRIPTION 42
TABLE 8-18: OPERATION CONTROL REGISTER DESCRIPTION 43
TABLE 8-19: MAXIMUM RETURN SIZE REGISTER DESCRIPTION 44
TABLE 8-20: RETURN DATA COUNT REGISTER DESCRIPTION 45
TABLE 8-21: ACK RESPONSE STATUS REGISTER DESCRIPTION 46
TABLE 8-22: LINE CONTROL REGISTER DESCRIPTION 47
TABLE 8-23: INTERRUPT CONTROL REGISTER DESCRIPTION 49
TABLE 8-24: INTERRUPT STATUS REGISTER DESCRIPTION 50
TABLE 8-25: ERROR STATUS REGISTER DESCRIPTION 52
TABLE 8-26: DELAY ADJUSTMENT REGISTER 1 DESCRIPTION 54
TABLE 8-27: DELAY ADJUSTMENT REGISTER 2 DESCRIPTION 55
TABLE 8-28: DELAY ADJUSTMENT REGISTER 3 DESCRIPTION 56
TABLE 8-29: DELAY ADJUSTMENT REGISTER 4 0/1 DESCRIPTION 57
TABLE 8-30: DELAY ADJUSTMENT REGISTER 5 DESCRIPTION 58
TABLE 8-31: DELAY ADJUSTMENT REGISTER 6 DESCRIPTION 59
TABLE 8-32: HS TX TIMER REGISTER 1 DESCRIPTION 60
TABLE 8-33: HS RX TIMER REGISTER 2 DESCRIPTION 61
TABLE 8-34: LP TX TIMER REGISTER 1 DESCRIPTION 62
TABLE 8-35: LP TX TIMER REGISTER 2 DESCRIPTION 63
TABLE 8-36: TE STATUS REGISTER DESCRIPTION 64
TABLE 8-37: SPI READ REGISTER DESCRIPTION 65
TABLE 8-38: PLL LOCK REGISTER DESCRIPTION 66
TABLE 8-39: TEST REGISTER DESCRIPTION 67
TABLE 8-40: TE COUNT REGISTER DESCRIPTION 69
TABLE 8-41: ANALOG CONTROL 1 REGISTER DESCRIPTION 70
TABLE 8-42: ANALOG CONTROL REGISTER 2 DESCRIPTION 71
TABLE 8-43: ANALOG CONTROL REGISTER 3 DESCRIPTION 72
TABLE 8-44: ANALOG CONTROL REGISTER 4 DESCRIPTION 73
TABLE 8-45: INTERRUPT OUTPUT CONTROL REGISTER DESCRIPTION 74
TABLE 8-46: RGB INTERFACE CONTROL REGISTER 7 DESCRIPTION 75
TABLE 8-47: LANE CONFIGURATION REGISTER DESCRIPTION 76
TABLE 8-48: DELAY ADJUSTMENT REGISTER 7 DESCRIPTION 77
TABLE 8-49: PULL CONTROL REGISTER 1 DESCRIPTION 78
TABLE 8-50: PULL CONTROL REGISTER 2 DESCRIPTION 80
TABLE 8-51: PULL CONTROL REGISTER 3 DESCRIPTION 81

TABLE 8-52: CABC BRIGHTNESS CONTROL REGISTER 1 DESCRIPTION 82
TABLE 8-53: CABC BRIGHTNESS CONTROL REGISTER 2 DESCRIPTION 83
TABLE 8-54: CABC BRIGHTNESS STATUS REGISTER DESCRIPTION 84
TABLE 8-55: ENCODER CONTROL REGISTER DESCRIPTION 85
TABLE 8-56: VIDEO SYNC DELAY REGISTER DESCRIPTION 86
TABLE 8-57: TRIMMING REGISTER DESCRIPTION 87
TABLE 8-58: GPIO1 REGISTER DESCRIPTION 89
TABLE 8-59: GPIO1 REGISTER DESCRIPTION 91
TABLE 8-60: DLYA01 REGISTER DESCRIPTION 93
TABLE 8-61: DLYA23 REGISTER DESCRIPTION 94
TABLE 8-62: DLYB01 REGISTER DESCRIPTION 95
TABLE 8-63: DLYB23 REGISTER DESCRIPTION 96
TABLE 8-64: DLYC01 REGISTER DESCRIPTION 97
TABLE 8-65: DLYC23 REGISTER DESCRIPTION 98
TABLE 8-66: ACR5 REGISTER DESCRIPTION 99
TABLE 8-67: READ REGISTER DESCRIPTION 101
TABLE 9-1: SSD2828 LANE MANAGEMENT 102
TABLE 9-2: OPERATION DURING VIDEO MODE BLLP PERIOD 104
TABLE 9-3: DSI STATE CODE AND DC CHARACTERISTICS 105
TABLE 9-4: DATA LANE MODE ENTERING/EXITING SEQUENCES 106
TABLE 9-5: START-OF-TRANSMISSION SEQUENCE 107
TABLE 9-6: END-OF-TRANSMISSION SEQUENCE 107
TABLE 9-7: MIPI ESCAPE MODE ENTRY CODE 110
TABLE 9-8: DATA TYPES FOR PROCESSOR-SOURCED PACKETS 118
TABLE 9-9: DATA TYPES FOR PERIPHERAL-SOURCED PACKETS 119
TABLE 9-10: PLL SETTING FOR NON-BURST MODE (PLL REFERENCE USING PCLK) 123
TABLE 9-11: PLL SETTING FOR NON-BURST MODE (PLL REFERENCE USING TX_CLK) 123
TABLE 9-12: PLL SETTING FOR BURST MODE 124
TABLE 9-13: MIPI ERROR REPORT 132
TABLE 11-1: MAXIMUM RATINGS (VOLTAGE REFERENCED TO V_{SS}) 149
TABLE 12-1: RECOMMENDED OPERATING CONDITIONS 150
TABLE 13-1: DC CHARACTERISTICS 151
TABLE 13-2: HS TRANSMITTER DC CHARACTERISTICS 152
TABLE 13-3: LP TRANSMITTER DC CHARACTERISTICS 152
TABLE 13-4: LP RECEIVER DC CHARACTERISTICS 152
TABLE 14-1: 8 BIT 4 WIRE SPI INTERFACE TIMING CHARACTERISTICS 154
TABLE 14-2: 8 BIT 3 WIRE SPI INTERFACE TIMING CHARACTERISTICS 155
TABLE 14-3: 24 BIT 3 WIRE SPI INTERFACE TIMING CHARACTERISTICS 156
TABLE 14-4: RGB INTERFACE TIMING CHARACTERISTICS 157
TABLE 14-5: RESET TIMING 158
TABLE 14-6: TX_CLK TIMING CHARACTERISTICS 158

FIGURES

FIGURE 4-1: OVERVIEW OF DISPLAY SYSTEM USING SSD2828 11
FIGURE 4-2: SSD2828 INTERFACE DIAGRAM 12
FIGURE 4-3: BLOCK DIAGRAM 13
FIGURE 5-1: THE CLOCKING SCHEME OF SSD2828 14
FIGURE 8-1: TIMING FOR DELAY CALCULATION 54
FIGURE 8-2: TIMING FOR DELAY CALCULATION 55
FIGURE 8-3: T_{WAKEUP} PERIOD DELAY CALCULATION 58
FIGURE 8-4: TIMING FOR DELAY CALCULATION 59
FIGURE 9-1: SSD2828 WITH RGB AND SPI INTERFACE 103
FIGURE 9-2: MIPI LINE LEVELS 105
FIGURE 9-3: SWITCHING THE CLOCK LANE BETWEEN HIGH SPEED MODE AND LOW-POWER MODE 106
FIGURE 9-4: HIGH-SPEED DATA TRANSMISSION IN BURSTS 108
FIGURE 9-5: TURNAROUND PROCEDURE 109
FIGURE 9-6: LOW POWER DATA TRANSMISSION 111
FIGURE 9-7: TRIGGER – RESET COMMAND IN ESCAPE MODE 112
FIGURE 9-8: TEARING EFFECT COMMAND IN ESCAPE MODE 113
FIGURE 9-9: ACKNOWLEDGE COMMAND IN ESCAPE MODE 114
FIGURE 9-10: TWO DATA TRANSMISSION MODE (SEPARATE, SINGLE) 115
FIGURE 9-11: ONE LANE DATA TRANSMISSION EXAMPLE 115
FIGURE 9-12: TWO LANE HS TRANSMISSION EXAMPLE 115
FIGURE 9-13: ENDIAN EXAMPLE (LONG PACKET) 116
FIGURE 9-14: LONG PACKET STRUCTURE 116
FIGURE 9-15: SHORT PACKET STRUCTURE 117
FIGURE 9-16: DATA INDENTIFIER STRUCTURE 117
FIGURE 9-17: 16-BIT PER PIXEL RGB COLOR FORMAT, LONG PACKET FOR MIPI INTERFACE 120
FIGURE 9-18: 18-BIT PER PIXEL– RGB COLOR FORMAT, LONG PACKET FOR MIPI INTERFACE 120
FIGURE 9-19: 18-BIT PER PIXEL IN THREE BYTES – RGB COLOR FORMAT, LONG PACKET FOR MIPI INTERFACE 121
FIGURE 9-20: 24-BIT PER PIXEL – RGB COLOR FORMAT, LONG PACKET FOR MIPI INTERFACE 121
FIGURE 9-21: ILLUSTRATION OF RGB INTERFACE PARAMETERS FOR NON-BURST MODE WITH SYNC PULSES 122
FIGURE 9-22: ILLUSTRATION OF RGB INTERFACE PARAMETERS FOR NON-BURST MODE WITH SYNC EVENTS AND BURST MODE 123
FIGURE 9-23: NON-BURST MODE MIPI STRUCTURE 124
FIGURE 9-24: BURST MODE MIPI STRUCTURE 125
FIGURE 9-25: ACKNOWLEDGEMENT HANDLING AFTER NON-READ COMMAND 130
FIGURE 9-26: ACKNOWLEDGEMENT HANDLING AFTER READ COMMAND 131
FIGURE 9-27: ILLUSTRATION OF INTERRUPT LATENCY 134
FIGURE 10-1: ILLUSTRATION OF WRITE OPERATION FOR 8 BIT 4 WIRE INTERFACE 140
FIGURE 10-2: ILLUSTRATION OF READ OPERATION FOR 8 BIT 4 WIRE INTERFACE 140
FIGURE 10-3: ILLUSTRATION OF WRITE OPERATION FOR 8 BIT 3 WIRE INTERFACE 141
FIGURE 10-4: ILLUSTRATION OF READ OPERATION FOR 8 BIT 3 WIRE INTERFACE 142
FIGURE 10-5: ILLUSTRATION OF WRITE OPERATION FOR 24 BIT 3 WIRE INTERFACE 145
FIGURE 10-6: ILLUSTRATION OF READ OPERATION FOR 24 BIT 3 WIRE INTERFACE 146
FIGURE 14-1: 8 BIT 4 WIRE SPI INTERFACE TIMING DIAGRAM 154
FIGURE 14-2: 8 BIT 3 WIRE SPI INTERFACE TIMING DIAGRAM 155
FIGURE 14-3: 24 BIT 3 WIRE SPI INTERFACE TIMING DIAGRAM 156
FIGURE 14-4: RGB INTERFACE TIMING DIAGRAM 157
FIGURE 14-5: TX_CLK TIMING DIAGRAM 158
FIGURE 18-1- PACKAGE INFORMATION 165
FIGURE 18-2- MARKING INFORMATION 166
FIGURE 18-3- TRAY INFORMATION 167

1 GENERAL DESCRIPTION

The SSD2828 IC is an MIPI master bridge chip that connects an application processor with traditional parallel LCD interface and an LCD driver with MIPI slave interface. The 2828 supports up to 1Gbps per lane speed with maximum 4 lanes using both parallel RGB interface and serial SPI interface.

2 FEATURES

- Support up to total of 4Gbps over the serial link
- Support up to 4 data lanes
- Number of signals is significantly reduced when compare to traditional RGB transfer
- Support up to 1920 pixels per display row in Video mode, up to 60hz refresh rate
- Support up to 2560 pixels per display row in Video mode, up to 30hz refresh rate
- Reduce power consumption and decrease EMI by using low amplitude signal over differential pair for serial data.
- Support parallel RGB interface (DPI 2.0) up to 24-bits
- Support serial SPI interface (DBI 2.0) up to 16-bits
- Support both command mode and video mode in MIPI DSI standard
- Support 16, 18 and 24-bit per pixel in Raw or Pixel mode for command mode transfer
- Support independent bi-directional data transfer (forward link in High Speed and Low Power mode and reverse link in Low Power mode) for each DSI
- Support Ultra low power mode in idle state for each DSI
- Support CABC function for Video mode
- On-chip PLL with variable output frequency
- MIPI analog and digital power supply: (MVDD) 1.2V +/-10%
- IO Power supply: (VDDIO) 1.8 ~ 3.3V +/-10%
- Support of MIPI standard DSI(v1.01.00), DCS(v1.02.00), D-PHY (v1.00.00)

2.1 References

- MIPI Alliance Standard for Display Serial Interface, version 1.01
- MIPI Alliance Standard for Display Command Set, version 1.02
- MIPI Alliance Standard for D-PHY, version 1.00
- MIPI Alliance Standard for Display Bus Interface, version 2.0
- MIPI Alliance Standard for Display Pixel Interface, version 2.0

2.2 Definitions

- HS High Speed
- SPI Type C interface option 1 of MIPI Alliance Standard for Display Bus Interface v2.0 (DBI-2)
- LP Low Power
- ULPS Ultra Low Power State
- RGB MIPI Alliance Standard for Display Pixel Interface v2.0 (DPI-2)
- VC Virtual Channel

3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	Package Form
SSD2828QN4	68 QFN-EP (in Tray form)

4 BLOCK DIAGRAM

The SSD2828 IC consists of the following modules.

- Clock and reset module
- External interface
- PCU (protocol control unit)
- PPU (packet processing unit)
- ECC/CRC
- Long and command buffers
- D-PHY controller
- Analog MIPI transceiver
- Internal PLL

The usage of SSD2828 is given in the diagram below.

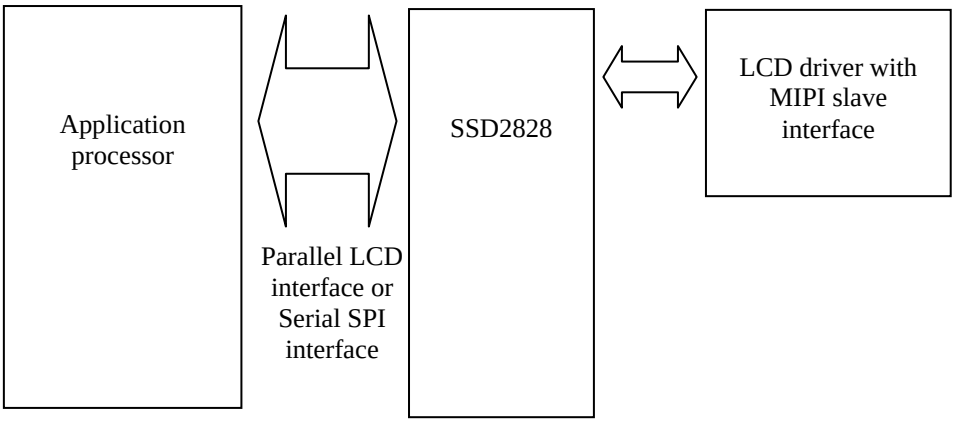


Figure 4-1: Overview of display system using SSD2828

Below is the interface diagram for the SSD2828 driving MIPI slave panel. Three types of interface are supported which are RGB and SPI interfaces. The interfaces can be selected through ps[1:0] pins.

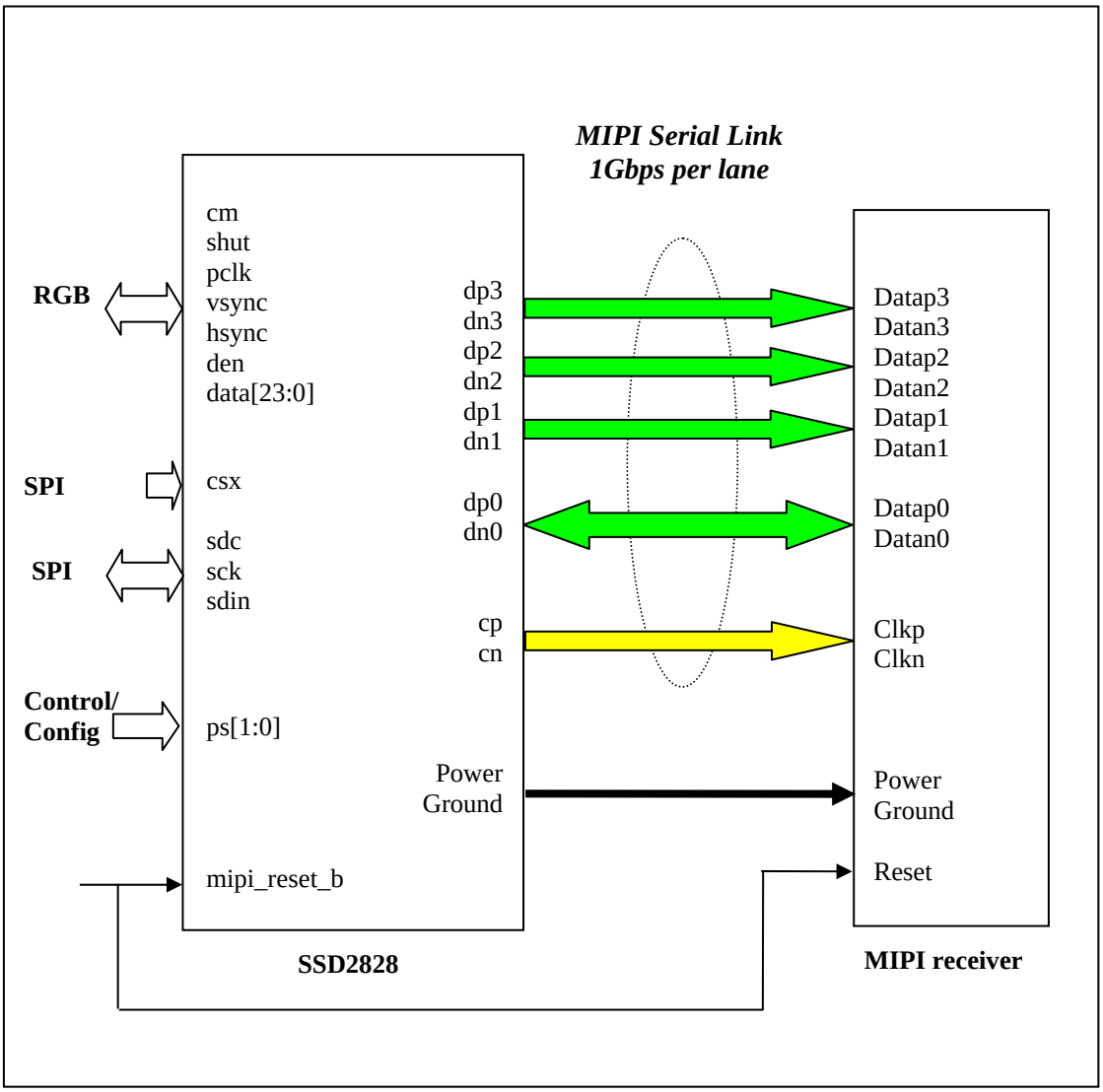
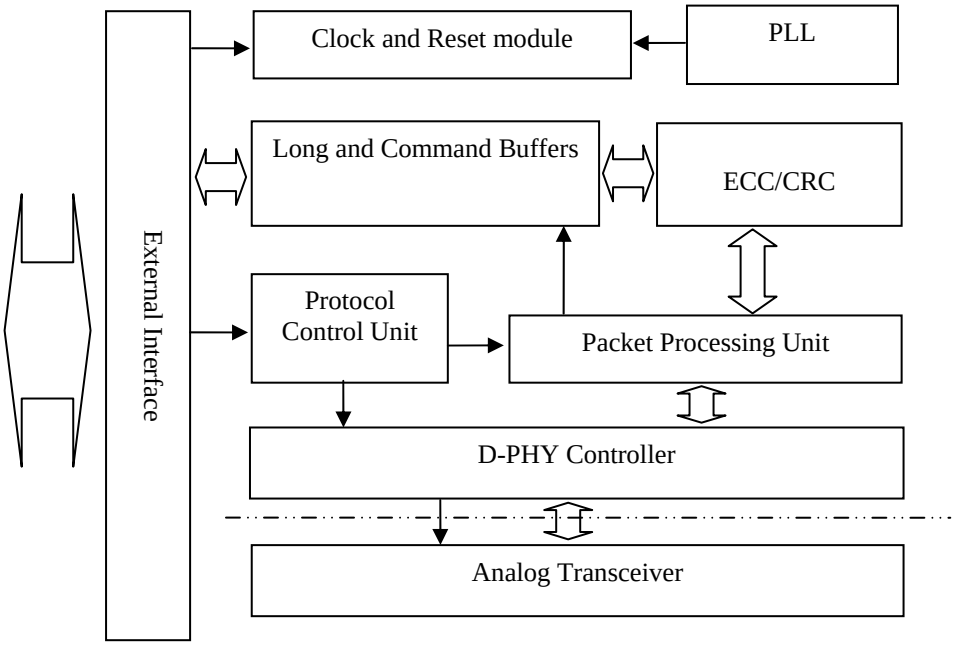


Figure 4-2: SSD2828 Interface Diagram

Figure 4-3: Block Diagram



5 FUNCTIONAL DESCRIPTION

5.1 Functional Blocks

5.2 Clock and Reset Module

The clock and reset module controls the generation of the operation clock for the whole system. There are two reference clock sources for the PLL. One is from the tx_clk and the other is from the pclk. The application processor can choose the reference clock for the PLL by program the **CSS**. The PLL output clock is used to generate the clock and data on the serial link during HS mode. The PLL frequency is the same as the data rate on 1 data lane. Hence, the PLL needs to be programmed according to the HS speed. Please refer to 9.3.5 for how to program the PLL.

NOTE: The default value of the **CSS** is 0 which selects the tx_clk. Hence, after power up, tx_clk must be present so that the registers can be programmed. If the application processor wants to switch the clock source, tx_clk must be provided first so that the **CSS** field can be programmed. After the **CSS** is programmed, the tx_clk can be turned off.

After powering up, the PLL is in sleep mode. The host needs to program the PLL setting before enable the PLL. If the host needs to switch the clock source of the PLL, it needs to put the PLL into sleep mode first. Afterwards, the host needs to program the PLL with new setting and enable the PLL. In both cases, the PLL needs a certain amount of time to lock the output clock frequency after being enabled. Hence, when the PLL is in sleep mode or when the PLL is enabled but not locked, the whole system is operating using the reference clock. After the PLL gets locked, the system is operating using the PLL output clock. Please see the diagram below for detailed clocking scheme. Since the reference clock is much slower than the PLL output clock, the host needs to operate at low speed too, before the PLL gets locked. Please refer to 14 for the requirement of low speed and normal speed.

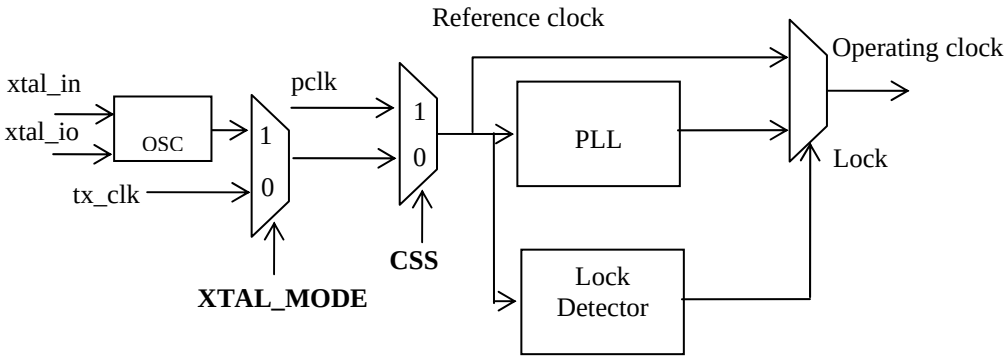


Figure 5-1: The Clocking Scheme of SSD2828

An output lock signal is provided for indication. This signal is connected to one of the interrupt source. The host can use the interrupt signal int to decide whether to operate at low speed or normal speed. The host can also poll the status bit **PLS** for the lock status.

Various clocks are mentioned in this document. Below is the explanation for each of them.

- Bit clock

It is the output clock from PLL. It is the clock source of all the clocks in the SSD2828.

- Nibble clock

It is a clock whose frequency is 1/4 of the bit clock.

- Byte clock

It is a clock whose frequency is 1/8 of the bit clock.

- Low power clock

It is a clock generated from byte clock. The divider value is given by field **LPD**. Please refer to 8.1.12. The low power clock period corresponds to 2 x T_{LPX}, as defined in MIPI D-PHY specification.

5.3 External Interface

The external interface is in charge of the communication with the application processor. It supports 2 types of interface, which are RGB and SPI.

- Parallel RGB interface for dumb display controller. The data bus width can be 16-bit, 18-bit and 24-bit.
- Serial SPI interface for smart display controller. The SPI interface supports 3 modes, which are 8-Bit 3 wire, 8-Bit 4 wire and 24-bit 3 wire. The 8-Bit 3 wire mode is the type C option 1 interface as specified in MIPI DBI 2.0. The 8-Bit 4 wire mode is the type C option 3 interface as specified in MIPI DBI 2.0.

The SPI interface is a completely separate interface from the other. Please see the pin table description for detailed scheme.

The SSD2828 supports one interface configuration.

- A combination of RGB and SPI interface

  This configuration is mainly used to drive a dumb display panel through the MIPI link. The RGB interface inputs the display data to the dumb display. The SPI interface inputs the data which is to configure the dumb display. Alternatively, the SPI interface can also input the data which is to drive a smart display panel, if the MIPI slave can control a dumb display panel and a smart one at the same time.

5.4 Protocol Control Unit (PCU)

The PCU is in charge of the handling of outgoing and incoming data stream. It has a state machine to decide what packet to be sent when an event comes in and how to react to the received packet.

5.5 Packet Processing Unit (PPU)

The PPU is in charge of packet assembly and disassembly. During transmission, it will form the packet according to the instruction from the PCU. During reception, it will extract necessary information from the packet and pass to the PCU.

5.6 Error Correction Code/ Cyclic Redundancy Check (ECC/CRC)

During transmission, the ECC/CRC module will generate the ECC or CRC for the outgoing bit stream.

During reception, the ECC/CRC module will check the correctness of the ECC and CRC field of the incoming stream.

If there is 1 bit of error in the data and ECC field, this error will be corrected by the ECC module. If there are more than 1 bit of error in the data and ECC field, the ECC module will detect the error and report it. If there is at least 1 bit of error in the data and CRC field, the CRC module will detect the error and report it.

5.7 Long and Command Buffers

In the forward direction, the SSD2828 supports DCS short write, DCS long write, Generic short write, Generic long write packets and all video packets. The internal buffers are used as temporary storage for incoming data, so that the application processor does not need to wait for the packet to be transmitted before writing the next one. All the command packets will be stored in the command buffers, except DCS command 2C/3C. All the long packets in video mode and the long packets with DCS command 2C/3C in command mode will be stored in the long buffer. After a complete packet is written into the buffer, the SSD2828 will send out the packet.

The command buffer can contain one or multiple packets, up to the size of 1024 bytes. As long as 1 complete packet is received, the state machine will instructs the D-PHY Controller to send out the packet.

Each long buffer can contain, maximum, 2 packets.

For each buffer, there are 2 status bits associated. One is buffer empty and the other is buffer available. Buffer empty means there is no packet in the buffer. Buffer available means that there is space to hold at least one packet. The buffer status can be reflected to the application processor through interrupt signal.

5.8 Interrupt signal

An interrupt signal is provided to trigger the application processor for certain event in the SSD2828. The events include internal long or command buffer empty, internal long or command buffer available, data ready for read back, acknowledgement response from MIPI slave, BTA response from the MIPI slave, time out, and packet operation ready. Please see the interrupt register description and 9.3.1.6 for more details.

5.9 D-PHY Controller

The D-PHY controller is in charge of the communication with the analog transceiver. During transmission, it receives data from PPU and informs the analog transmitter how to transmit. During reception, it receives data from analog receiver and passes the data to the PPU for further processing. At the same time, it is also performing the handshaking process, such as, bus turn around and switching between different modes.

5.10 Analog Transceiver

It consists of 4 data lane controllers and 1 clock lane controller. 1 of the data lane controllers is capable of providing reverse transmission.

5.11 Internal PLL

The internal PLL will generate the required high speed clock for the whole system operation. The input reference clock can come from either the tx_clk (_XIN, _XIO) or the pclk.

6 SSD2828QN4 Pin Assignment

Table 6-1: SSD2828QN4 Pinout Diagram – 68 QFN-EP (Top view)

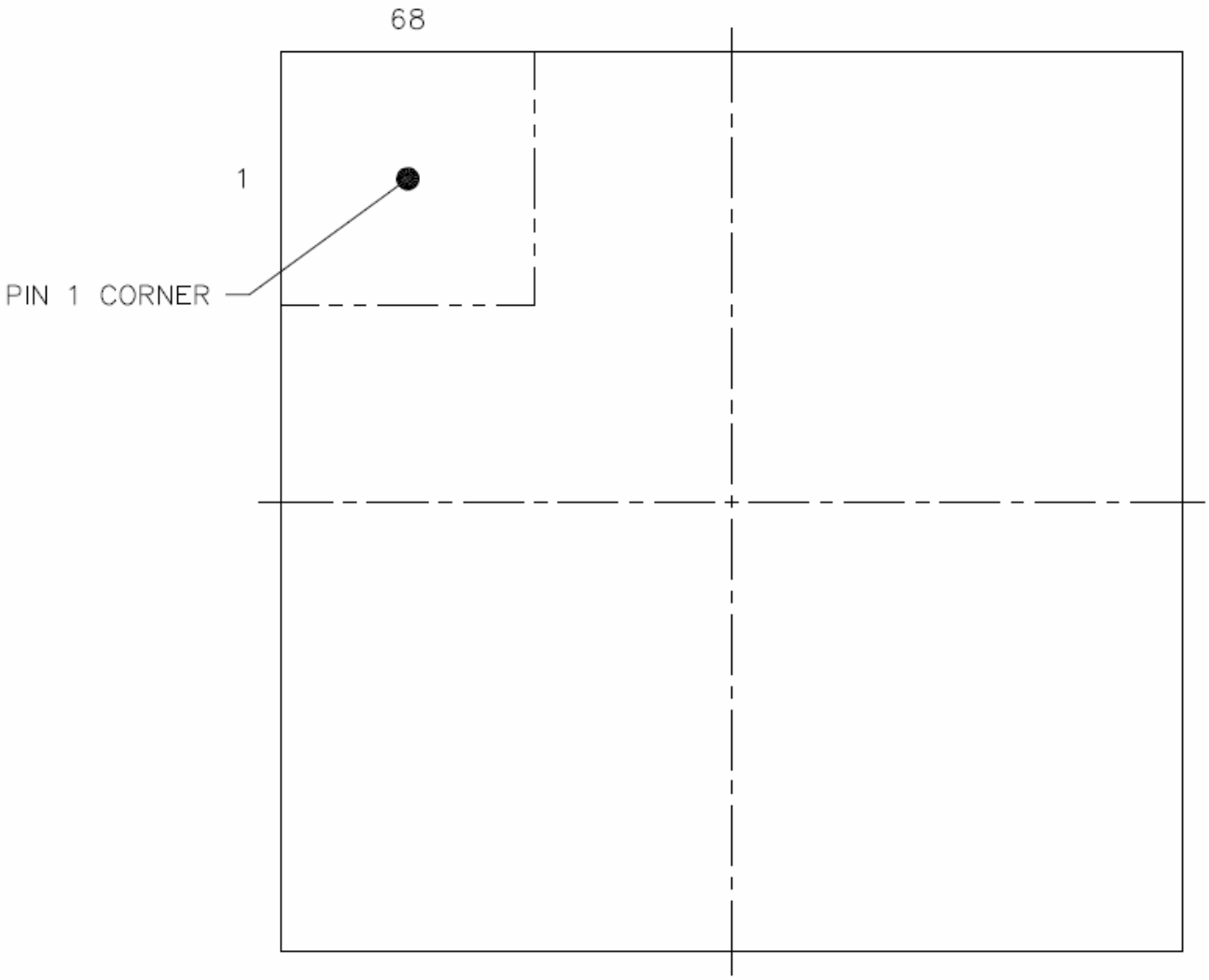


Table 6-2: SSD2828QN4 Pin Assignment – 68 QFN-EP (Top view)

QFN pin #	Net name	QFN pin #	Net name
1	DATAP0	35	DATA0
2	DATAN0	36	DATA1
3	GND	37	DATA2
4	DATAP1	38	DATA3
5	DATAN1	39	DATA4
6	GND	40	DATA5
7	CLKP	41	DATA6
8	CLKN	42	DATA7
9	GND	43	DATA8
10	DATAP2	44	DATA9
11	DATAN2	45	DATA10
12	GND	46	DATA11
13	DATAP3	47	DATA12
14	DATAN3	48	DATA13
15	MVDD	49	DATA14
16	VDDIO	50	DATA15
17	PS0	51	DATA16
18	PS1	52	DATA17
19	NC	53	DATA18
20	NC	54	DATA19
21	NC	55	DATA20
22	RESET	56	DATA21
23	SDO	57	DATA22
24	SDI	58	DATA23
25	SCK	59	CSX0
26	SDC	60	MVDD
27	SHUT	61	SYS_CLK_OUT
28	DEN	62	TX_CLK_XIO
29	HSYNC	63	TX_CLK_XIN
30	PCLK	64	VDDIO
31	MVDD	65	GND
32	GND	66	MVDD
33	VDDIO	67	GND
34	VSYNC	68	VDDIO

Table 6-3: SSD2828QN4 RGB data arrangement

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
24bpp	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18bpp	X	X	X	X	X	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16bpp	X	X	X	X	X	X	X	X	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

7 Pin Description

SSD2828 Pin Function Description

Key:

I = Input
O =Output
I/O = Bi-directional (input/output)
P = Power pin
GND = System VSS

Table 7-1: Power Supply Pins

Name	Type	Connect to	Function	Description	When not in use
GND	P	GND	Ground of Power Supply	Ground for IC	-
MVDD	P	Power	Power for Analog/Digital Circuits and PLL Circuit	Power supply for the internal analog/digital circuit and PLL circuit. (1.2V +/-10%)	-
VDDIO			Power for IO and Digital Interface Circuits	Power supply for IO and digital interface circuit. (1.8~3.3V +/-10%)	-

Table 7-1: MIPI Pins

Name	Type	Connect to	Function	Description	When not in use
CLKP0	O	MIPI Rx	MIPI Signals	Positive differential clock signal for DSI_0	Open
CLKN0				Negative differential clock signal for DSI_0	
DATAP0	I/O			Positive differential data signal 0 for DSI_0	
DATAN0				Negative differential data signal 0 for DSI_0	
DATAP1	O			Positive differential data signal 1 for DSI_0	
DATAN1				Negative differential data signal 1 for DSI_0	
DATAP2	O			Positive differential data signal 2 for DSI_0	
DATAN2				Negative differential data signal 2 for DSI_0	
DATAP3	O			Positive differential data signal 3 for DSI_0	
DATAN3				Negative differential data signal 3 for DSI_0	

Table 7-2: Interface Logic Pins

Name	Type	Connect to	Function	Description	When not in use
DATA[23:0]	I/O	AP	RGB Interface	RGB data for RGB interface	Open
VSYNC	I			VSYNC for RGB interface	VDDIO or GND
PCLK				PCLK for RGB interface	VDDIO or GND
DEN				DEN for RGB interface	VDDIO or GND
HSYNC				HSYNC for RGB interface	VDDIO or GND
SDC			SPI Interface	Data or command for SPI interface (for 8 bit 4 wire)	VDDIO or GND
CSX0				Chip select of DSI_0 for SPI interface	VDDIO
SCK				Serial clock for SPI interface (for 8 bit 3 wire, 8 bit 4 wire, 24 bit 3 wire)	VDDIO or GND
SDI				Serial data input for SPI interface (for 8 bit 3 wire, 8 bit 4 wire, 24 bit 3 wire)	VDDIO or GND
SDO	O	-		Serial data output for SPI interface (for 8 bit 3 wire, 8 bit 4 wire, 24 bit 3 wire)	Open

Table 7-3: Miscellaneous Pins

Name	Type	Connect to	Function	Description	When not in use
SHUT	I	VDDIO or GND	Control Signal	Shutdown signal of RGB interface (to put the driver into sleep mode). - 1: The panel is shut down (Sending 22h packet when SHUT changes from "0" → "1" in video mode) - 0: The panel is operating (Sending 32h packet at the beginning of video mode automatically)	VDDIO
PS[1:0]				Interface selection signal PS[1:0] is for SPI interface - 00: 3 wire 24 bit SPI interface - 01: 3 wire 8 bit SPI interface - 10: 4 wire 8 bit SPI interface - 11: SSL internal test mode	GND
TX_CLK_XIN		External CLK		Input system clock. 8 ~ 30MHz --- Input crystal range for the crystal oscillator input. 8Mhz to 30Mhz	-
TX_CLK_XIO	I/O	-		Input system clock. Open. --- Input crystal range for the crystal oscillator input. 8Mhz to 30Mhz	Open
SYS_CLK_OUT	O	-		Output system clock for MIPI slave	Open
RESET	I	VDDIO or GND		Active low reset signal to the chip	VDDIO

8 COMMAND TABLE

Table 8-1: SSD2828 Register Summary

Offset	Name	Mnemonic	Reset Value
0xB0	Device Identification Register	DIR	0x2828
0xB1	RGB Interface Control Register 1	VICR1	0x020A
0xB2	RGB Interface Control Register 2	VICR2	0x0214
0xB3	RGB Interface Control Register 3	VICR3	0x0428
0xB4	RGB Interface Control Register 4	VICR4	0x0780
0xB5	RGB Interface Control Register 5	VICR5	0x0438
0xB6	RGB Interface Control Register 6	VICR6	0x0024
0xB7	Configuration Register	CFGR	0x0301
0xB8	VC Control Register	VCR	0x0045
0xB9	PLL Control Register	PCR	0x0000
0xBA	PLL Configuration Register	PLCR	0x8120
0xBB	Clock Control Register	CCR	0x0003
0xBC	Packet Size Control Register 1	PSCR1	0x0000
0xBD	Packet Size Control Register 2	PSCR2	0x0000
0xBE	Packet Size Control Register 3	PSCR3	0x0100
0xBF	Packet Drop Register	PDR	0x0000
0xC0	Operation Control Register	OCR	0x0000
0xC1	Maximum Return Size Register	MRSR	0x0001
0xC2	Return Data Count Register	RDCR	0x0000
0xC3	ACK Response Register	ARSR	0x0000
0xC4	Line Control Register	LCR	0x0000
0xC5	Interrupt Control Register	ICR	0x0080
0xC6	Interrupt Status Register	ISR	0xCF06
0xC7	Error Status Register	ESR	0x0000
0xC9	Delay Adjustment Register 1	DAR1	0x1402
0xCA	Delay Adjustment Register 2	DAR2	0x2803
0xCB	Delay Adjustment Register 3	DAR3	0x0416
0xCC	Delay Adjustment Register 4	DAR4	0x0A0A
0xCD	Delay Adjustment Register 5	DAR5	0x1000
0xCE	Delay Adjustment Register 6	DAR6	0x0405
0xCF	HS TX Timer Register 1	HTTR1	0x0000
0xD0	HS TX Timer Register 2	HTTR2	0x0010
0xD1	LP RX Timer Register 1	LRTR1	0x0000
0xD2	LP RX Timer Register 2	LRTR2	0x0010
0xD3	TE Status Register	TSR	0x0000
0xD4	SPI Read Register	LRR	0x00FA
0xD5	PLL Lock Register	PLLR	0x1450
0xD6	Test Register	TR	0x0005
0xD7	TE Count Register	TECR	0x0001
0xD8	Analog Control Register 1	ACR1	0x2020
0xD9	Analog Control Register 2	ACR2	0x64A0
0xDA	Analog Control Register 3	ACR3	0x99A4
0xDB	Analog Control Register 4	ACR4	0x8098
0xDC	Interrupt Output Control Register	IOCR	0x0000
0xDD	RGB Interface Control Register 7	VICR7	0x0000
0xDE	Lane Configuration Register	LCFR	0x0000
0xDF	Delay Adjustment Register 7	DAR7	0x0010
0xE0	Pull Control Register 1	PUCR1	0x5556
0xE1	Pull Control Register 2	PUCR2	0x6656
0xE2	Pull Control Register 3	PUCR3	0x0159

Offset	Name	Mnemonic	Reset Value
0xE9	CABC Brightness Control Register 1	CBCR1	0x0000
0xEA	CABC Brightness Control Register 2	CBCR2	0x6900
0xEB	CABC Brightness Status Register	CBSR	0x0000
0xEC	Encoder Control Register	ECR	0x7800
0xED	Video Sync Delay Register	VSDR	0x0002
0xEE	Trimming Register	TMR	0x0000
0xEF	GPIO Register 1	GPIO1	0x0000
0xF0	GPIO Register 2	GPIO2	0x0000
0xF1	DLYA01 Register	DLYA01	0x2020
0xF2	DLYA23 Register	DLYA23	0x2020
0xF3	DLYB01 Register	DLYB01	0x2020
0xF4	DLYB23 Register	DLYB23	0x2020
0xF5	DLYC01 Register	DLYC01	0x2020
0xF6	DLYC23 Register	DLYC23	0x2020
0xF7	Analog Control Register 5	ACR5	0x0000
0xFF	Read Register	RR	0x0000

8.1 Register Description

8.1.1 Device Identification Register

Offset Address

DIR **Device Identification Register** **0xB0**

BIT	15	14	13	12	11	10	9	8
NAME	**DIR[15:8]**							
TYPE	RO							
RESET	**0x28**							
BIT	7	6	5	4	3	2	1	0
NAME	**DIR[7:0]**							
TYPE	RO							
RESET	**0x28**							

Table 8-2: Device Identification Register Description

Name	Description	Setting
DIR Bit 15-0	**Device Identification Number**	0x2828

8.1.2 RGB Interface Control Register 1

Offset Address

VICR1 **RGB Interface Control Register 1** **0xB1**

BIT	15	14	13	12	11	10	9	8
NAME	**VSA**							
TYPE	RW							
RESET	0x02							
BIT	7	6	5	4	3	2	1	0
NAME	**HSA**							
TYPE	RW							
RESET	0x0A							

Table 8-3: RGB Interface Control Register 1 Description

Name	Description	Setting
VSA Bit 15-8	**Vertical Sync Active Period** – These bits specify the Vsync active period. The Vsync active period is from the Vsync falling edge to rising edge, in terms of Hsync pulses. It is only used in non-burst mode with Sync pulses. Please refer to 9.3 for more details.	The minimum value is 1.
HSA Bit 7-0	**Horizontal Sync Active Period** – These bits specify the Hsync active period. The Hsync active period is from the Hsync falling edge to rising edge, in terms of pclk. It is only used in non-burst mode with Sync pulses. Please refer to 9.3 for more details.	The minimum value is 1.

8.1.3 RGB Interface Control Register 2

Offset Address

VICR2 **RGB Interface Control Register 2** **0xB2**

BIT	15	14	13	12	11	10	9	8
NAME	**VBP**							
TYPE	RW							
RESET	0x02							
BIT	7	6	5	4	3	2	1	0
NAME	**HBP**							
TYPE	RW							
RESET	0x14							

Table 8-4: RGB Interface Control Register 2 Description

Name	Description	Setting
VBP Bit 15-8	**Vertical Back Porch Period** – These bits specify the vertical back porch period in terms of Hsync pulses. The vertical back porch period depends on the video mode setting. If the mode is non-burst mode with Sync pulses, it is from the Vsync rising edge to the Hsync of the first line of active display. If the mode is non-burst mode with Sync events, it is from the Vsync falling edge to the Hsync of the first line of active display. If the mode is burst mode, it is the same as the non-burst mode with Sync events. Please refer to 9.3 for more details.	
HBP Bit 7-0	**Horizontal Back Porch Period** – These bits specify the horizontal back porch period in terms of pclk. The horizontal back porch period depends on the non-burst mode setting. If the mode is non-burst mode with Sync pulses, it is from the Hsync rising edge to the start of the valid display pixel. If the mode is non-burst mode with Sync events, it is from the Hsync falling edge to the start of the valid display pixel. If the mode is burst mode, it is the same as the non-burst mode with Sync events. Please refer to 9.3for more details.	

8.1.4 RGB Interface Control Register 3

Offset Address

VICR3 **RGB Interface Control Register3** **0xB3**

BIT	15	14	13	12	11	10	9	8
NAME	**VFP**							
TYPE	RW							
RESET	0x04							
BIT	7	6	5	4	3	2	1	0
NAME	**HFP**							
TYPE	RW							
RESET	0x28							

Table 8-5: RGB Interface Control Register 3 Description

Name	Description	Setting
VFP Bit 15-8	**Vertical Front Porch Period** – These bits specify the vertical front porch period in terms of Hsync pulses. The vertical front porch period is from the first Hsync after the last line of active display to the next Vsync falling edge. Please refer to 9.3 for more details.	
HFP Bit 7-0	**Horizontal Front Porch Period** – These bits specify the horizontal front porch period in terms of pclk. The horizontal front porch period is from the end of the valid display pixel to the next Hsync falling edge. Please refer to 9.3 for more details.	

8.1.5 RGB Interface Control Register 4

Offset Address

VICR4 **RGB Interface Control Register 4** **0xB4**

BIT	15	14	13	12	11	10	9	8
NAME	**HACT[15:8]**							
TYPE	RW							
RESET	0x07							
BIT	7	6	5	4	3	2	1	0
NAME	**HACT[7:0]**							
TYPE	RW							
RESET	0x80							

Table 8-6: RGB Interface Control Register 4 Description

Name	Description	Setting
HACT Bit 15-0	**Horizontal Active Period** – These bits specify the horizontal active period in terms of pclk. During the horizontal active period, the den signal should always be high. Please refer to 9.3 for more details.	The maximum value is 0x0A00.

8.1.6 RGB Interface Control Register 5

Offset Address

VICR5 **RGB Interface Control Register 5** **0xB5**

BIT	15	14	13	12	11	10	9	8
NAME	**VACT[15:8]**							
TYPE	RW							
RESET	0x04							
BIT	7	6	5	4	3	2	1	0
NAME	**VACT[7:0]**							
TYPE	RW							
RESET	0x38							

Table 8-7: RGB Interface Control Register 5 Description

Name	Description	Setting
VACT Bit 15-0	**Vertical Active Period** – These bits specify the vertical active period in terms of Hsync pulses. Please refer to 9.3 for more details.	The minimum value is 1.

8.1.7 RGB Interface Control Register 6

Offset Address

VICR6 **RGB Interface Control Register6** **0xB6**

BIT	15	14	13	12	11	10	9	8
NAME	**VS_P**	**HS_P**	**PCLK_P**					**CBM**
TYPE	RW	RW	RW	RO	RO	RO	RO	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**NVB**	**NVD**	**BLLP**	**VCS**	**VM**		**VPF**	
TYPE	RW	RW	RW	RW	RW		RW	
RESET	0x0	0x0	0x1	0x0	0x1		0x0	

Table 8-8: RGB Interface Control Register 6 Description

Name	Description	Setting
VS_P Bit 15	**VS_P** – This bit control the polarity of the Vsync pulse input.	0 – Vsync Pulse is active low 1 – Vsync Pulse is active high
HS_P Bit 14	**HS_P** – This bit control the polarity of the Hsync pulse output.	0 – Hsync Pulse is active low 1 – Hsync Pulse is active high
PCLK_P Bit 13	**PCLK_P** – This bit control the polarity of the CM output.	0 – Data is launch at falling edge, SSD2828 latch data at rising edge 1 – Data is launch at rising edge, SSD2828 latch data at falling edge
Reserved Bit 12-9		
CBM Bit 8	**Compress Burst Mode Control –** If the mode is burst and this bit is 1, MIPITX will send video packet in compressed burst mode (i.e. no blanking packet after horizontal sync packet)	0 – Video with blanking packet. 1 - Video with no blanking packet.
NVB Bit 7	**Non Video Data Burst Mode Control –** This bit specifies how non video data will be interleaved with video data transmission in burst mode.	0 – Non video data will be transmitted during any BLLP period. 1 - Non video data will only be transmitted during vertical blanking period.
NVD Bit 6	**Non Video Data Transmission Control –**This bit specifies how non video data will be interleaved with video data transmission. Please refer to 9.2.1 for more details. The SSD2828 will send non video data (written from the SPI interface) during the vertical blanking period (non burst mode) or any **BLLP** period in burst mode (depends on **NVB** setting). The data can be sent either in high speed mode or low power mode. This bit selects which mode to use. If LP mode is selected, the data	0 – Non video data will be transmitted using HS mode. 1 – Non video data will be transmitted using LP mode.

Name	Description	Setting
	lane will enter LP mode for **BLLP** period, even if there is no non-video data to send. Please note that sending data in LP mode is much slower than HS mode. It is the responsibility of the host processor to make sure that the duration is long enough to finish the data transfer and the timing of Hsync and Vsync is not affected.	
BLLP Bit 5	**BLLP Control –** This bit specifies the SSD2828 operation during BLLP period. This bit takes effect only for non burst mode and **NVD** being 0. When the video mode is burst mode, the SSD2828 will not send any blanking packet during BLLP. It will enter LP mode. When **NVD** is 1 in non burst mode, the SSD2828 will stay in LP mode after sending the non video data (if there is any), until the BLLP period ends. When **NVD** is 0 in non burst mode, the SSD2828 will use this bit to decide whether to send blanking packet or enter LP mode after sending non video data (if there is any), until the **BLLP** period ends. Please note that entering and exiting from LP mode needs more time, as the speed of LP mode is slow. It is the responsibility of the host processor to make sure that the period is long enough to finish the data transfer and the timing of Hsync and Vsync is not affected.	0 – Blanking packet will be sent during BLLP period. 1 – LP mode will be used during BLLP period.
VCS Bit 4	**Video Clock Suspend –** This bit specifies the clock lane behavior. This bit is only applicable for burst mode. When the video mode is non burst mode, the clock lane will remain in HS mode all the time.	0 – The clock lane remains in HS mode, when there is no data to transmit. 1 – The clock lane enters LP mode when there is no data to transmit.
VM Bit 3-2	**Video Mode –** These bits specify the video mode the SSD2828 will use, when RGB interface is selected. Please refer to MIPI DSI for the definition of different modes.	00 – Non burst mode with sync pulses 01 – Non burst mode with sync events 10 – Burst mode 11 – Reserved
VPF Bit 1-0	**Video Pixel Format** – These bits specify the pixel format for video mode.	00 – 16bpp 01 – 18bpp, packed 10 – 18bpp, loosely packed 11 – 24bpp

24bpp	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18bpp	**X**	**X**	**X**	**X**	**X**	**X**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
16bpp	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

8.1.8 Configuration Register

Offset Address

CFGR	Configuration Register	0xB7

BIT	15	14	13	12	11	10	9	8
NAME					**TXD**	**LPE**	**EOT**	**ECD**
TYPE	RO	RO	RO	RO	RW	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x1	0x1
BIT	7	6	5	4	3	2	1	0
NAME	**REN**	**DCS**	**CSS**	**HCLK**	**VEN**	**SLP**	**CKE**	**HS**
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x1

Table 8-9: Configuration Register Description

Name	Description	Setting
Reserved Bit 15-12		
TXD Bit 11	**Transmit Disable –** This bit specifies whether the SSD2828 will disable the sending of MIPI Packets stored in the buffers. Software can enable **TXD**, fill out the buffers and then disable it to send all packets out in 1 burst.	0 – Transmit on 1 – Transmit halt
LPE Bit 10	**Long Packet Enable –** This bit specifies whether the SSD2828 will send out a Generic Long Write Packet or Generic Short Write Packet when the payload is no more than 2 bytes. It also specifies whether the SSD2828 will send out a DCS Long Write Packet or DCS Short Write Packet when the payload is no more than 1 byte.	0 – Short Packet 1 – Long Packet
EOT Bit 9	**EOT Packet Enable –** This bit specifies whether the SSD2828 will send out the EOT packet at the end of HS transmission or not.	0 – Do not send 1 – Send
ECD Bit 8	**ECC CRC Check Disable –** This bit specifies whether SSD2828 will perform ECC and CRC checking for the packets received from the MIPI slave.	0 – Enable 1 – Disable
REN Bit 7	**Read Enable –**This bit specifies whether the next operation is a write or read operation.	0 – Write operation 1 – Read operation
DCS Bit 6	**DCS Enable –** This bit specifies whether the packet to be sent is DCS packet or generic packet. This bit applies for both write and read operation.	0 – Generic packet (The packet can be any one of Generic Long Write, Generic Short Write, Generic Read packet, depending on the configuration.) 1 – DCS packet (The packet can be any one of DCS Long Write, DCS Short Write, DCS Read packet, depending on the configuration.)

Name	Description	Setting
CSS Bit 5	**Clock Source Select –** This bit selects the clock source for the PLL. Please refer to 5.2 for the system behavior when the clock source is switched. The **CSS** setting should be programmed only when **PEN** is 0. It has no effect when **PEN** is 1.	0 – The clock source is tx_clk 1 – The clock source is pclk
HCLK Bit 4	**HS Clock Disable –** This bit controls the clock lane behavior during the reverse direction communication. This bit takes effect only when **CKE** is 0 and **VEN** is 0.	0 – HS clock is enabled 1 – HS clock is disabled
VEN Bit 3	**Video Mode Enable** – This bit controls the video mode operation. Only after this bit is set to 1, video mode is enabled. This bit takes effect only when the interface setting is RGB + SPI. Please refer to 0 for the video mode operation.	0 – Video mode is disabled 1 – Video mode is enabled
SLP Bit 2	**Sleep Mode Enable –** This bit controls the sleep mode operation. Please refer to 9.3.2 for the sleep mode operation. When this bit is set to 1, the **HS** bit will be cleared to 0 automatically.	0 – Sleep mode is disabled 1 – Sleep mode is enabled. Only the register interface is active.
CKE Bit 1	**Clock Lane Enable –** This bit controls the clock lane mode when data lane enters LP mode.	0 – Clock lane will enter LP mode, if it is not in reverse direction communication. Clock lane will follow the setting of **HCLK**, if it is in reverse direction communication. 1 – Clock lane will enter HS mode for all the cases.
HS Bit 0	**HS Mode –** This bit controls whether the SSD2828 is using HS or LP mode to send data. This bit can be affected by the **SLP** bit value.	0 – LP mode 1 – HS mode

8.1.9 VC Control Register

Offset Address

VCR **VC Control Register** **0xB8**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**VCM**		**VCE**		**VC2**		**VC1**	
TYPE	RW		RW		RW		RW	
RESET	0x1		0x0		0x1		0x1	

Table 8-10: VC Control Register Description

Name	Description	Setting
Reserved Bit 15-8		
VCM Bit 7-6	**Virtual Channel ID for Maximum Return Size Packet –** These bits specify the VC ID for the Maximum Return Size Packet sent by SSD2828. This register field is included as the VC ID for this packet might be different from the VC ID for the packets carrying the actual data.	
VCE Bit 5-4	**Virtual Channel ID for EOT Packet –** These bits specify the VC ID for the EOT Packet sent by SSD2828. This register field is included as the VC ID for this packet might be different from the VC ID for the packets carrying the actual data.	
VC2 Bit 3-2	**Virtual Channel ID for SPI Interface –** These bits specify the VC ID for the packets written in through the SPI interface, when the interface setting is RGB + SPI This register field is included as the RGB + SPI interface can address two different LCD panels at the same time. The VC ID for the two panels is different.	
VC1 Bit 1-0	**Virtual Channel ID for RGB Interface –** These bits specify the VC ID for the packets written in through the RGB interface, when the interface is RGB + SPI	

8.1.10 PLL Control Register

Offset Address

PCR **PLL Control Register** **0xB9**

BIT	15	14	13	12	11	10	9	8
NAME	**SYSD**		**SYS_DIS**					
TYPE	RW		RW	RO	RO	RO	RO	RO
RESET	0x0		0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME								**PEN**
TYPE	RO	RO	RO	RO	RO	RO	RO	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-11: PLL Control Register Description

Name	Description	Setting
SYSD Bit 15-14	**SYS_clk Divider** – These bits give the divider value for generating the sys_clk output from the tx_clk or crystal input.	00 – Divide by 1 01 – Divide by 2 10 – Divide by 4 11 – Divide by 8
SYS_DIS Bit 13	**SYS_clk DISable** – This bit will shut off the Sys_clk signal output when enabled.	0 – Enable Sys_clk output 1 – Disable Sys_clk output
Reserved Bit 12-1		
PEN Bit 0	**PLL Enable** – This bit controls the PLL operation.	0 – PLL power down 1 – PLL enable

Remark: Frequency of PLL can only be changed during PEN = 0

8.1.11 PLL Configuration Register

Offset Address

PLCR **PLL Configuration Register** **0xBA**

BIT	15	14	13	12	11	10	9	8
NAME	**FR**			**MS**				
TYPE	RW		RO	RW				
RESET	0x2		0x0	0x01				
BIT	7	6	5	4	3	2	1	0
NAME	**NS**							
TYPE	RW							
RESET	0x20							

Table 8-12: PLL Configuration Register Description

Name	Description	Setting
FR Bit 15-14	**Frequency Range –** These bits select the range of the output clock. The **FR** setting should be programmed only when **PEN** is 0. It has no effect when **PEN** is 1.	00 – 62.5 < f_{OUT} < 125 01 – 126 < f_{OUT} < 250 10 – 251 < f_{OUT} < 500 11 – 501 < f_{OUT} < 1000
Reserved Bit 13		
MS Bit 12-8	**PLL Divider –** These bits specify the PLL pre-divider value, **MS**. The frequency of the phase detector, f_{REF} is determined by $f_{PRE} = f_{IN} / MS$ The input frequency, f_{IN} and phase detector frequency, f_{REF} should be between 5Mhz to 100Mhz. The **MS** setting should be programmed only when **PEN** is 0. It has no effect when **PEN** is 1.	- 0x00 : MS=1 - 0x01 : MS=1 - 0x02 : MS=2 … - 0x1F : MS=31
NS Bit 7-0	**PLL Multiplier** – These bits specify the PLL output frequency multiplier value, **NS**. The output frequency, f_{OUT} is determined by $f_{OUT} = f_{PRE} * NF$ The **NS** setting should be programmed only when **PEN** is 0. It has no effect when **PEN** is 1.	- 0x00 : NS=1 - 0x01 : NS=1 - 0x02 : NS=2 … - 0xFF : NS=255

e.g. TX_CLK = 10MHz, 0xBAh = 0x8028h

PLL = 40 x 10 / 1 = 400Mbps

8.1.12 Clock Control Register

Offset Address

CCR **Clock Control Register** **0xBB**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME			**LPD**					
TYPE	RO	RO	RW					
RESET	0x0	0x0	0x03					

Table 8-13: Clock Control Register Description

Name	Description	Setting
Reserved Bit 15-6		
LPD Bit 5-0	**LP Clock Divider** – These bits give the divider value for generating the LP mode clock from the byte clock.	0x0 – Divide by 1 0x1 – Divide by 2 … 0x3F – Divide by 64

Remark: e.g. LPD = 0x4

PLL = 400Mbps

LP clock = 400Mbps / LPD / 8 = 400 / 5 / 8 = 10MHz

8.1.13 Packet Size Control Register 1

Offset Address

PSCR1 **Packet Size Control Register1** **0xBC**

BIT	15	14	13	12	11	10	9	8
NAME	**TDC[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**TDC[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-14: Packet Size Control Register 1 Description

Name	Description	Setting
TDC Bit 15-0	**Transmit Data Count** – These bits set the total number of data bytes to be transmitted by the SSD2828 in the next operation. The SSD2828 will use the value in this field to decide what type of packet to send out. The settings of **TDC** and **PST**(0xBE) will configure the transfer mode into partition and non-partition mode when the command is 0x2C or 0x3C. Partition mode(**TDC** > **PST**) For DCS Long Write packet with DCS command being 0x2C or 0x3C, there is no limit in the maximum number of bytes to be transmitted in 1 write. The **PST** value can be set to maximum of 4096 bytes. The SSD2828 will auto insert 0x3C command at these boundaries. The maximum MCU speed at the input is 1/12 of the link frequency. Non-Partition mode(**TDC** <= **PST**) For DCS Long Write packet with DCS command being 0x2C or 0x3C, the maximum number of bytes to be transmitted in 1 write is 4096 bytes(**TDC**). In this mode, the **PST** value is the same or greater than the **TDC** value. The maximum MCU speed at the input is 1/8 of the link frequency. Please refer to 9.3.1.1 for more details.	Partition mode When **TDC** > **PST**. Non-partition mode When **TDC** <= **PST**. Maximum **TDC** = 4096(0x1000)

8.1.14 Packet Size Control Register 2

Offset Address

PSCR2 **Packet Size Control Register 2** **0xBD**

BIT	15	14	13	12	11	10	9	8
NAME	**TDC[31:24]**							
TYPE	RW							
RESET	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**TDC[23:16]**							
TYPE	RW							
RESET	0x0							

Table 8-15: Packet Size Control Register 2 Description

Name	Description	Setting
TDC[31:16] Bit 31-0	**Transmit Data Count** – Please see the description of Packet Size Control Register 1.	

8.1.15 Packet Size Control Register 3

Offset Address

PSCR2 **Packet Size Control Register 3** **0xBE**

BIT	15	14	13	12	11	10	9	8
NAME				**PST[12:8]**				
TYPE	RO	RO	RO	RW				
RESET	0x0	0x0	0x0	0x1				
BIT	7	6	5	4	3	2	1	0
NAME	**PST[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-16: Packet Size Control Register 3 Description

Name	Description	Setting
Reserved Bit 15-13		
PST Bit 12-0	**Packet Size Threshold** – These bits give the threshold value for partitioning the incoming long packet data into smaller packets. The partitioning only applies to the DCS Long Write packet with DCS command being 0x2C or 0x3C in Command mode(if_sel=1). The payload will be partitioned into multiple packets. The **PST** represents the threshold in term of bytes. The maximum MCU speed at the input is 1/10 of the link frequency. Please refer to 9.3.1.1 for more details.	The maximum value allowed is 4096 bytes. Program **PST<TDC** will allows auto insertion of 0x3C at the **PST** boundary(Partition mode). If the user tries to program a larger value than the maximum allowed value into this field, SSD2828 will cap the value to the maximum value. When the interface setting is 16-bit, the value in this field must be multiple of 2 bytes, or even number. If an odd number is written in, it will be automatically truncated to an even number. For example, 0x5 will be truncated to 0x4. When the interface setting is 24-bit, the value in this field must be in multiple of 3 bytes

8.1.16 Generic Packet Drop Register

Offset Address

GPDR **Generic Packet Drop Register** **0xBF**

BIT	15	14	13	12	11	10	9	8
NAME	**GPD[15:8]**							
TYPE	WO							
RESET	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**GPD[7:0]**							
TYPE	WO							
RESET	0x0							

Table 8-17: Generic Packet Drop Register Description

Name	Description	Setting
GPD Bit 15-0	**Generic Packet Drop** – This register is not a true register. It is the entry point for the internal buffer. The payload of the generic packets (Generic Short Write, Generic Long Write, and Generic Read) or the command and payload if DCS packet should be written into this register. The SSD2828 will send them out using the corresponding generic or DCS packet. DCS field of CFGR register will be used to determine the data drop into this register is for generic or DCS packet generation. The application processor can treat this register as an FIFO and continuously write data into it. When the interface is 16-bit, the width of this field is 16-bit. When the interface is 8-bit, the width of this field is 8-bit. Since the register is only the entry point of the internal buffer, the application processor is not able to read the data written into the buffer.	

8.1.17 Operation Control Register

Offset Address

OCR **Operation Control Register** **0xC0**

BIT	15	14	13	12	11	10	9	8
NAME								**RST**
TYPE	RO	RO	RO	RO	RO	RO	RO	RWAC
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME								**COP**
TYPE	RO	RO	RO	RO	RO	RO	RO	RWAC
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-18: Operation Control Register Description

Name	Description	Setting
Reserved Bit 15-9		
RST Bit 8	**Software Reset** - Writing a '1' to this bit will reset the entire module except SSD2828 local register setting. This bit will be cleared after the reset is completed. Wrting a '1' to this bit will cause the MIPI link enters TX stop state immediately and any outgoing MIPI packet will be terminated immediately.	0 – NOP 1 – Software Reset
Reserved Bit 7-1		
COP Bit 0	**Cancel Operation** – This bit is to cancel the current operation. When this bit is set to 1, the SSD2828 will still finish transmitting the current packet. (Otherwise, the serial link operation will lose sync.) Afterwards, the SSD2828 will stop any further transmission. It will clear its internal buffer such that all the data being written in and not sent out yet will be cleared. It will also bring the state machine to its initial state. Once this process is finished, the **COP** bit will be automatically set to 0. At the same time, the **PO** bit of the status register will be set to 1 too. At this stage, there is no data in the internal buffer. The application processor can start a new operation. This operation is not valid in video mode(**VEN=1)**.	0 – NOP 1 – Cancel the current operation

8.1.18 Maximum Return Size Register

Offset Address

MRSR **Maximum Return Size Register** **0xC1**

BIT	15	14	13	12	11	10	9	8
NAME	**MRS**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**MRS**							
TYPE	RW							
RESET	0x01							

Table 8-19: Maximum Return Size Register Description

Name	Description	Setting
MRS Bit 15-0	**Maximum Return Size** – These bits set the maximum return size of the read response packet returned by the MIPI slave. The SSD2828 will automatically send out the Set Maximum Return Size packet using the value in this field, before every read operation. It informs the MIPI slave about the limit of the SSD2828. The application processor does not need to program the register before every read operation, if the maximum return size does not change. However, the Set Maximum Return Size packet will always be sent.	

8.1.19 Return Data Count Register

Offset Address

RDCR **Return Data Count Register** **0xC2**

BIT	15	14	13	12	11	10	9	8
NAME	**RDC**							
TYPE	RO							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**RDC**							
TYPE	RO							
RESET	0x00							

Table 8-20: Return Data Count Register Description

Name	Description	Setting
RDC Bit 15-0	**Return Data Count** – These bits reflect the number of data bytes received from the MIPI slave read response packet. This register can only be updated by the SSD2828 hardware.	

8.1.20 ACK Response Status Register

Offset Address

ARSR **ACK Response Status Register** **0xC3**

BIT	15	14	13	12	11	10	9	8
NAME	**AR**							
TYPE	RO							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**AR**							
TYPE	RO							
RESET	0x00							

Table 8-21: ACK Response Status Register Description

Name	Description	Setting
AR Bit 15-0	**ACK Response** – These bits contain the ACK response from the MIPI slave. The register will be updated when ACK with Error Report packet is received. Otherwise, the value will be set to 0. The bits in this register follow the definition in MIPI DSI. This register can only be updated by the SSD2828 hardware.	

8.1.21 Line Control Register

Offset Address

LCR **Line Control Register** **0xC4**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME			**IBC**	**RT**	**RTB**	**FBC**	**FBT**	**FBW**
TYPE	RO	RO	RW	RWAC	RWAC	RWAC	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-22: Line Control Register Description

Name	Description	Setting
Reserved Bit 15-6		
IBC Bit 5	**Ignore Bus Contention** – This bit is to detect bus contention reported by the Analog Phy. If this bit is disabled, whenever bus contention is detected, the state machine will ignore it and continue sending new packet if available. If this bit is enabled, the state machine will halt further transmission.	0 – Detect Bus Contention from Analog Phy 1 – Ignore Bus Contention detected by Analog Phy
RT Bit 4	**Reset Trigger** – This bit is to send a Reset Trigger Message. When this bit is set to 1, the SSD2828 will send a Reset Trigger Message. It is recommended to enter LP mode and send this trigger message. If this bit is programmed during vertical active data is being sent on MIPI link, the reset trigger will be delayed to next vertical blanking period so that the reset trigger message will not disturb the video timing on the MIPI link. Once the Reset Trigger Message is sent out, **RT** bit will be automatically set to 0.	0 – NOP 1 – Send a Reset Trigger Message
RTB **Bit 3**	**Register Triggered BTA** – This bit automatically perform Bus Turnaround(BTA) when link is not used. When bus is returned back from the slave, the link will remains in Low Power state until a new request come in where HS bit determination the transfer mode.	0 – NOP 1 – Automatically perform BTA when link is available. In video mode, it will be sent at the next vertical blanking period.
FBC Bit 2	**Force Bus Contention –** This bit controls whether to force a bus contention on the data lane. This bit will be changed to 0, after the bus contention is not detected.	0 – NOP 1 – Drive the data lane to LP11 to force a bus contention.
FBT	**Force BTA TE –** This bit controls whether to	0 – No BTA after previous BTA

Name	Description	Setting
Bit 1	perform automatic BTA after previous BTA so as to get the TE response from MIPI slave.	1 – Perform automatic BTA after previous BTA
FBW Bit 0	**Force BTA After Write –** This bit controls whether to automatically generate a BTA after a write operation. It is only valid for write operation. After performing BTA, the bus authority has been passed to the MIPI slave. The SSD2828 is not able to send any data to the MIPI slave before the bus authority is passed back. It is the responsibility of the application processor to check the status of the bus before sending any data.	0 – Not BTA after the next write packet. 1 – Automatically perform BTA after the next write packet.

8.1.22 Interrupt Control Register

Offset Address

ICR **Interrupt Control Register** **0xC5**

BIT	15	14	13	12	11	10	9	8
NAME	**CBEE**	**CBAE**					**MLEE**	**MLAE**
TYPE	RW	RW	RO	RO	RO	RO	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**PLSE**	**LPTOE**	**HSTOE**		**ARRE**	**BTARE**	**POE**	**RDRE**
TYPE	RW	RW	RW	RO	RW	RW	RW	RW
RESET	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-23: Interrupt Control Register Description

Name	Description	Setting
CBEE Bit 15	**Command Buffer Empty Enable –** This bit enables the mapping of **CBE** interrupt to the int pin.	0 – Not enabled 1 – Enabled
CBAE Bit 14	**Command Buffer Available Enable –** This bit enables the mapping of **CBA** interrupt to the int pin.	0 – Not enabled 1 – Enabled
Reserved Bit 13-10		
MLEE Bit 9	**MCU Long Buffer Empty Enable –** This bit enables the mapping of **MLE** interrupt to the int pin.	0 – Not enabled 1 – Enabled
MLAE Bit 8	**MCU Long Buffer Available Enable –** This bit enables the mapping of M**LA** interrupt to the int pin.	0 – Not enabled 1 – Enabled
PLSE Bit 7	**PLL Lock Status Enable –** This bit enables the mapping of the **PLS** interrupt to the int pin.	0 – Not enabled 1 – Enabled
LPTOE Bit 6	**LP RX Time Out Enable –** This bit enables the mapping of the **LPTO** interrupt to the int pin.	0 – Not enabled 1 – Enabled
HSTOE Bit 5	**HS TX Time Out Enable –** This bit enables the mapping of the **HSTO** interrupt to the int pin.	0 – Not enabled 1 – Enabled
Reserved Bit 4		
ARRE Bit 3	**ACK Response Ready Enable –** This bit enables the mapping of **ARR** interrupt to the int pin.	0 – Not enabled 1 – Enabled
BTARE Bit 2	**BTA Response Enable –** This bit enables the mapping of the **BTAR** interrupt to the int pin.	0 – Not enabled 1 – Enabled
POE Bit 1	**Packet Operation Enable –** This bit enables the mapping of the **PO** interrupt to the int pin.	0 – Not enabled 1 – Enabled
RDRE Bit 0	**Read Data Ready Enable –** This bit enables the mapping of the **RDR** interrupt to the int pin.	0 – Not enabled 1 – Enabled

8.1.23 Interrupt Status Register

Offset Address

ISR **Interrupt Status Register** **0xC6**

BIT	15	14	13	12	11	10	9	8
NAME	**CBE**	**CBA**			**CST**	**DST**	**MLE**	**MLA**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x1	0x1	0x0	0x0	0x1	0x1	0x1	0x1
BIT	7	6	5	4	3	2	1	0
NAME	**PLS**	**LPTO**	**HSTO**	**ATR**	**ARR**	**BTAR**	**PO**	**RDR**
TYPE	RO	RW1C	RW1C	RW1C	RW1C	RW1C	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x1	0x1	0x0

Table 8-24: Interrupt Status Register Description

Name	Description	Setting
CBE Bit 15	**Command Buffer Empty –** This bit reflects the status of the internal command buffer of the SPI interface. If the command buffer is empty, this bit will be set to 1. The application processor can write up to the maximum size of the command buffer.	0 – The command buffer is not empty. 1 – The command buffer is empty.
CBA Bit 14	**Command Buffer Available –** This bit reflects the status of the internal command buffer of the SPI interface. If the command buffer is not full, this bit will be set to 1. The application processor can write at least 1 packet to the command buffer.	0 – The command buffer is full. 1 – The command buffer is not full.
Reserved Bit 13-12		
CST Bit 11	**Clock Lane Status –** This bit reflects the status at the MIPI Clock lane.	0 – Clock lane is not in LP-11. 1 – Clock lane is in LP-11.
DST Bit 10	**Data Lane Status –** This bit reflects the status at the MIPI Data lane.	0 – Data lane is not in LP-11. 1 – Data lane is in LP-11.
MLE Bit 9	Reserved	Reserved
MLA Bit 8	Reserved	Reserved
PLS Bit 7	**PLL Lock Status –** This bit reflects the status of the PLL. Before the PLL is locked, the whole system is running at the reference clock input of the PLL, as the PLL has no output before getting lock. Hence, the application processor must access the registers using slow speed.	0 – PLL has not been locked 1 – PLL has been locked
LPTO Bit 6	**LP RX Time Out –** This bit reflects the status of the LP RX timer.	0 – The LP RX timer has expired. 1 – The LP RX timer has not expired.
HSTO Bit 5	**HS TX Time Out –** This bit reflects the status of the HS TX timer.	0 – The HS TX timer has expired. 1 – The HS TX timer has not expired.

Name	Description	Setting
ATR Bit 4	**ACK Trigger Response –** This bit reflects whether the ACK trigger message has been received or not.	0 – ACK trigger message has not been received. 1 – ACK trigger message has been received.
ARR Bit 3	**ACK Response Ready –** This bit reflects whether the ACK response has been received or not. The ACK response can be an ACK trigger message or ACK with Error Report packet.	0 – Response has not been received. 1 – Response has been received.
BTAR Bit 2	**BTA Response –** This bit reflects the data lane status after SSD2828 has made a BTA.	0 – The MIPI slave has not passed the lane authority back. 1 – The MIPI slave has passed the lane authority back.
PO Bit 1	**Packet Operation –** This bit reflects whether the SSD2828 is ready to take in more data from the application processor.	0 – Not ready 1 – Ready
RDR Bit 0	**Read Data Ready –** This bit reflects whether the data from the MIPI slave is ready for read by the application processor. This bit is valid only during the read operation. This bit will be automatically cleared when all the received data are read out.	0 – Not ready 1 – Ready

8.1.24 Error Status Register

Offset Address

ESR **Error Status Register** **0xC7**

BIT	15	14	13	12	11	10	9	8
NAME						**CRCE**	**ECCE2**	**ECCE1**
TYPE	RO	RO	RO	RO	RO	RW1C	RW1C	RW1C
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**SO**			**MLO**		**CONT**		**VMM**
TYPE	RW1C	RO	RO	RW1C	RO	RO	RO	RW1C
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-25: Error Status Register Description

Name	Description	Setting
Reserved Bit 15-11		
CRCE Bit 10	**CRC Error –** This bit reflects the status of CRC checking for the packets received from the MIPI slave. The status is valid only when the **ECD** bit is set to 0. Once a CRC error occurs, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – No CRC error since this bit is cleared 1 – At least 1 CRC error since this bit is cleared
ECCE2 Bit 9	**ECC Multi Bit Error –** This bit reflects the status of ECC checking for the packets received from the MIPI slave. The status is valid only when the **ECD** bit is set to 0. Once an ECC multi-bit error occurs, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – No ECC multi-bit error since this bit is cleared 1 – At least 1 ECC multi-bit error since this bit is cleared
ECCE1 Bit 8	**ECC Single Bit Error –** This bit reflects the status of ECC checking for the packets received from the MIPI slave. The status is valid only when the **ECD** bit is set to 0. Once an ECC single-bit error occurs, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – No ECC single-bit error since this bit is cleared 1 – At least 1 ECC single-bit error since this bit is cleared
CBO Bit 7	**Command Buffer Overflow –** This bit reflects the status of internal command buffer of the SPI interface. If the command buffer has overflowed, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – Overflow has not occurred 1 – Overflow has occurred
Reserved Bit 6-5		
MLO Bit 4	Reserved	Reserved
Reserved Bit 3		
CONT	**Contention –** This bit reflects the status of the	0 – No contention

Name	Description	Setting
Bit 2	data lane contention detector.	1 – Contention has occurred
Reserved Bit 1		
VMM Bit 0	**VC Mis Match –** This bit reflects whether there is a mismatch between the VC ID transmitted by the SSD2828 and the VC ID received from the MIPI slave	0 – No mismatch 1 – Mismatch has occurred

8.1.25 Delay Adjustment Register 1

Offset Address

DAR1 **Delay Adjustment Register 1** **0xC9**

BIT	15	14	13	12	11	10	9	8
NAME	**HZD**							
TYPE	RW							
RESET	0x14							
BIT	7	6	5	4	3	2	1	0
NAME	**HPD**							
TYPE	RW							
RESET	0x02							

Table 8-26: Delay Adjustment Register 1 Description

Name	Description	Setting
HZD Bit 15-8	**HS Zero Delay** – These bits specifies the number of nibble clock for HS zero delay period $T_{HS-ZERO}$.	
HPD Bit 7-0	**HS Prepare Delay** – These bits specifies the number of nibble clock for HS prepare delay period $T_{HS-PREPARE}$.	

HZD

It defined how many nibble clock is the $T_{HS-ZERO}$ period (Figure 9-1).

For example, if the PLL is running 600Mbps, the nibble clock frequency will be 150Mhz, or 6.67ns. The default of 20 means there are 133ns for $T_{HS-ZERO}$ period.

The $T_{HS-ZERO}$ period will be 20 * nibble_clk = 20 * 6.67ns = 133.4ns.

HPD

It defined how many nibble clock is the $T_{HS-PREPARE}$ period (Figure 9-1). There is an inherence delay of around 4 nibble_clk from the edge of the LP-00. Hence the actual $T_{HS-PREPARE}$ period will be 4 nibble_clk + HPD * nibble_clk periods.

For example, if the PLL is running 600bps, the nibble clock frequency will be 150Mhz, or 6.67ns.

The $T_{HS-PREPARE}$ period will be 4 * nibble_clk + 2 * nibble_clk = 4 * 6.67ns + 2 * 6.67ns = 40.02ns.

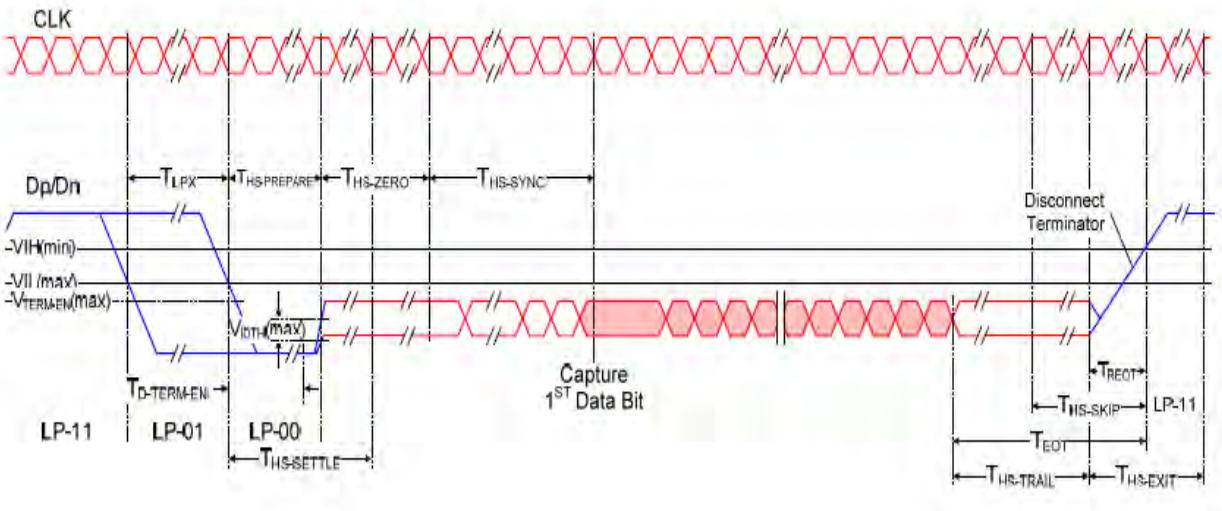


Figure 8-1: Timing for delay calculation

8.1.26 Delay Adjustment Register 2

Offset Address

DAR2	Delay Adjustment Register 2							0xCA
BIT	15	14	13	12	11	10	9	8
NAME	CZD							
TYPE	RW							
RESET	0x28							
BIT	7	6	5	4	3	2	1	0
NAME	CPD							
TYPE	RW							
RESET	0x03							

Table 8-27: Delay Adjustment Register 2 Description

Name	Description	Setting
CZD Bit 15-8	**CLK Zero Delay** – These bits specifies the number of nibble clock for CLK zero delay period $T_{CLK-ZERO}$.	
CPD Bit 7-0	**CLK Prepare Delay** – These bits specifies the number of nibble clock for CLK prepare delay period $T_{CLK-PREPARE}$.	

CZD

It defined how many nibble clock is the $T_{CLK-ZERO}$ period (Figure 9-2).
For example, if the PLL is running 600bps, the nibble clock frequency will be 150Mhz, or 6.67ns.
The $T_{CLK-ZERO}$ period will be 40 * nibble_clk = 40 * 6.67ns ~= 266.8ns.

CPD

It defined how many nibble clock is the $T_{CLK-PREPARE}$ period (Figure 9-2). There is an inherence delay of around 3 nibble_clk from the edge of the LP-00. Hence the actual $T_{CLK-PREPARE}$ period will be 3 nibble_clk + CPD * nibble_clk periods.
For example, if the PLL is running 600bps, the nibble clock frequency will be 150Mhz, or 6.67ns.
The $T_{CLK-PREPARE}$ period will be 3 * nibble_clk + 3 * nibble_clk = 3 * 6.67ns + 3 * 6.67ns ~= 40.02ns.

Note : nibble_clk = PLL / 4

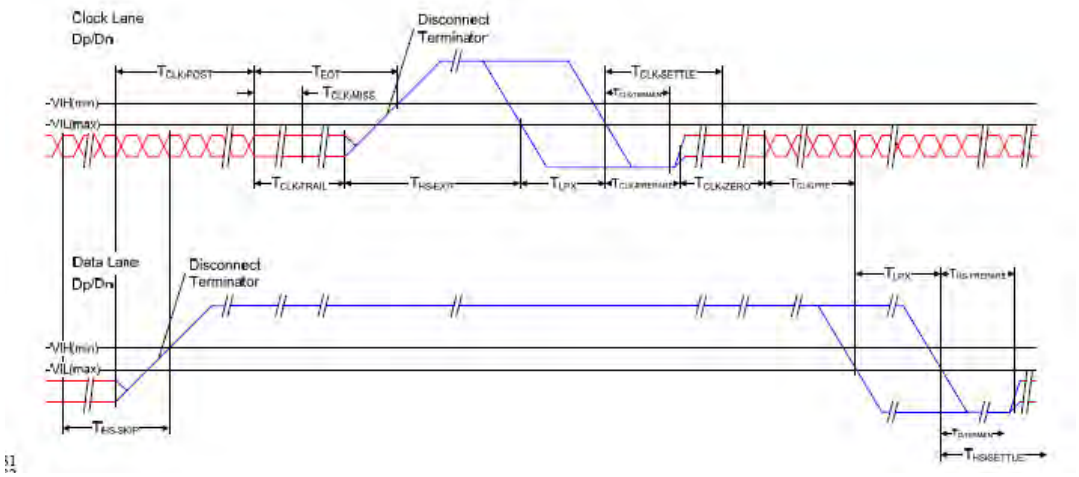


Figure 8-2: Timing for delay calculation

8.1.27 Delay Adjustment Register 3

Offset Address

DAR3 **Delay Adjustment Register 3** **0xCB**

BIT	15	14	13	12	11	10	9	8
NAME	**CPED**							
TYPE	RW							
RESET	0x04							
BIT	7	6	5	4	3	2	1	0
NAME	**CPTD**							
TYPE	RW							
RESET	0x16							

Table 8-28: Delay Adjustment Register 3 Description

Name	Description	Setting
CPED Bit 15-8	**CLK Pre Delay** – These bits specifies the number of nibble clock for CLK pre delay period $T_{CLK-PER}$.	
CPTD Bit 7-0	**CLK Post Delay** – These bits specifies the number of nibble clock for CLK post delay period $T_{CLK-POST}$.	

CPED

It defined how many nibble clock is the $T_{CLK-PRE}$ period (Figure 9-2). There is an inherence delay of 0~1 lp_clk for the $T_{CLK-PRE}$ period.

For example, if the PLL is running 600bps, the nibble clock frequency will be 150Mhz, or 6.67ns. If the lpdiv is 7, then lp_clk is 9.375Mhz, or 106.67ns.

The $T_{CLK-PRE}$ period (min) will be 4 * nibble_clk + 0 * lp_clk = 4 * 6.67ns ~= 26.68ns

The $T_{CLK-PRE}$ period (max) will be 4 * nibble_clk + 1 * lp_clk = 4 * 6.67ns + 1 * 106.67ns ~= 133.35ns

CPTD

It defined how many nibble clock is the $T_{CLK-POST}$ period (Figure 9-2).

For example, if the PLL is running 600bps, the nibble clock frequency will be 150Mhz, or 6.67ns.

The $T_{CLK-POST}$ period will be 22 * nibble_clk = 22 * 6.67ns ~= 146.74ns.

Note : lp_clk = PLL / (8 * (lpd+1))

8.1.28 Delay Adjustment Register 4

Offset Address

DAR4 **Delay Adjustment Register 4** **0xCC**

BIT	15	14	13	12	11	10	9	8
NAME	**CTD**							
TYPE	RW							
RESET	0x0A							
BIT	7	6	5	4	3	2	1	0
NAME	**HTD**							
TYPE	RW							
RESET	0x0A							

Table 8-29: Delay Adjustment Register 4 0/1 Description

Name	Description	Setting
CTD Bit 15-8	**CLK Trail Delay** – These bits specifies the number of nibble clock for CLK trail delay period $T_{CLK-TRAIL}$.	
HTD Bit 7-0	**HS Trail Delay** – These bits specifies the number of nibble clock for HS trail delay period $T_{HS-TRAIL}$. Please note that the minimum value for the $T_{HS-TRAIL}$ is 3.	

CTD

It defined how many nibble clock is the $T_{CLK-TRAIL}$ period (Figure 9-2).
For example, if the PLL is running 600bps, the nibble clock frequency will be 150Mhz, or 6.67ns.
The $T_{CLK-TRAIL}$ period will be 10 * nibble_clk = 10 * 6.67ns ~= 66.7ns

HTD

It defined how many nibble clock is the $T_{HS-TRAIL}$ period (Figure 9-2).
For example, if the PLL is running 600bps, the nibble clock frequency will be 150Mhz, or 6.67ns.

The $T_{HS-TRAIL}$ period will be 10 * nibble_clk = 10 * 6.67ns ~= 66.7ns.

8.1.29 Delay Adjustment Register 5

Offset Address

DAR5 **Delay Adjustment Register 5** **0xCD**

BIT	15	14	13	12	11	10	9	8
NAME	**WUD[15:8]**							
TYPE	RW							
RESET	0x10							
BIT	7	6	5	4	3	2	1	0
NAME	**WUD[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-30: Delay Adjustment Register 5 Description

Name	Description	Setting
WUD Bit 15-0	**Wake Up Delay** – These bits specifies the number of clock cycles for wake up delay period T_{WAKEUP}. The delay is used to wake up the MIPI slave from ULPS state. The clock is the low power clock.	

WUD

It defined how many low power clock (lp_clk) is the T_{WAKEUP} period (Figure 9-3), from LP-10 to LP-11.
For example, if the PLL is running 600bps, the nibble clock frequency will be 150Mhz, or 6.67ns. If the lpdiv = 7, lp_clk will be 9.375Mhz, or 106.6ns.
The T_{WAKEUP} period will be 4096 * lp_clk = 4096 * 106.6ns ~= 436633 ns

Note : lp_clk = PLL / (8 * (lpd+1))

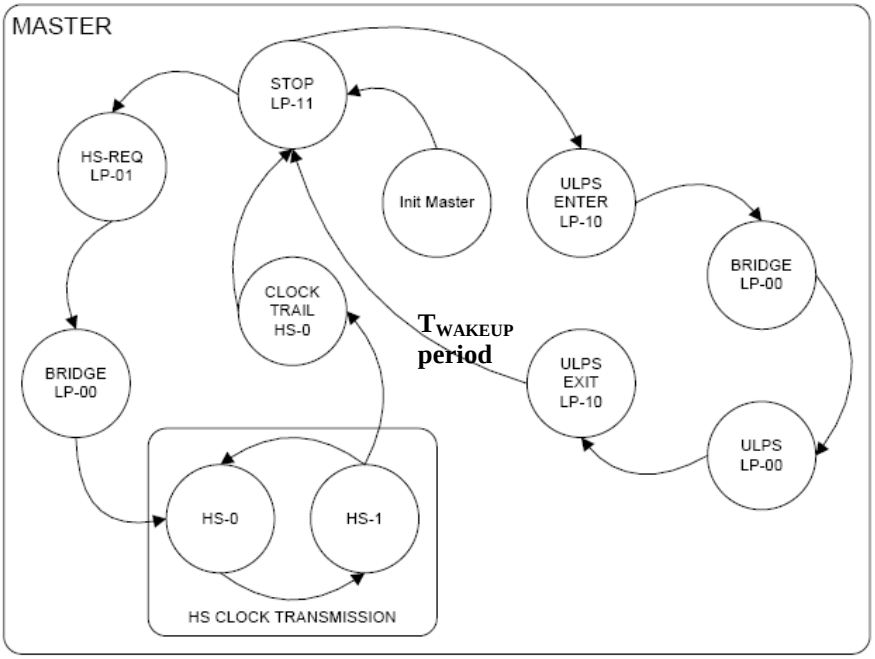


Figure 8-3: T_{WAKEUP} period delay calculation

8.1.30 Delay Adjustment Register 6

Offset Address

DAR6 **Delay Adjustment Register 6** **0xCE**

BIT	15	14	13	12	11	10	9	8
NAME					**TGO**			
TYPE	RO	RO	RO	RO	RW			
RESET	0x0	0x0	0x0	0x0	0x4			
BIT	7	6	5	4	3	2	1	0
NAME					**TGET**			
TYPE	RO	RO	RO	RO	RW			
RESET	0x0	0x0	0x0	0x0	0x5			

Table 8-31: Delay Adjustment Register 6 Description

Name	Description	Setting
Reserved Bit 15-12		
TGO Bit 11-8	**TA Go Delay** – These bits specifies the number of T_{LPX} for TA go delay period T_{TA-GO}.	
Reserved Bit 7-4		
TGET Bit 3-0	**TA Get Delay** – These bits specifies the number of T_{LPX} for TA get delay period T_{TA-GET}.	

TGO

It defined how many T_{LPX} is the T_{TA-GO} period (Figure 9-4). T_{LPX} is half period of lp_clk.

For example, if the PLL is running 600bps, the nibble clock frequency will be 150Mhz, or 6.67ns. If the lpdiv = 7, lp_clk will be 9.375Mhz, or 106.6ns.

The T_{TA-GO} will be 4 * lp_clk/2 = 4 * 106.6/2 ~= 213.33ns

TGET

It defined how many T_{LPX} is the T_{TA-GET} period (Figure 9-4). T_{LPX} is half period of lp_clk.

For example, if the PLL is running 600bps, the nibble clock frequency will be 150Mhz, or 6.67ns. If the lpdiv = 7, lp_clk will be 9.375Mhz, or 106.6ns.

The T_{TA-GET} will be 5 * lp_clk/2 = 5 * 106.6/2 ~= 266.5ns

Note : lp_clk = PLL / (8 * (lpd+1))

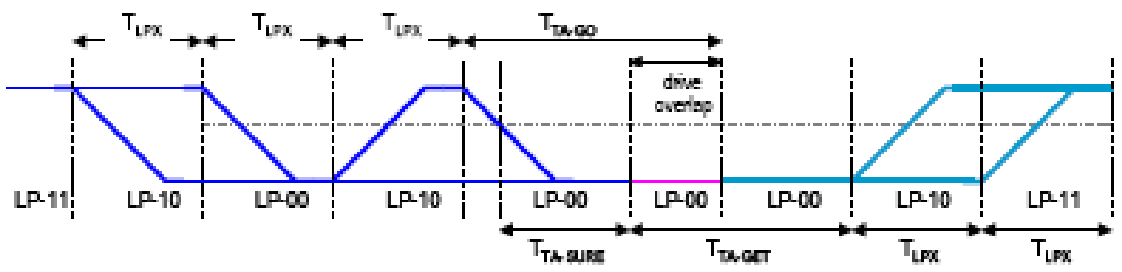


Figure 8-4: Timing for delay calculation

8.1.31 HS TX Timer Register 1

Offset Address

HTTR1 **HS TX Timer Register 1** **0xCF**

BIT	15	14	13	12	11	10	9	8
NAME	**HTT[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**HTT[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-32: HS TX Timer Register 1 Description

Name	Description	Setting
HTT Bit 31-0	**HS TX Timer** – These bits specify the HS TX timer timeout value. PLL reference clock is used to increment an internal timer. The timer starts when the SSD2828 enters HS transmit mode. When the SSD2828 exits from HS transmit mode, the timer will be reset. If the timer expires before the end of HS transmission, the SSD2828 will signal an error and switch to LP mode to continue the transmission. At the same time, the **HS** bit will be cleared to 0. Software intervention is required so that the SSD2828 can go back to proper HS transmission mode.	

8.1.32 HS TX Timer Register 2

Offset Address

HTTR2 **HS TX Timer Register 2** **0xD0**

BIT	15	14	13	12	11	10	9	8
NAME	**HTT[31:24]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**HTT [23:16]**							
TYPE	RW							
RESET	0x10							

Table 8-33: HS RX Timer Register 2 Description

Name	Description	Setting
HTT Bit 31-0	Please see the description of HS TX Timer Register 1	

8.1.33 LP RX Timer Register 1

Offset Address

LRTR1 **LP RX Timer Register 1** **0xD1**

BIT	15	14	13	12	11	10	9	8
NAME	**LRT[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**LRT[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-34: LP TX Timer Register 1 Description

Name	Description	Setting
LRT Bit 31-0	**LP RX Timer** – These bits specify the LP RX timer timeout value. PLL reference clock is used to increment an internal timer. The timer starts when the SSD2828 enters LP receive mode. When the SSD2828 exits from LP receive mode, the timer will be reset. If the timer expires before exiting from LP receive mode, the SSD2828 will signal an error and switch to LP transmit mode. The DPHY will drive the data lane to LP11 state. Software intervention is required so that any possible error could be cleared.	

8.1.34 LP RX Timer Register 2

Offset Address

LRTR2 **LP RX Timer Register 2** **0xD2**

BIT	15	14	13	12	11	10	9	8
NAME	**LRT[31:24]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**LRT[23:16]**							
TYPE	RW							
RESET	0x10							

Table 8-35: LP TX Timer Register 2 Description

Name	Description	Setting
LRT Bit 31-0	Please see the description of LP RX Timer Register 1	

8.1.35 TE Status Register

Offset Address

TSR **TE Status Register** **0xD3**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME								**TER**
TYPE	RO	RO	RO	RO	RO	RO	RO	RW1C
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-36: TE Status Register Description

Name	Description	Setting
Reserved Bit 15-1		
TER Bit 0	**TE Response –** This bit reflects whether a TE response has been received or not. Once a TE response is received, this bit will be set to 1. At the same time, the output te signal will go high. The host processor can write 1 to clear this bit. Once the bit is cleared, the te signal will go low.	0 –TE response has not been received. 1 – TE response has been received.

8.1.36 SPI Read Register

Offset Address

LRR **SPI Read Register** **0xD4**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**RRA**							
TYPE	RW							
RESET	0xFA							

Table 8-37: SPI Read Register Description

Name	Description	Setting
Reserved Bit 15-8		
RRA Bit 7-0	**Register Read Address** – These bits specify the address of the register to be read through the SPI interface, when the interface is SPI 8-bit (either 3 wire or 4 wire).	

8.1.37 PLL Lock Register

Offset Address

PLLR **PLL Lock Register** **0xD5**

BIT	15	14	13	12	11	10	9	8
NAME	**LOCK**							
TYPE	RW							
RESET	0x14							
BIT	7	6	5	4	3	2	1	0
NAME	**LOCK**							
TYPE	RW							
RESET	0x50							

Table 8-38: PLL Lock Register Description

Name	Description	Setting
LOCK Bit 15-0	**LOCK –** These bits specify the PLL lock range in term of PLL reference frequency, f_{FIN} . The maximum PLL lock period is 500us and the default setting assumed the reference clock, f_{FIN} is 10Mhz from tx_clk. The **LOCK** setting should be programmed only when **PEN** is 0. It has no effect when **PEN** is 1.	0x1450 * f_{FIN} = 520us

8.1.38 Test Register

Offset Address

TR **Test Register** **0xD6**

BIT	15	14	13	12	11	10	9	8
NAME	**TM/FL0**		**EIC**					**FLM**
TYPE	RW		RW					RW
RESET	0x0		0x00					0x0
BIT	7	6	5	4	3	2	1	0
NAME	**PNB**						**END**	**CO**
TYPE	RW						RW	RW
RESET	0x01						0x0	0x1

Table 8-39: Test Register Description

Name	Description	Setting
TM/FL0 Bit 15-14	**Test Mode –** These bits selects whether to inject CRC/ECC error for the outgoing streams. They are used for debugging purpose only. They should be set to 00 in normal mode! **Force Lane 0** – These bits are valid when **FLM** is 1. During this mode, user can write Low Power value to the MIPI lane 0 data using these bits. SSD2828 will not respond to the normal request through RGB or SPI interface. **FL0**[1] controls MIPI_DP0 and **FL0**[0] controls MIPI_DN0.	00 – Normal mode 01 – Inject CRC error 10 – Inject 1 bit ECC error 11 – Inject 2 bit ECC error
EIC Bit 13-9	**Error Injection Control –** These bits controls the position of the error being injected for testing. It is only applicable when **TM** is 01.	
FLM Bit 8	**Force Lane Mode –** This bit enable user to write to **FL0** bits to directly control the analog lane DP0 and DP1. The lane should be in Low Power mode(**HS**=0) when write using **FL0**.	0 – Normal Mode 1 – Force Lane Mode
PNB Bit 7-2	**Packet Number in Blanking Period –** These bits controls the number of packet to send during video mode blanking period.	
END Bit 1	**Endianess** – Internal test only. Default as 0	
CO Bit 0	**Color Order** – This bit specifies the order of the color component in the pixel. During command mode transmission, this bit takes effect only when the **IFS** bit is 1 and the transmitted packet is DCS write memory packet, 0x2C or 0x3C. During video mode transmission, this bit must be set to 1 so as to follow the MIPI DSI specification.	1 – RGB. R is in the higher portion of the pixel. 0 – BGR. B is in the higher portion of the pixel.

Remark: 24 bits color format

CO	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
0	B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0

8.1.39 TE Count Register

Offset Address

TECR **TE Count Register** **0xD7**

BIT	15	14	13	12	11	10	9	8
NAME	**TEC[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**TEC[7:0]**							
TYPE	RW							
RESET	0x01							

Table 8-40: TE Count Register Description

Name	Description	Setting
TEC Bit 15-0	**TE Count** – These bits determines the pulse width of the output te signal. A counter will be started after the TE signal goes to 1. When the counter reaches the value in **TEC** field, the te signal will be set to 0. The counter uses the PLL reference clock to do counting.	The minimum value is 1.

8.1.40 Analog Control Register

Offset Address

ACR1 **Analog Control 1 Register** **0xD8**

BIT	15	14	13	12	11	10	9	8
NAME	**D3_DELAY_SEL[3:2]**		**D1_DELAY_SEL**					
TYPE	RW		RW					
RESET	0x0		0x20					
BIT	7	6	5	4	3	2	1	0
NAME	**D3_DELAY_SEL[1:0]**		**D0_DELAY_SEL**					
TYPE	RW		RW					
RESET	0x0		0x20					

Table 8-41: Analog Control 1 Register Description

Name	Description	Setting
D3_DELAY_SEL[3:2] Bit 15-14	**Data lane 3 DELAY SELect[3:2]** – These bits control the delay for serializer output to the HS transmitter.	
D1_DELAY_SEL Bit 13-8	**Data lane 1 DELAY SELect** – These bits control the delay for serializer output to the HS transmitter.	
D3_DELAY_SEL[1:0] Bit 7-6	**Data lane 3 DELAY SELect[1:0]** – These bits control the delay for serializer output to the HS transmitter.	
D0_DELAY_SEL Bit 5-0	**Data lane 0 DELAY SELect** – These bits control the delay for serializer output to the HS transmitter.	

8.1.41 Analog Control Register 2

Offset Address

ACR2 **Analog Control Register 2** **0xD9**

BIT	15	14	13	12	11	10	9	8
NAME	**HSTX_Z**		**LPTXDS**			**HSTX_DS**		
TYPE	RW		RW			RW		
RESET	0x1		0x4			0x4		
BIT	7	6	5	4	3	2	1	0
NAME	**D3_DELAY_SEL[5:4]**		**D2_DELAY_SEL**					
TYPE	RW		RW					
RESET	0x2		0x20					

Table 8-42: Analog Control Register 2 Description

Name	Description	Setting
HSTX_Z Bit 15-14	**High Speed Transmit Trimming control** – These bits control the trimming for output impedance control.	
LPTXDS Bit 13-11	**Low Power TX Drive strength Selection** – These bits control the drive strength for the TX in low power mode.	
HSTX_DS Bit 10-8	**High Speed TX current Driver Selection** – These bits control the driving current for the TX in high speed mode.	
D3_DELAY_SEL[5:4] Bit 7-6	**Data lane 3 DELAY SELect[5:4]** –These bits control the delay for serializer output to the HS transmitter.	
D2_DELAY_SEL Bit 5-0	**Data lane 2 DELAY SELect** – These bits control the delay for serializer output to the HS transmitter.	

8.1.42 Analog Control Register 3

Offset Address

ACR3 **Analog Control Register 3** **0xDA**

BIT	15	14	13	12	11	10	9	8
NAME	**TLFT1**	**TLFT0**	**PREEM_SEL**			**PREEM_MOD**		**PREEM_E**
TYPE	RW	RW	RW			RW		RW
RESET	0x1	0x0	0x3			0x0		0x1
BIT	7	6	5	4	3	2	1	0
NAME	**THFT1**	**THFT0**	**TC**			**ISEL**		
TYPE	RW	RW	RW			RW		
RESET	0x1	0x0	0x04			0x04		

Table 8-43: Analog Control Register 3 Description

Name	Description	Setting
TLFT1 Bit 15		
TLFT0 Bit 14		
PREEM_SEL Bit 13-11	**PREEM_SEL –** Used for tap selection for preemphasis.	
PREEM_MOD Bit 10-9	**PREEM_MOD –** Preemphasis mode selection.	
PREEM_E Bit 8	**PRE-EMphasis Enable –** Used for HSTX.	
THFT1 Bit 7	**ThresHold 1 –** This bit controls the low power receiver schmitt trigger high to low threshold selection1.	
THFT0 Bit 6	**ThresHold 0 –** This bit controls the low power receiver schmitt trigger high to low threshold selection 0.	
TC Bit 5-3	**Temperature Coefficient Select –** These bits control the temperature coefficient of the bandbap regulator.	
ISEL Bit 2-0	**Current Output Trim –** These bits control current output trim of the bandgap regulator.	

8.1.43 Analog Control Register 4

Offset Address

ACR4 **Analog Control Register 4** **0xDB**

BIT	15	14	13	12	11	10	9	8
NAME	**CLK_DELAY_SEL**						**CKF**	
TYPE	RW						RW	RO
RESET	0x20						0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**TCI**			**ENLV**	**CD_EN**	**GFFT1**	**GFFT0**	**GF_E**
TYPE	RW			RW	RW	RW	RW	RW
RESET	0x4			0x1	0x1	0x0	0x0	0x0

Table 8-44: Analog Control Register 4 Description

Name	Description	Setting
CLK_DELAY_SEL Bit 15-10	**CLocK lane DELAY SELect** – These bits control the delay for serializer output to the HS transmitter.	
CKF Bit 9	**ClocK Flip** – This bit controls whether to flip the TX_LP_CP and TX_LP_CN to the analog block. It should be set to 0 for normal operation.	
Reserved Bit 8		
TCI Bit 7-5	**Current Temperature Coefficient Select**	
ENLV Bit 4	**BandGap Reference Enable**	
CD_EN Bit 3	**Contention Detection Enable**	
GFFT1 Bit 2	**Glitch Filter Selection 1**	
GFFT0 Bit 1	**Glitch Filter Selection 0**	
GF_E Bit 0	**Glitch filter Enable**	

8.1.44 Interrupt Output Control Register

Offset Address

IOCR **Interrupt Output Control Register** **0xDC**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME						**IOT**		**IAS**
TYPE	RO	RO	RO	RO	RO	RW		RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0		0x0

Table 8-45: Interrupt Output Control Register Description

Name	Description	Setting
Reserved Bit 15-3		
IOT Bit 2-1	**Interrupt Output Type –** These bits specify the type of output for the int. Write to this bit is only valid when all the enable bits in the Interrupt Control Registers(0xC5) are 0.	00 – CMOS output 01 – Open Drain active low output(Wired-AND). The IAS should be 0 when selected. 1x – Open Drain active high output(Wired-OR). The IAS should be 1 when selected. 11 – NA
IAS Bit 0	**Interrupt Active State –** This bit selects the polarity of the int pin at the chip IO. Write to this bit is only valid when all the enable bits in the Interrupt Control Registers(0xC5) are 0.	0 – int pin is active low, when there is no interrupt events, it is normally high. 1 – int pin is active high, when there is no interrupt events, it is normally low.

8.1.45 RGB Interface Control Register 7

Offset Address

VICR7 **RGB Interface Control Register7** **0xDD**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**VBN**				**VFN**			
TYPE	RW				RW			
RESET	0x00				0x00			

Table 8-46: RGB Interface Control Register 7 Description

Name	Description	Setting
Reserved Bit 15-8		
VBN Bit 7-4	**Vertical Front Porch Non Video Data Window** These fields specify the number of vertical back porch counting backward from the first vertical active line in which non-video data is not allowed to be sent via MIPI link. This field is only valid when **VEN** is 1 and the interface setting is RGB + SPI. This field should not larger than VBP. If it is larger, the internal logic will cap this field to VBP.	
VFN Bit 3-0	**Vertical Back Porch Non Video Data Window** These fields specify the number of vertical front porch from the last vertical active line in which non-video data is not allowed to be sent via MIPI link. This field is only valid when **VEN** is 1 and the interface setting is RGB + SPI. This field should not larger than VFP. If it is larger, the internal logic will cap this field to VFP.	

Note: Setting VBN ≥ VBP and VFN ≥ VFP at the same time will cause non-video data not being sent out through MIPI link when the video mode is non-burst mode or burst mode with **NVB** = 1.

8.1.46 Lane Configuration Register

Offset Address

LCFR **Lane Configuration Register** **0xDE**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME							**LS**	
TYPE	RO	RO	RO	RO	RO	RO	RW	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x00	

Table 8-47: Lane Configuration Register Description

Name	Description	Setting
Reserved Bit 15-2		
LS0 Bit 1-0	**Lane Select** – These bits define the number of lane to be used for SSD2828.	00 – 1 lane mode 01 – 2 lane mode 10 – 3 lane mode 11 – 4 lane mode

8.1.47 Delay Adjustment Register 7

Offset Address

DAR7 **Delay Adjustment Register 7** **0xDF**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME			**HED**					
TYPE	RO	RO	RW					
RESET	0x0	0x0	0x10					

Table 8-48: Delay Adjustment Register 7 Description

Name	Description	Setting
Reserved Bit 15-6		
HED Bit 5-0	**HS Exit Delay** – These bits specifies the number of nibble clock for HS exit delay period for data and clock lane.	

8.1.48 Pull Control Register 1

Offset Address

PUCR1 **Pull Control Register 1** **0xE0**

BIT	15	14	13	12	11	10	9	8
NAME	**XTAL_PULL**		**PS4_PULL**		**PS3_PULL**		**PS2_PULL**	
TYPE	RW		RW		RW		RW	
RESET	0x1		0x1		0x1		0x1	
BIT	7	6	5	4	3	2	1	0
NAME	**PS1_PULL**		**PS0_PULL**		**IS_PULL**		**MR_PULL**	
TYPE	RW		RW		RW		RW	
RESET	0x1		0x1		0x1		0x2	

Table 8-49: Pull Control Register 1 Description

Name	Description	Setting
CSX_PULL Bit 15-14	**Chip Select Pull** – These bits select the pull state of the pin csx.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
XTAL_PULL Bit 15-14	**Xtal Mode Pull** – These bits select the pull state of the pin xtal_mode.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
PS4_PULL Bit 13-12	**Pin Select 3 Pull** – These bits select the pull state of the pin ps[4].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
PS3_PULL Bit 11-10	**Pin Select 3 Pull** – These bits select the pull state of the pin ps[3].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
PS2_PULL Bit 9-8	**Pin Select 2 Pull** – These bits select the pull state of the pin ps[2].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
PS1_PULL Bit 7-6	**Pin Select 1 Pull** – These bits select the pull state of the pin ps[1].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
PS0_PULL Bit 5-4	**Pin Select 0 Pull** – These bits select the pull state of the pin ps[0].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
IS_PULL Bit 3-2	**If_Sel Pull** – These bits select the pull state of the pin if_sel.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
MR_PULL Bit 1-0	**MIPI Reset Pull** – These bits select the pull state of the pin mipi_reset_b.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down

Name	Description	Setting
		11 – 75k Keeper

8.1.49 Pull Control Register 2

Offset Address

PUCR2 **Pull Control Register 2** **0xE1**

BIT	15	14	13	12	11	10	9	8
NAME	**DEN_PULL**		**HS_PULL**		**PC_PULL**		**VS_PULL**	
TYPE	RW		RW		RW		RW	
RESET	0x1		0x2		0x1		0x2	
BIT	7	6	5	4	3	2	1	0
NAME	**DH_PULL**		**DM_PULL**		**DL_PULL**		**CSX_PULL**	
TYPE	RW		RW		RW		RW	
RESET	0x1		0x1		0x1		0x2	

Table 8-50: Pull Control Register 2 Description

Name	Description	Setting
DEN_PULL Bit 15-14	**Den Pull** – These bits select the pull state of the pin den.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
HS_PULL Bit 13-12	**Hsync Pull** – These bits select the pull state of the pin hsync.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
PC_PULL Bit 11-10	**Pixel_clk Pull** – These bits select the pull state of the pin pclk.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
VS_PULL Bit 9-8	**Vsync Pull** – These bits select the pull state of the pin vsync.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
DH_PULL Bit 7-6	**Data high byte Pull** – These bits select the pull state of the pins data[23:16].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
DM_PULL Bit 5-4	**Data medium byte Pull** – These bits select the pull state of the pins data[15:8].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
DL_PULL Bit 3-2	**Data low byte Pull** – These bits select the pull state of the pins data[7:0].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
CSX_PULL Bit 1-0	**Chip Select Pull** – These bits select the pull state of the pin csx.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper

8.1.50 Pull Control Register 3

Offset Address

PUCR3 **Pull Control Register 3** **0xE2**

BIT	15	14	13	12	11	10	9	8
NAME							**SDI_PULL**	
TYPE	RO	RO	RO	RO	RO	RO	RW	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x1	
BIT	7	6	5	4	3	2	1	0
NAME	**SCK_PULL**		**SDC_PULL**		**SHUT_PULL**		**CM_PULL**	
TYPE	RW		RW		RW		RW	
RESET	0x1		0x1		0x2		0x1	

Table 8-51: Pull Control Register 3 Description

Name	Description	Setting
Reserved Bit 15-10		
SDI_PULL Bit 9-8	**SDI Pull** – These bits select the pull state of the pin sdi.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
SCK_PULL Bit 7-6	**SCK Pull** – These bits select the pull state of the pin sck.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
SDC_PULL Bit 5-4	**SDC Pull** – These bits select the pull state of the pin sdc.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
SHUT_PULL Bit 3-2	**Shut Pull** – These bits select the pull state of the pin shut.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
CM_PULL Bit 1-0	**CM Pull** – These bits select the pull state of the pin cm.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper

8.1.51 CABC Brightness Control Register 1

Offset Address

CBCR1 **CABC Brightness Control Register 1** **0xE9**

BIT	15	14	13	12	11	10	9	8
NAME	**WDBV**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME		**GAM18**	**BL**	**DD**	**BCTR**	**BP_MODE**		**CABC_EN**
TYPE	RO	RW	RW	RW	RW	RW		RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0		0x0

Table 8-52: CABC Brightness Control Register 1 Description

Name	Description	Setting
WDBV Bit 15-8	**Write Display Brightness Value** – These bits control the brightness setting.	
Reserved Bit 7		
GAM18 Bit 6	**Gamma 18** – This bit controls gamma 18 select.	
BL Bit 5	**BackLight Control** – This bit controls the backlight on/off at BC line.	0 – Off (Completely turn off backlight circuit) 1 – On
DD Bit 4	**Display Dimming** – This bit controls the display dimming feature.	0 – Display Dimming Off 1 – Display Dimming On
BCTR Bit 3	**Brightness Control** – This bit controls the On/Off state of the Brightness Control block.	0 – Off 1 – On
BP_MODE Bit 2-1	**BP MODE** – These bits control the Brightness Preservation of the CABC.	00 – Disable DABC 01 – Conservation Mode (Or User Interface Mode) 10 – Normal Mode (Or Still Picture Mode) 11 – Aggressive Mode (Or Moving Image Mode)
CABC_EN Bit 0	**CABC ENable** – This bit enable the CABC feature. This bit is valid only when if_sel is 0.	0 – CABC is disable 1 – CABC is enable

8.1.52 CABC Brightness Control Register 2

Offset Address

CBCR2 **CABC Brightbess Control Register 2** **0xEA**

BIT	15	14	13	12	11	10	9	8
NAME	**PWM_PS**				**BCB_PS**			
TYPE	RW				RW			
RESET	0x6				0x9			
BIT	7	6	5	4	3	2	1	0
NAME	**CABC_MB**							
TYPE	RW							
RESET	0x00							

Table 8-53: CABC Brightness Control Register 2 Description

Name	Description	Setting
PWM_PS Bit 15-12	**PWM PreScale** – These bits control the PWM signal frequency.	This will depend on pixel clock speed (pclk). For example, 10MHz = “0111” or “1000” 20MHz = “0110” or “0101”
BCD_PS Bit 11-8	**BCB PreScale** – These bits control the number of iternation per second carried out by the BCB unit.	This will depend on pixel clock speed (pclk). For example, 5MHz = “0101” 10MHz = “0110” 25MHz = “1001” 50MHz = “1011” 75MHz = “1100”
CABC_MB Bit 7-0	**CABC Minimum Brightness** – These bits control the CABC Minimum Brightness level.	

8.1.53 CABC Brightness Status Register

Offset Address

CBSR **CABC Brightness Status Register** **0xEB**

BIT	15	14	13	12	11	10	9	8
NAME	**VGA_SEL**							**BCL**
TYPE	RW				RO	RO	RO	RO
RESET	0x0				0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**RDBV**							
TYPE	RO							
RESET	0x00							

Table 8-54: CABC Brightness Status Register Description

Name	Description	Setting
VGA_SEL Bit 15-12	**VGA SELect –** These bits select the type of resolution of the RGB frame. Panel resolutions need not be matched exactly. For example, "0111" will work for any panel with 384000 pixels (+/- 15%). In other words, the range is 326400 to 441600 pixels. Hence, 800x480, 480x800, 512x750 and 750x512 will be supported by **VGA_SEL**= "0111".	0001 - 400x240 (WQVGA) 0010 - 400x300 (SQVGA) 0011 - 480x320 (FVGA) 0100 - 540x360 (FVGA+) 0101 - 600x400 (FVGA++) 0110 - 640x480 (VGA) 0111 - 800x480 (WVGA) 1000 - 800x600 (SVGA) 1001 - 1024x600 (WSVGA) 1010 - 1024x768 (XGA) 1011 - 1280x768 (WXGA) 1100 - 1280x960 (SXGA) 1101 - Reserved 1110 - Reserved 1111 - Reserved
Reserved Bit 11-9		
BCL Bit 8	**Brightness Control Line** – This bit is the pulse width modulation signal output to control external backlight power source. This output is used for Architecture I.	
RDBV Bit 7-0	**Read Display Brightness Value** – These bits show the brightness value of the CABC. This output is used for Architecture II.	

8.1.54 Encoder Control Register

Offset Address

ECR **Encoder Control Register** **0xEC**

BIT	15	14	13	12	11	10	9	8
NAME	**ENC_LW**							
TYPE	RW							
RESET	0x78							
BIT	7	6	5	4	3	2	1	0
NAME	**ENC_LW**						**ENC_MODE**	**ENC_EN**
TYPE	RW				RO	RO	RW	RW
RESET	0x0				0x0	0x0	0x0	0x0

Table 8-55: Encoder Control Register Description

Name	Description	Setting
ENC_LW Bit 15-4	**ENCoder LineWidth** – These bits define the input line width of the Encoder input.	
Reserved Bit 3-2		
ENC_MODE Bit 1	**ENCoder Mode** – This bit select the Smartlink Encoder mode. This bit is valid only when if_sel is 0.	0 – Type 1 1 – Type 2
ENC_EN Bit 0	**ENCoder ENable** – This bit enable the Smartlink Encoder feature. This bit is valid only when if_sel is 0.	0 – Encoder is disable 1 – Encoder is enable

8.1.55 Video Sync Delay Register

Offset Address

VSDR **Video Sync Delay Register** **0xED**

BIT	15	14	13	12	11	10	9	8
NAME	**VSD**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**HSD**							
TYPE	RW							
RESET	0x02							

Table 8-56: Video Sync Delay Register Description

Name	Description	Setting
VSD Bit 15:8	**VSync Delay** – These bits control the internal pipeline delay of the Vsync input.	
HSD Bit 7:0	**HSync Delay** – These bits control the internal pipeline delay of the Hsync input.	

8.1.56 Trimming Register

Offset Address

TMR **Trimming Register** **0xEE**

BIT	15	14	13	12	11	10	9	8
NAME	**TRIM_ DONE**	**TRIM_ PASS**	**XORC_ DONE**	**XORC_ SEL**	**XORC_ EN**	**VBIST_ SRT**	**VBIST_ EN**	**TRIM_EN**
TYPE	RO	RO	RO	RW	RWAC	RW	RW	RWAC
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**TRIM_CMD[7:4]**				**TRIM_CMD[3:0]/XORC_FILTER[3:0]**			
TYPE	RW				RW			
RESET	0x0				0x0			

Table 8-57: Trimming Register Description

Name	Description	Setting
TRIM_DONE Bit 15	**TRIMming DONE** – This bit indicates if the trimming process is done.	
TRIM_PASS Bit 14	**TRIMming PASS** – This bit indicates if the trimming process is successful. It is valid when bit 15 is set to 1.	
XORC_DONE Bit 13	**XOR Calibration DONE** – This bit indicates if the trimming process is done. This bit will be cleared when read.	
XORC_SEL Bit 12	**XOR Calibration SELect** – This bit select the internal byte data for calibration to be 8'hAA or 8'h55.	0 = 8'h55 1 = 8'hAA
XORC_EN Bit 11	**XOR Calibration ENable** – This bit starts the internal XOR calibration process and when the calibration is done, this bit will be auto clear and the status bits at bit 13 indicates that the calibration process is done.	
VBIST_SRT Bit 10	**Video BIST StaRT** – This bit starts the video bist process. Once clear, the video bist engine will stop at the frame boundary. The software should wait for at least 1 frame time before disabling the VBIST_EN bit.	
VBIST_EN Bit 9	**Video BIST ENable** – This bit enables the video bist function. The SSD2828 will automatically send the color, red, green, blue, black and white repeatedly base on current setting. This bit should be 0 in normal mode.	
TRIM_EN Bit 8	**TRIMming ENable** – This bit enables the auto trimming process and when the trimming is done, this bit will be auto clear and the status bits at bit 14 and bit 15 indicates if the trimming process is successful.	

Name	Description	Setting
	This bit should be 0 in normal mode.	
TRIM_CMD Bit 7:4	**TRIMming CoMmanD** – These bits define the upper 4 bits of the command header byte to be used in auto-trimming mode, when TRIM_EN=1, where SSD2828 send out a read request to the MIPI receiver.	
TRIM_CMD /XORC_FIL TER Bit 3:0	**TRIMming CoMmanD** – These bits define the lower 4 bits of the command header byte to be used in auto-trimming mode, when TRIM_EN=1, where SSD2828 send out a read request to the MIPI receiver. When XORC_EN=1, these bits define the filter to qualify the XOR calibration pulse width.	

8.1.57 GPIO1 Register

Offset Address

GPIO1 **GPIO1 Register** **0xEF**

BIT	15	14	13	12	11	10	9	8
NAME	**GPIO1_STAT**	**GPIO1_CTR**						
TYPE	RO	RW						
RESET	0x0	0x00						
BIT	7	6	5	4	3	2	1	0
NAME	**GPIO0_STAT**	**GPIO0_CTR**						
TYPE	RO	RW						
RESET	0x0	0x00						

Table 8-58: GPIO1 Register Description

Name	Description	Setting
GPIO1_CTR Bit 15	**GPIO 1 Status** – This bit provide the status of the te pin when it is configured as input.	
GPIO1_CTR Bit 14:8	**GPIO 1 Control** – These bits control the output behavior of the te pin.	Please see the description at bit 6-0.
GPIO0_CTR Bit 7	**GPIO 0 Status** – This bit provide the status of the dbcl pin when it is configured as input.	
GPIO0_CTR Bit 6:0	**GPIO 0 Control** – These bits control the output behavior of the dbcl pin.	Bit 0 – Module or Register This bit controls the pin to be module controlled or register controlled. 0 – Module controlled 1 – Register controlled Bit 1 – Direction This bit controls the direction of the pin when bit 0 is 1. When bit 0 is 0, it has no effect. 0 – Pin is input 1 – Pin is output Bit 2 : Output State This bit controls the output state of the pin when bit 0 is 1. When bit 0 is 0, it has no effect. 0 – Output state is 0 1 – Output state is 1 Bit 4-3 : Pull State These bits control the pull state of the pin when it is in input state. 00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper

Name	Description	Setting
		Bit 5 : Interrupt Enable This bit enables the GPIO0 input(bit 1 = 0) interrupt to the int pin. When bit 0 is 0, it has no effect. Bit 6 : Interrupt Polarity This bit selects the polarity of the GPIO0 input(bit 1 = 0) when bit 5 is enabled. When bit 0 is 0, it has no effect. 0 – Active low 1 – Active high

8.1.58 GPIO2 Register

Offset Address

GPIO2 **GPIO2 Register** **0xF0**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**GPIO2_STAT**	**GPIO2_CTR**						
TYPE	RO	RW						
RESET	0x0	0x00						

Table 8-59: GPIO1 Register Description

Name	Description	Setting
Reserved Bit 15-8		
GPIO2_CTR Bit 7	**GPIO 2 Status** – This bit provide the status of the sys_clk_out pin when it is configured as input.	
GPIO2_CTR Bit 6:0	**GPIO 2 Control** – These bits control the output behavior of the sys_clk_out pin.	Bit 0 – Module or Register This bit controls the pin to be module controlled or register controlled. 0 – Module controlled 1 – Register controlled Bit 1 – Direction This bit controls the direction of the pin when bit 0 is 1. When bit 0 is 0, it has no effect. 0 – Pin is input 1 – Pin is output Bit 2 : Output State This bit controls the output state of the pin when bit 0 is 1. When bit 0 is 0, it has no effect. 0 – Output state is 0 1 – Output state is 1 Bit 4-3 : Pull State These bits control the pull state of the pin when it is in input state. 00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper Bit 5 : Interrupt Enable

Name	Description	Setting
		This bit enables the GPIO0 input(bit 1 = 0) interrupt to the int pin. When bit 0 is 0, it has no effect. Bit 6 : Interrupt Polarity This bit selects the polarity of the GPIO0 input(bit 1 = 0) when bit 5 is enabled. When bit 0 is 0, it has no effect. 0 – Active low 1 – Active high

8.1.59 DLYA01 Register

Offset Address

DLYA01 **DLYA01 Register** **0xF1**

BIT	15	14	13	12	11	10	9	8
NAME			**DELAY_A_1**					
TYPE	RO	RO	RO					
RESET	0x0	0x0	0x20					
BIT	7	6	5	4	3	2	1	0
NAME			**DELAY_A_0**					
TYPE	RO	RO	RO					
RESET	0x0	0x0	0x20					

Table 8-60: DLYA01 Register Description

Name	Description	Setting
Reserved Bit 15-14		
DELAY_A_1 Bit 13-8	**DELAY A for lane 1** – These bits provide the status of the XOR calibration results when **XORC_SEL** is set to 0.	
Reserved Bit 7-6		
DELAY_A_0 Bit 5-0	**DELAY A for lane 0** – These bits provide the status of the XOR calibration results when **XORC_SEL** is set to 0.	

8.1.60 DLYA23 Register

Offset Address

DLYA23 **DLYA23 Register** **0xF2**

BIT	15	14	13	12	11	10	9	8
NAME			**DELAY_A_3**					
TYPE	RO	RO	RO					
RESET	0x0	0x0	0x20					
BIT	7	6	5	4	3	2	1	0
NAME			**DELAY_A_2**					
TYPE	RO	RO	RO					
RESET	0x0	0x0	0x20					

Table 8-61: DLYA23 Register Description

Name	Description	Setting
Reserved Bit 15-14		
DELAY_A_3 Bit 13-8	**DELAY A for lane 3** – These bits provide the status of the XOR calibration results when **XORC_SEL** is set to 0.	
Reserved Bit 7-6		
DELAY_A_2 Bit 5-0	**DELAY A for lane 2** – These bits provide the status of the XOR calibration results when **XORC_SEL** is set to 0.	

8.1.61 DLYB01 Register

Offset Address

DLYB01 **DLYB01 Register** **0xF3**

BIT	15	14	13	12	11	10	9	8
NAME			**DELAY_B_1**					
TYPE	RO	RO	RO					
RESET	0x0	0x0	0x20					
BIT	7	6	5	4	3	2	1	0
NAME			**DELAY_B_0**					
TYPE	RO	RO	RO					
RESET	0x0	0x0	0x20					

Table 8-62: DLYB01 Register Description

Name	Description	Setting
Reserved Bit 15-14		
DELAY_B_1 Bit 13-8	**DELAY B for lane 1** – These bits provide the status of the XOR calibration results when **XORC_SEL** is set to 1.	
Reserved Bit 7-6		
DELAY_B_0 Bit 5-0	**DELAY B for lane 0** – These bits provide the status of the XOR calibration results when **XORC_SEL** is set to 1.	

8.1.62 DLYB23 Register

Offset Address

DLYB23 **DLYB23 Register** **0xF4**

BIT	15	14	13	12	11	10	9	8
NAME			**DELAY_B_3**					
TYPE	RO	RO	RO					
RESET	0x0	0x0	0x20					
BIT	7	6	5	4	3	2	1	0
NAME			**DELAY_B_2**					
TYPE	RO	RO	RO					
RESET	0x0	0x0	0x20					

Table 8-63: DLYB23 Register Description

Name	Description	Setting
Reserved Bit 15-14		
DELAY_B_3 Bit 13-8	**DELAY B for lane 3** – These bits provide the status of the XOR calibration results when **XORC_SEL** is set to 1.	
Reserved Bit 7-6		
DELAY_B_2 Bit 5-0	**DELAY B for lane 2** – These bits provide the status of the XOR calibration results when **XORC_SEL** is set to 1.	

8.1.63 DLYC01 Register

Offset Address

DLYC01 **DLYC01 Register** **0xF5**

BIT	15	14	13	12	11	10	9	8
NAME			**DELAY_C_1**					
TYPE	RO	RO	RO					
RESET	0x0	0x0	0x20					
BIT	7	6	5	4	3	2	1	0
NAME			**DELAY_C_0**					
TYPE	RO	RO	RO					
RESET	0x0	0x0	0x20					

Table 8-64: DLYC01 Register Description

Name	Description	Setting
Reserved Bit 15-14		
DELAY_C_1 Bit 13-8	**DELAY C for lane 1** – These bits provide the status of the average XOR calibration results from DELAY_A_1 and DELAY_B_1.	
Reserved Bit 7-6		
DELAY_C_0 Bit 5-0	**DELAY C for lane 0** – These bits provide the status of the average XOR calibration results from DELAY_A_0 and DELAY_B_0.	

8.1.64 DLYC23 Register

Offset Address

DLYC23 **DLYC23 Register** **0xF6**

BIT	15	14	13	12	11	10	9	8
NAME			**DELAY_C_3**					
TYPE	RO	RO	RO					
RESET	0x0	0x0	0x20					
BIT	7	6	5	4	3	2	1	0
NAME			**DELAY_C_2**					
TYPE	RO	RO	RO					
RESET	0x0	0x0	0x20					

Table 8-65: DLYC23 Register Description

Name	Description	Setting
Reserved Bit 15-14		
DELAY_C_3 Bit 13-8	**DELAY C for lane 3** – These bits provide the status of the average XOR calibration results from DELAY_A_3 and DELAY_B_3.	
Reserved Bit 7-6		
DELAY_C_2 Bit 5-0	**DELAY C for lane 2** – These bits provide the status of the average XOR calibration results from DELAY_A_2 and DELAY_B_2.	

8.1.65 Analog Control Register 5

Offset Address

ACR5 **ACR5 Register** **0xF7**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**DEC_XOR_E**	**DEC_FB_E**	**D3_FB_E**	**D2_FB_E**	**D1_FB_E**	**D0_FB_E**	**XOR_TUNE_EN**	**REG_CTR**
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-66: ACR5 Register Description

Name	Description	Setting
Reserved Bit 15-8		
DEC_XOR_E Bit 7	**DECoder XOR Enable** – This bit enables the XOR function in the analog when Bit[0] is set. This bit is used for internal testing and should be programmed to 0 for normal use.	
DEC_FB_E Bit 6	**DECoder FeedBack Enable** – This bit enables the Decoder function in the analog when Bit[0] is set. This bit is used for internal testing and should be programmed to 0 for normal use.	
D3_FB_E Bit 5	**D3 FeedBack Enable** – This bit enables the XOR Feedback Tuning for lane 3 when Bit[0] is set. This bit is used for internal testing and should be programmed to 0 for normal use.	
D2_FB_E Bit 4	**D2 FeedBack Enable** – This bit enables the XOR Feedback Tuning for lane 2 when Bit[0] is set. This bit is used for internal testing and should be programmed to 0 for normal use.	
D1_FB_E Bit 3	**D1 FeedBack Enable** – This bit enables the XOR Feedback Tuning for lane 1 when Bit[0] is set. This bit is used for internal testing and should be programmed to 0 for normal use.	
D0_FB_E Bit 2	**D0 FeedBack Enable** – This bit enables the XOR Feedback Tuning for lane 0 when Bit[0] is set.	

Name	Description	Setting
	This bit is used for internal testing and should be programmed to 0 for normal use.	
XOR_TUNE_EN Bit 1	**XOR TUNE ENable** – This bit enables the XOR Feedback Tuning when Bit[0] is set. This bit is used for internal testing and should be programmed to 0 for normal use.	
REG_CTR Bit 0	**Analog REGister ConTRol** – This bit enable the control of the XOR feedback tuning through register Bit[7:1] or through Analog Test mode 4. This bit is used for internal testing and should be programmed to 0 for normal use.	0 – Controlled by Analog Test mode 4. 1 – Controlled from Bit[7:1].

8.1.66 Read Register

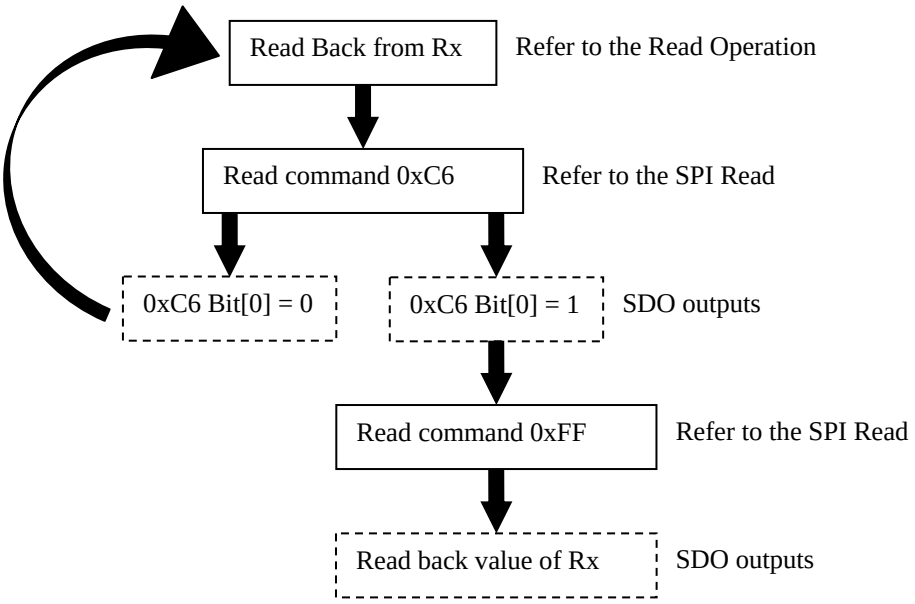
Offset Address

RR **Read Register** **0xFF**

BIT	15	14	13	12	11	10	9	8
NAME	**RD[15:8]**							
TYPE	RO							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**RD[7:0]**							
TYPE	RO							
RESET	0x00							

Table 8-67: Read Register Description

Name	Description	Setting
RD Bit 15-0	**Read Data** – This register is not a true register. It is the entry point for the internal buffer. It is used to read the data returned by the MIPI slave. The application processor can treat this register as an FIFO and continuously read data from it. When the interface is 16-bit, the width of this field is 16-bit. When the interface is 8-bit, the width of this field is 8-bit. The read of this register is only valid when the **RDY** bit is 1. In other words, only when the data returned by the MIPI slave is received, the application processor can read this register to get return data.	



9 Configuration

The SSD2828 can be configured to support various operations. The signals involved are ps[1:0] pins, LS register bits. These signals define the interface type supported at the front-end as well as lane distribution at the MIPI link. The features that define the operation of SSD2828 are as below.

- Number of lane for each MIPI link
- RGB and SPI interfaces select at the front-end
- Dump and smart configurations

9.1 Lane Management

The number of lanes used in SSD2828 is determined by the LS(0xDE[1:0]) bits. The SSD2828 DPHY lanes consist of 1 clock lane(CL) and 4 data lanes(DL0, DL1, DL2, DL3).

The table below list down all the combination of lane usage and the active state of each of the DPHY lanes.

LS	SSD2828	CL	DL0	DL1	DL2	DL3	Max. Speed
00	1 lane	ON	ON	OFF	OFF	OFF	Up to 1.0Gbps
01	2 lanes	ON	ON	ON	OFF	OFF	Up to 2.0Gbps
10	3 lanes	ON	ON	ON	ON	OFF	Up to 3.0Gbps
11	4 lanes	ON	ON	ON	ON	ON	Up to 4.0Gbps

Table 9-1: SSD2828 Lane Management

9.2 Use cases

The SSD2828 can support one interface configuration. Combination of RGB and SPI interfaces. The details of supported configuration are listed below.

9.2.1 RGB + SPI Interface

The application processor can use this configuration to drive a dumb display panel or a smart display panel or both panels. The user needs to set ps[1:0] to select the desired SPI interface. When the SPI interface is not used, the csx pin needs to be kept high.

Since the RGB and SPI interface are completely separated, the two interfaces can operate independently. The RGB interface is used to provide display data for the video mode. The SPI interface is used to program the local registers of SSD2828. If a dumb display panel is driven and the registers of the display need to be programmed, the SPI interface can also be used for register programming. If a smart display panel is driven, the SPI interface can also be used to configure the smart display and send display data, in command mode. Below are some illustrations for the use case.

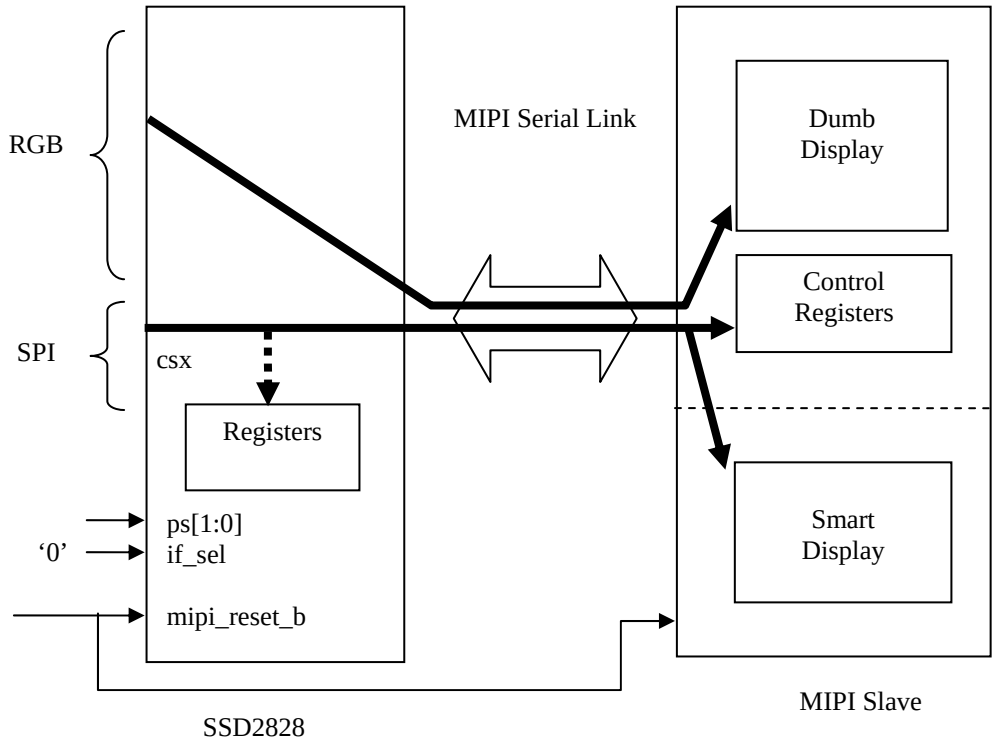


Figure 9-1: SSD2828 with RGB and SPI Interface

The data for different destinations are separated by the VC field of the packets. The user can program the register **VCR** to set the VC field. When this configuration is used, the primary usage of the serial link is for sending display video data to the dumb panel. If there is a need to send non-video data through SPI interface concurrently, the SSD2828 can put them into generic write or DCS write packet and interleave them with the video packets.

If the non-burst video mode is selected, the non-video data packet will only be sent during vertical blanking period. If burst video mode is selected, the non-video data packet can be sent during both horizontal and vertical blanking period (e.g. BLLP period).

During both horizontal and vertical blanking period, the serial link can either remain in HS mode (sending blanking packet) or enter LP mode. The non-video data can also be sent in HS or LP mode. Options have been provided for whether to use HS or LP mode for the blanking period and whether to send the non-video data in HS or LP mode. The **NVD** and **BLLP** bits in register **VICR6** are provided for this purpose. Please refer to the table below for details.

Table 9-2: Operation during Video Mode BLLP Period

NVD	BLLP	Non-burst mode	Burst mode
0	0	If there is no non-video data to send, the serial link will send blanking packet in HS mode during BLLP period. If there is non-video data to send, the non-video data will be sent in HS mode. Afterwards, the serial link will send blanking packet in HS mode for the remaining period of BLLP period.	If there is no non-video data to send, the serial link will enter LP mode during BLLP period. If there is non-video data to send, non-video data will be sent in HS mode. Afterwards, the serial link will enter LP mode for the remaining period of BLLP period.
0	1	If there is no non-video data to send, the serial link will enter LP mode during BLLP period. If there is non-video data to send, non-video data will be sent in HS mode. Afterwards, the serial link will enter LP mode for the remaining period of BLLP period.	Same as non-burst mode.
1	x	The serial link will enter LP mode for BLLP mode. If there is non-video data to send, the data will be sent in LP mode at the beginning of BLLP period.	Same as non-burst mode.

9.2.2 MIPI DC Characteristics

Different State Code of the DSI represents different DC voltage levels in the Data and Clock Lanes as stated in below table.

Table 9-3: DSI State Code and DC Characteristics

State Code	Line Voltage Levels	
	Dp-Line	**Dn-Line**
HS-0	HS Low	HS High
HS-1	HS High	HS Low
LP-00	LP Low	LP Low
LP-01	LP Low	LP High
LP-10	LP High	LP Low
LP-11	LP High	LP High

As shown in Figure 9-2, the logic level is different in different state.

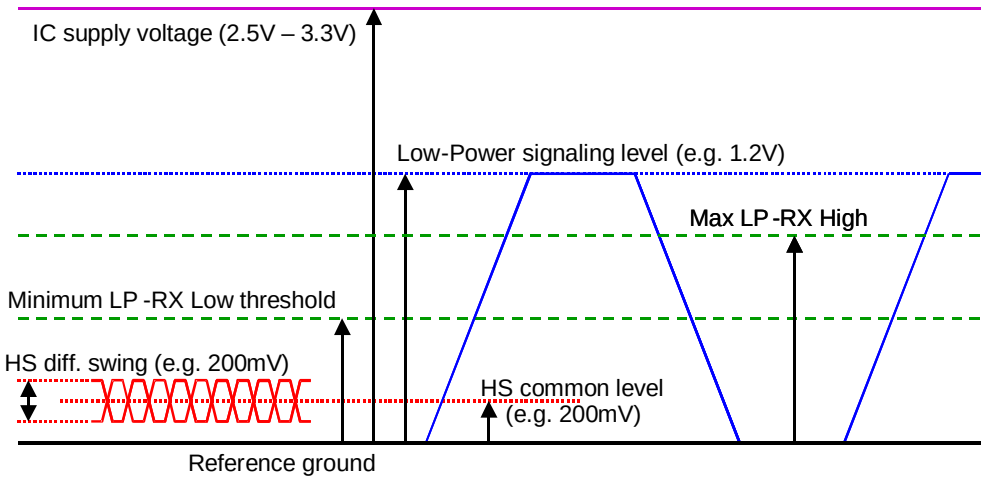


Figure 9-2: MIPI Line Levels

9.2.3 High Speed Clock Transmission

In High-Speed mode the Clock Lane provides a low-swing, differential DDR (half-rate) clock signal from Master to Slave for High-Speed Data Transmission. The Clock Start and Stop procedures are shown in the following figure.

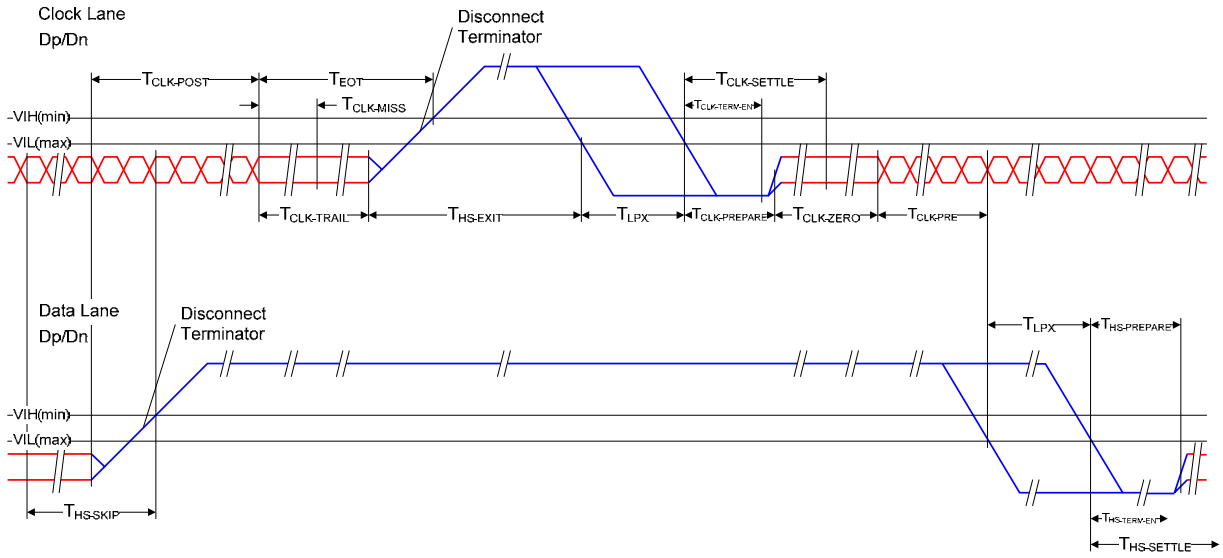


Figure 9-3: Switching the Clock Lane between High Speed Mode and Low-Power Mode

9.2.4 Data Lane State Flow

There are three modes that the Data Lane can be driven into:

1. High Speed Data Transmission
2. Bi-Directional Data Lane Turnaround
3. Escape Mode

Table 9-4: Data Lane Mode Entering/Exiting Sequences

Mode	Entering Mode Sequences	Exiting Mode Sequences
High Speed Data Transmission	LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00	LP-00 =>LP-10 =>LP-11
Bi-Directional Data Lane Turnaround	LP-11 =>LP-01 =>LP-00 =>HS-0	(HS-0 or HS-1) =>LP-11
Escape	LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00	High-Z

9.2.5 High Speed Data Transmission

High-Speed Data Transmission occurs in bursts. Transmission starts from, and ends with, a Stop state. During the intermediate time between bursts a Data Lane shall remain in the Stop state, unless a Turnaround or Escape request is presented on the Lane. During a HS Data Burst the Clock Lane shall be in High-Speed mode, providing a DDR Clock to the Slave side.

After a Transmit request, a Data Lane leaves the Stop state and prepares for High-Speed mode by means of a Start-of-Transmission (SoT) procedure.
Table 9-5 describes the sequence of events on TX and RX side.

Table 9-5: Start-of-Transmission Sequence

Observes Stop state
Observes transition from LP-11 to LP-01 on the Lines
Observes transition form LP-01 to LP-00 on the Lines, enables Line Termination after time $T_{D\text{-}TERM\text{-}EN}$
Enables HS-RX and waits for Time-out $T_{HS\text{-}SETTLE}$ in order to neglect transition effects
Starts looking for Leader-Sequence
Synchronizes upon recognition of Leader Sequence '011101'
Receives payload data

At the end of a Data Burst, a Data Lane leaves High-Speed Transmission mode and enters the Stop state by means of an End-of-Transmission (EoT) procedure. Table 9-6 shows a possible sequence of events during the EoT procedure. Note, EoT processing may be handled by the protocol or by the D-PHY.

Table 9-6: End-of-Transmission Sequence

Receives payload data
Detects the Lines leaving LP-00 state and entering Stop state (LP-11) and disables Termination
Neglect bits of last period $T_{HS\text{-}SKIP}$ to hide transition effects
Detect last transition in valid Data, determine last valid Data byte and skip trailer sequence

The following shows the sequence of the high speed data transmission including SoT data.

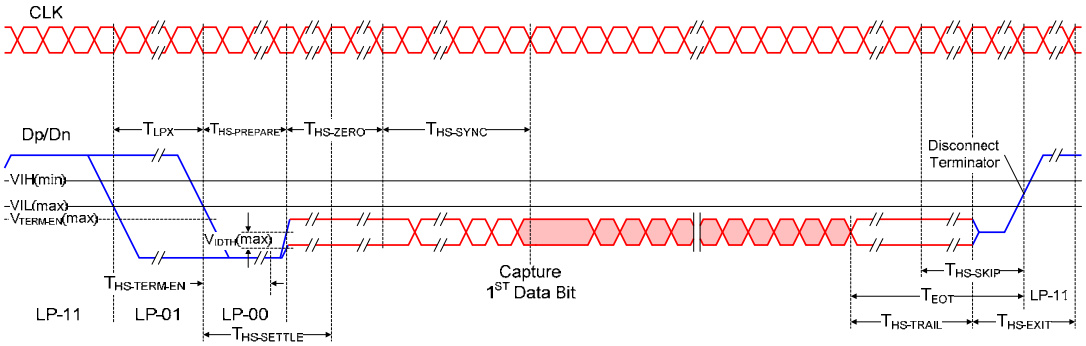


Figure 9-4: High-Speed Data transmission in Bursts

9.2.6 Bi-Directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction.

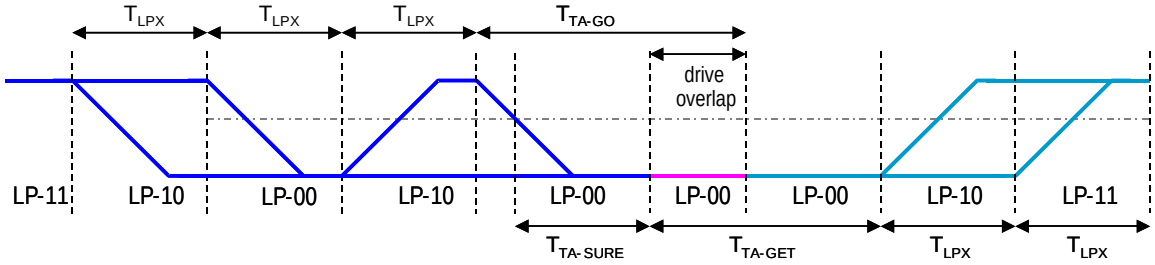


Figure 9-5: Turnaround Procedure

9.2.7 Escape Mode

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and is optional in the Reverse direction. If supported, Escape mode does not have to include all available features.

A Data Lane enters Escape mode via an Escape mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape mode in Space state (LP-00). If an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

For Data Lanes, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. Table 9-7 lists all currently available Escape mode commands and actions. All unassigned commands are reserved for future expansion.

The Stop state is be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state.

Table 9-7: MIPI Escape Mode Entry Code

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Tearing Effect	Trigger	01011101
Acknowledge	Trigger	00100001
Unknown-5	Trigger	10100000

9.2.8 Low Power Data Transmission

The Low Power Data Transmission can be started as the following sequences:

- Start: LP-11
- Escape Mode Entry: LP-11, LP-10, LP-00, LP-01,LP-00
- Low Power Data Transmission command: 11100001
  - One or more bytes (8 bit)
  - Pause mode when data lane are stopped
- Exit Escape Mode: LP-00, LP-10, LP-11
- Stop State : LP-11

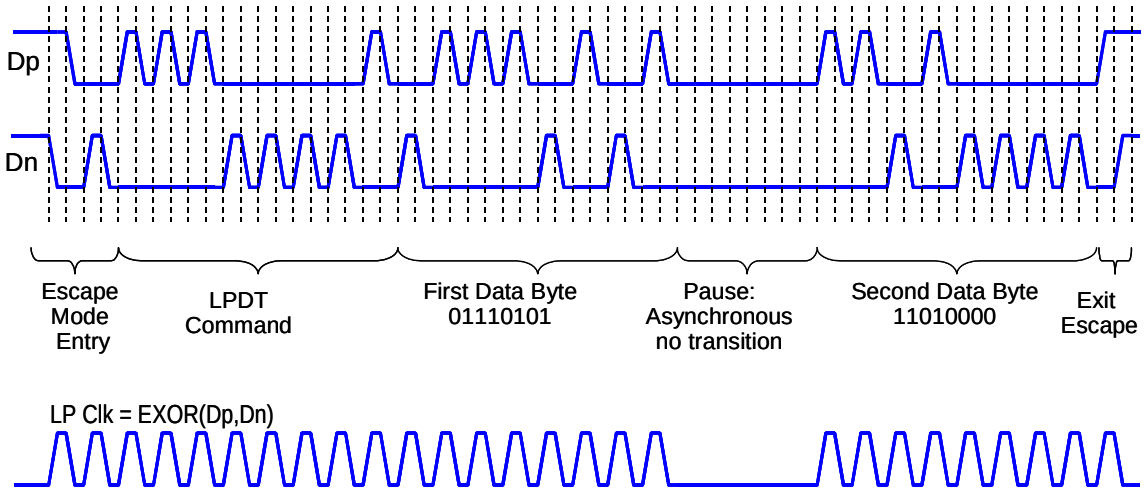


Figure 9-6: Low Power Data Transmission

9.2.9 Reset Trigger

The AP can inform to the display module that it should be reseted in Reset trigger when data lanes are entering in Escape Mode.
The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11, LP-10, LP-00, LP-01, LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00, LP-10, LP-11
- Stop State: LP-11

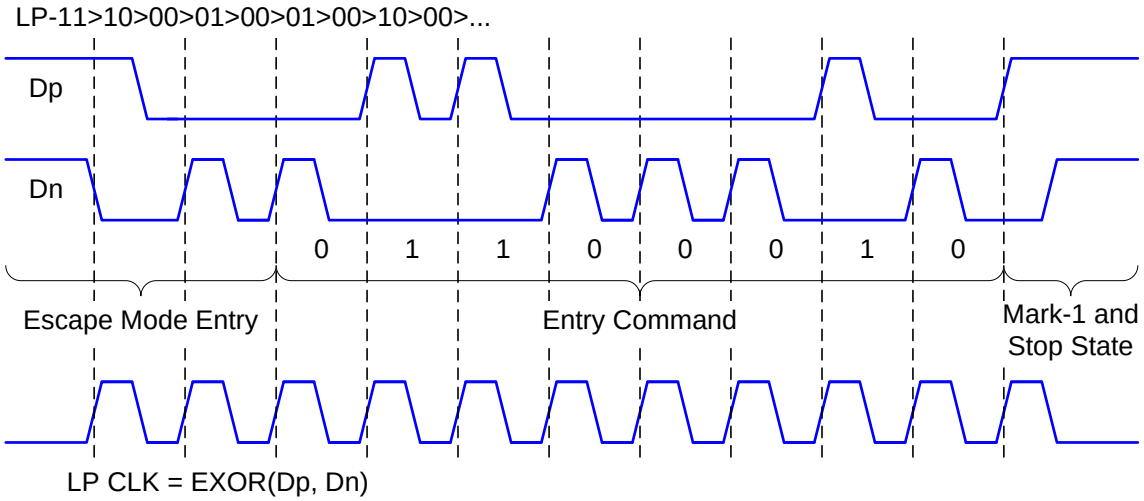


Figure 9-7: Trigger – Reset Command in Escape Mode

9.2.10 Tearing Effect

The display module can inform to the AP when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11, LP-10, LP-00, LP-01, LP-00
- Tearing Effect: 0101 1101 (First to Last bit)
- Mark-1: LP-00, LP-10, LP-11
- Stop State: LP-11

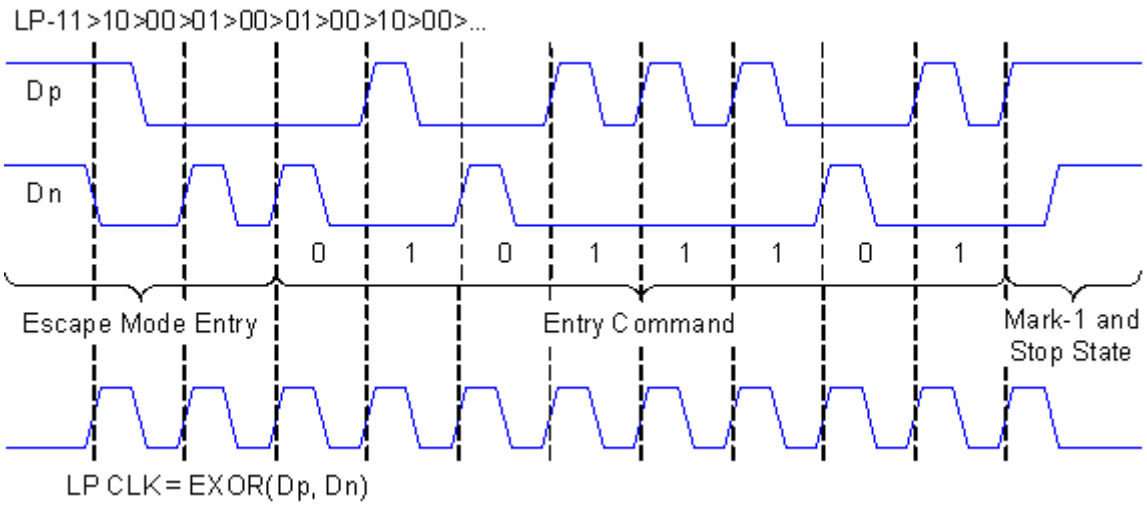


Figure 9-8: Tearing Effect Command in Escape Mode

9.2.11 Acknowledge

The display module can inform to the AP when an error has not recognized on it by Acknowledge (ACK). The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11, LP-10, LP-00, LP-01, LP-00
- Acknowledge (ACK) command: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- Stop State: LP-11

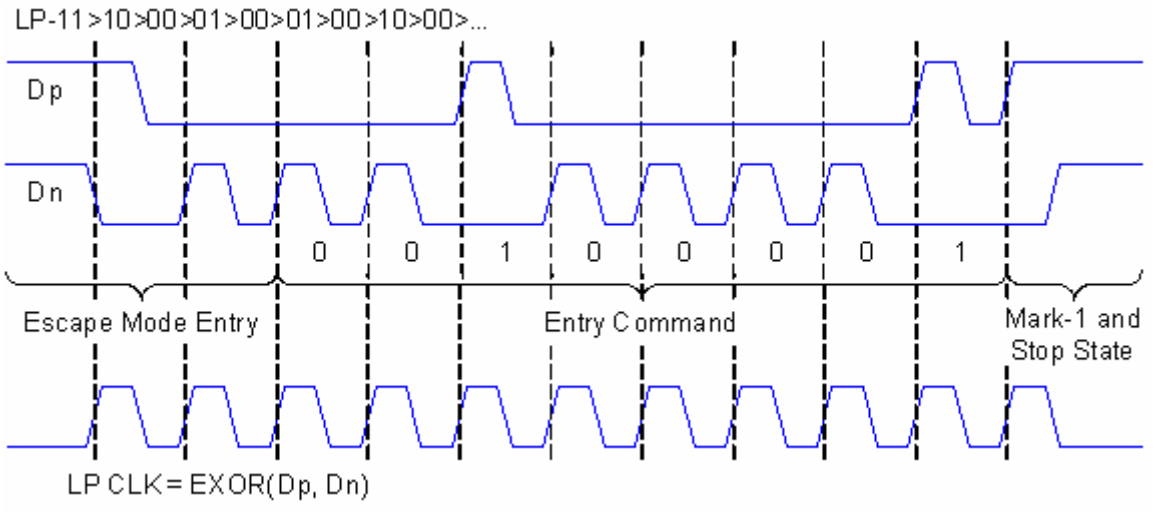
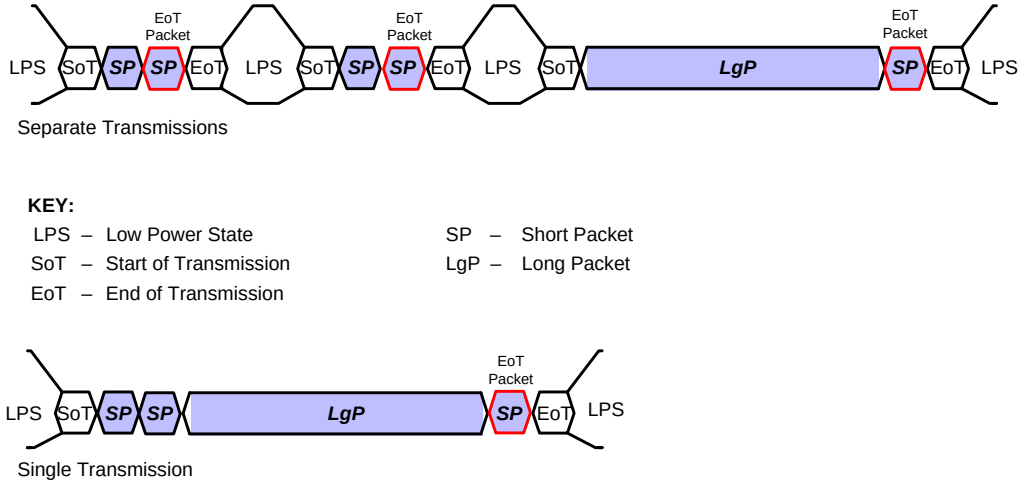


Figure 9-9: Acknowledge Command in Escape Mode

9.2.12 Packet Transmission

SSL MIPI CORE supports two data transmission defined in MIPI DSI specification.

Figure 9-10: Two Data Transmission Mode (Separate, single)



9.2.13 HS Transmission Example

Figure 9-11: One Lane Data Transmission Example

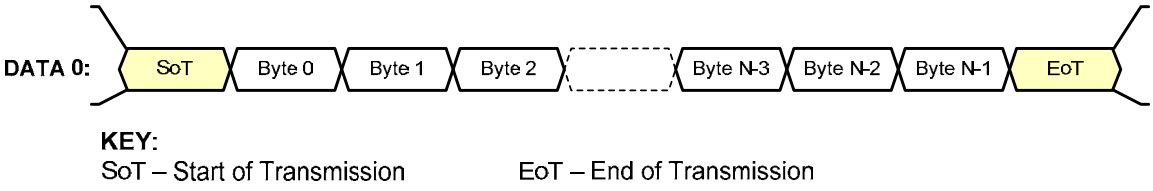
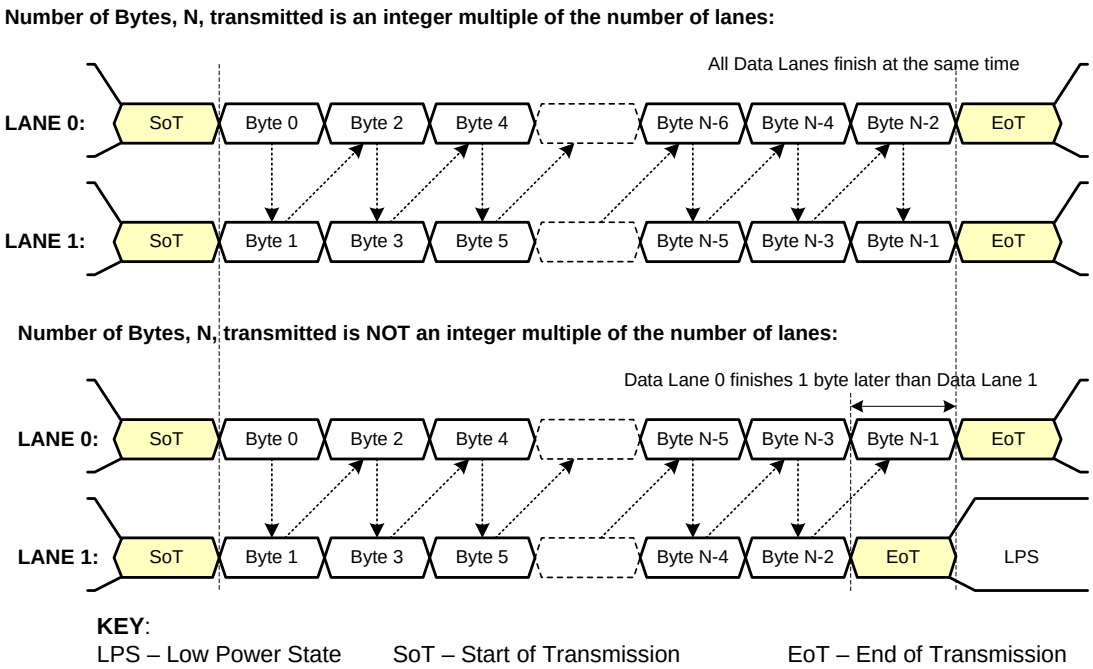


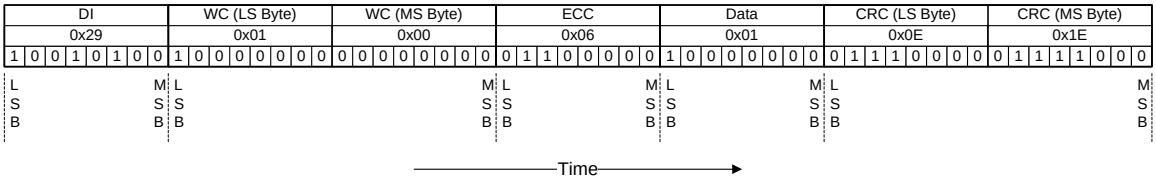
Figure 9-12: Two Lane HS Transmission Example



9.2.14 General Packet Structure

Two packet structures are defined for low-level protocol communication: Long packets and Short packets. For both packet structures, the Data Identifier is always the first byte of the packet. All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

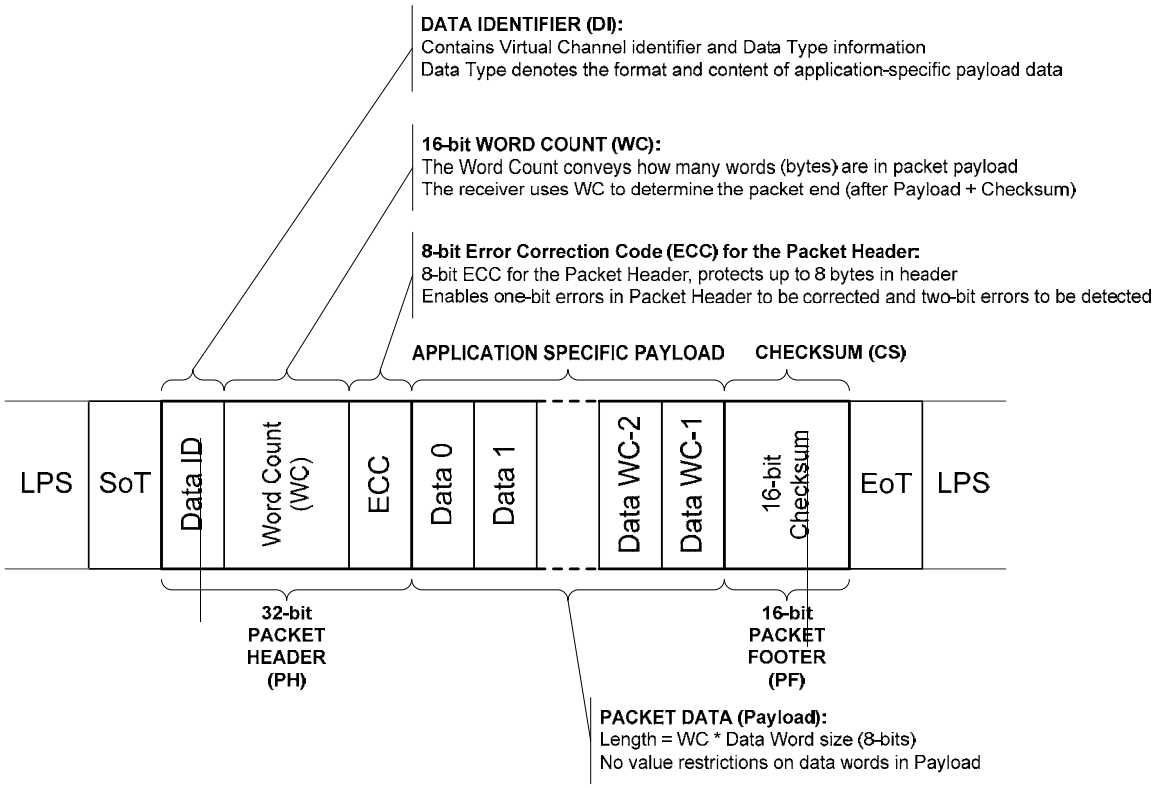
Figure 9-13: Endian Example (Long Packet)



9.2.15 Long Packet Format

Figure 9-14 shows the structure of the Long packet. A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

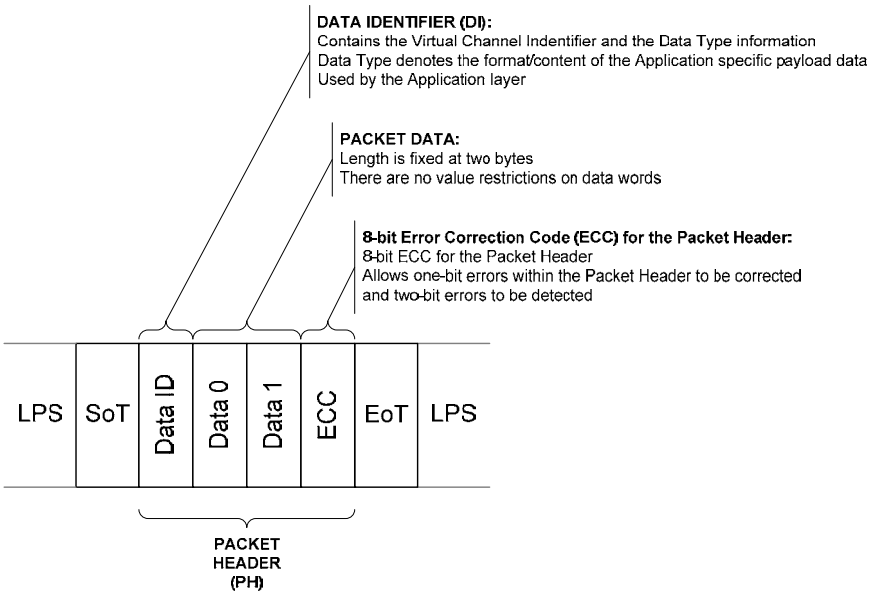
Figure 9-14: Long Packet Structure



9.2.16 Short Packet Structure

Figure 9-15 shows the structure of the Short packet. A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.

Figure 9-15: Short Packet Structure



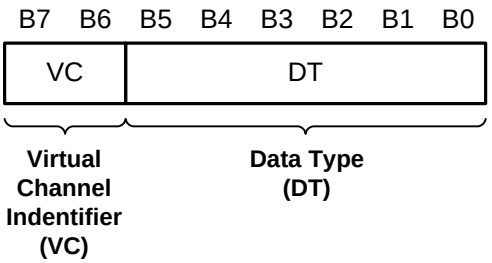
All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

Figure 9-13 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

9.2.17 Data Identifier (DI)

The Data Identifier defines the Virtual Channel for the data and the Data Type for the application specific payload data.

Figure 9-16: Data Indentifier Structure



9.2.18 Victual Channel Identifier (VC)

The VC is the address of the channel between the AP and the display modules. During the data transactions, both AP and display module will use the same VC for communication. In SSD2085, the VC for the command mode is 0x02H and the VC for the video mode is 0x01H.

9.2.19 Data Type (DT)

There are two groups of Data Type:

- Processor to Display Module,
- Display Module to Processor

Table 9-8: Data Types for Processor-sourced Packets

Data Type, hex	Data Type, binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission (EoT) packet	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	Generic READ, no parameters	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS WRITE, no parameters	Short
15h	01 0101	DCS WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long

Data Type, hex	Data Type, binary	Description	Packet Size
19h	01 1001	Blanking Packet, no data	Long
29h	10 1001	Generic Long Write	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
x0h and xFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

Table 9-9: Data Types for Peripheral-sourced Packets

Data Type, hex	Data Type, binary	Description	Packet Size
00h – 01h	00 000x	Reserved	Short
02h	00 0010	Acknowledge and Error Report	Short
03h – 07h	00 0011 – 00 0111	Reserved	
08h	00 1000	End of Transmission (EoT) packet	Short
09h – 10h	00 1001 – 01 0000	Reserved	
11h	01 0001	Generic Short READ Response, 1 byte returned	Short
12h	01 0010	Generic Short READ Response, 2 bytes returned	Short
13h – 19h	01 0011 – 01 1001	Reserved	
1Ah	01 1010	Generic Long READ Response	Long
1Bh	01 1011	Reserved	
1Ch	01 1100	DCS Long READ Response	Long
1Dh – 20h	01 1101 – 10 0000	Reserved	
21h	10 0001	DCS Short READ Response, 1 byte returned	Short
22h	10 0010	DCS Short READ Response, 2 bytes returned	Short
23h – 3Fh	10 0011 – 11 1111	Reserved	

Figure 9-17: 16-bit per pixel RGB Color Format, Long packet for MIPI Interface

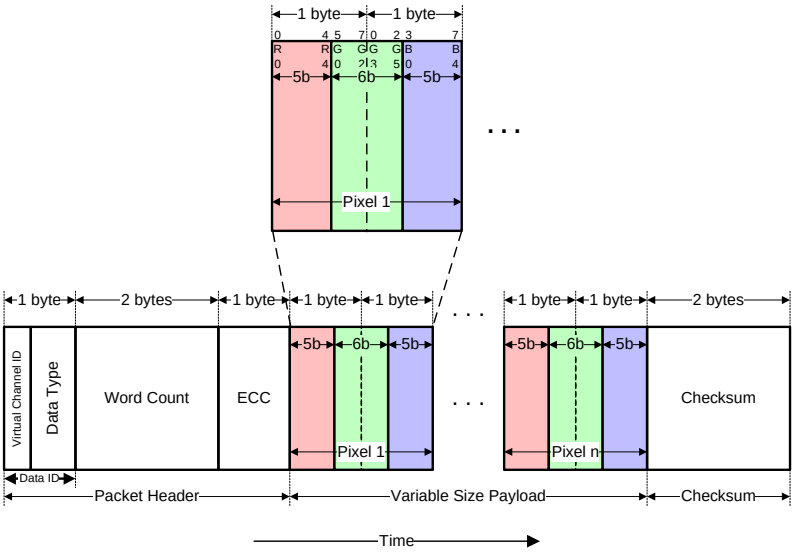


Figure 9-18: 18-bit per Pixel– RGB Color Format, Long packet for MIPI Interface

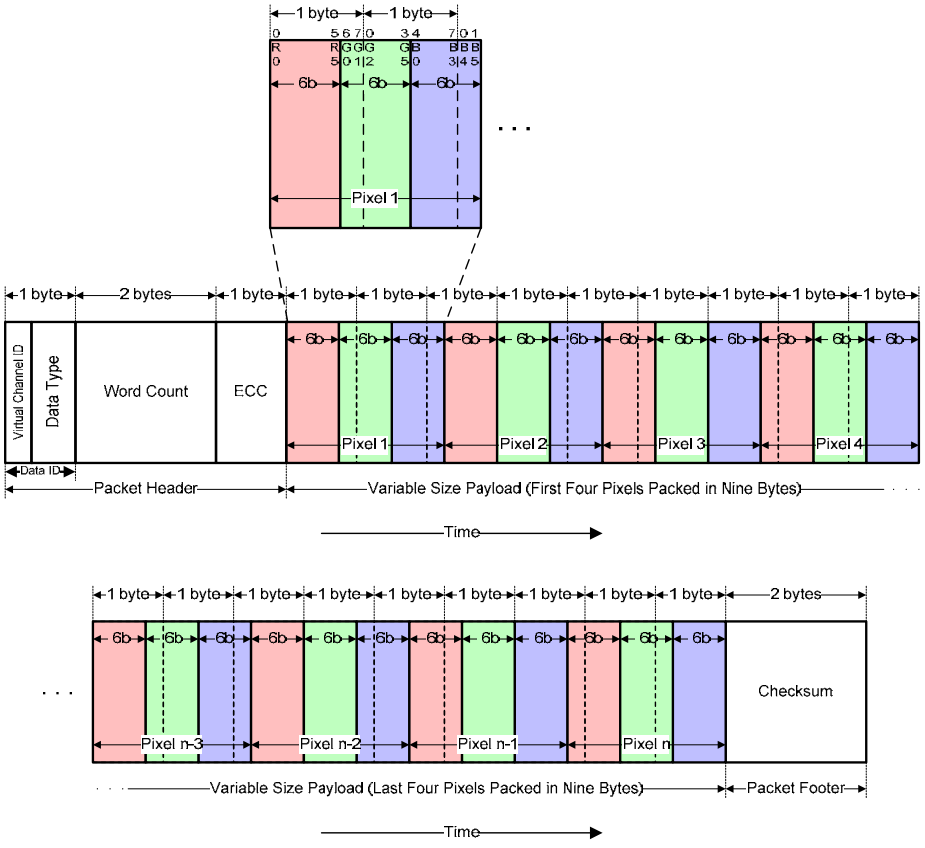


Figure 9-19: 18-bit per Pixel in Three Bytes – RGB Color Format, Long packet for MIPI Interface

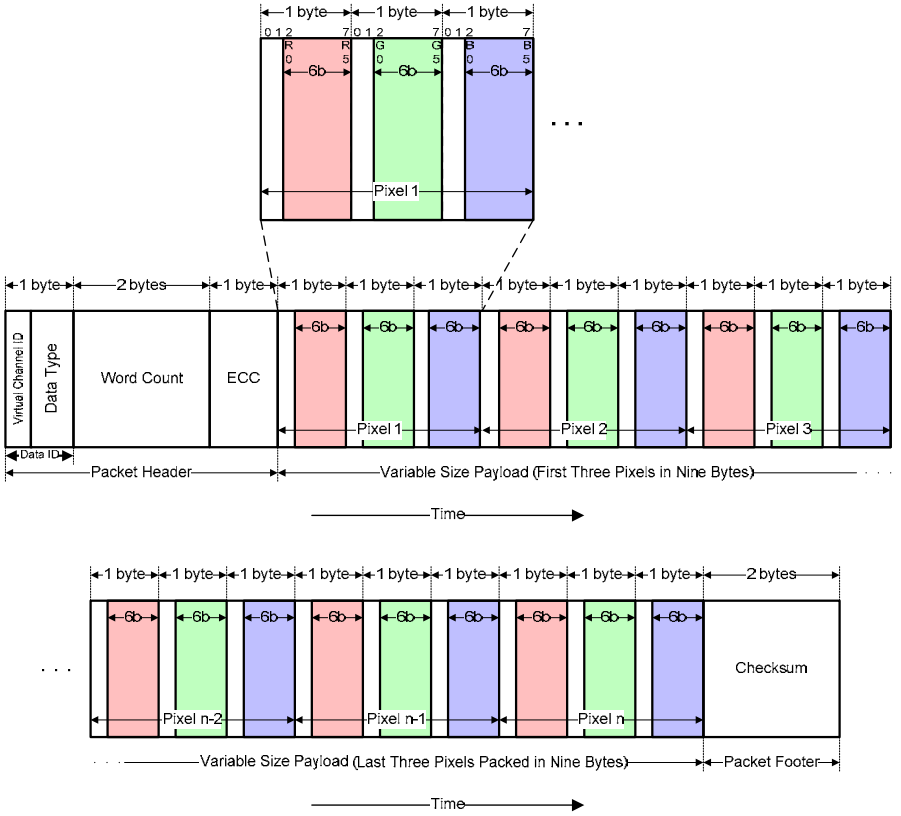
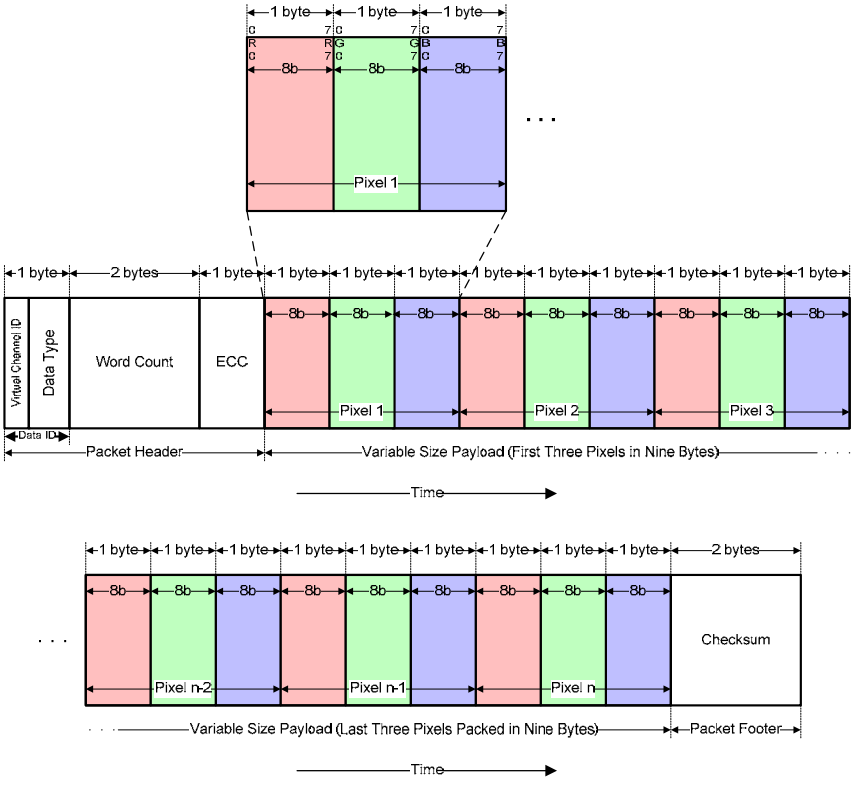


Figure 9-20: 24-bit per Pixel – RGB Color Format, Long packet for MIPI Interface



9.3 Operating Modes

The video data come from the RGB interface and the configuration is done through the SPI interface. To support different bpp settings, the following data pins are used. For all cases, R should be at the upper bits and B should be at the lower bits.

- data[15:0] for 16 bpp.
- data[17:0] for 18 bpp, packed.
- data[17:0] for 18 bpp, loosely packed.
- data[23:0] for 24 bpp.

The user, first, needs to program the registers **VICR1** to **VICR6** with correct values. The user also needs to program the **END** and **CO** bits to 0 and 1 respectively. After programming those register fields, the user can turn on the RGB interface and enable the **VEN** bit to start transmission. All three video mode sequence defined in the MIPI DSI specification are supported.

In Non-Burst Mode, the **CSS** (register 0xB7 bit 5) can be set to 0 or 1. When it is set to 1 to select the pclk as PLL reference clock, the PLL multiplication factor should be equal to the bpp value. When it is set to 0 to select the tx_clk as PLL reference clock, the PLL multiplication factor should be set such that the serial link data rte is faster than the incoming data rate. Please refer to the table below for the PLL settings. Registers **VICR1** to **VICR6** (0xB1 to 0xB6) needs to be programmed. (**VICR1** is not used for non-burst mode with Sync Events). (**VICR1** is not used for non-burst mode with Sync Events.) Below is the diagram to illustrate the definition of all the fields.

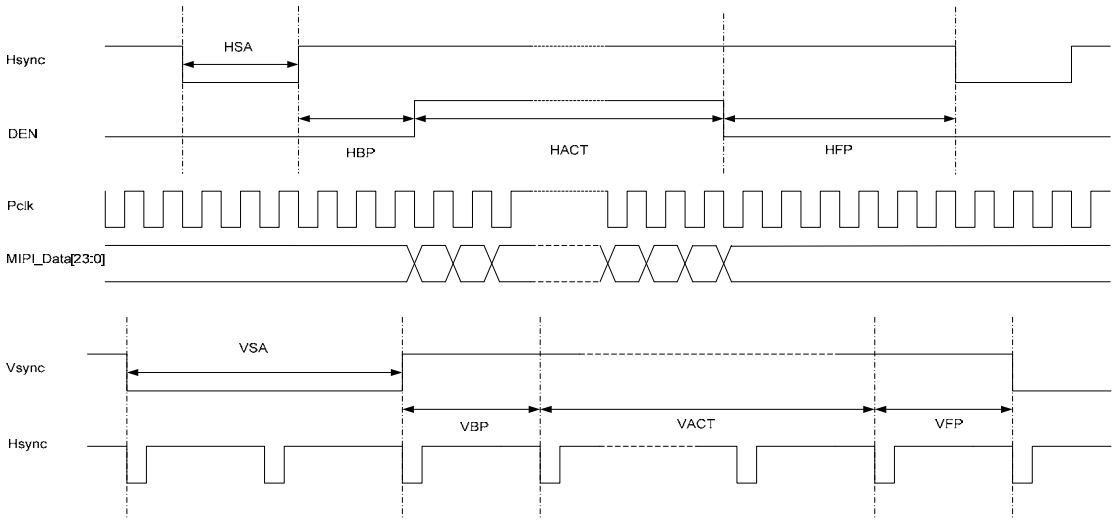


Figure 9-21: Illustration of RGB Interface Parameters for Non-burst Mode with Sync Pulses

Table 9-10: PLL Setting for Non-burst Mode (PLL reference using pclk)

BPP (bit per pixel)	PLL Multiplication Factor		PLL Output Clock Frequency	
	1 data lane	**2 data lane**	**1 data lane**	**2 data lane**
16	16	8	16 x pclk	8 x pclk
18, packed	18	9	18 x pclk	9 x pclk
18, loosely packed	24	12	24 x pclk	12 x pclk
24	24	12	24 x pclk	12 x pclk
	3 data lane	**4 data lane**	**3 data lane**	**4 data lane**
16	5.33	4	5.33 x pclk	4 x pclk
18, packed	6	4.5	6 x pclk	4.5 x pclk
18, loosely packed	8	6	8 x pclk	6 x pclk
24	8	6	8 x pclk	6 x pclk

Table 9-11: PLL Setting for Non-burst Mode (PLL reference using tx_clk)

BPP (bit per pixel)	PLL Multiplication Factor		PLL Output Clock Frequency	
	1 data lane	**2 data lane**	**1 data lane**	**2 data lane**
16	NA	NA	>= 16 x pclk	>= 8 x pclk
18, packed	NA	NA	>= 18 x pclk	>= 9 x pclk
18, loosely packed	NA	NA	>= 24 x pclk	>= 12 x pclk
24	NA	NA	>= 24 x pclk	>= 12 x pclk
	3 data lane	**4 data lane**	**3 data lane**	**4 data lane**
16	NA	NA	>= 5.33 x pclk	>= 4 x pclk
18, packed	NA	NA	>= 6 x pclk	>= 4.5 x pclk
18, loosely packed	NA	NA	>= 8 x pclk	>= 6 x pclk
24	NA	NA	>= 8 x pclk	>= 6 x pclk

In Burst Mode, the **CSS** (register 0xB7 bit 5) needs to be set to 0 to select the tx_clk as PLL reference clock. The PLL multiplication factor should be set such that the serial link data rate is faster than the incoming data rate. Please refer to the table below for the PLL settings. Registers **VICR2** to **VICR6** (0xB1 to 0xB6) needs to be programmed. **VICR1** is not used for this mode. The definition of all the fields is the same as non-burst mode with Sync Events.

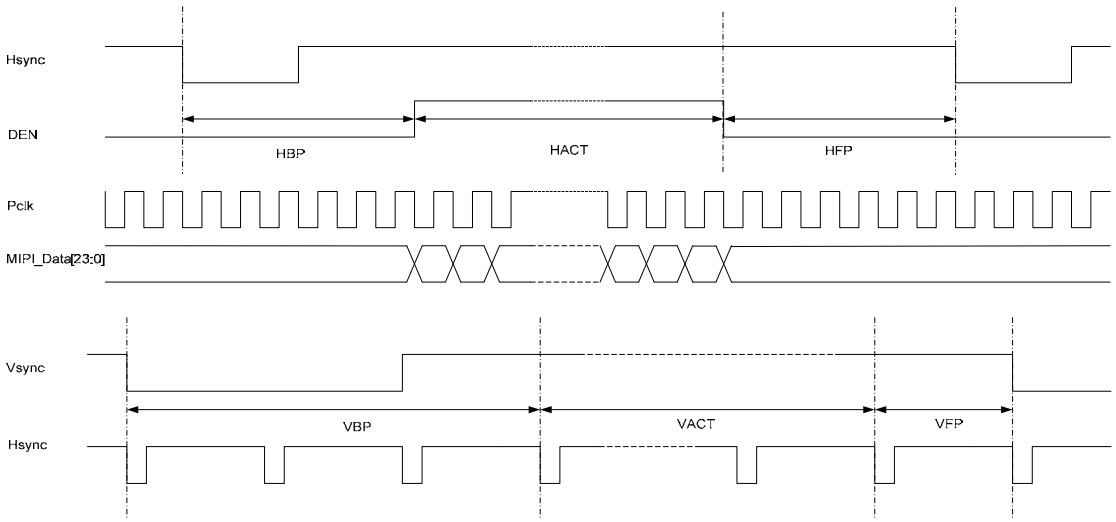


Figure 9-22: Illustration of RGB Interface Parameters for Non-burst Mode with Sync Events and Burst Mode

Table 9-12: PLL Setting for Burst Mode

BPP (bit per pixel)	PLL Multiplication Factor		PLL Output Clock Frequency	
	1 data lane	**2 data lane**	**1 data lane**	**2 data lane**
16	NA	NA	>= 16 x pclk	>= 8 x pclk
18, packed	NA	NA	>= 18 x pclk	>= 9 x pclk
18, loosely packed	NA	NA	>= 24 x pclk	>= 12 x pclk
24	NA	NA	>= 24 x pclk	>= 12 x pclk
	3 data lane	**4 data lane**	**3 data lane**	**4 data lane**
16	NA	NA	>= 5.33 x pclk	>= 4 x pclk
18, packed	NA	NA	>= 6 x pclk	>= 4.5 x pclk
18, loosely packed	NA	NA	>= 8 x pclk	>= 6 x pclk
24	NA	NA	>= 8 x pclk	>= 6 x pclk

*: This value should be set such that the serial link data rate is faster than incoming data rate

The SSD2828 will also monitor the status of CM and SHUT signal. When there is a change of these signals, it will send out appropriate packets. On the rising edge of CM, the CM on packet will be sent. On the falling edge of CM, the CM off packet will be sent. On the rising edge of SHUT, the Shut Down Peripheral packet will be sent. On the falling edge of SHUT, the Turn On Peripheral packet will be sent. With these packets, the MIPI slave will be able to reconstruct the RGB interface signals.

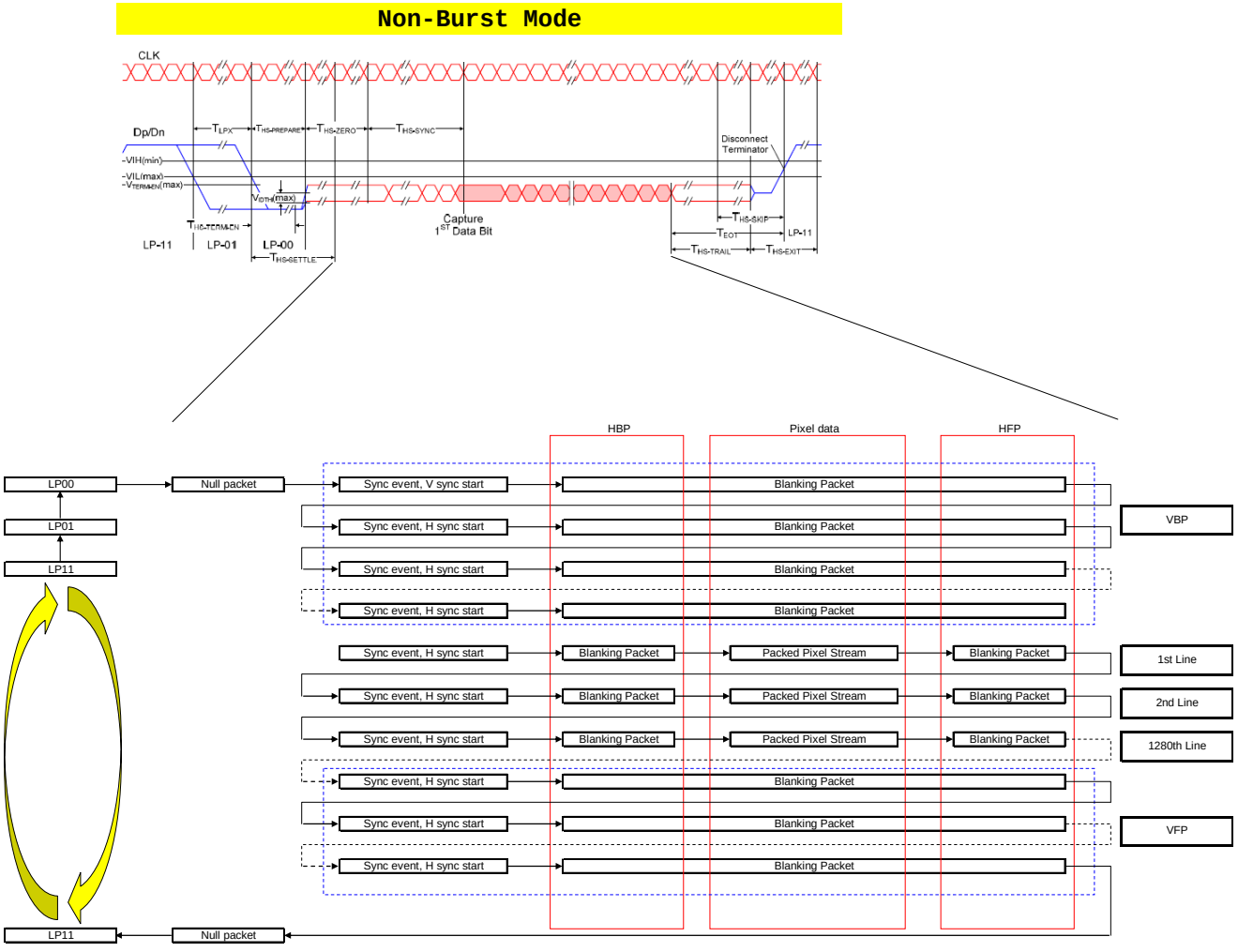


Figure 9-23: Non-Burst mode MIPI structure

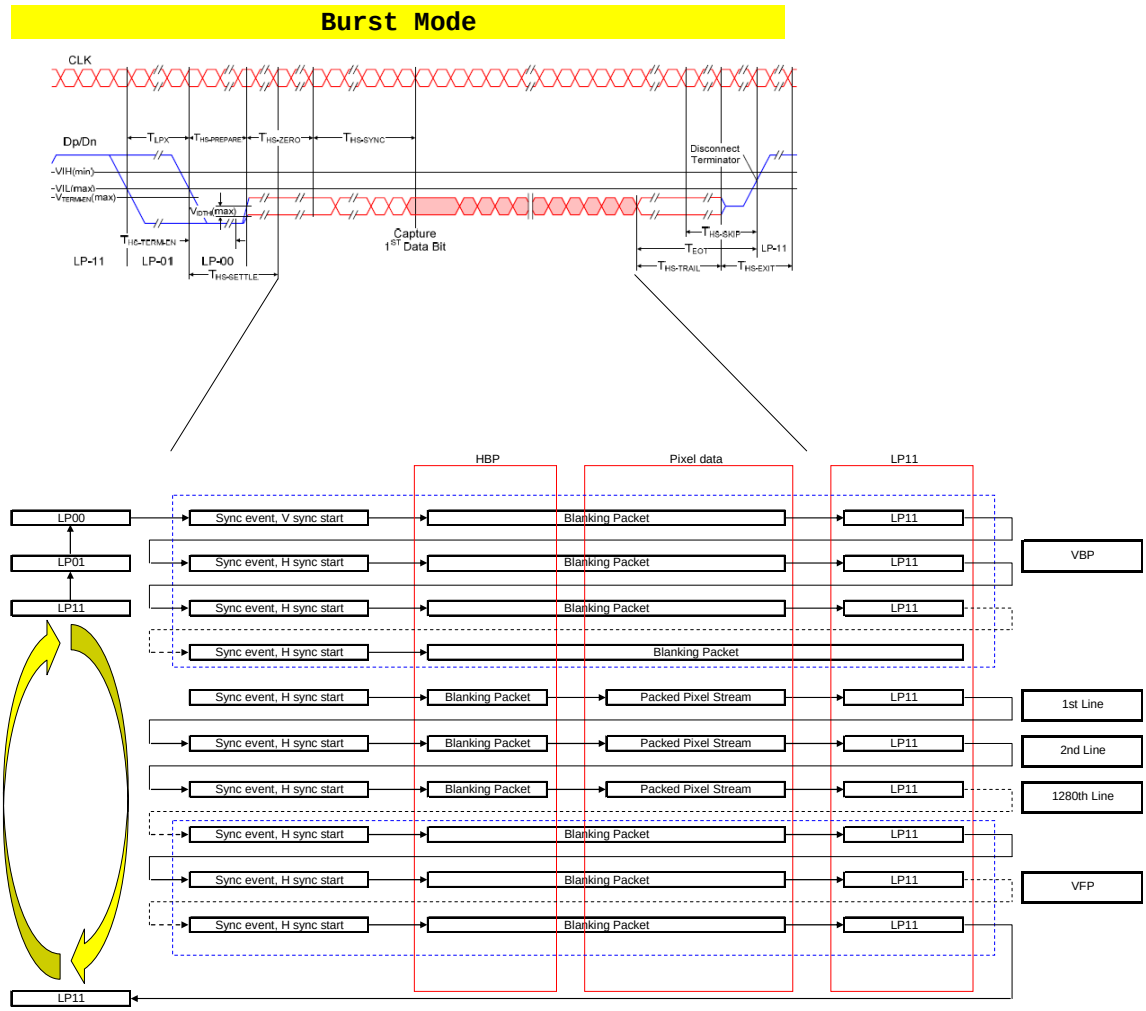


Figure 9-24: Burst mode MIPI structure

9.3.1.1 Write Operation

To perform write operation, the user needs to set the **REN** bit to 0. The SSD2828 can issue four kinds of packets for write operation, which are Generic Short Write Packet, Generic Long Write Packet, DCS Short Write Packet and DCS Long Write Packet. The bit **DCS** controls whether Generic Write Packet or DCS Write Packet will be sent out. The **VC1** or **VC2** field determines the VC ID of the outgoing packets. (Please see the 8.1.9 for the difference between **VC1** and **VC2**.)

The SSD2828 needs to know the payload size of the outgoing packets. Hence, the user needs to program the corresponding control registers. **PSCR1** and **PSCR2** form the **TDC** field that indicates the total number of payload bytes.

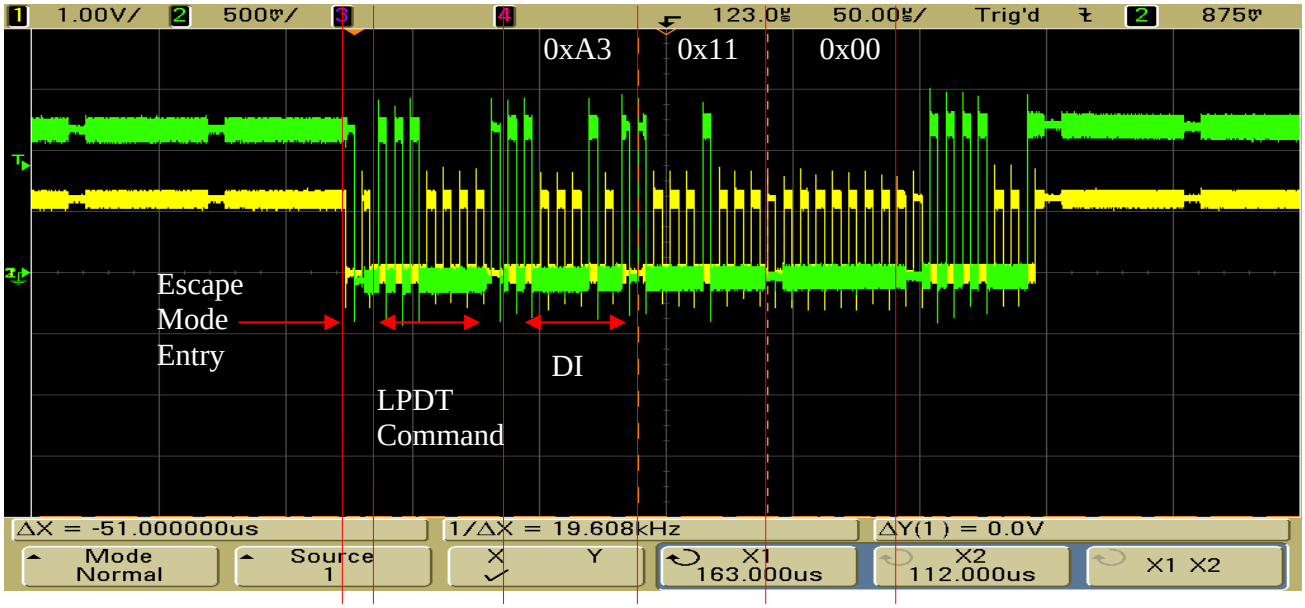
To send a DCS Write Packet, the user needs to write the DCS command/header and the payload to the register **PDR** and **DCS** bit set to 1**.** If the **TDC** field is no more than 2, the SSD2828 will send out DCS Short Write Packet with the correct type. Otherwise, DCS Long Write Packet will be sent out.

To send a Generic Write Packet, the user needs to write the payload to the register **PDR** and **DCS** bit set to 0. If the **TDC** field is no more than 2, the SSD2828 will send out Generic Short Write Packet with the correct type. Otherwise, Generic Long Write Packet will be sent out.

For DCS Write Packet, the partition is only enabled if the DCS command is 0x2C or 0x3C. Otherwise, SSD2828 will not perform automatic partition. (This is because the DCS command 0x2C and 0x3C are to write display data into the LCD panel display memory.) The payload will be partitioned into a few packets where the payload of each packet is **PST** bytes. The first byte is the DCS command and the following **PST** bytes are the payload. Only the last packet might contain less payload, as the total payload might not be integer multiple of **PST**. If the incoming DCS command is 0x2C, the DCS command for the first packet is 0x2C and the DCS command for all other packets is 0x3C. If the incoming DCS command is 0x3C, the DCS command of all the packets is 0x3C.

For example, in the raw data mode(**IFC**=0), if the **TDC** field is 200 and **PST** field is 80, 3 packets will be sent. The first two have 80 bytes of payload. The last packet has 40 bytes of payload.

After performing a write operation, the user can optionally make a BTA to let the MIPI slave report its status. This is done by setting **FBW** bit to 1. The SSD2828 will automatically make a BTA after each write operation. Please refer to 0 for how to handle the acknowledgement received.

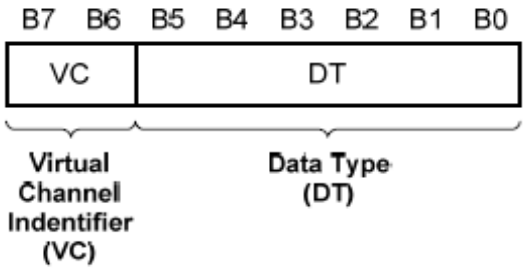


DI = 1010 0011

VC = 10

DT = 10 0011

Generic Short WRITE, 2 parameters



9.3.1.2 Read Operation

To perform read operation, the user needs to set the **REN** bit to 1. The SSD2828 can issue two kinds of packets for read operation, which are Generic Read Packet, and DCS Read Packet. The bit **DCS** controls whether Generic Read Packet or DCS Read Packet will be sent out. The **VC1** or **VC2** field determines the VC ID of the outgoing packets. (Please see the 8.1.9 for the difference between **VC1** and **VC2**.)

Before the read packet is sent out, the SSD2828 will always send out the Set Maximum Return Size Packet. This is to limit the Read Response Packet sent by the MIPI slave such that there is no over flow. Two factors determine the maximum size. One is the limit of the SSD2828 and the other is the limit of the application processor. The user should choose the smaller one among these two limits to use as the maximum return size.

The parameter in the Set Maximum Return Size Packet is taken from register **MRSR**. The user could program the **MRSR** before every read so that the correct value is sent through Set Maximum Return Size Packet. If the value in the **MRSR** is already the desired value, the user can choose not to program it. The SSD2828 will always automatically send out Set Maximum Return Size Packet using the value in **MRSR**.

To send a DCS Read Packet, the user just needs to write the DCS command (as there is no parameter for DCS read) to PDR register and **DCS** bit set to 1.

To send a Generic Read Packet, the user needs to write the payload to the register **PDR** and **DCS** bit set to 0.

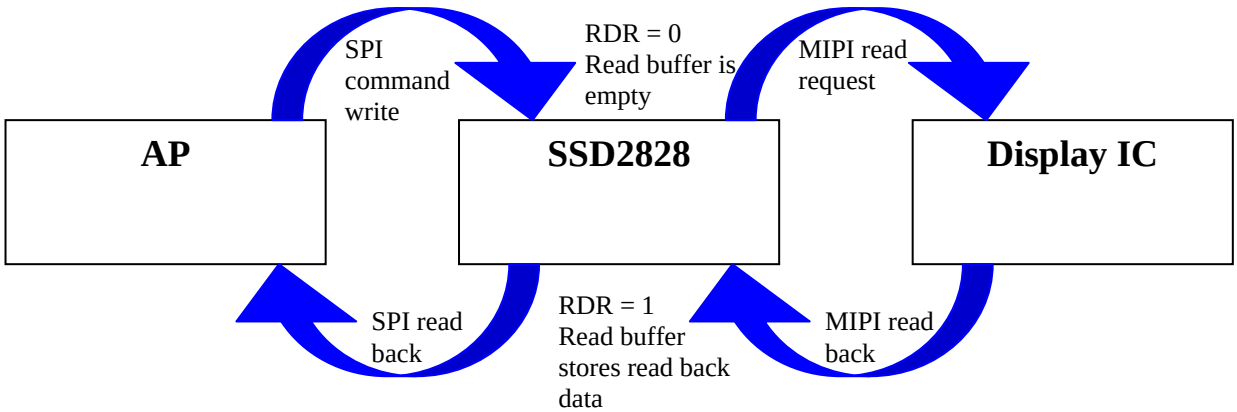
Similar to the write operation, the **TDC** field is used to determine the payload size of the outgoing packet. For DCS Read Packet, the payload is just the DCS command. There is no parameter associated. For Generic Read Packet, the SSD2828 will send out the correct packet type according to the **TDC** value.

After sending out the read packet, the SSD2828 will automatically perform a BTA to wait for the Read Response Packet from the MIPI slave. The return data will be stored in register **RR**. No matter what read packet is sent out, there is only one packet returning data. Therefore, no matter whether the read is DCS read or Generic read, no matter what command is used in DCS read, the return data is always stored in register **RR**. The user can read the data out when the **RDR** bit is set to 1. After seeing **RDR** bit been set to 1, the user should first read register **RDCR** which contains the number of bytes returned by the MIPI slave. By using this information, the user will know how many data should be read out from register **RR**. After all the return data are read out, the **RDR** bit will be set to 0 by the SSD2828.

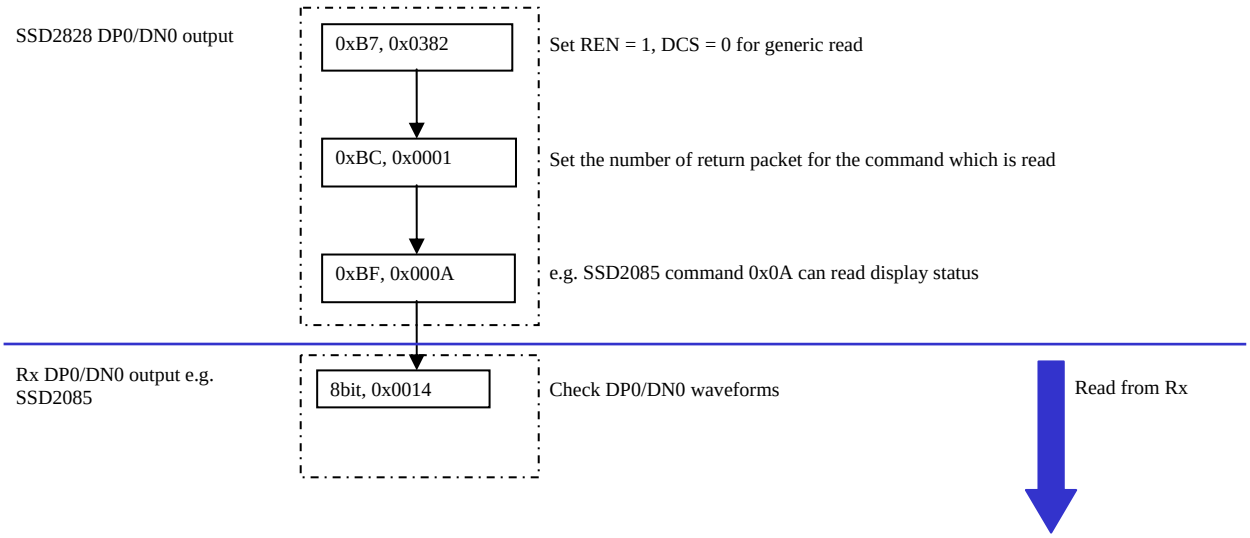
After the **RDR** bit been set to 1, the user can choose not to read the data out from register **RR**. The user can continue performing another operation. Once the user does so, the **RDR** bit will be set to 0 by the SSD2828.

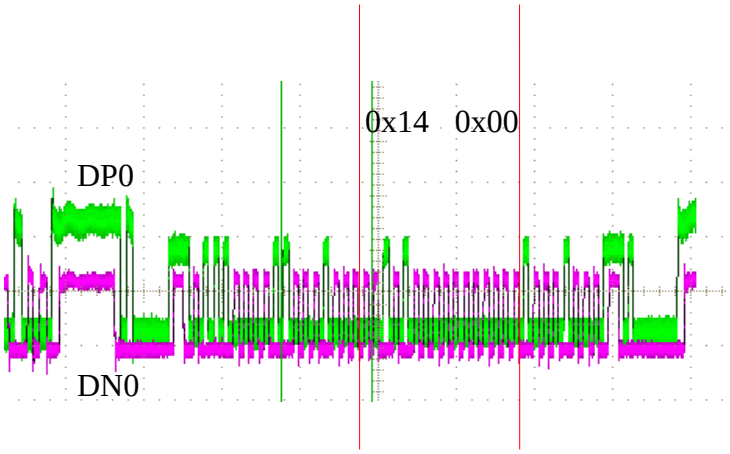
There might be Acknowledge and Error Report Packet sent by the MIPI slave at the same time. The operation of acknowledgement handling is described in 0.

Under certain circumstance, the MIPI slave might only send back Acknowledge and Error Report Packet without any data. Thus, the **RDR** bit will not be set. Therefore, it is recommended that the user check the bit **BTAR** first. The **BTAR** is to indicate whether the MIPI slave has passed the bus authority back to the SSD2828 or not. Only when the **BTAR** is 1, there might be return data. If there is no return data, the user should follow 0 to handle the acknowledgement.



MIPI read back





9.3.1.3 Acknowledgement Operation

The SSD2828 can perform a BTA to give the bus authority to the MIPI slave and let it report its status. The BTA can be enabled by setting **FBW** bit to 1 and performing a write operation, or just performing a read operation. After the MIPI slave passes the bus authority back, the SDD2828 will set bit **BTAR** to 1.

If there is no error on the slave side, the MIPI slave will return ACK trigger message, if the packet before BTA is a write packet. The MIPI slave will return Read Response Packet, if the packet before BTA is a read packet. In this case, after receiving the response from the MIPI slave, SSD2828 will set bit **ARR** and **ATR** bits to 1. **ARR** indicates that response has been received from MIPI slave. **ATR** indicates that the MIPI slave has reported no error with ACK trigger message. Consequently, the register **ARSR** will be cleared to 0.

If there is error on the slave side, the MIPI slave will return Acknowledge and Error Report packet, if the packet before BTA is a write packet. The MIPI slave will return Read Response Packet (depending on the error type) and Acknowledge and Error Report Packet, if the packet before BTA is a read packet. In this case, after receiving the response from the MIPI slave, SSD2828 will set bit **ARR** bit to 1 and **ATR** bits to 0. **ARR** indicates that response has been received from MIPI slave. **ATR** indicates that the MIPI slave has sent Acknowledge and Error Report Packet instead of ACK trigger message. Therefore, the MIPI slave has reported error. The error reported by the MIPI slave will be stored in register **ARSR**. The user can read this register to see what error the MIPI slave has encountered.

For the detailed description of each error bit, please refer to MIPI DSI specification. Below are the flow charts of handling the MIPI slave acknowledgement. They are just for reference.

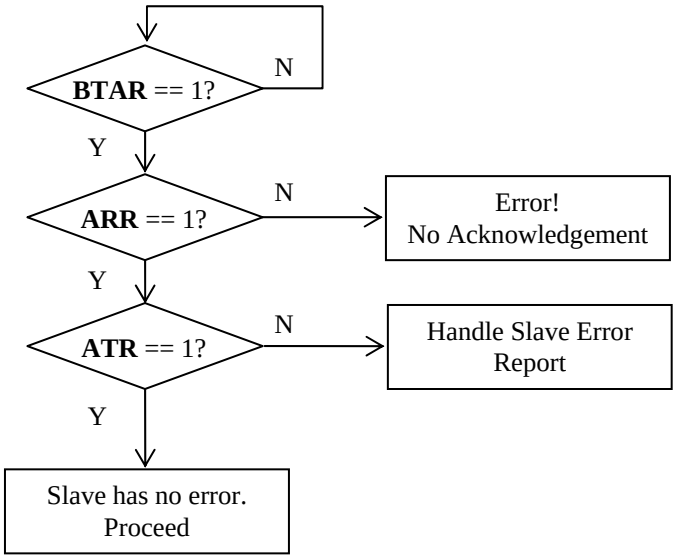


Figure 9-25: Acknowledgement Handling after Non-Read Command

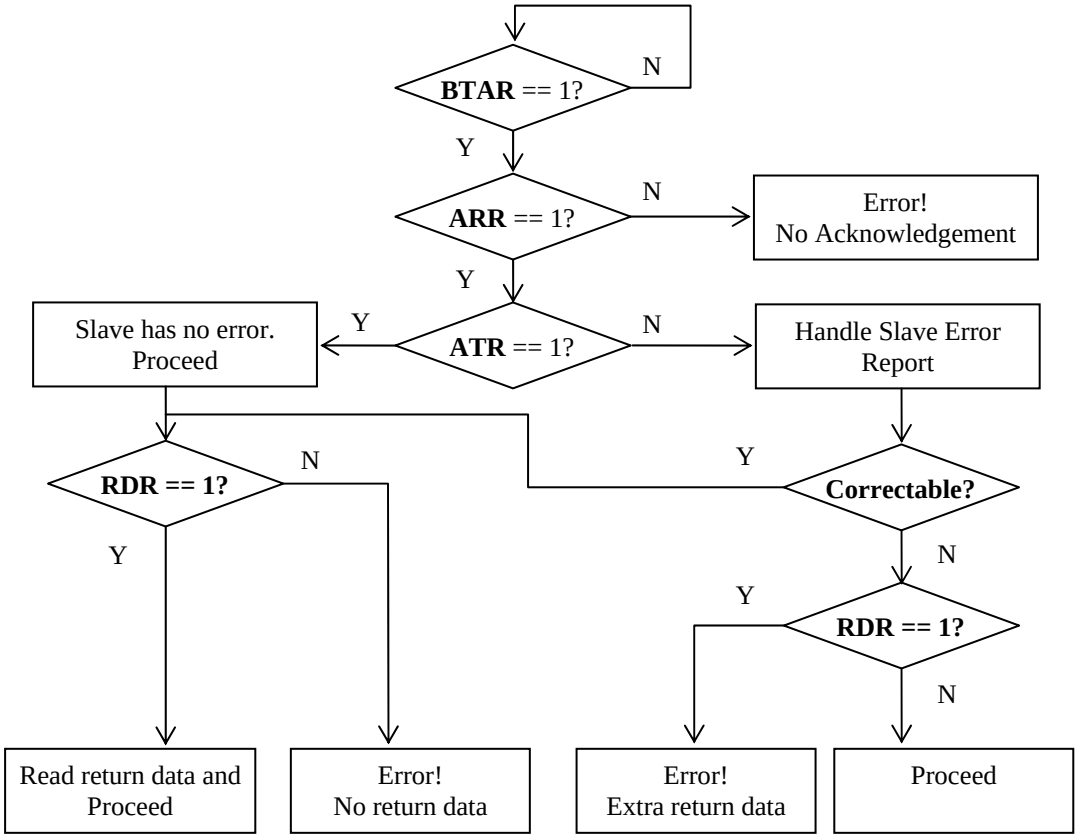
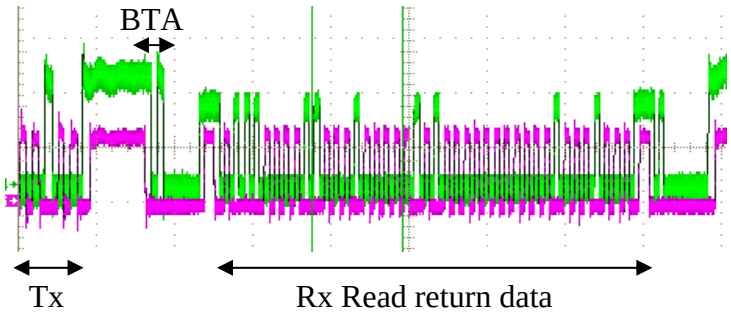


Figure 9-26: Acknowledgement Handling after Read Command



Remark: LP clock of Rx must be within 10% of Tx LP clock

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	False Control Error
7	Contention Detected
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

Table 9-13: MIPI error report

9.3.1.4 Tearing Effect (TE) Operation

The TE operation is to perform a BTA following the previous BTA without transmitting anything in between. The bus is handed to the MIPI slave for providing TE information. After getting the TE event from display driver, the MIPI slave will pass the bus authority back to the SSD2828 by using BTA trigger message.

The TE operation can be enabled by setting bit **FBT** and **FBW** to 1 before writing the last command to the MIPI slave. Afterwards, the application processor can instruct the SSD2828 to send out the last command in a write packet. Since **FBW** is 1, the SSD2828 will automatically perform a BTA after the write operation. The MIPI slave will response and pass the bus authority back. Since **FBT** is 1, the SSD2828 will perform another BTA without sending any data. This makes the MIPI slave enter TE mode.

The MIPI slave will send a TE trigger message back when it gets the TE event. After getting the trigger message, the SSD2828 will set the TE pin to 1 to indicate that TE event has been received. DATA[16] is used as the TE pin. At the same time, bit **TER** will be set to 1. The application processor can write 1 to this bit to clear it. As the TE trigger message only determines when the TE pin will be set to 1, a counter is used to determine when to set the TE pin to 0. The TE pin will be set to 0, once the counter reaches the value in **TEC**. The counter uses the reference clock to do counting.

If the MIPI slave does not send back the TE trigger message but just perform a BTA to pass the bus back, the SSD2828 will automatically perform another BTA to pass the bus to the MIPI slave again. It will continue do so until the MIPI slave respond with the TE trigger message, or the **FBT** bit is set to 0, or the LP RX timer expires.

If the MIPI slave does not send back the TE trigger message and still holds the bus, the user can set the bit **FBC** to 1 to force a bus contention. After bus contention is resolved, the slave will pass the bus back to SSD2828.

9.3.1.5 Contention Detection and Timer Operation

Two timers have been defined in SSD2828 to resolve the potential contention issue on the bus. The two timers are the HS TX timer and LP RX timer. Please see the register description for the detailed usage.

Whenever the SSD2828 sees a contention being detected, it will reset the state machine and enter the default mode, which is LP TX idle mode. The data line will be kept at LP11.

9.3.1.6 Interrupt Operation

An interrupt signal int_0/int_1 has been provided to interrupt the application processor so that it does not need to poll the status all the time. This will save the processing time of the application processor. int_0/int_1 is an active low signal, in other words, when the event has happened, it will go low.

There are many sources that can be mapped to the interrupt signal. The user can select different source to perform different task. If more than 1 source is selected, the int_0/int_1 signal will go low when the event for 1 of the sources has happened. In this case, the user needs to read the register **ISR** to determine what event has happened. The different sources can be enabled/disabled through register **ICR**. Below is the list of available interrupt sources and their usage.

RDR

To indicate that return data from MIPI slave is available for read.

BTAR

To indicate whether the SSD2828 has the bus authority or not. It can be used after SSD2828 makes a BTA. If the MIPI slave has returned the bus authority back to SSD2828, the interrupt will be set to indicate so. Please note that, on power up, the bus authority is already on the SSD2828. Hence, the SSD2828 will show that it has the bus authority.

ARR

To indicate whether the SSD2828 has received the acknowledge response from the MIPI slave. The acknowledge response can either report error or not error. This is to be determined by the **ATR** bit.

The above three interrupts are provided to the user to handle reading data from the MIPI slave or getting acknowledgement response from the MIPI slave.

PLS

To indicate whether the PLL has been locked or not. If the PLL is not locked, the programming speed at the external interface must be slow. After changing the PLL setting or changing the reference clock source, the user also needs to use this interrupt to determine the PLL status.

On power up, only **PLS** interrupt is enabled. This is to let the user determine the programming speed before configuring the SSD2828.

LPTO

To indicate that there is LP RX time out.

HSTO

To indicate that there is HS TX time out.

The above two interrupts are provided to the user for error handling.

PO

To indicate whether the SSD2828 is ready to accept any data from the user. The SSD2828 has several internal buffers to hold the data written by the user. When the user writes after than the serial link speed, those buffers will be full. If the user still writes data to SSD2828, those data will be lost. The length of the payload of the next packet that the user is going to write is determined by **TDC**, **PST**, and **DCS** fields. The SSD2828 will use these fields to decide whether the user can write the next packet or not. Hence, after programming the above mentioned fields, the user needs to check the interrupt status before writing.

SE, SA, SLE, SLA, MLE, MLA

All these interrupts are provided to indicate the status of the internal data buffers. They are used if the user is familiar with the buffer management of the SSD2828. Otherwise, it is recommended to use the **PO** interrupt.

One important thing to note is the interrupt latency. The output interrupt signal does not change immediately after an operation. This is due to the internal processing of the SSD2828. For example, after changing the interrupt source from one to another, the output int_0/int_1 level will remain at the old level for a short period after the programming is done. Another example is that after programming the **TDC** field, the interrupt will take a short period to reflect the correct **PO** status on int_0/int_1. There is always a delay between the actual event and the interrupt.

In order to guarantee that the user can get the correct interrupt, it is recommended that the user performs a read of any SSD2828 local register before taking in the interrupt signal or polling the interrupt status bits. The read operation will cover the interrupt latency period. Alternatively, the user can wait for certain amount of time to make sure the interrupt reflects the true status. Below is a diagram for illustration.

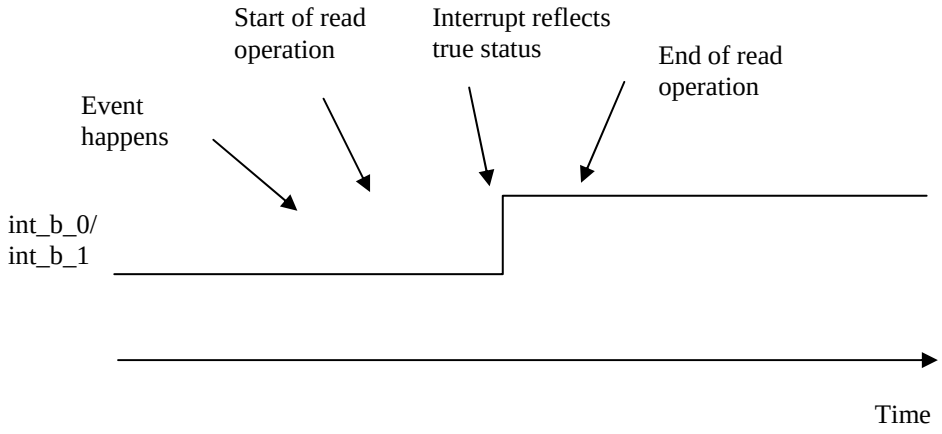


Figure 9-27: Illustration of Interrupt Latency

9.3.1.7 Internal Buffer Status

There are totally 1 data buffer inside the SSD2828QN4, which is SPI command interface buffer (CB).

For CB buffers, all packets will be stored into them. They can store multiple packets and each packet size can be set to 1023 bytes. Below is a list of possible packets

- Generic Short Write Packet
- Generic Read Packet
- DCS Short Write Packet
- DCS Read Packet
- Generic Long Write Packet
- DCS Long Write Packet

In case of automatic partitioning, the packet length is determined by the **PST** field. It is not recommended to make the **PST** field so small.

The user can write the data through SPI interface. All packets will be written into the CB buffers. Hence, the user needs to check the corresponding interrupts. The usage of the interrupts is listed below.

CBE

To indicate that the Command buffer is empty.

CBA

To indicate that the Command buffer can hold at least 1 more packet. The user can write 1 such packet into CB buffer.

The interrupts mentioned here can be used as flow control between the application processor and the SSD2828. However, it requires the user to know the buffer operation well. The **PO** interrupt is a combination of the eight. It makes decision according to the parameters provided by the user for the next packet to be written. Hence, the user does not need to know which buffer is going to be used and how the buffer status is.

9.3.2 State machine operation

The state machine controls the sending and receiving of the data packet over the serial link. It is triggered by an event from the application processor or the received data. Once a complete packet is written into the SSD2828 buffer, it will send it out through the serial link. The user can write 1 to bit **COP** at any time to cancel all the current operations. Please see 8.1.17 for the description.

When the SSD2828 is in high speed mode, the serial link is mainly used to send display data. If there is no data to send, it will send null packet to maintain the serial link timing. If the application processor does not have display data to send in a long period, it can turn the serial link into low power mode by setting the register bit **HS** to 0.

When the SSD2828 is in low power mode, the serial link is mainly used to send command and configuration data. If there is no data to sent, the SSD2828 will be idle in LP TX stop mode.

The user can also enter sleep mode by writing 1 to **SLP** bit. Once the **SLP** bit is set to 1, the SSD2828 will automatically enter LP mode. If the **HS** bit is 1, the SSD2828 will clear the **HS** bit to 0 and switch from HS to LP mode. Afterwards, the SSD2828 will issue ULPS trigger message to the MIPI slave to enter Ultra Low Power State. During this state, the clock to SSD2828 can be switched off such that the SSD2828 only consumes leakage current. This will save the overall system power consumption. When exiting from the ULPS, the user can write 0 to **SLP** bit. However, the user should be aware that the time to exit from ULPS is relatively long (pleaser refer to MIPI DPHY specification). Hence, the user cannot perform any data transmission before the system exits from ULPS.

During reception, the state machine will disassemble the incoming data packet and put the received register content into the internal buffer for reading out. Once all the data are put into the buffers, it will set the register bit **RDY** to 1 to indicate that the SSD2828 is ready for read. The total number of received bytes will also be stored in **RDCR**.

After the reception is completed, the SSD2828 will perform a bus turn around to enter the transmission mode. It will always come back to the LP TX stop mode before it enters any other mode.

9.3.3 D-PHY operation

D-PHY controls the operation of the analog transceiver. It controls whether the serial link is in high speed or low power mode and whether it's in transmit or receive mode.

In transmit mode, the D-PHY will perform the handshaking procedure when switching between LP mode and HS mode according to the control from PCU. During HS mode, D-PHY will provide parallel data and clock to the analog transmitter for transmitting in differential signals serially. During LP mode, D-PHY will directly drive the Datap and Datan line output. It will provide serial data to the analog transmitter.

In receive mode, D-PHY will detect the handshaking sequence in LP mode and inform the PCU. Once entering escape mode, it will collect the serial data from analog receiver and put them in byte form for the PCU to process.

Various timing parameter has been defined in MIPI DPHY specification. The timing parameters are a mixture of absolute time and cycle counts. Hence, for different operation speed, there is different timing requirement. Registers **DAR1** to **DAR6** are provided for this purpose. The user can adjust the value in these registers to have different DPHY timing parameters. This gives maximum flexibility for different operation speed.

9.3.4 Analog Transceiver

9.3.5 PLL

The PLL output frequency is calculated by the equations below,

$$f_{PRE} = \frac{f_{IN}}{MS}$$
$$f_{OUT} = f_{PRE} * NS$$

where the f_{IN} is the input reference clock frequency and f_{OUT} is the output clock frequency of the PLL.

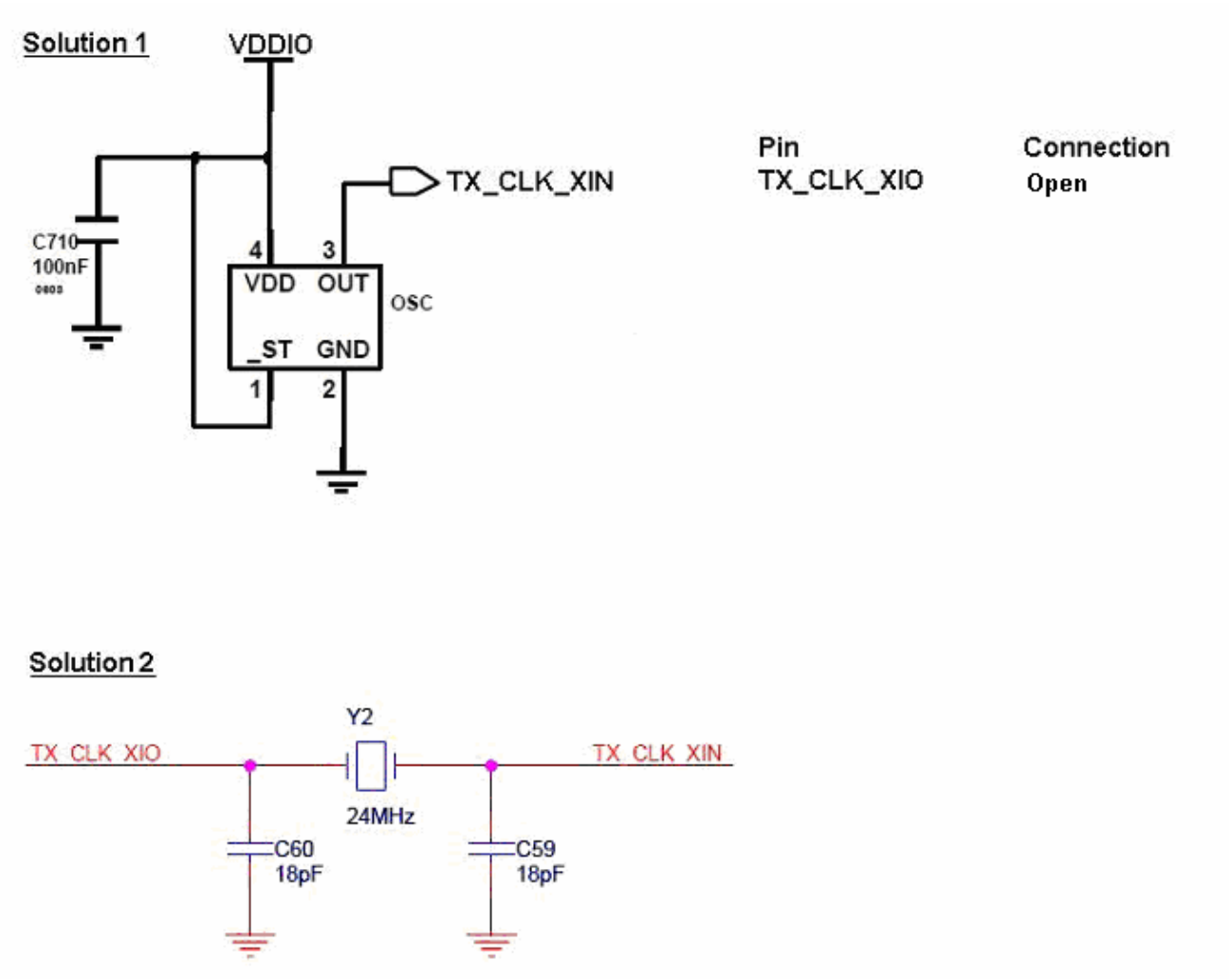
The clock frequencies need to satisfy the constraint below.

$$5MHz > f_{IN} \geq 100MHz$$
$$5MHz > f_{REF} \geq 100MHz$$
$$62.5MHz > f_{OUT} \geq 1000MHz$$

The value of FR, MS, and NS are controlled in the register **PLCR**.

All the values of FR, MS and NS can only be modified when the PLL is turned off. Hence, the sequence for modification is to turn off PLL, modify register value, and turn on PLL.

9.3.6 Clock Source Example



10 External Interface

The SSD2828 supports three types of SPI interface,

- 8-Bit 3 wire (type C option 1, DBI 2.0)
- 8-Bit 4 wire (type C option 3, DBI 2.0)
- 24-bit 3 wire

and RGB interfaces.

The selection is controlled by ps[1:0] pins.

RGB interface supports 4 bpp settings. Below are the data pins used for each interface. For all cases, R should be at the upper bits and B should be at the lower bits.

- data[15:0] for 16 bpp.
- data[17:0] for 18 bpp, packed.
- data[17:0] for 18 bpp, loosely packed.
- data[24:0] for 24 bpp.

SPI interface supports 8-Bit data bus. The least significant byte should be written first.

Below is the operation and timing diagram for each of the interfaces.

10.1 SPI Interface 8 bit 4 Wire

This interface consists of sdcx, sck, sdin, sdout and csx. It only supports 8-Bit data. Each cycle contains 8-Bit data. The first cycle should be a command write cycle to specify the register address for access. The subsequent cycles are read or write cycles for read or write operations.

The csx should be driven from 1 to 0 to start an operation and from 0 to 1 to end an operation. During 1 operation, the application processor can write or read multiple bytes.

sdcx indicates whether the operation is for data or command. When sdcx is 1, the operation is for data. When sdcx is 0, the operation is for command. sdcx is sampled at every 8th rising edge of sck during 1 operation.

During write operation, sdin will be sampled by SSD2828 at the rising edge of sck. The first rising edge of sck after the falling edge of csx samples the bit 7 of the 8-Bit data. The second rising edge of sck samples the bit 6 of the 8-Bit data, and so on. The value of sdcx is sampled at the 8th rising edge of sck, together with bit 0 of the 8-Bit data. Please see the diagram below for illustration. Optionally, the csx can be driven to 1 in between cycles.

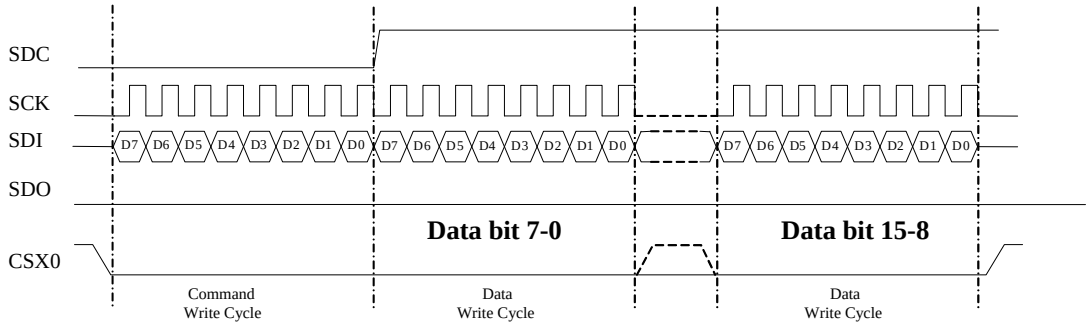


Figure 10-1: Illustration of Write Operation for 8 bit 4 Wire Interface

Remark: Send LSB 8bit of data before MSB 8bit

During read operation, since there is no rwx signal to indicate whether the operation is read or write. After csx is driven low, the first cycle is always a command write cycle, which specifies the register to access. The second cycle is still a command write cycle. If the command in this cycle matches the command in register LRR, the SPI interface will enter read mode. The subsequent cycles will be read cycles. If the command does not match, the SPI interface will remain in write mode.

After entering the read mode, the return data is provided on sdout, on the falling edge of sck. The application processor should use the rising edge of sck to sample the data. sdcx should be driven to 1 during the read cycles. Please see the diagram below for illustration. Optionally, the csx can be driven to 1 in between cycles.

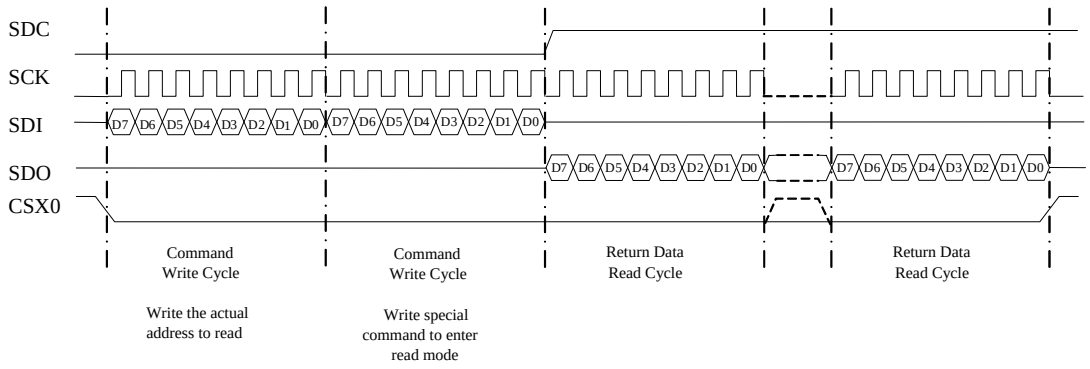


Figure 10-2: Illustration of Read Operation for 8 bit 4 Wire Interface

10.2 SPI Interface 8 bit 3 Wire

This interface consists of sck, sdin, sdout and csx. It only supports 8-Bit data. Each cycle contains 8-Bit data. The first cycle should be a write cycle to specify the register address for access. The subsequent cycles are read or write cycles for read or write operations.

The csx should be driven from 1 to 0 to start an operation and from 0 to 1 to end an operation. During 1 operation, the application processor can write or read multiple bytes.

Instead of sdcx, an sdcx bit is used to indicate whether the operation is for data or command. Each byte is associated with an sdcx bit. When sdcx is 1, the operation is for display data. When sdcx is 0, the operation is for command. The sdcx bit is sent priori to each byte. In other words, the sdcx bit is the first bit of every 9 bits during 1 operation.

During write operation, sdin will be sampled by SSD2828 at the rising edge of sck. The first rising edge of sck after the falling edge of csx samples the sdcx bit. The second rising edge samples bit 7 of the 8-Bit data. The third rising edge of sck samples the bit 6 of the 8-Bit data, and so on. Please see the diagram below for illustration. Optionally, the csx can be driven to 1 in between cycles.

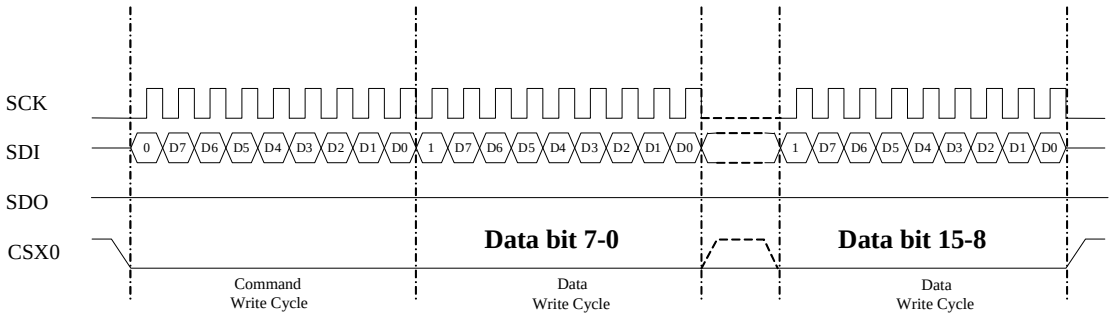


Figure 10-3: Illustration of Write Operation for 8 bit 3 Wire Interface

Remark: Send LSB 8bit of data before MSB 8bit

During read operation, since there is no rwx signal to indicate whether the operation is read or write. After csx is driven low, the first cycle is always a command write cycle, which specifies the register to access. The second cycle is still a command write cycle. If the command in this cycle matches the command in register LRR, the SPI interface will enter read mode. The subsequent cycles will be read cycles. If the command does not match, the SPI interface will remain in write mode.

After entering the read mode, the return data is provided on sdout, on the falling edge of sck. The application processor should use the rising edge of sck to sample the data. Please note that there is no sdcx bit to read out from SSD2828. Hence, each read cycle consists of 8-Bits instead of 9 bits. This is the difference between read and write cycles. Please see the diagram below for illustration. Optionally, the csx can be driven to 1 in between cycles.

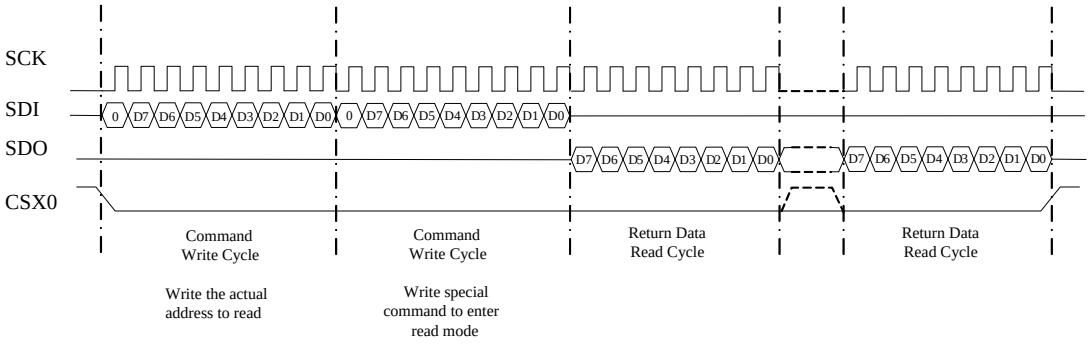
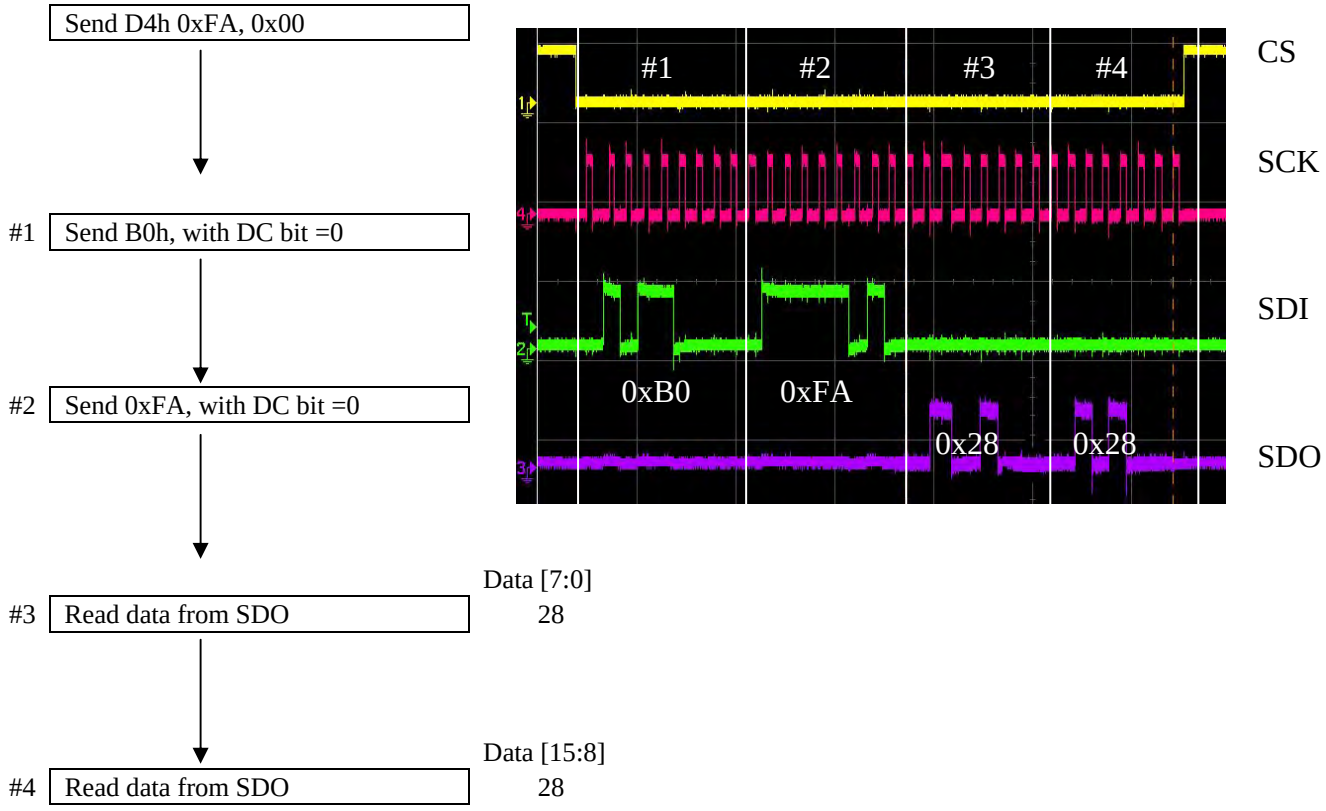
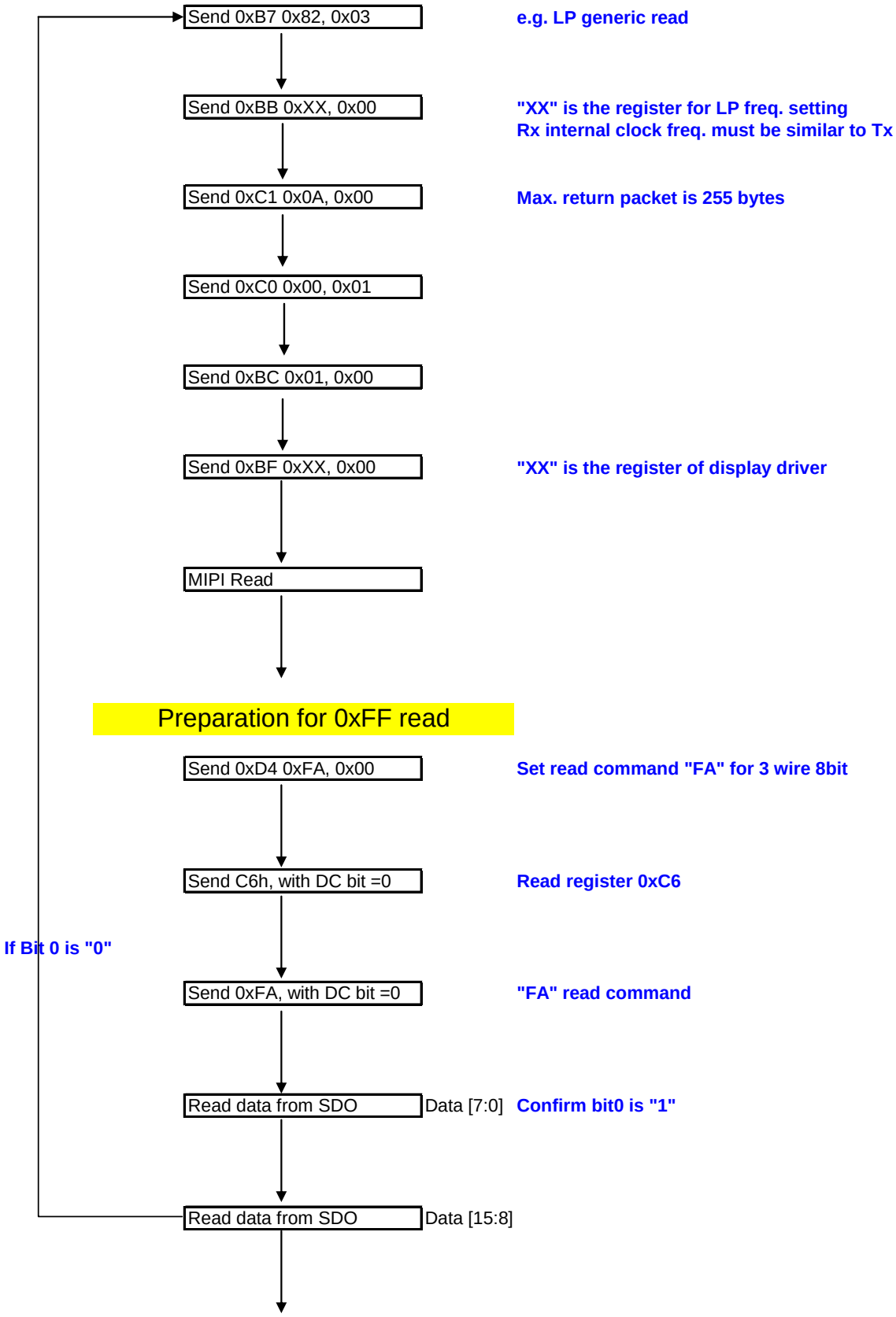


Figure 10-4: Illustration of Read Operation for 8 bit 3 Wire Interface

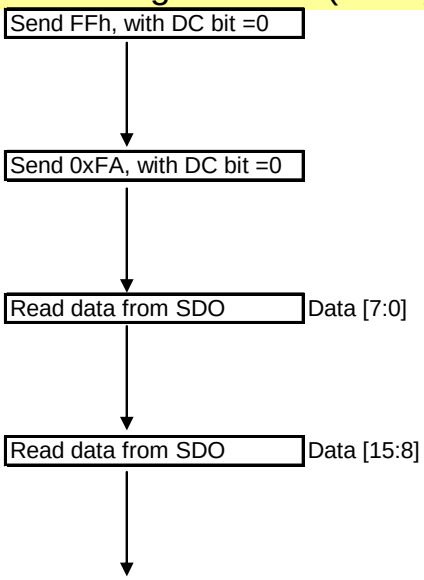
Read sequence of register e.g.0xB0h



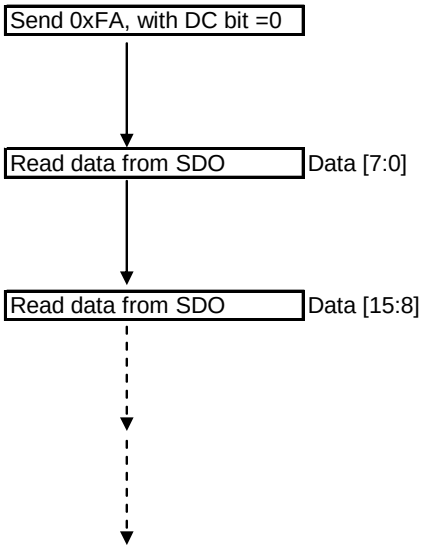
10.2.1 3 or 4 wires 8bit SPI read back sequence for 0xFF register which is stored MIPI read back data



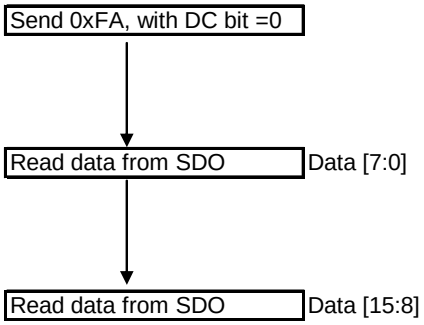
Read sequence of register FFh (1st Byte data of 0xXX)



Read sequence of register FFh (2nd Byte data of 0xXX)



Read sequence of register FFh (xxth Byte data of 0xXX)



10.3 SPI Interface 24 bit 3 Wire

This interface consists of sck, sdin, sdout and csx. It only supports 16-bit data. Each cycle contains 16-bit data. The first cycle should be a write cycle to specify the register address for access. The subsequent cycles are read or write cycles for read or write operations.

The csx should be driven from 1 to 0 to start cycle and from 0 to 1 to end a cycle. During 1 operation, the application processor can have multiple write or read cycles. However, the csx must go from 0 to 1 at the end of each cycle.

Each cycle contains 24-bit data. Among the 24-bit data, the first 8-Bit are for control purpose and the next 16-bit are the actual data. The first 6 bits are the ID bit for SSD2828, which must be 011100. If this field does not match, the cycle will not be taken in. The 7th bit is the sdcx bit which is the same as the 8-Bit 3 wire interface. The 8th bit is the RW bit which indicates whether the current cycle is a read or write cycle. When RW is 1, the cycle is a read cycle. When RW is 0, the cycle is a write cycle.

During write operation, sdin will be sampled by SSD2828 at the rising edge of sck. Please see the diagram below for illustration. It is an example for writing data 0x1264 to register address 0x28.

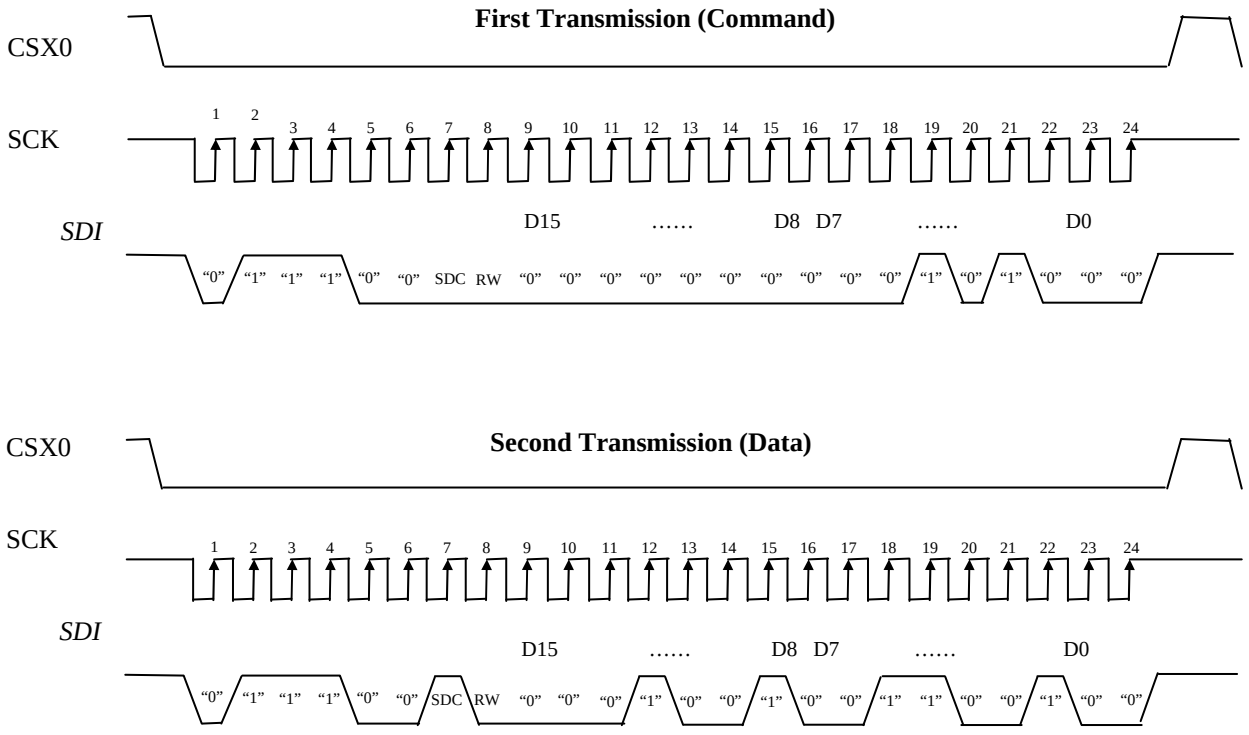


Figure 10-5: Illustration of Write Operation for 24 bit 3 wire Interface

Remark: Send MSB 8bit of data before LSB 8bit

During read operation, the first 8-Bit are still written by the application processor to specify whether the following 16-bit are for command or data. Afterwards, the SSD2828 will provide the return data on sdout, on the falling edge of sck. The application processor should use the rising edge of sck to sample. Please see the diagram below for illustration.

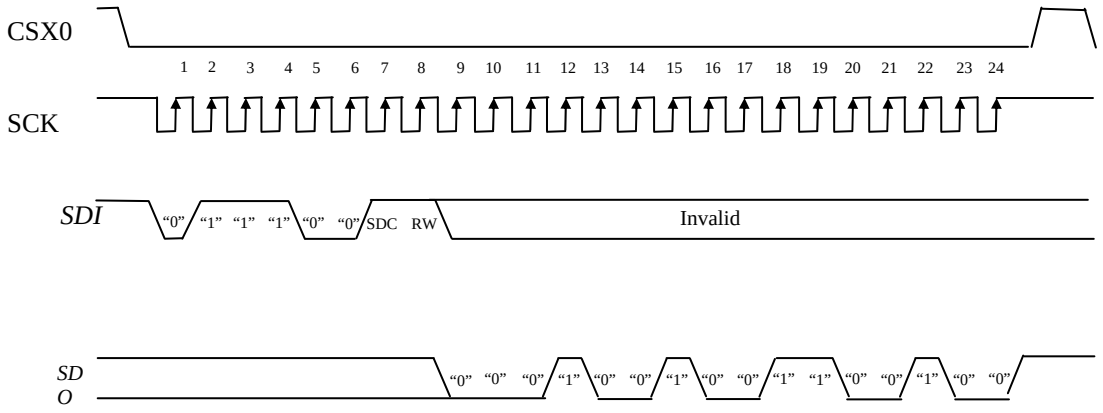
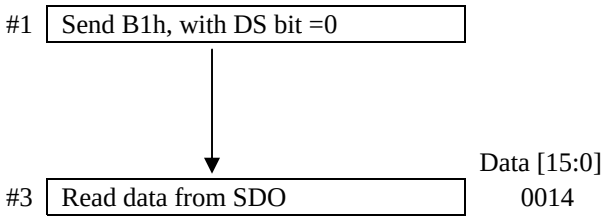
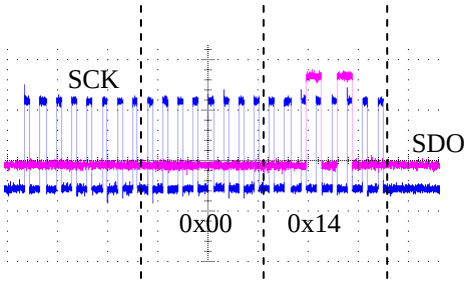


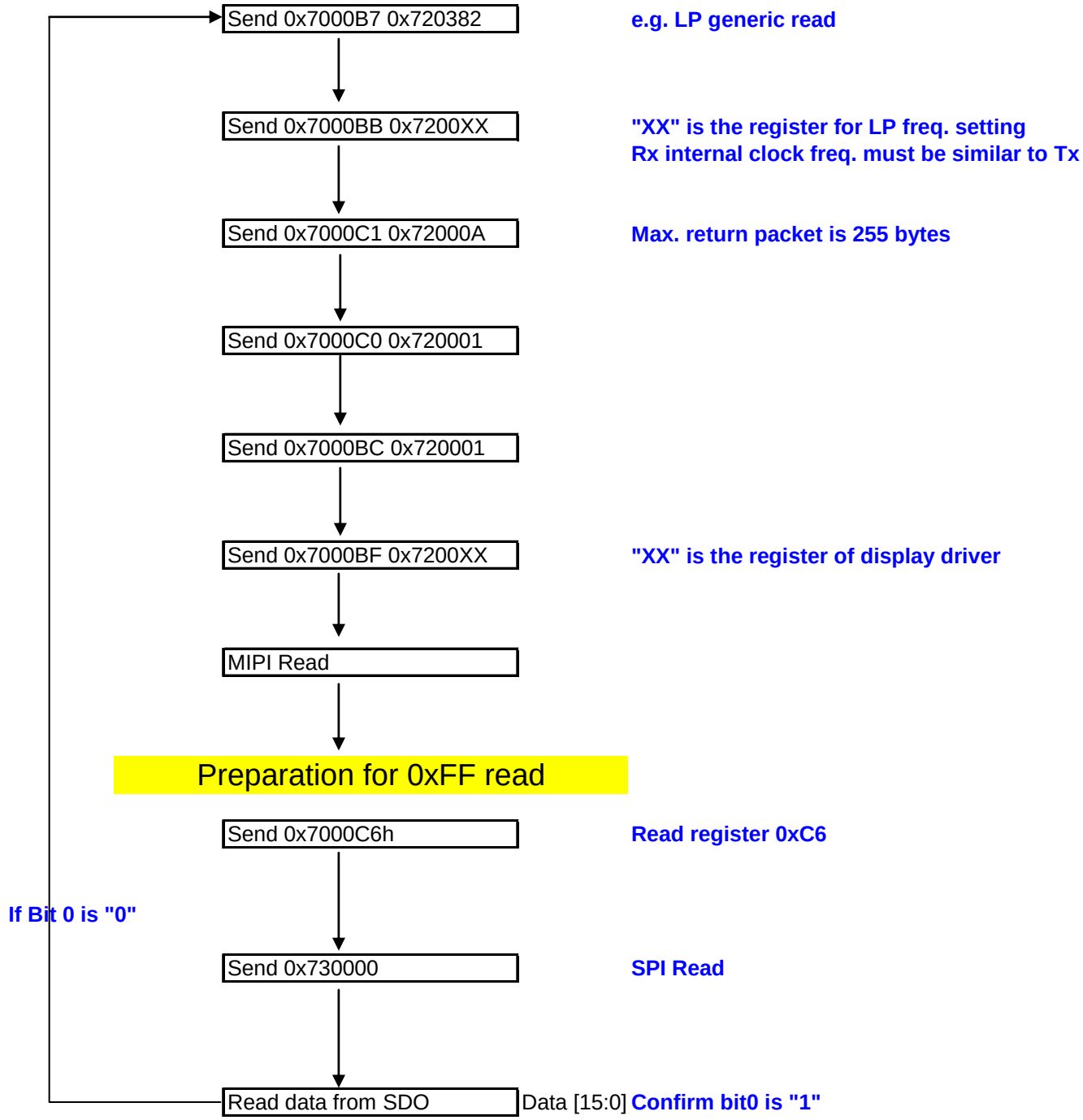
Figure 10-6: Illustration of Read Operation for 24 bit 3 Wire Interface

Read sequence of register e.g.0xB1h

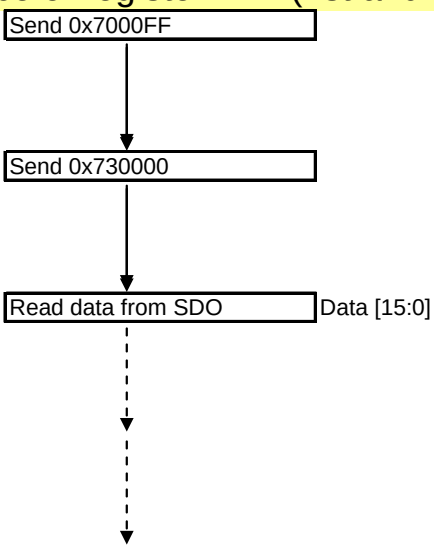




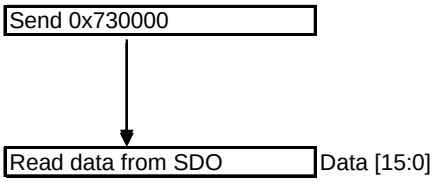
10.3.1 3 wires 24bit SPI read back sequence for 0xFF register which is stored MIPI read back data



Read sequence of register FFh (1st and 2nd Byte data of 0xXX)



Read sequence of register FFh (nth and n+1th Byte data of 0xXX)



11 MAXIMUM RATINGS

Table 11-1: Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
MVDD	Core Power Supply	-0.3 to 1.44	V
VDDIO	I/O Power Supply	-0.3 to 4.0	V
T_{SOL}	Solder Temperature / Time	225 for 40 sec max at solder ball	^{o}C
T_{STG}	Storage Temperature	-40 to 100	^{o}C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits specified in the electrical characteristics tables and Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 RECOMMENDED OPERATING CONDITIONS

Table 12-1: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
MVDD	Digital Core Power Supply	1.08	1.2	1.32	V
VDDIO	I/O AND Digital Power Supply	2.97	3.3	3.63	V
		1.62	1.8	1.98	V
T_A	Operating Temperature	-30	25	85	^oC

13 DC Characteristics

Conditions: Voltage referenced to GND
MVDD = 1.2V
VDDIO = 1.8V
Frame frequency = 60Hz
Number of lane = 4
Display pattern = 1080x1920, 8 colors vertical bar
T_A = 25°C

Table 13-1: DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{MVDD_HS}	High Speed Mode Current	1Gbps	-	46.8	76.2	mA
I_{VDDIO_HS} (1.8V)			-	0.36	0.75	mA
I_{VDDIO_HS} (3.3V)			-	0.79	1.64	mA
I_{MVDD_LP}	Low Power Mode Current	10Mbps	-	16.00	39.90	mA
I_{VDDIO_LP} (1.8V)			-	0.17	0.43	mA
I_{VDDIO_LP} (3.3V)			-	0.37	0.94	mA
I_{MVDD_ULPS}	Ultra Low Power State Current	PLL off, no change in all input signals	-	292.4	435	µA
I_{VDDIO_ULPS} (1.8V)			-	75.6	150	µA
I_{VDDIO_ULPS} (3.3V)			-	165.2	327.8	µA
$V_{OH\ (CMOS)}$	Output High Voltage (CMOS)	I_{OH} = -2 ~ -16 mA	V_{DDIO} x 0.8	-	-	V
$V_{OL\ (CMOS)}$	Output Low Voltage (CMOS)	I_{OL}= 2 ~ 16 mA	-	-	V_{DDIO} x 0.15	V
$V_{IH\ (CMOS)}$	Input High Voltage (CMOS)		V_{DDIO} x 0.7	-	-	V
$V_{IL\ (CMOS)}$	Input Low Voltage (CMOS)		-	-	V_{DDIO} x 0.2	V
I_{OZ}	Tri-state Output Leakage Current		-	+/-1	-	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DDIO} or GND	-	+/-1	-	µA
C_{IN}	Input Capacitance		-	2.2	-	pF

Table 13-2: HS Transmitter DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{CMTX}	HS Transmit Static Common-mode Voltage	150	-	250	mV
$\|V_{OD}\|$	HS Transmit Differential Voltage	140	-	270	mV
$\|\Delta V_{OD}\|$	HS Differential Mismatch	-	-	10	mV
V_{OHHS}	HS Output High Voltage	-	-	360	mV

Table 13-3: LP Transmitter DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	LP Thevenin Output High Level	1.1	1.2	1.3	V
V_{OL}	LP Thevenin Output Low Level	-50	-	50	mV
Z_{OLP}	LP Transmitter Output Impedance	110	-	-	Ohm

Table 13-4: LP Receiver DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	LP Logic 1 Input Voltage	880	-	-	mV
V_{IL}	LP Logic 0 Input Voltage	-	-	550	mV

14 AC Characteristics

NOTE:

1. After PLL gets locked, T is the period of the PLL output clock unless specified. Before PLL gets locked, T is the period of PLL input reference clock. The reference clock can be either the tx_clk or the pclk, depending on the **CSS** bit.

   1 / T = PLL / 2,

   e.g. When PLL is Off <0xB9 0x0000>,

   TX_CLK = 10MHz,

   PLL = TX_CLK x 2 = 20Mbps

   1 / T = 10MHz

2. W is the width of the display, e.g. the number of pixels for the horizontal line.

3. The AC characteristics specifie the maximum speed of the incoming signals at the input interface. However, the data throughput on the serial link is another factor affecting the speed. If the user takes in the INT signal, there will be automatic flow control. If the user does not take the INT signal, the user needs to ensure that the output throughput is larger than the incoming data rate.

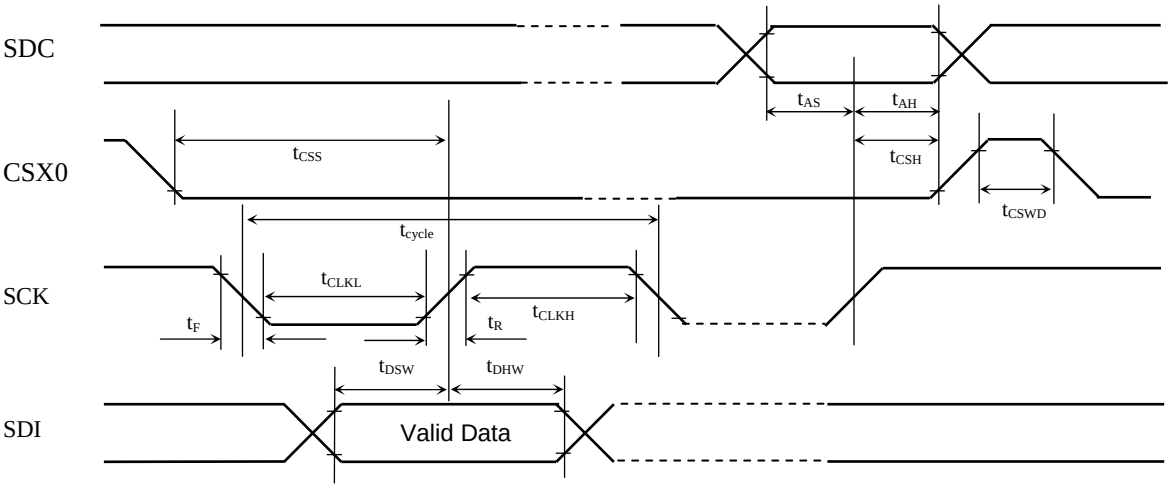
14.1 8 Bit 4 Wire SPI Interface Timing

Table 14-1: 8 Bit 4 Wire SPI Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	8T		-	ns
f_{CLK}	Serial Clock Cycle Time	-		1/8T	MHz
t_{AS}	Register select Setup Time	4		-	ns
t_{AH}	Register select Hold Time	0		-	ns
t_{CSS}	Chip Select Setup Time	4		-	ns
t_{CSH}	Chip Select Hold Time	0		-	ns
t_{DSW}	Write Data Setup Time	4		-	ns
t_{DHW}	Write Data Hold Time	0		-	ns
t_{ACC}	Read Data Access Time	-		4.4+6T	ns
t_{DHR}	Read Data Hold Time	1.2+4T		4.4+6T	ns
t_{CLKL}	Clock Low Time	4T		-	ns
t_{CLKH}	Clock High Time	4T		-	ns
t_{CSWD}	Chip Select Write Delay Time	8T		-	ns
t_{CSRD}	Chip Select Read Delay Time	16T		-	ns
t_R	Rise time	-		2	ns
t_F	Fall time	-		2	ns

Note: All timings are based on 20% to 80% of supply voltage

Write



Read

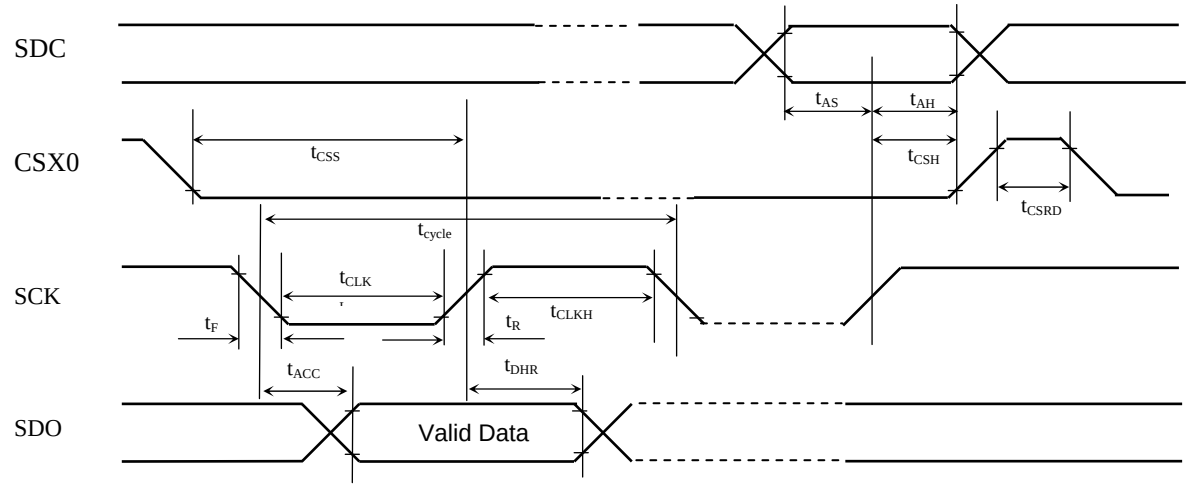


Figure 14-1: 8 Bit 4 Wire SPI Interface Timing Diagram

14.2 8 Bit 3 Wire SPI Interface Timing

Table 14-2: 8 Bit 3 Wire SPI Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	8T		-	ns
f_{CLK}	Serial Clock Cycle Time	-		1/8T	MHz
t_{CSS}	Chip Select Setup Time	4		-	ns
t_{CSH}	Chip Select Hold Time	0		-	ns
t_{DSW}	Write Data Setup Time	4		-	ns
t_{OHW}	Write Data Hold Time	0		-	ns
t_{ACC}	Read Data Access Time	-		4.4+6T	ns
t_{DHR}	Read Data Hold Time	1.2+4T		4.4+6T	ns
t_{CLKL}	Clock Low Time	4T		-	ns
t_{CLKH}	Clock High Time	4T		-	ns
t_{CSWD}	Chip Select Write Delay Time	8T		-	ns
t_{CSRD}	Chip Select Read Delay Time	16T		-	ns
t_R	Rise time	-		2	ns
t_F	Fall time	-		2	ns

Note: All timings are based on 20% to 80% of supply voltage

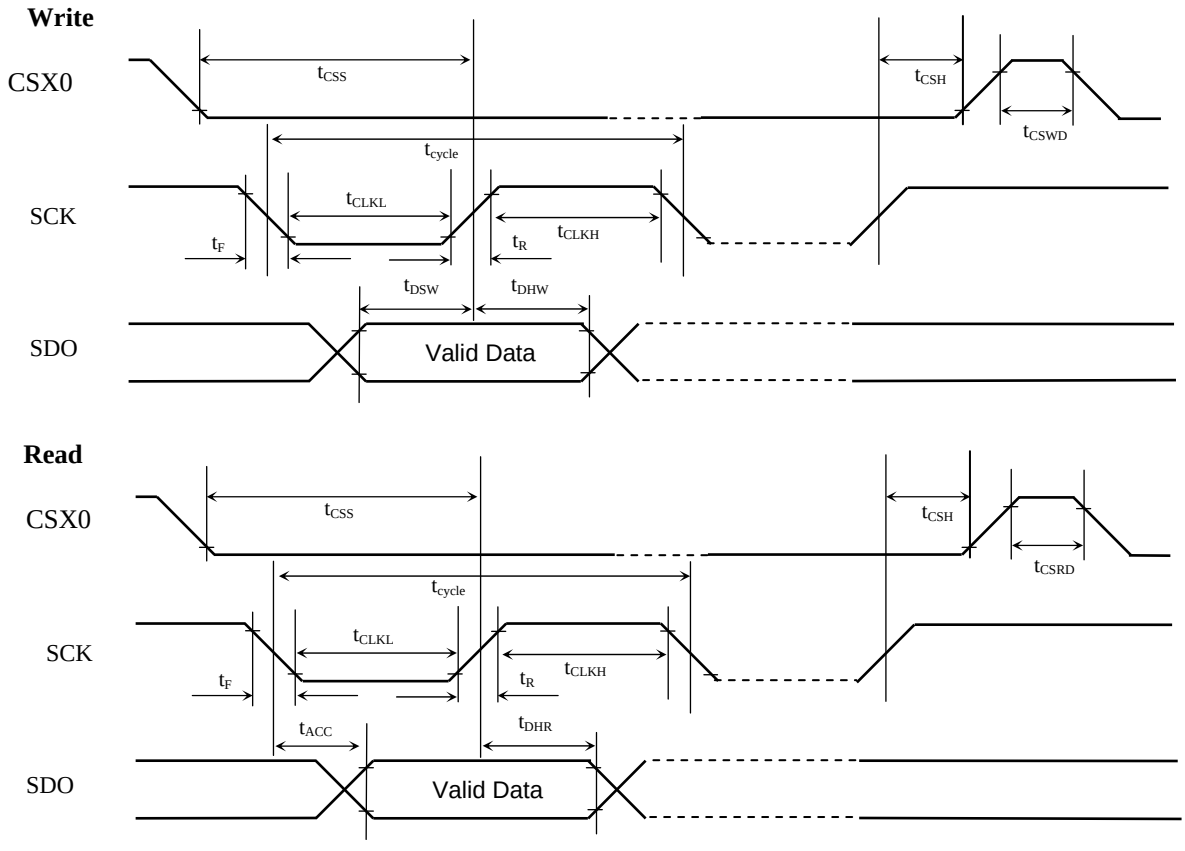


Figure 14-2: 8 Bit 3 Wire SPI Interface Timing Diagram

14.3 24 Bit 3 Wire SPI Interface Timing

Table 14-3: 24 Bit 3 Wire SPI Interface Timing Characteristics

Symbol	Parameters	Min	Typ	Max	Units
t_{cycle}	Clock Cycle Time	8T		-	ns
f_{CLK}	Serial Clock Cycle Time	-		1/8T	MHz
t_{CSS}	Chip Select Setup Time	4		-	ns
t_{CSH}	Chip Select Hold Time	0		-	ns
t_{DSW}	Write Data Setup Time	4		-	ns
t_{OHW}	Write Data Hold Time	0		-	ns
t_{ACC}	Read Data Access Time	-		4.4+6T	ns
t_{DHR}	Read Data Hold Time	1.2+4T		4.4+6T	ns
t_{CLKL}	Clock Low Time	4T		-	ns
t_{CLKH}	Clock High Time	4T		-	ns
t_{CSWD}	Chip Select Write Delay Time	8T		-	ns
t_{CSRD}	Chip Select Read Delay Time	16T		-	ns
t_R	Rise time	-		2	ns
t_F	Fall time	-		2	ns

Note: All timings are based on 20% to 80% of supply voltage

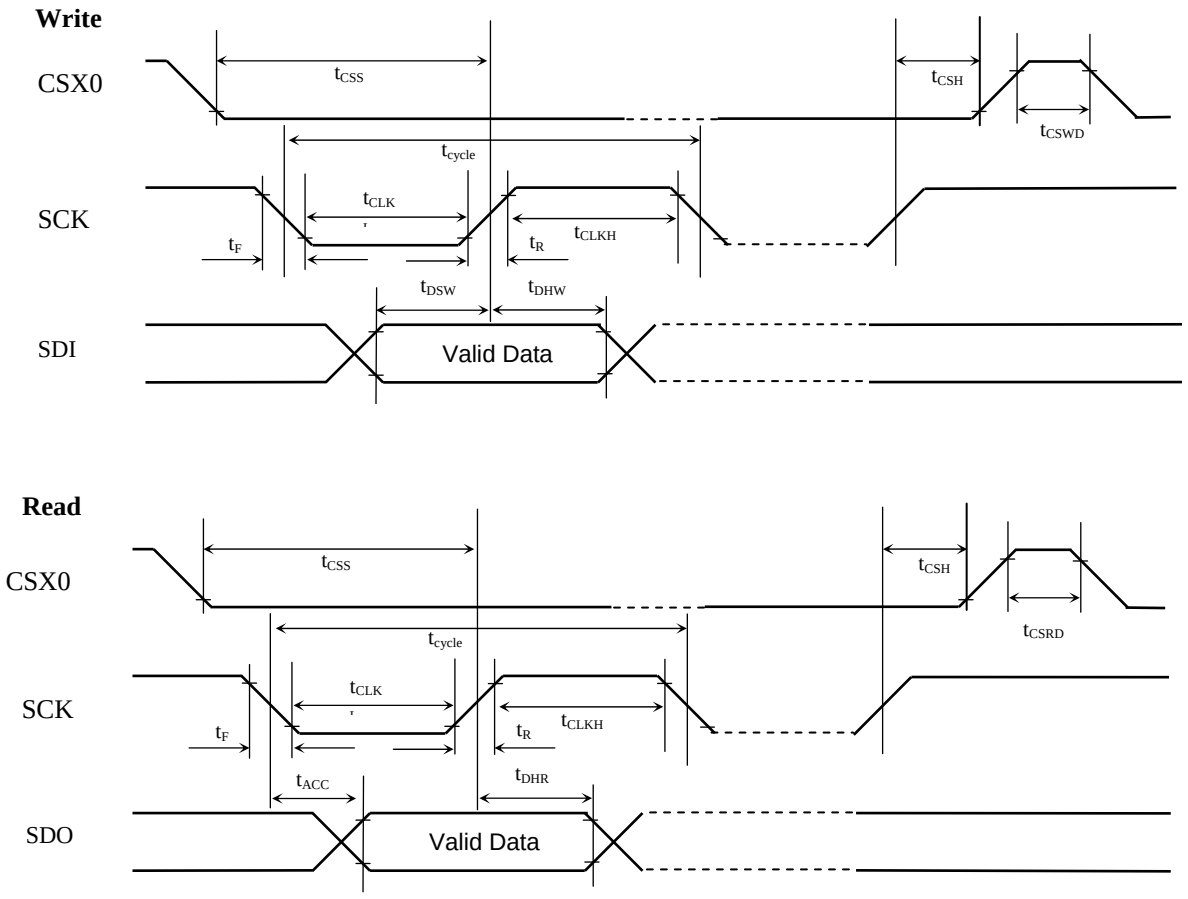


Figure 14-3: 24 Bit 3 Wire SPI Interface Timing Diagram

14.4 RGB Interface Timing

Table 14-4: RGB Interface Timing Characteristics

Symbol	Parameters	Min	Typ	Max	Units
t_{pclk}	pclk Period	16/18/24T	16/18/24T		ns
t_{vsys}	Vertical Sync Setup Time	5			ns
t_{vsyh}	Vertical Sync Hold Time	5			ns
t_{hsys}	Horizontal Sync Setup Time	5			ns
t_{hsyh}	Horizontal Sync Hold Time	5			ns
t_{hv}	Phase difference of Sync Signal Falling Edge	0		W	t_{pclk}
t_{CKL}	pclk Low Period	8/9/12T	8/9/12T		ns
t_{CKH}	pclk High Period	8/9/12T	8/9/12T		ns
t_{ds}	Data Setup Time	3.3			ns
t_{dh}	Data hold Time	3.3			ns

Note:

1. T represents the total bit rate
   Tmax = 1 / (PLL x number of lane)
   Tmax = 1 / 4G = 250ps
2. All timings are based on 20% to 80% of supply voltage
3. W is the number of pixel in a horizontal line
4. The pclk period depends on the bit per pixel (bpp) setting and whether the video mode is burst or non-burst mode. In burst mode, the values in the Min column should be followed. In non-burst mode, the values in the Typ column should be followed.

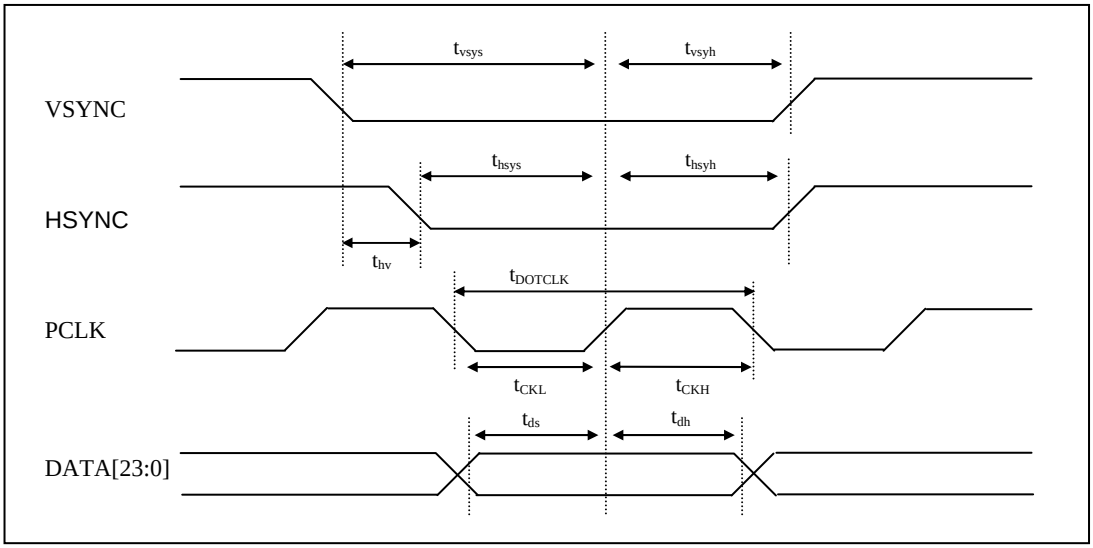


Figure 14-4: RGB Interface Timing Diagram

14.5 RESET Timing

Table 14-5: RESET Timing

Symbol	Parameters	Min	Typ	Max	Units
T_{RESET}	RESET "Low" Pulse Width	10	-	-	ms

14.6 TX_CLK Timing

Table 14-6: TX_CLK Timing Characteristics

Symbol	Parameters	Min	Typ	Max	Units
f_{TXCLK}	TX_CLK Frequency	8	-	30	MHz
t_R	Rise Time	-		10	ns
t_F	Fall Time	-		10	ns

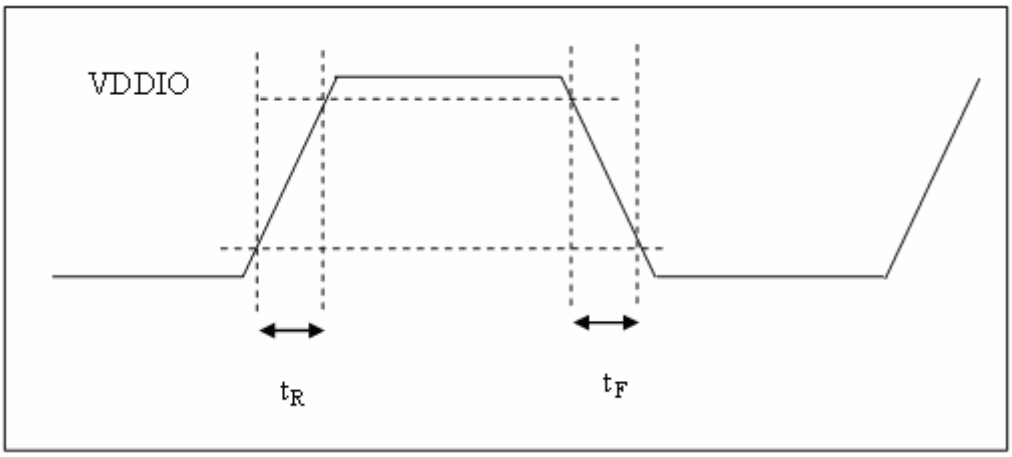
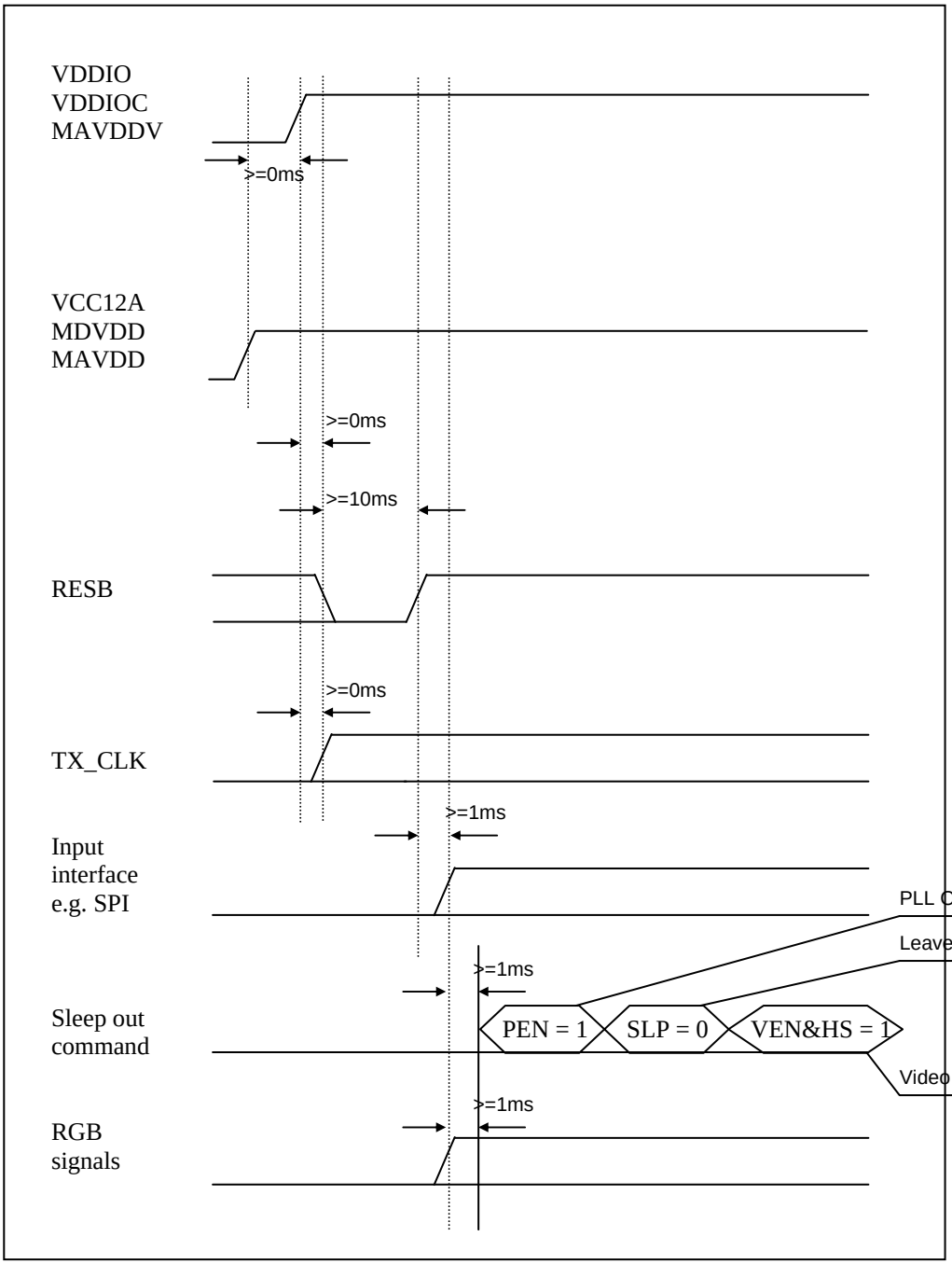
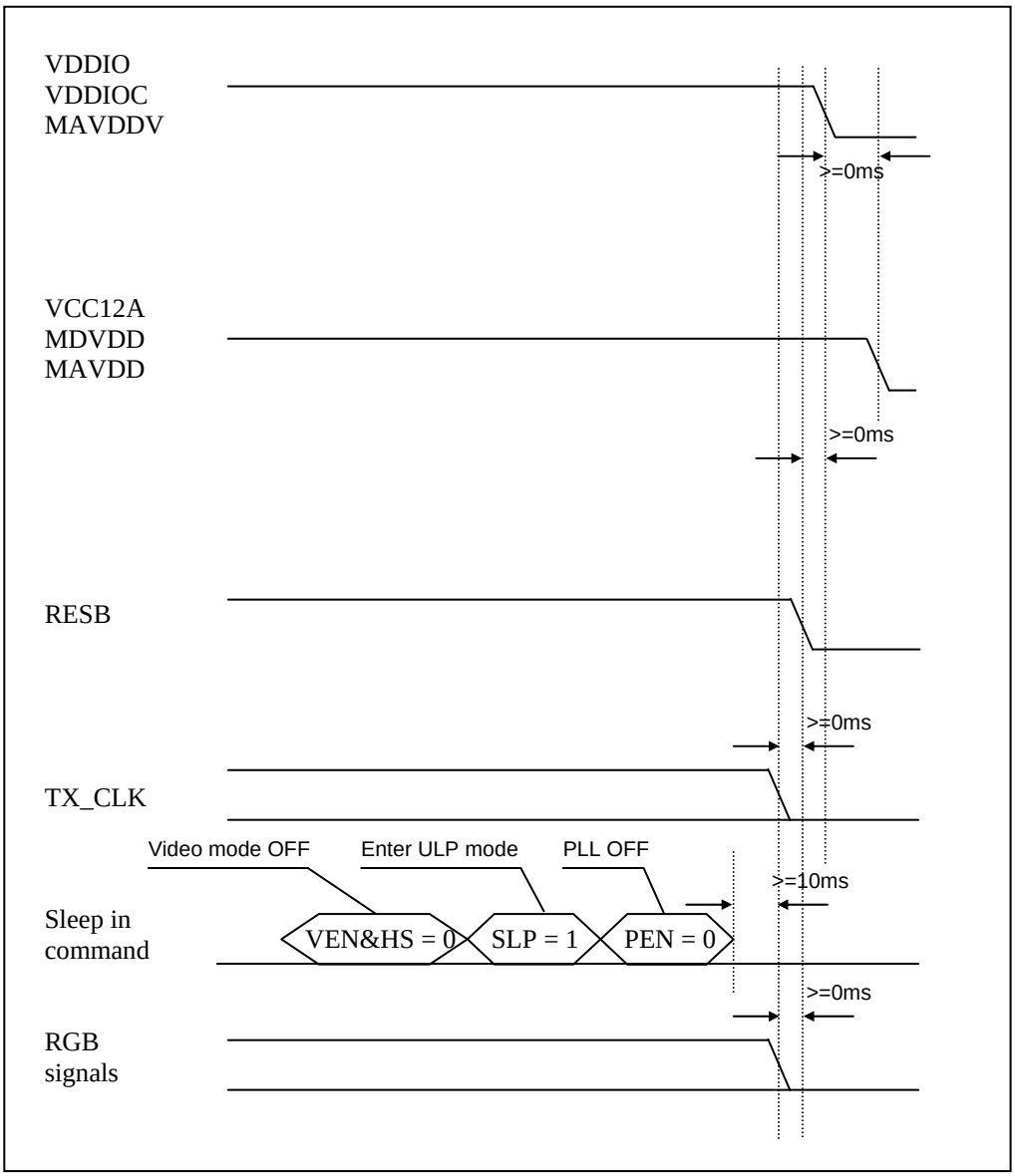


Figure 14-5: TX_CLK Timing Diagram

15 Power up sequence

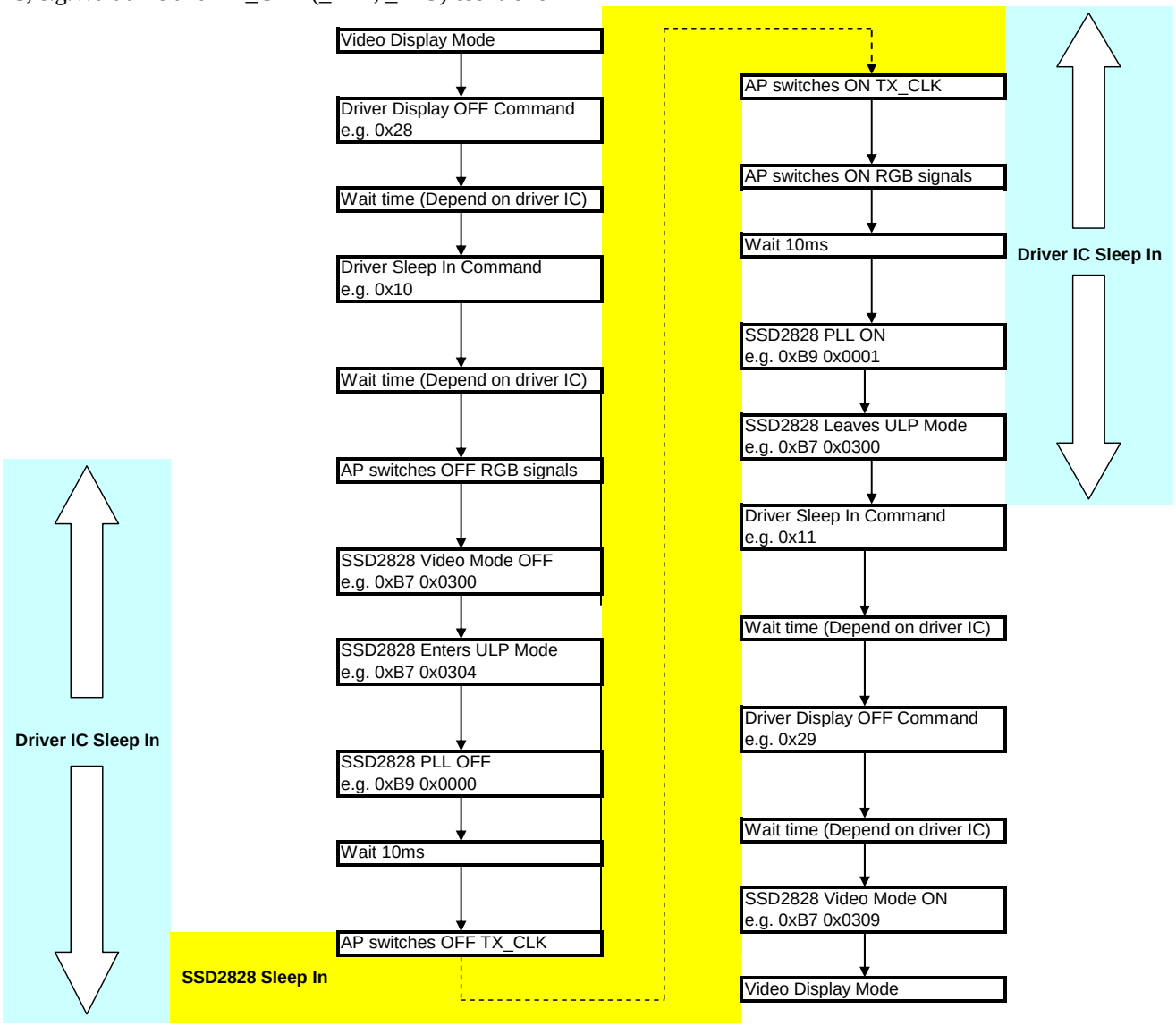


16 Power off sequence



17 Example for system sleep in and out

Note: Following example is only for reference, application must be related to the particular information of AP and driver IC, e.g.Wait time and TX_CLK (_XIN, _XIO) csontrol of AP



18 Serial Link Data Order

There are many possible ways of doing parallel to serial conversion. SSD2828 provides flexibility by programming two register bits **END** and **CO**. During video mode, they must be programmed to 0 and 1 respectively.

Below is the order to receive the display data over the serial link, when the **END** bit is 1 and **CO** bit is 0.

For 16 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Time

For 18 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4

Time

For 24 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0

Time

Below is the order to send the display data over the serial link, when the **END** bit is 0 and **CO** bit is 0.

For 16 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
G2	G1	G0	B4	B3	B2	B1	B0	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	R4	R3	R2	R1	R0	G5	G4	G3

Time

For 18 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
G1	G0	B5	B4	B3	B2	B1	B0	R3	R2	R1	R0	G5	G4	G3	G2	B5	B4	B3	B2	B1	B0	R5	R4	R1	R0	G5	G4	G3	G2	G1	G0

Time

For 24 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0	R7	R6	R5	R4	R3	R2	R1	R0

Time

Below is the order to send the display data over the serial link, when the **END** bit is 1 and **CO** bit is 1.

For 16 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R4	R3	R2	R1	R0	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R4	R3	R2	R1	R0

Time

For 18 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0	B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4

Time

For 24 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0	R7	R6	R5	R4	R3	R2	R1	R0

Time

Below is the order to send the display data over the serial link, when the **END** bit is 0 and **CO** bit is 1.

For 16 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
G2	G1	G0	R4	R3	R2	R1	R0	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R4	R3	R2	R1	R0	B4	B3	B2	B1	B0	G5	G4	G3

Time

For 18 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

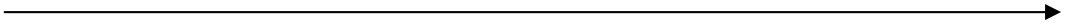
MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							

G1	G0	R5	R4	R3	R2	R1	R0	B3	B2	B1	B0	G5	G4	G3	G2	R5	R4	R3	R2	R1	R0	B5	B4	B1	B0	G5	G4	G3	G2	G1	G0

Time

For 24 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0

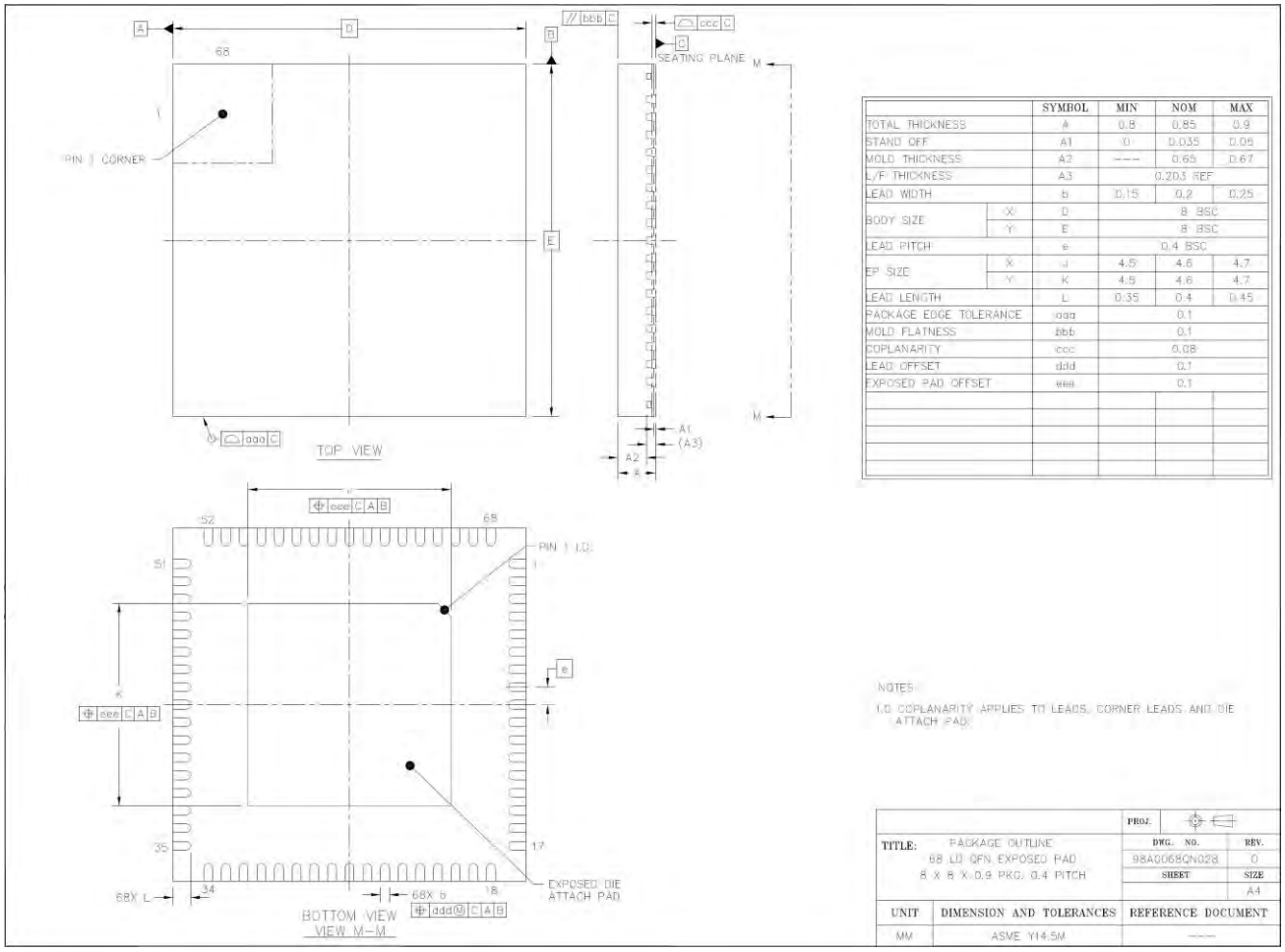


Time

19 PACKAGE INFORMATION

19.1 Dimension for SSD2828QN4

Figure 19-1- Package Information



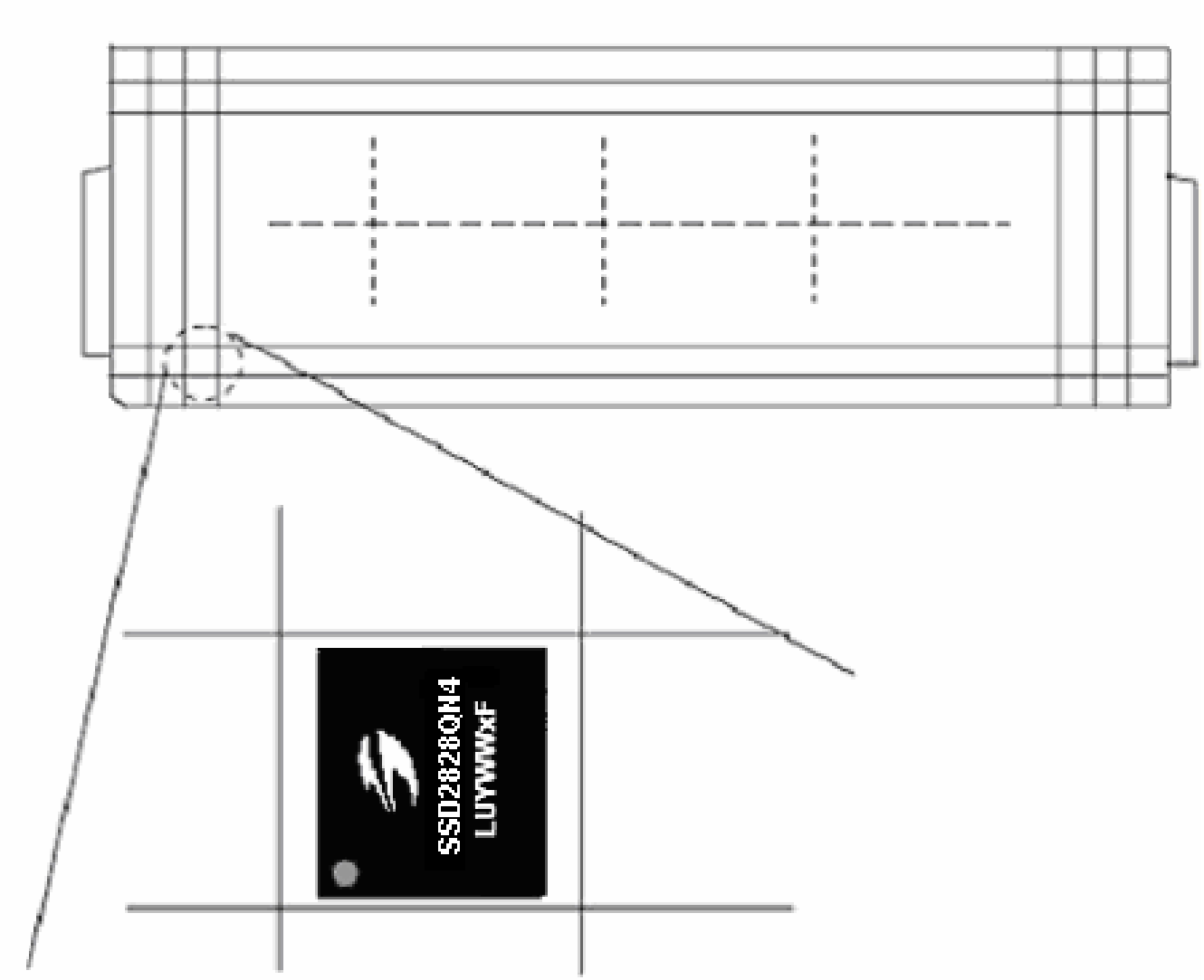
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	----	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	4.5	4.6	4.7
	Y	K	4.5	4.6	4.7
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

TITLE: PACKAGE OUTLINE 68 LD QFN EXPOSED PAD 8 X 8 X 0.9 PKG 0.4 PITCH		PROJ.	
		DWG. NO.	REV.
		98A0068QN028	0
		SHEET	SIZE
			A4
UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT	
MM	ASME Y14.5M	----	

Figure 19-2- Marking Information



Figure 19-3- Tray Information



Solomon Systech reserves the right to make changes without notice to any products herein. Solomon Systech makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Solomon Systech assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any, and all, liability, including without limitation consequential or incidental damages. “Typical” parameters can and do vary in different applications. All operating parameters, including “Typical” must be validated for each customer application by the customer’s technical experts. Solomon Systech does not convey any license under its patent rights nor the rights of others. Solomon Systech products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Solomon Systech product could create a situation where personal injury or death may occur. Should Buyer purchase or use Solomon Systech products for any such unintended or unauthorized application, Buyer shall indemnify and hold Solomon Systech and its offices, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Solomon Systech was negligent regarding the design or manufacture of the part.

The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

http://www.solomon-systech.com