Advanced Power MOSFET

SSF25N40A

FEATURES

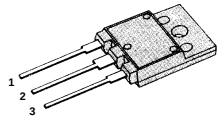
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10 μA (Max.) @ V_{DS} = 400V
- Low $R_{DS(ON)}$: 0.162 Ω (Typ.)

BV_{DSS} = 400 V

$R_{DS(on)}$ = 0.2 Ω

I_D = 14.3 A

TO-3PF



1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	400	V
I_D	Continuous Drain Current (T_C=25 °C)	14.3	A
	Continuous Drain Current (T_C=100 °C)	9.1	
I_{DM}	Drain Current-Pulsed ①	100	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy ②	1753	mJ
I_{AR}	Avalanche Current ①	14.3	A
E_{AR}	Repetitive Avalanche Energy ①	10	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
P_D	Total Power Dissipation (T_C=25 °C)	100	W
	Linear Derating Factor	0.8	W/°C
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	°C
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.25	°C/W
$R_{\theta JA}$	Junction-to-Ambient	--	40	

Rev. B

FAIRCHILD SEMICONDUCTOR™

Electrical Characteristics (T_C=25°Cunless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	400	--	--	V	V_{GS}=0V,I_D=250μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.52	--	V/°C	I_D=250μA ***See Fig 7***
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=5V,I_D=250μA
I_{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	V_{GS}=30V
	Gate-Source Leakage , Reverse	--	--	-100		V_{GS}=-30V
I_{DSS}	Drain-to-Source Leakage Current	--	--	10	μA	V_{DS}=400V
		--	--	100		V_{DS}=320V,T_C=125°C
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.2	Ω	V_{GS}=10V,I_D=7.15A ④
g_{fs}	Forward Transconductance	--	14.28	--	Ω	V_{DS}=50V,I_D=7.15A ④
C_{iss}	Input Capacitance	--	3180	4130	pF	V_{GS}=0V,V_{DS}=25V,f =1MHz ***See Fig 5***
C_{oss}	Output Capacitance	--	435	500		
C_{rss}	Reverse Transfer Capacitance	--	200	240		
$t_{d(on)}$	Turn-On Delay Time	--	22	55	ns	V_{DD}=200V,I_D=25A, R_G=5.3Ω ***See Fig 13*** ④⑤
t_r	Rise Time	--	25	60		
$t_{d(off)}$	Turn-Off Delay Time	--	127	260		
t_f	Fall Time	--	38	85		
Q_g	Total Gate Charge	--	140	182	nC	V_{DS}=320V,V_{GS}=10V, I_D=25A ***See Fig 6 & Fig 12*** ④⑤
Q_{gs}	Gate-Source Charge	--	21	--		
Q_{gd}	Gate-Drain(“Miller”) Charge	--	64.8	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	14.3	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	100		
V_{SD}	Diode Forward Voltage ④	--	--	1.5	V	T_J=25°C,I_S=14.3A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	484	--	ns	T_J=25°C,I_F=25A
Q_{rr}	Reverse Recovery Charge	--	7.6	--	μC	di_F/dt=100A/μs ④

Notes ;

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

② L=15mH, I_{AS}=14.3A, V_{DD}=50V, R_G=27Ω, Starting T_J=25 °C

③ I_{SD} ≤ 25A, di/dt ≤ 320A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J=25 °C

④ Pulse Test : Pulse Width = 250 μs, Duty Cycle ≤ 2%

⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

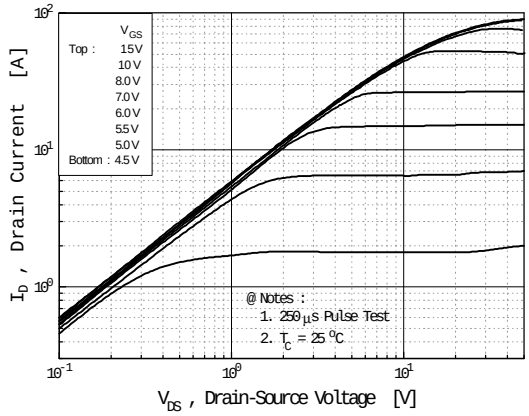


Fig 2. Transfer Characteristics

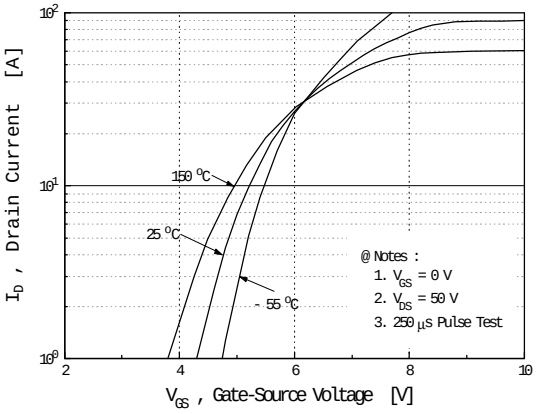


Fig 3. On-Resistance vs. Drain Current

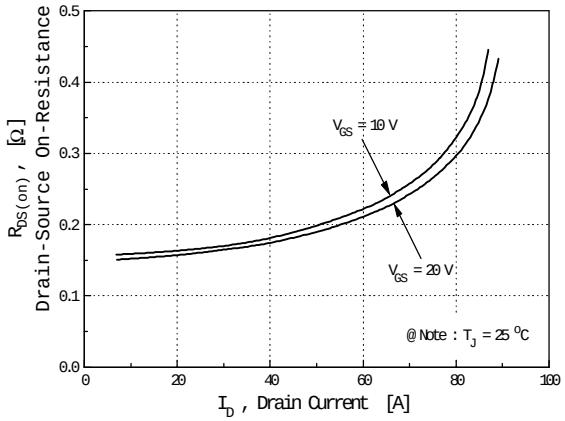


Fig 4. Source-Drain Diode Forward Voltage

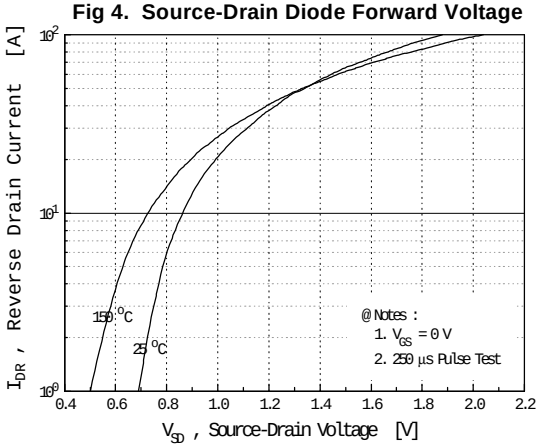


Fig 5. Capacitance vs. Drain-Source Voltage

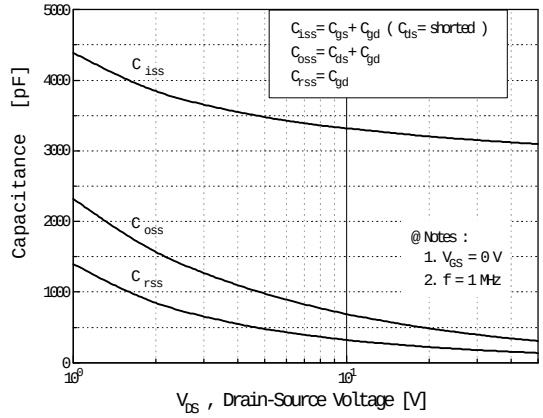


Fig 6. Gate Charge vs. Gate-Source Voltage

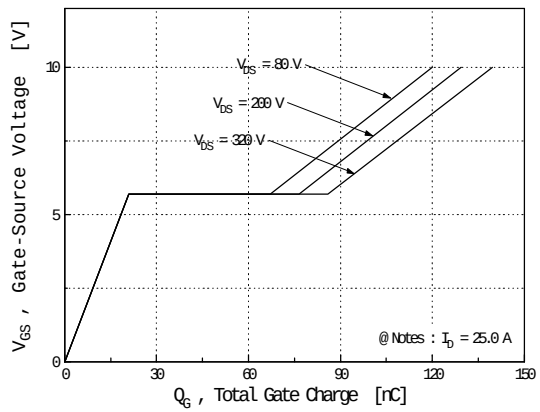


Fig 7. Breakdown Voltage vs. Temperature

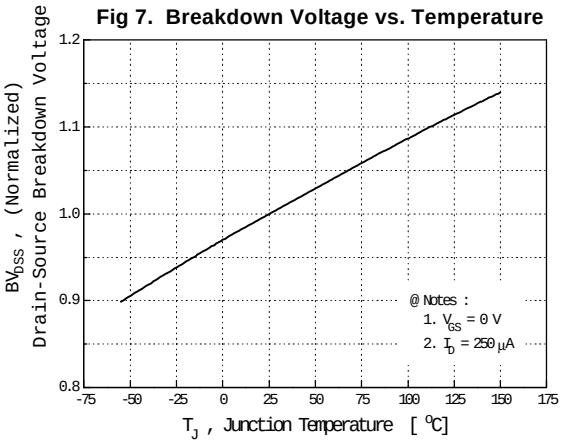


Fig 8. On-Resistance vs. Temperature

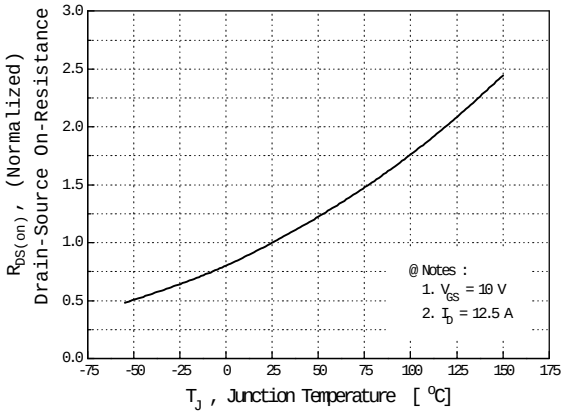


Fig 9. Max. Safe Operating Area

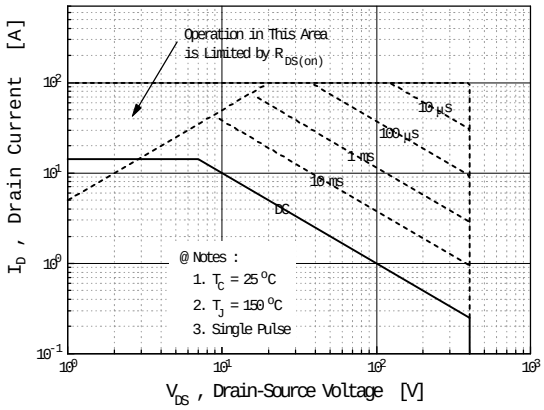


Fig 10. Max. Drain Current vs. Case Temperature

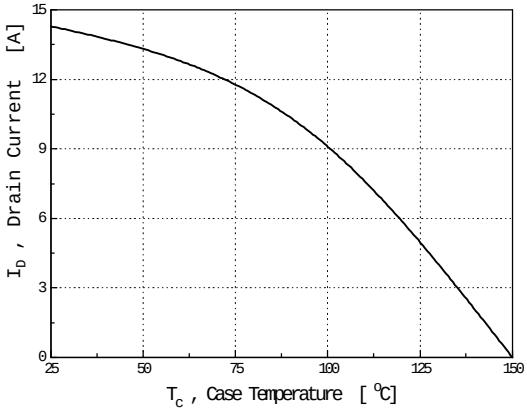


Fig 11. Thermal Response

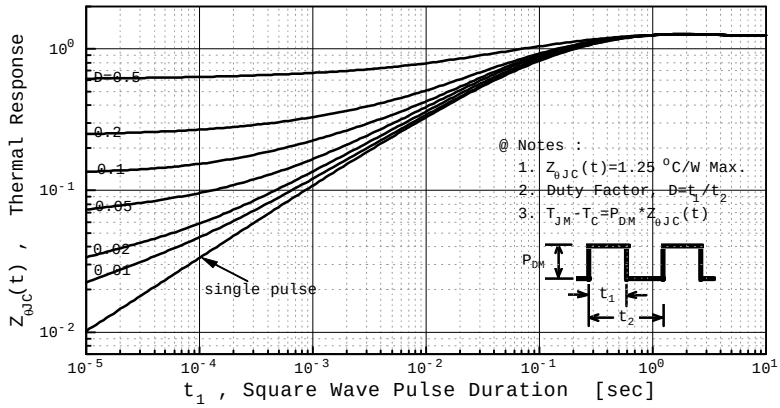


Fig 12. Gate Charge Test Circuit & Waveform

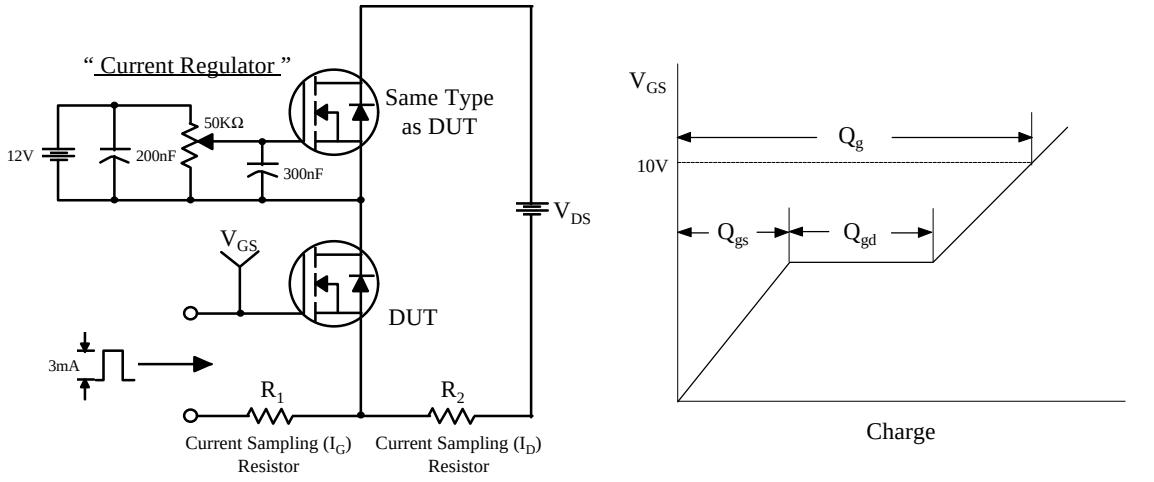


Fig 13. Resistive Switching Test Circuit & Waveforms

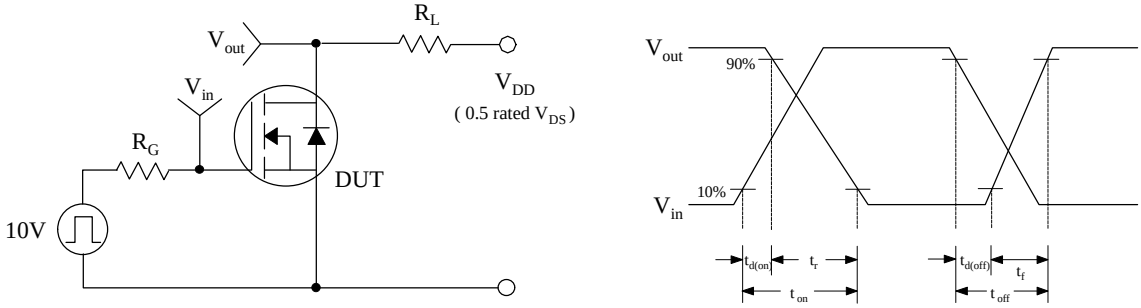


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

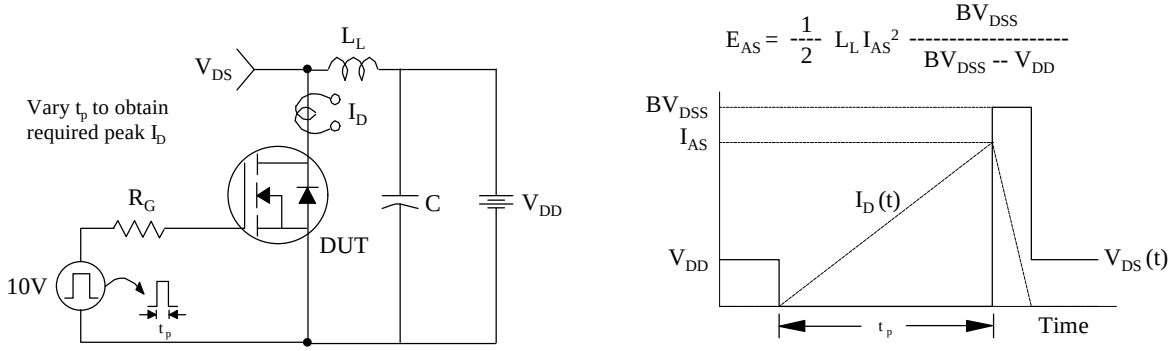
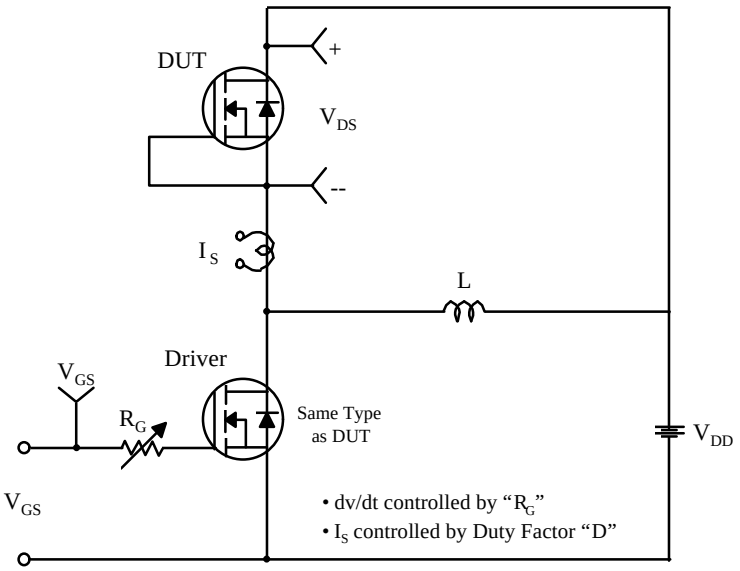
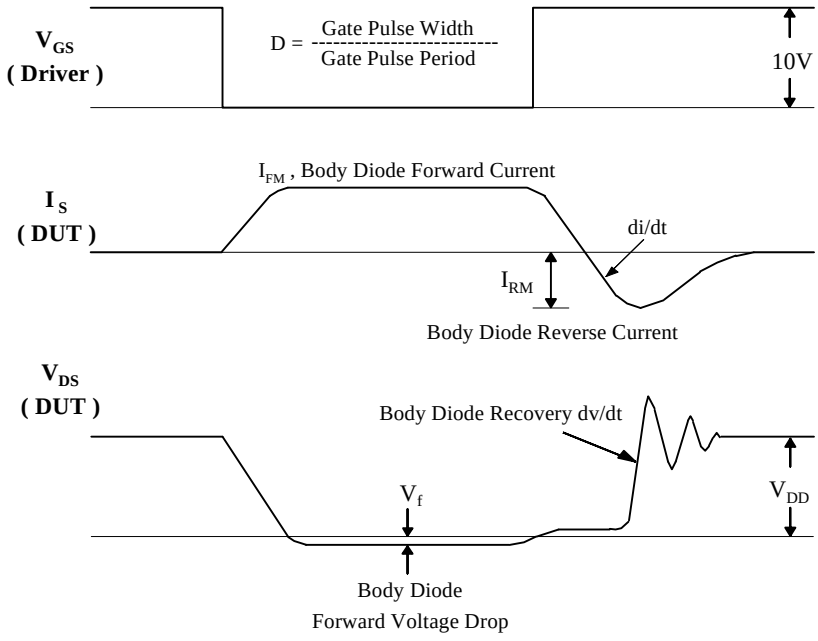


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





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