CDB42L42

Evaluation Board for the CS42L42

Features

- Analog I/O uses four-conductor, 1/8” (3.5 mm) audio with presence detection
- SoundWire compatible—CS42L42 can operate as a SoundWire slave device
- Headset mic input
- CS42L42 S/PDIF OUT (transmit) jack
- Configurable serial audio headers
- Headphone output from the CS42L42
- S/PDIF Rx/Tx into CS42L42
- FlexGUI software control from USB mini-B
  - — Windows® compatible
  - — Predefined and user-configurable scripts

Description

The CDB42L42 is a dedicated platform for testing and evaluating the CS42L42, a high-fidelity audio codec with SoundWire™–I²S/TDM and audio processing. To allow comprehensive testing of CS42L42 features and performance, extensive software-configurable options are available on the CDB42L42.

Software options, such as register settings for the CS42L42, are configured via FlexGUI software, which communicates with the CDB42L42 via USB from a Windows-compatible computer.

The CDB42L42 also serves as the component and layout reference for the CS42L42.

Ordering Information

CDB42L42	Evaluation Board

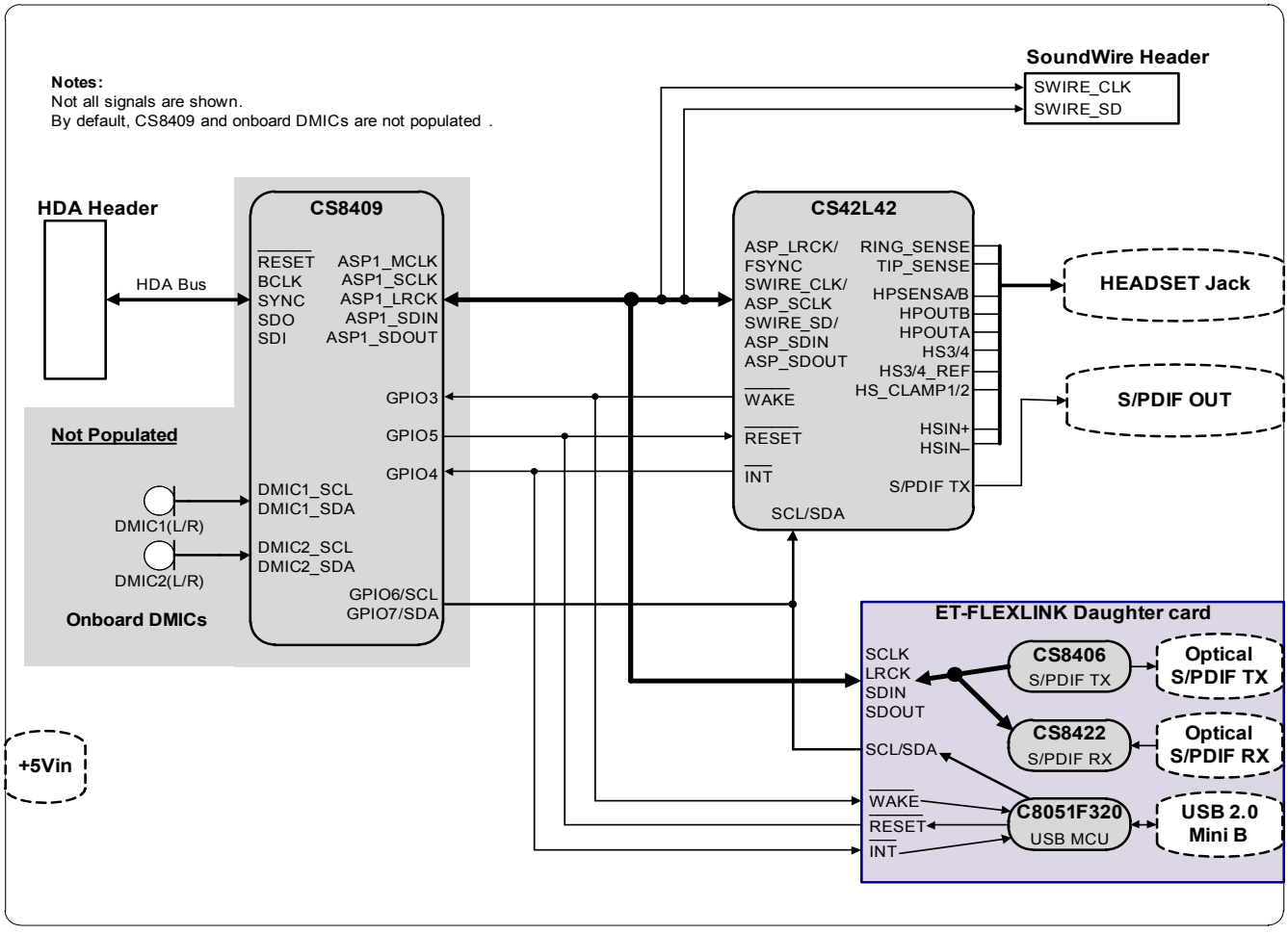


Table of Contents

1 CDB42L42 System Overview

The CDB42L42 evaluation board is a convenient platform for evaluating the CS42L42, a high-fidelity audio codec with I²S/TDM and audio processing. By default, the audio serial port is a slave device; however, it can be configured as a hybrid-master device via I²C. The port can also be configured as a SoundWire slave . It supports multiple power supply and signal I/O configurations and serves as the component and layout reference for the CS42L42.

The following subsections describe the CDB42L42 evaluation board in detail. Fig. 1-1 shows a detailed view of the system.

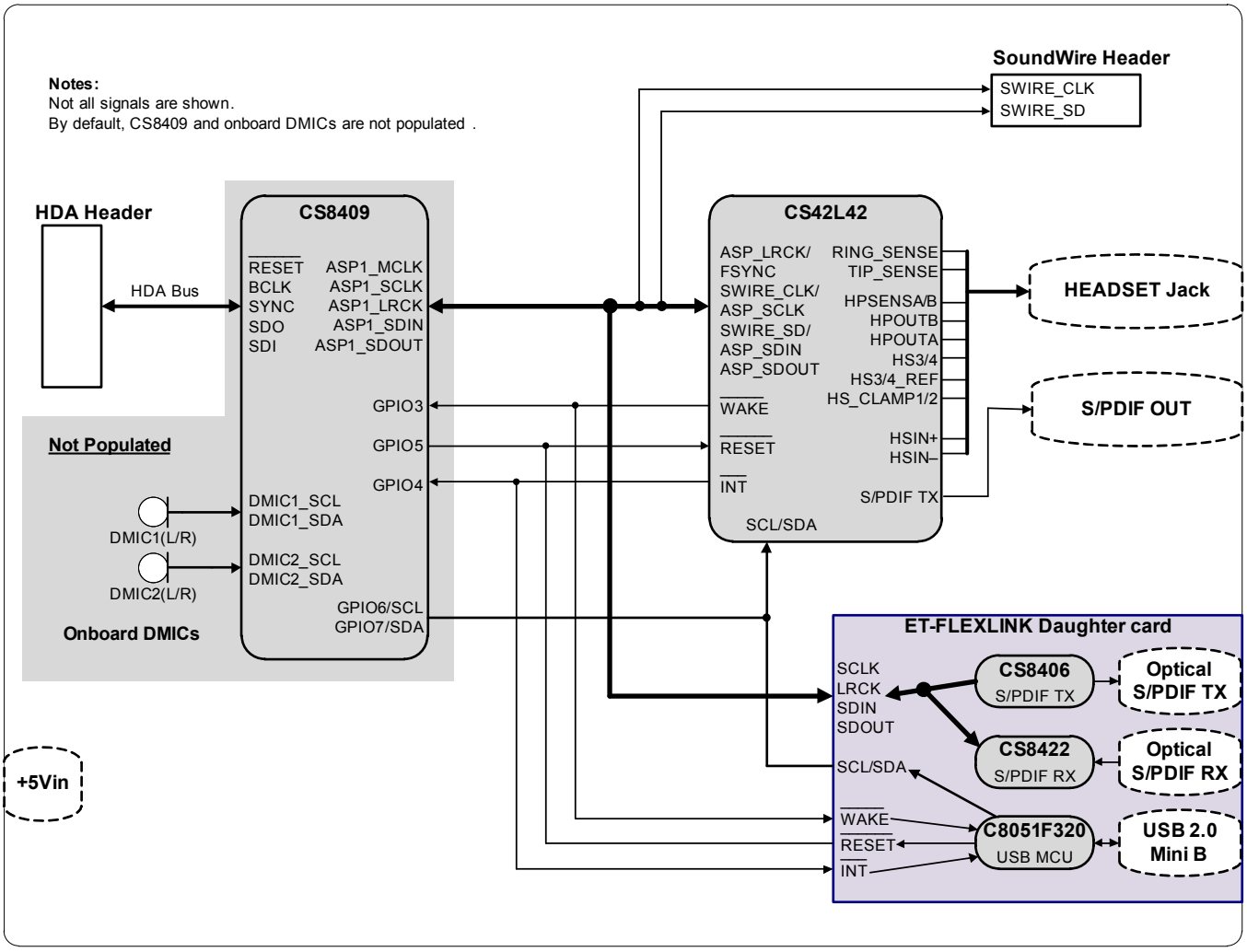


Figure 1-1. CDB42L42 Block Diagram

1.1 Power-Supply Circuitry

The CDB42L42 can be powered from a +5-V wall-wart DC power jack (see entry for J2 in Table 4-1).

Low-dropout regulators step down the +5-V supply to provide a clean and stable +1.2-V (x2), +1.8-V, and +3.3-V rails to the CS42L42 and peripheral circuits on the board. This includes a 1.8-V LDO, a 3.3-V LDO, and two 1.2-V LDOs. The 1.2-V LDOs provide a way to externally power up the VD_FILT power pin while supplying 1.2 V for VL. Fig. 1-2 shows the CDB42L42 power routing and configurations.

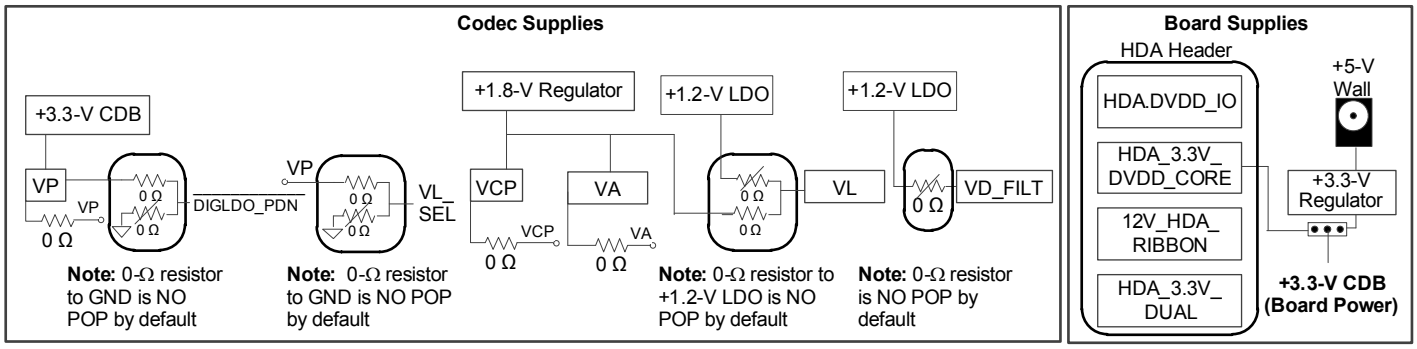


Figure 1-2. CDB42L42 Power Supplies

1.2 Serial Audio I/O Headers

Header J8 provides visibility for the I²S serial audio clocks and data. The header signals are described in Table 1-1The default logic level is 1.8 V.

Table 1-1. Serial Audio Input Header (J8)

Pin	Header Pin	Direction	Description
1	CS42L42_SCLK/SWIRE_CLK	I	ASP system/SoundWire clock
3	CS42L42_LRCK	I/O	ASP frame clock
5	CS42L42_SDOUT	O	ASP data out
7	CS42L42_SDIN/SWIRE_SD	I/O	ASP data input/SoundWire data I/O
2, 4, 6, 8	Ground	Ground reference	Board ground

1.3 S/PDIF Transmitter

The CS42L42 provides an S/PDIF transmitter output, routed to the 3.5-mm jack through a 1.8- to 3.3-V level translator.

1.4 Headset Jack

The CDB42L42 platform contains 1-1/8” TRRS jack for headset connection. The jack connects to the HSIN+,HSIN–, HPOUTA, HPOUTB, HPSENSA, HPSENSB, RING_SENSE, TIP_SENSE, HS_CLAMP1, HS_CLAMP2, HS3, HS4, HS3_REF, and HS4_REF signals on the CS42L42.

1.5 LEDs

There are LED indicators showing the state of the serial buses and GPIO signals—green for Logic 1 and red for Logic 0. In addition, several green LEDs indicate whether respective power supplies are present. The ET-FLEXLINK LEDs are shown in Table 1-2 below. CDB42L42 LEDs are shown in Table 1-2 below.

Table 1-2. ET-FLEXLINK LEDs

LED	Color	Silkscreen	Description
D0 D1 D2 D3	Orange	D0 D1 D2 D3	MCU outputs, not used by FlexGUI
D4	Green	+5V	Illuminated when +5V rail is present
D5	Green	USB.VBUS	Illuminated when USB (J2) VBUS is present
D6	Green	+5V.CDB	Illuminated when +5V.CDB rail is present
D7	Green	+3.3V	Illuminated when +3.3V rail is present
D8	Green	+1.8V	Illuminated when +1.8V rail is present
D9	Green	+VIO	Illuminated when +VIO rail is present

Table 1-3. CDB42L42 LEDs

LED	Color	Silkscreen	Description
D3	Green	+12V	Illuminated when +12V_HDA_RIBBON rail is present
D5	Green	+3.3V_DUAL	Illuminated when +3.3V_DUAL rail is present
D6	Green	VL_HD	Illuminated when HDA.3_3V.DUAL rail is present
D7	Green	+3.3V	Illuminated when +3.3V_CDB rail is present
D8	Green	+1.8V	Illuminated when +1.8V_CDB rail is present
D9	Green	VP	Illuminated when +5V_CDB rail is present
D11/D10	Green/Red	H/L GPIO7 SDA	Green/Red when GPIO7/SDA is high/low
D14/D13	Green/Red	H/L GPIO6 SCL	Green/Red when GPIO6 SCL is high/low
D16/D15	Green/Red	H/L GPIO5 L42 RST	Green/Red when GPIO5/L42 RST is high/low
D18/D17	Green/Red	H/L GPIO4 L42 INT	Green/Red when GPIO4/'L42 INT is high/low
D20/D19	Green/Red	H/L GPIO3 L42 WAKE MISO2	Green/Red when GPIO3/L42 WAKE is high/low
D22/D21	Green/Red	H/L GPIO2 CS2	Green/Red when GPIO2/CS2 is high/low
D24/D23	Green/Red	H/L GPIO1 CS1	Green/Red when GPIO1/CS1 is high/low
D26/D25	Green/Red	H/L GPIO0 MISO1	Green/Red when GPIO0/MISO1 is high/low

1.6 S/PDIF RX/TX

The CDB42L42 platform contains the ET-FLEXLINK daughter card, which provides I²S audio data input to the CS42L42 from the CS8422 S/PDIF receiver and audio data output from the CS42L42 to the CS8406 S/PDIF transmitter. Fig. 1-3 shows the default I²S clocking architecture of the CS8422/CS8406 on the ET-FLEXLINK.

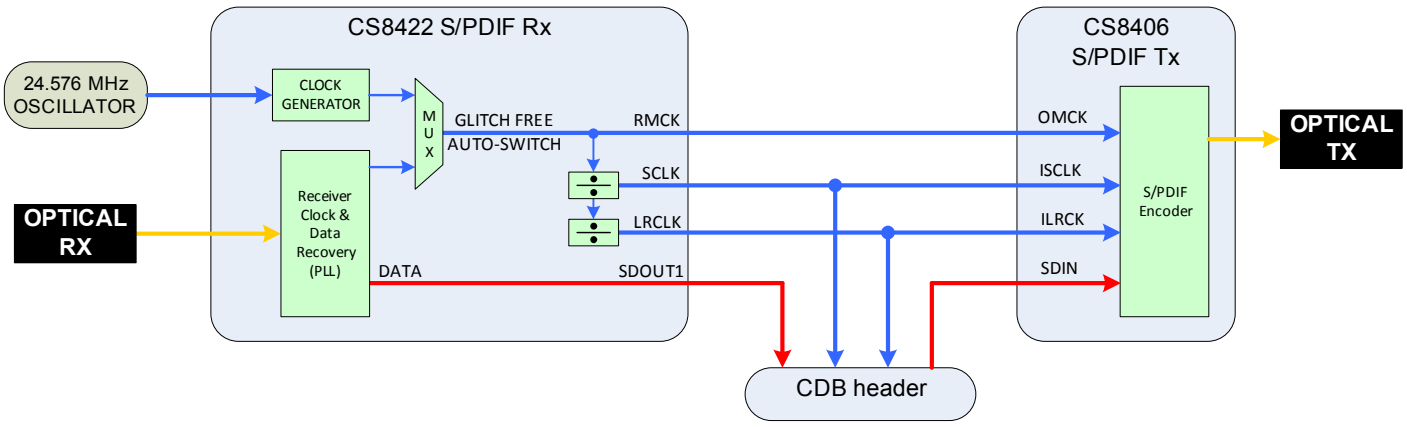


Figure 1-3. Default Clocking

2 Quick Setup Guide

The CDB42L42 can be configured in FlexGUI Mode with S/PDIF RX/TX, FlexGUI Mode with external I²S/TDM, or SoundWire™ Mode, as described in the following sections.

2.1 Quick Setup Guide—FlexGUI Mode with S/PDIF RX/TX

This short procedure sets the CDB42L42 to a standard state for evaluation in FlexGUI Mode with S/PDIF RX/TX.

1. Install the FlexGUI software. See Section 3.
2. Set CDB42L42 jumpers J3, J4, and J6 and ET-FLEXLINK J3, shown by red indicators in Fig. 2-1. See Table 4-1.
3. Connect cabling to the CDB42L42 as shown by green indicators in Fig. 2-1.
4. Launch FlexGUI software (Start → Programs → Cirrus Logic → FlexLoader → Launch FlexLoader.exe) and run the Quick Setup selection based on your desired sample rate. See Section 3.1.2.

Jumper Connections:	
J3.1 +5V	J3.3 CDB
J4.2 CDB	J4.3 +3.3V
J3.2 SCLK CS42L42	J3.3 SCLK AUDIO INTERFACE
J3.5 LRCK CS42L42	J3.6 LRCK AUDIO INTERFACE
J3.8 SDOUT CS42L42	J3.9 SDOUT AUDIO INTERFACE
J3.11 SDIN CS42L42	J3.12 SDIN AUDIO INTERFACE
J6.2 SEL SWIRE_SEL	J6.3 G SWIRE_SEL

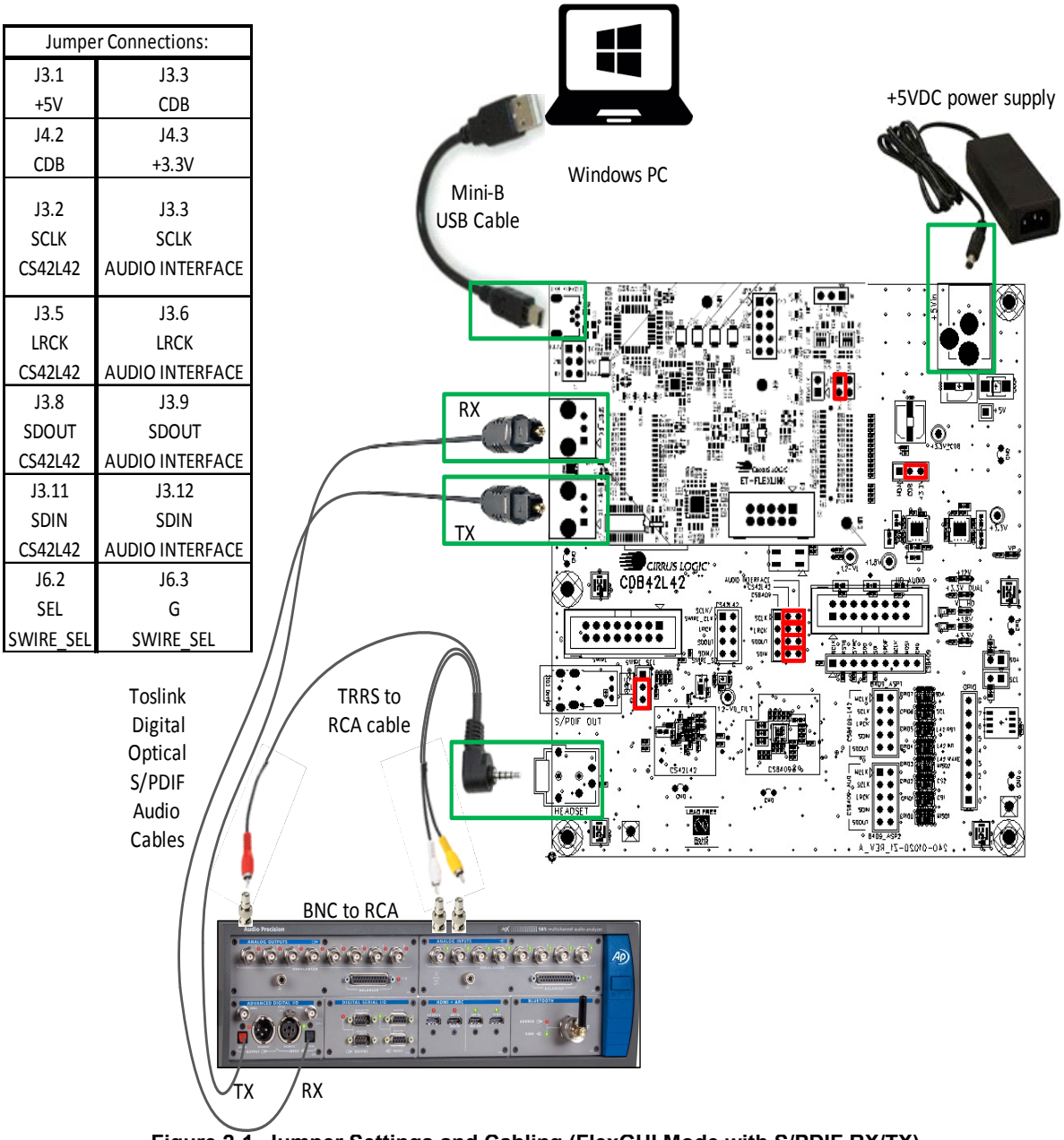


Figure 2-1. Jumper Settings and Cabling (FlexGUI Mode with S/PDIF RX/TX)

2.2 Quick Setup Guide—FlexGUI Mode with External I²S

This section describes a short procedure to set the CDB42L42 to a standard state for evaluation in FlexGUI Mode with external I²S.

1. Install the FlexGUI software. See Section 3.2.
2. Set jumpers on CDB42L42 J3, J4, and J6 and on ET-FLEXLINK J3, as shown by the red indicators in Fig. 2-2. See Table 4-1.
3. Connect Cabling to the CDB42L42 as shown by the green indicators in Fig. 2-2.
4. Launch FlexGUI software (Start → Programs → Cirrus Logic → FlexLoader → Launch FlexLoader.exe) and run the Quick Setup selection based on your desired sample rate. See Section 3.1.2.

Jumper Connections:	
J3.1 +5V	J3.3 CDB
J4.2 CDB	J4.3 +3.3V
J3.2 SCLK CS42L42	J3.3 SCLK AUDIO INTERFACE
J3.5 LRCK CS42L42	J3.6 LRCK AUDIO INTERFACE
J3.8 SDOUT CS42L42	J3.9 SDOUT AUDIO INTERFACE
J3.11 SDIN CS42L42	J3.12 SDIN AUDIO INTERFACE
J6.2 SEL SWIRE_SEL	J6.3 G SWIRE_SEL

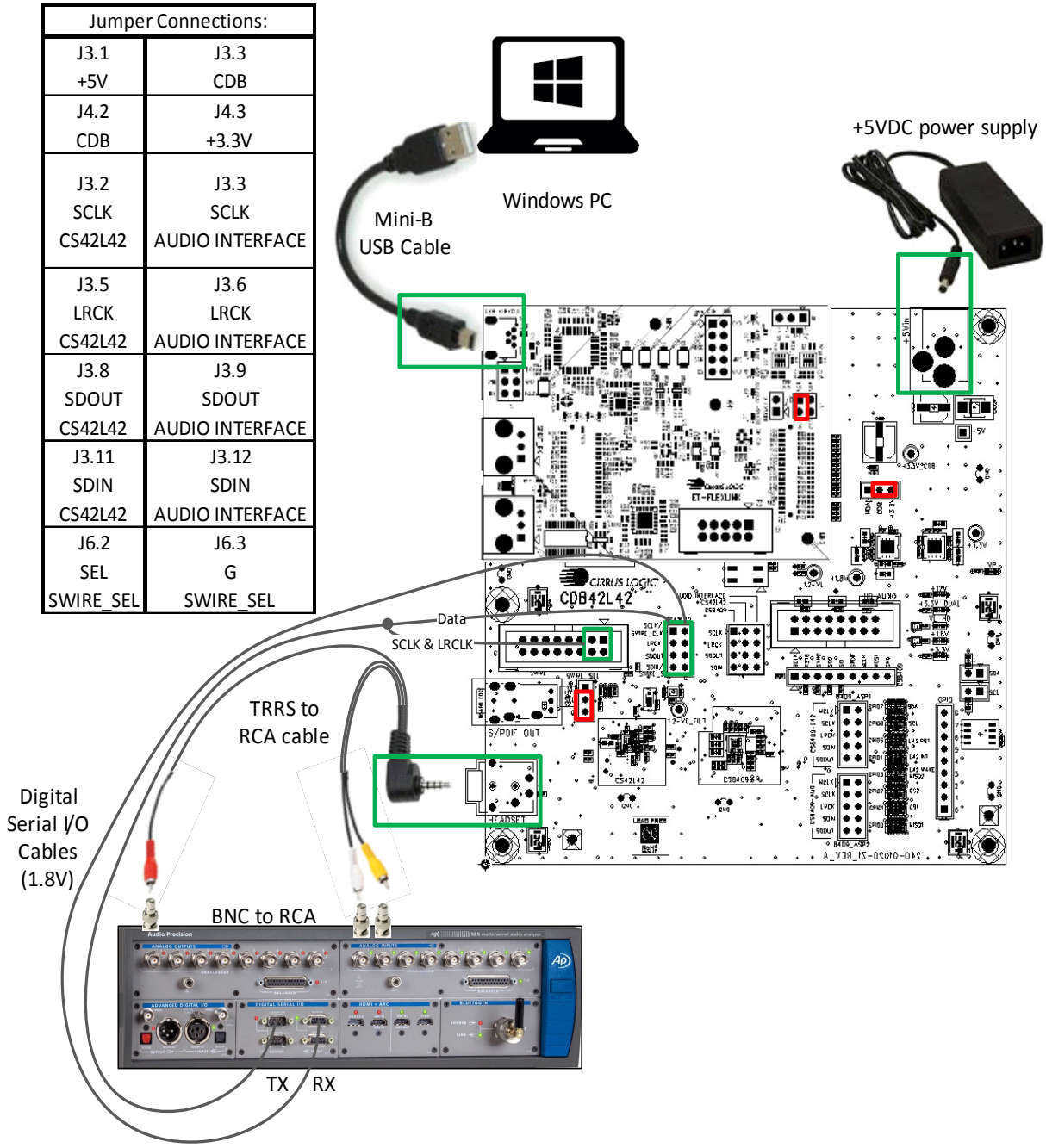


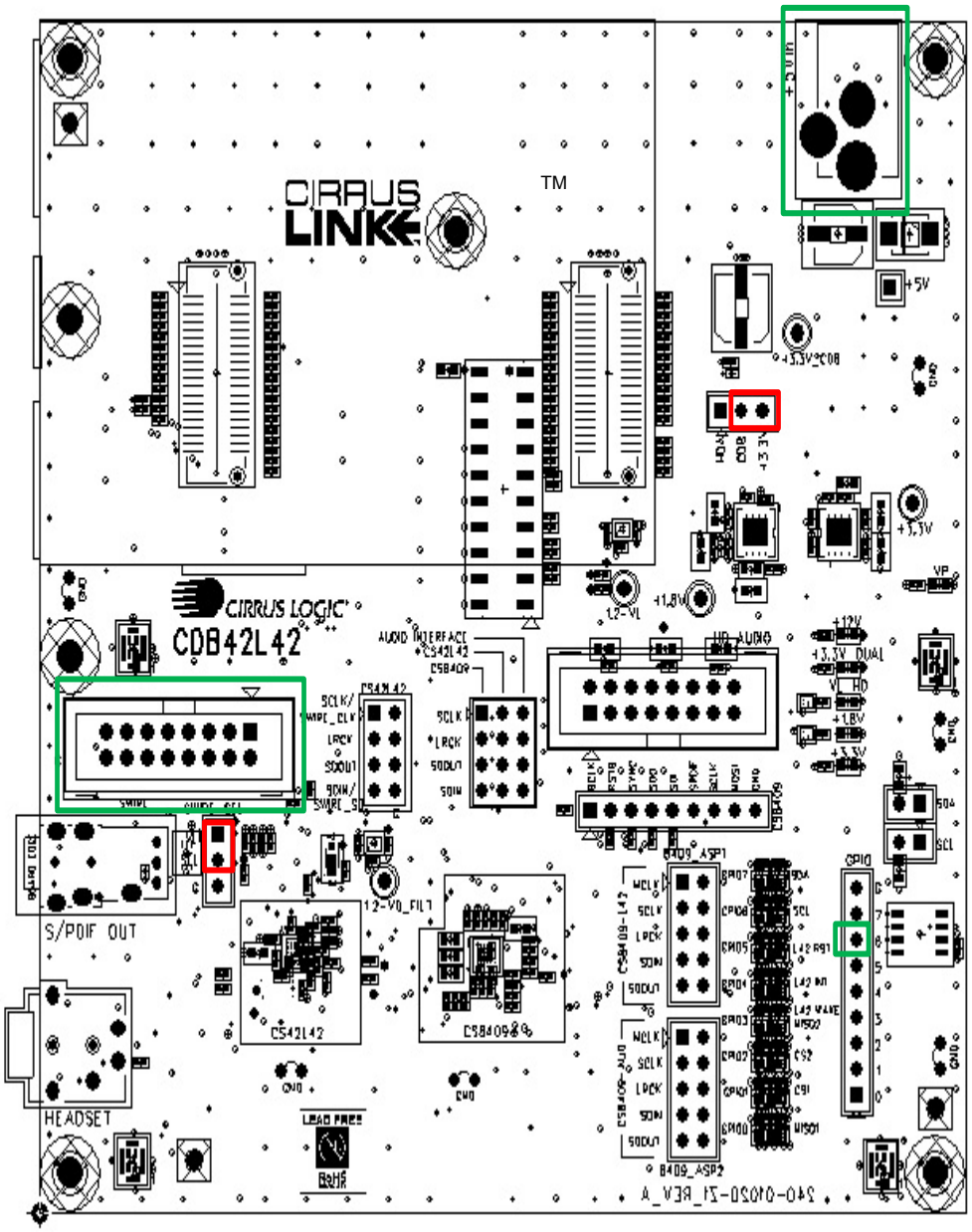
Figure 2-2. Jumper Settings (FlexGUI Mode with External I²S)

2.3 Quick Setup Guide—SoundWire Mode

This section describes a short procedure to set the CDB42L42 to a standard state for evaluation in SoundWire Mode.

Note: The ET-FLEXLINK daughter card supports only I²C operation. For SoundWire Mode, an external SoundWire master must be used.

1. Remove the ET-FLEXLINK daughter card. There is a standoff holding the ET-FLEXLINK daughter card to the CDB42L42.
2. Set jumpers J6 and J4 as shown by the red indicators in Fig. 2-3. See Table 4-1. Jumpers must be removed from J3.
3. Connect a SoundWire master to the SoundWire slave header (J10, shown in green on the left side; see Table 4-1).
4. Connect a RESET control signal from the master to J18 Pin 6, shown in green on the right side; see Table 4-1).
5. Connect a +5-V supply to the wall-wart jack (J2, shown in green in the top, right corner; see Table 4-1).



Jumper Connections:	
J4.2 CDB	J4.3 +3.3V
J6.1 VL	J6.2 SEL
SWIRE_SEL	SWIRE_SEL

Figure 2-3. Jumper Settings (SoundWire Mode)

3 Software Control Using FlexGUI

Note: The Cirrus Logic FlexGUI application allows users to easily configure software modifiable options on the CDB42L42, such as the register settings of the CS42L42 and the S/PDIF interface devices (CS8422, CS8406). FlexGUI supports only I²C operation. To use SoundWire, see the appropriate sections in Section 2. For SoundWire Mode, an external SoundWire master must be used.

FlexGUI Installation and First-Time Setup

1. Download the latest version of the FlexGUI control software from www.cirrus.com/msasoftware. Follow the installation instructions on the download page.
2. Connect the CDB42L42 to the host PC using a mini USB cable.
3. Launch FlexGUI. Note: Once the GUI is launched successfully, all registers are set to their default reset states.

Note: To start evaluating the CS42L42 immediately with several standard configurations used at the factory, load the predefined register settings as described in Section 3.1.2.

3.1 Working with Register Settings

3.1.1 Modifying Register Settings Manually

After FlexGUI is up and running, there are two ways to modify register settings manually:

- Use the high-level interface, which features intuitive GUI elements such as sliders, check boxes, and drop-down menus. See Section 3.2 for details on using the high-level interface.
- Use the low-level register map, which displays the user-configurable register space for each device on the CDB42L42 in table form. Changes can be made on a per-bit or per-address basis. See Section 3.3 for details.

3.1.2 Quick Start Register Settings

The Quick Start tab contains Quick Setup scripts that allow fast and easy configuration of the CS42L42 as shown in Fig. 3-1. The Quick Setup scripts have configurations for standard I2S sample rates and SCLK frequencies. The Quick Start tab also contains the RESET button for the CS42L42.

Quick Setup scripts:

1. Put all devices into RESET (CS42L42, CS8422 S/PDIF Rx, and CS8406 S/PDIF Tx)
2. Release from RESET and configure the CS8422 S/PDIF receiver.
3. Release from RESET and configure the CS8406 S/PDIF transmitter.
4. Release from RESET and configure the CS42L42 codec.

Fig. 3-1 shows the Quick Setup options. The setting specify I²S format with a variety of LRCLK and SCLK frequencies.

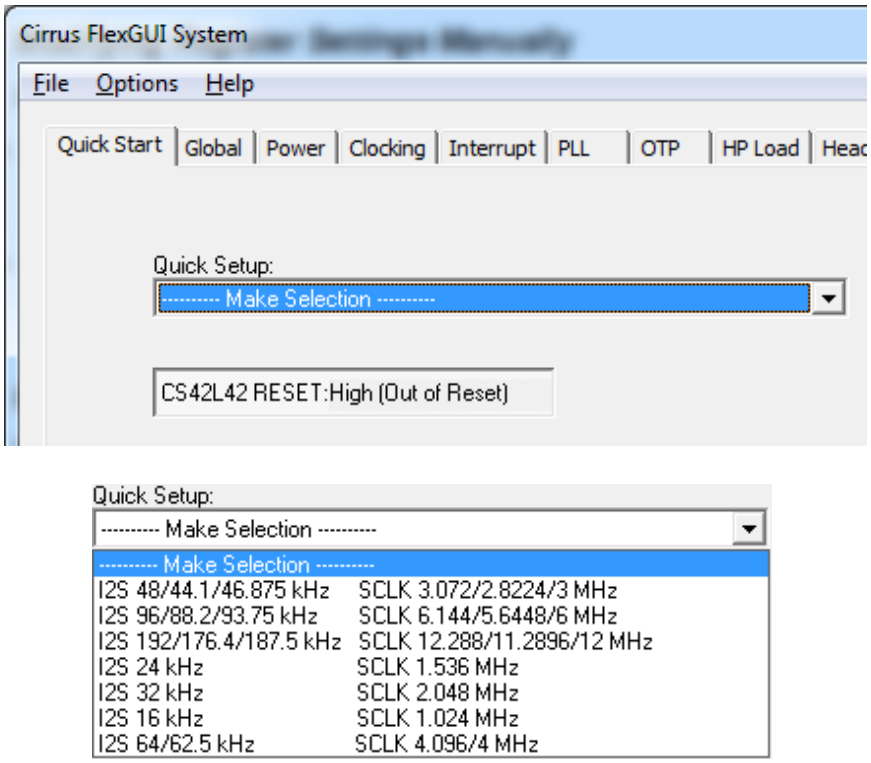


Figure 3-1. Quick Setup

3.2 Using the FlexGUI High-Level Interface Layout

The CS42L42 is versatile with many features and register settings. To keep the GUI easy to use and visually clean, the register controls for each page of the CS42L42 are grouped with each page number on a different tab.

To use the GUI controls for a given page (tab), first set the page register to the correct page number. Next it is recommended to update the GUI controls by pressing the Read Page button so that the GUI controls reflect the current state of the CS42L42 registers. Each GUI tab has a button for setting the page number, an indicator of the current page number, and a button to Read Page.

Fig. 3-2 shows the Global tab of the FlexGUI high-level interface layout.

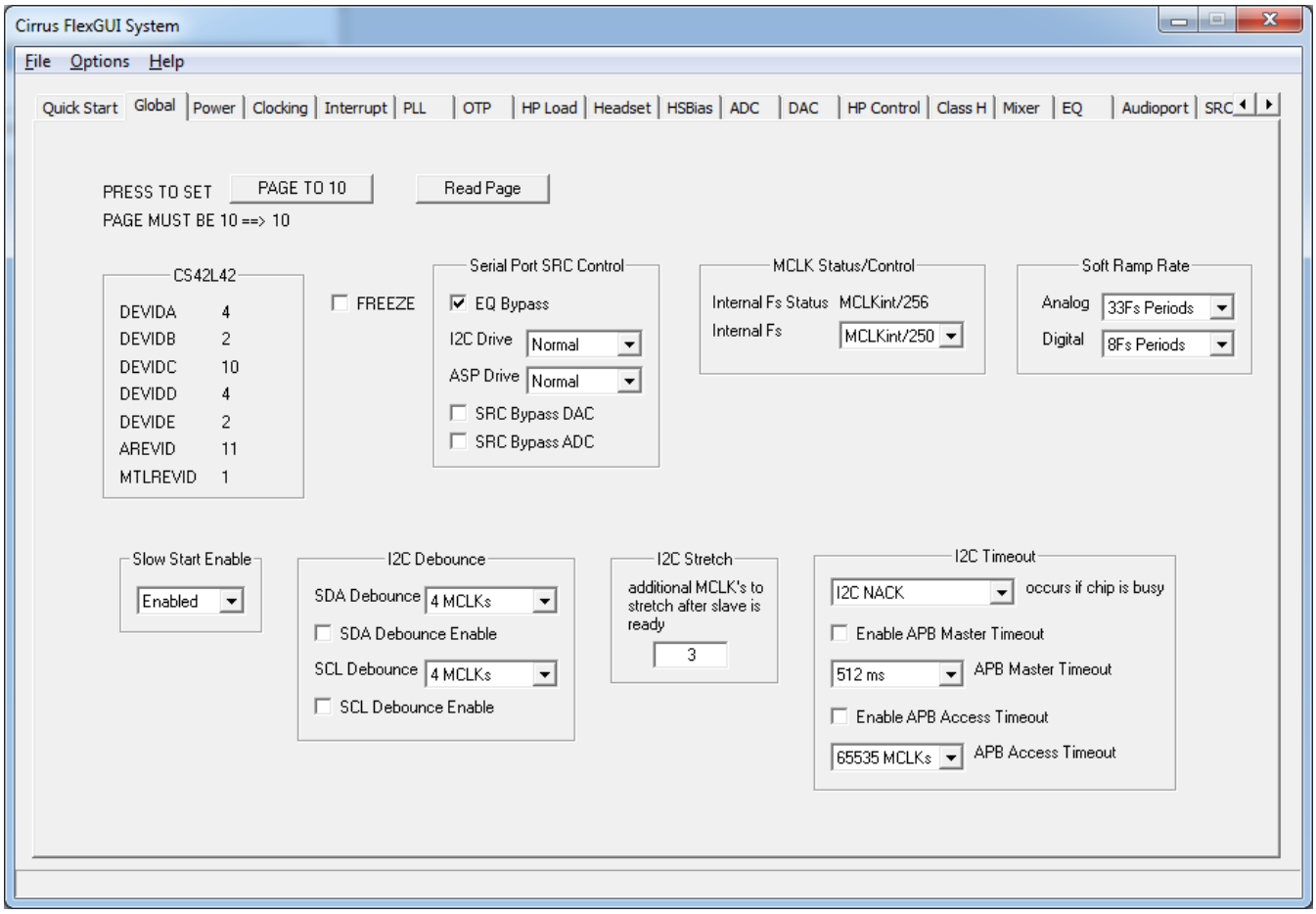


Figure 3-2. FlexGUI High-Level Interface

3.3 The Register Map

The register map shows the entire user-configurable register space for all programmable devices on the CDB42L42.

It is especially useful for reading/writing a device's register settings directly, one whole register at a time. To use the Register Map controls for the CS42L42, first set the page register to the correct page number. The page resister is register 0x00, this must match the page number of the current tab. It is then recommended to press the Update Device button so that the register map values reflect the current values in the CS42L42. Finally, click on the desired register cell, type the desired value, and press the return key (Enter) on the keyboard.

See Fig. 3-3. To change Register 0x01 on Page 0x20 from the default value of 0x0D (analog mute) to 0x01 (0 dB), first navigate to Register 0x00 by locating the cell at the intersection of row "00" and column "00". Click on the cell, type the page number "20", and press the return key (Enter) on the keyboard. Then press the Update Device button to update the register map on page 0x20 so that the values reflect the current values in the CS42L42. Finally locate the cell at the intersection of row "00" and column "01". Click on the cell, type "01", and press the return key (Enter) on the keyboard.

To modify one bit of a register at a time, navigate to the desired register cell, click it, then click on the applicable bits shown in the lower part of the register map page to toggle them.

Other useful controls:

- Reset All—Clicking this button asserts reset to all devices on the CDB42L42
- Update Register—Clicking this button refreshes the current selected register value
- Update Device—Clicking this button refreshes all register values of the device currently in view in the register map

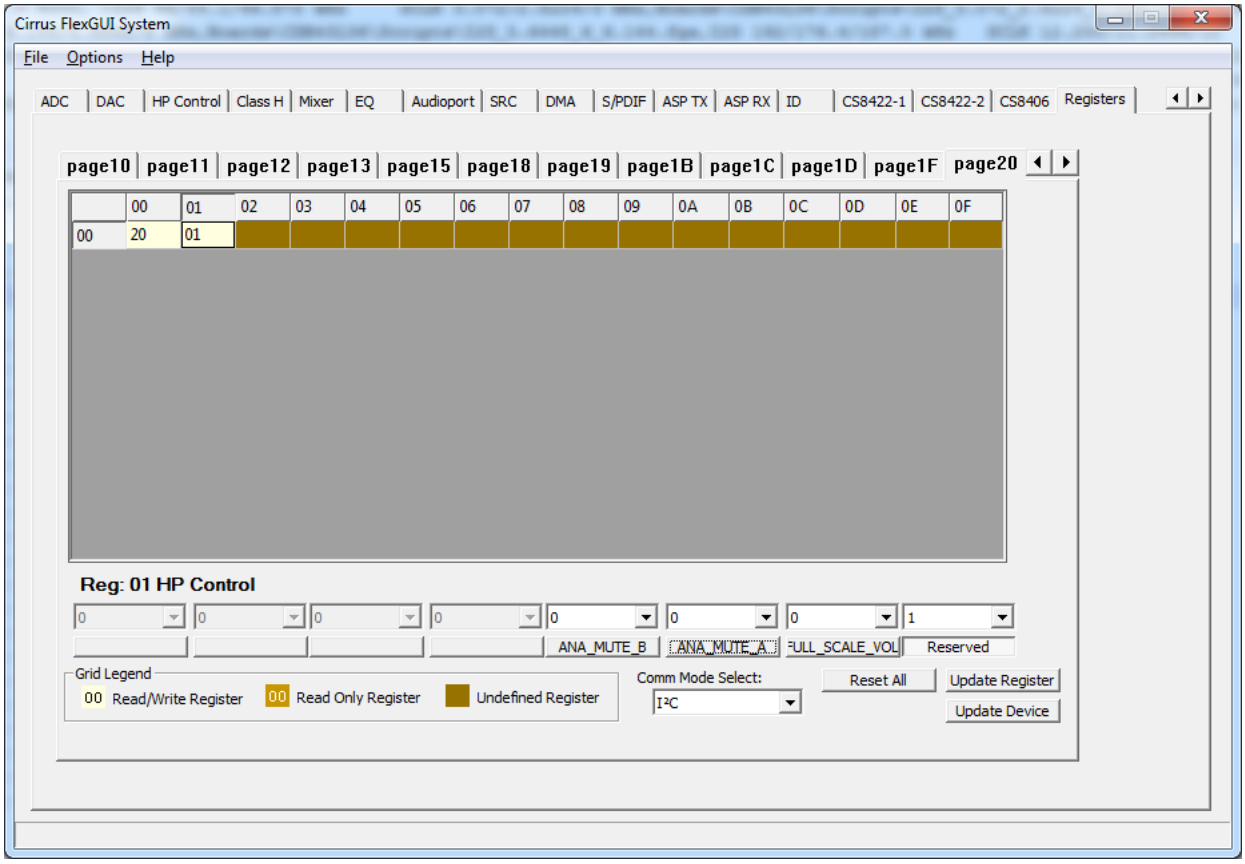


Figure 3-3. The "Register Maps" Tab in FlexGUI for the CDB42L42

4 System Connections and Jumper Settings

Table 4-1 lists the available jumpers and headers on the CDB42L42.

Table 4-1. Power and Signal I/O Connections

Reference Designator	Connection	Type	I/O	Description
J4	Board Power Select	Header 3x1	—	Board power select • Shunt pins 1–2 to select HDA 3.3 V • Shunt pins 2–3 to select 3.3-V regulator
J5/16	SCL/SDA	Header 2x1 (x2)	—	Shunt to use onboard I²C pull-up resistor. Leave open to use ET-FLEXLINK daughtercard I²C pull-up resistor.
J13/23	ET-FLEXLINK Headers	40-pin high-density headers	I/O	ET-FLEXLINK interface header
J10	SoundWire connector	Header 8x2	I/O	SoundWire connection
J2	5-V connection	Wall-wart jack	Input	5-V wall-wart DC power jack with a 5-A max rating (2.1 x 5.5-mm)
J6	SoundWire select	Jumper 3x1	—	SoundWire Select • Shunt pins 1–2 to select SoundWire Mode • Shunt pins 2–3 to select I²C/I²S mode
J8	CS42L42 audio header	Header 4x2	Output	CS42L42 visibility and external input/output header
J17/15	CS8409 ASP1/2 header	Header 5x2 (x2)	Output	CS8409 ASP1/2 visibility header
J18	GPIO header	Header 9x1	Output	GPIO visibility header
J3	CS42L42 audio source select	Header 4x3	—	CS42L42 audio source select • Shunt pins 1–2 (x4) to select CS8409 as source/destination • Shunt pins 2–3 (x4) to select ET-FLEXLINK S/PDIF RX/TX as source/destination • Remove all shunts to use J8 or J10 (SWIRE) as source/destination
J11	HD audio signal header	9x1	Output	HD audio visibility header
J7	HD audio connector	Header 8x2	Input	HD audio connection
J14	S/PDIF jack	Stereo 3.5-mm jack	I/O	S/PDIF jack
J26	USB audio module connector	Header 10x2	I/O	USB audio module header
J56	Headset jack	Stereo 3.5-mm jack	I/O	Stereo headset jack

Table 4-2 lists the available jumpers, headers, and I/O connectors on the ET-FLEXLINK.

Table 4-2. Power and Signal I/O Connections

Reference Designator	Connection	Type	I/O	Description
J3	Board Power Select	Header 2x2	—	Board power select • Shunt pins 1–3 to power ET-FLEXLINK from CDB42L42 +5Vin • Shunt pins 2–4 to power ET-FLEXLINK from USB J2 • Shunt both pins 1–3 and 2–4 to power both CDB42L42 and ET-FLEXLINK from USB J2. NOTE: CDB42L42 +5Vin must not be used in this mode.
J6	I/O voltage select header	Header 3x1	—	Not populated. Defaults to +1.8-V logic level. Remove R41, populated J6, and shunt pins 2–3 to select +3.3-V as I/O voltage level. NOTE: CDB42L42 supports only +1.8- and +1.2-V I/O voltage levels.
J1	UART	Header 3x2	I/O	UART header
P2	MCU C2 debug header	Header 5x2	I/O	Silicon Labs C2 interface for C8051F320 programming
JP3	I²C/SPI buses	Header 5x2	I/O	Logic level +3.3V I²C and SPI signals from C8051F320 MCU. Compatible with Total Phase Aardvark I²C/SPI Host Adapter and Beagle I²C/SPI Protocol Analyzer
TP1	+5V from/to CDB	Test Point 2x1	—	Not populated test point for +5V connection shared between CDB42L42 and ET-FLEXLINK.
J2	USB FLEXGUI	USB mini-B	I/O	Mini-B USB connection to C8051F320 MCU for FlexGUI.
SPDIF_TX	S/PDIF Transmitter	Optical	O	Optical S/PDIF output from CS8406
SPDIF_RX	S/PDIF Receiver	Optical	I	Optical S/PDIF input to CS8422

5 CDB42L42 Schematics and Layout

The CDB uses an eight-layer PCB that allows for optimal trace and power routing to the CS42L42 devices and surrounding circuitry. Local decoupling capacitors for the CDB42L42 are placed as close as possible to the device. The CDB42L42's double-sided component and ground fill is used extensively on the component layer to isolate critical nets when possible.

Contact your Cirrus Logic representative for the schematics, layout, and bill of materials, listed below:

- ET-FLEXLINK daughtercard used for USB communications and S/PDIF I/O to the CDB42L42:
- Schematic files:
  - CDB42L42_REV_C.pdf
  - CDB42L42_REV_C.sch
  - ET-FLEXLINK_Rev_A1.pdf
  - ET-FLEXLINK_Rev_A1.sch
- Layout files:
  - 240-01020-Z1.REV_C.LAYERS.pdf
  - CDB42L42_REV_C.pcb
  - 240-01177-Z1_REV_A_LAYERS.pdf
  - ET-FLEXLINK_Rev_A1.pcb

6 Revision History

Release	Changes
DB1 JAN ‘15	Initial release of Evaluation Board Rev. A
DB2 FEB ‘15	Revised board design to include the Quick-Start Guide, SoundWire, and HDA sections, and updated schematics.
DB3 MAY 17 ‘16	Replaced EE-CRUSLINK with ET-FLEXLINK interface card and removed ET-USB-AUDIO.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.