1.7 General Overview of STC15W1K16S series MCU

1.7.1 Introduction of STC15W1K16S series MCU (In abundant supply)

STC15W1K16S series MCU is a single-chip microcontroller based on a high performance 1T architecture 8051 CPU, which is produced by STC MCU Limited. It is a new generation of 8051 MCU of high speed, high stability, wide voltage range, low power consumption and super strong anti-disturbance. Besides, STC15W1K16S series MCU is a MCU of super advanced encryption, because it adopts the ninth generation of STC encryption technology. With the enhanced kernel, STC15W1K16S series MCU is faster than a traditional 8051 in executing instructions (about 8~12 times the rate of a traditional 8051 MCU), and has a fully compatible instruction set with traditional 8051 series microcontroller. External expensive crystal can be removed by being integrated internal high-precise R/C clock(±0.3%) with ±1% temperature drift (-40℃~+85℃) while ±0.6% in normal temperature (-20℃~+65℃) and wide frenquency adjustable between 5MHz and 35MHz. External reset curcuit also can be removed by being integrated internal highly reliable one with 16 levels optional threshold voltage of reset. The STC15W1K16S series MCU retains all features of the traditional 8051. In addition, it has three Timers/Counters, a power-down wake-up Timer, dual DPTR and a high-speed asynchronous serial port----UART(can be regarded as 3 serial ports by shifting among 3 groups of pins) and a high-speed synchronous serial peripheral interface----SPI. STC15W1K16S series MCU is usually used in serial communication or electrical control or some occasion with strong disturbance.

In Keil C development environment, select the Intel 8052 to compiling and only contain < reg51.h > as header file.

STC15 series MCU with super high-speed CPU core of STC-Y5 works 20% faster than STC early 1T series (such as STC12/STC11/STC10 series) at same clock frequency.

- Enhanced 8051 Central Processing Unit, 1T, single clock per machine cycle, faster 8~12 times than the rate of a traditional 8051.
- Operating voltage range: 5.5V ~ 2.5V
- On-chip 16K/24K/29/31.5K FLASH program memory with flexible ISP/IAP capability, can be repeatedly erased more than 100 thousand times.
- Large capacity of on-chip 1024 bytes SRAM: 256 byte scratch-pad RAM and 768 bytes of auxiliary RAM
- Be capable of addressing up to 64K byte of external RAM
- On-chip EEPROM with large capacity can be repeatedly erased more than 100 thousand times.
- Dual Data Pointer (DPTR) to speed up data movement
- ISP/IAP, In-System-Programming and In-Application-Programming , no need for programmer and emulator.
- Internal hghly reliable Reset with 8 levels optional threshold voltage of reset, external reset curcuit can be completely removed
- Internal high- precise R/C clock with ±1% temperature drift(-40℃~+85℃) while 5‰ in normal temperature and wide frenquency adjustable between 5MHz and 35MHz (5.5296MHz / 11.0592MHz / 22.1184MHz / 33.1776MHz).
- Internal high- precise R/C clock(±0.3%) with ±1% temperature drift (-40℃~+85℃) while ±0.6% (-20℃~+65℃) in normal temperature and wide frenquency adjustable between 5MHz and 35MHz (5.5296MHz / 11.0592MHz / 22.1184MHz / 33.1776MHz)
- No need external crystal and reset, and can output clock and low reset signal from MCU.

STC MCU Limited.

- Operating frequency range: 5- 35MHz, is equivalent to traditional 8051:60~420MHz.
- A high-speed asynchronous serial port----UART(can be used simultaneously and regarded as 3 serial ports by shifting among 3 groups of pins):
  UART1(RxD/P3.0, TxD/P3.1) can be switched to (RxD_2/P3.6, TxD_2/P3.7),
  also can be switched to (RxD_3/P1.6, TxD_3/P1.7).
- A high-speed synchronous serial peripheral interface----SPI.
- Support the function of Encryption Download (to protect your code from being intercepted).
- Support the function of RS485 Control
- Code protection for flash memory access, excellent noise immunity, very low power consumption
- Power management mode: Slow-Down mode, Idle mode(all interrupt can wake up Idle mode), Stop/Power-Down mode.
- Timers which can wake up stop/power-down mode: have internal low-power special wake-up Timer.
- Resource which can wake up stop/power-down mode are: INT0/P3.2, INT1/P3.3 (INT0/INT1, may be generated on both rising and falling edges), $\overline{\text{INT2}}$/P3.6, $\overline{\text{INT3}}$/P3.7, $\overline{\text{INT4}}$/P3.0 ($\overline{\text{INT2}}$/$\overline{\text{INT3}}$/$\overline{\text{INT4}}$, only be generated on falling edge); pins RxD; pins T0/T1/T2(their falling edge can wake up if T0/T1/T2 have been enabled before power-down mode, but no interrupts can be generatetd); internal low-power special wake-up Timer.
- threee 16-bit reloadable Timers/Counters(T0/T1/T2, T0 and T1 are compatible with Timer0/Timer1 of traditional 8051), T0/T1/T2 all can independently achieve external programmable clock output (3 channels).
- Programmable clock output function(output by dividing the frequency of the internal system clock or the input clock of external pin):
  The speed of external programmable clock output of 5V MCU is also not more than 13.5MHz, because the output speed of I/O port of STC15 series 5V MCU is not more than 13.5MHz.
  The speed of external programmable clock output of 3.3V MCU is also not more than 8MHz, because the output speed of I/O port of STC15 series 3.3V MCU is not more than 8MHz.
  ① The Programmable clock output of T0 is on P3.5/T0CLKO (output by dividing the frequency of the internal system clock or the input clock of external pin T0/P3.4)
  ② The Programmable clock output of T1 is on P3.4/T1CLKO (output by dividing the frequency of the internal system clock or the input clock of external pin T1/P3.5)
  ③ The Programmable clock output of T2 is on P3.0/T2CLKO (output by dividing the frequency of the internal system clock or the input clock of external pin T2/P3.1)
  Three timers/counters in above all can be output by dividing the frequency from 1 to 65536.
  ④ The Programmable clock output of master clock is on P5.4/MCLKO or P1.6/XTAL2/MCLKO_2, and its frequency can be divided into MCLK/1, MCLK/2, MCLK/4.
  The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.
  MCLK is the frequency of master clock. MCLKO is the output of master clock.
  It is on MCLKO/P3.4 that the Programmable clock output of master clock of STC15 series 8-pin MCU

STC MCU Limited.

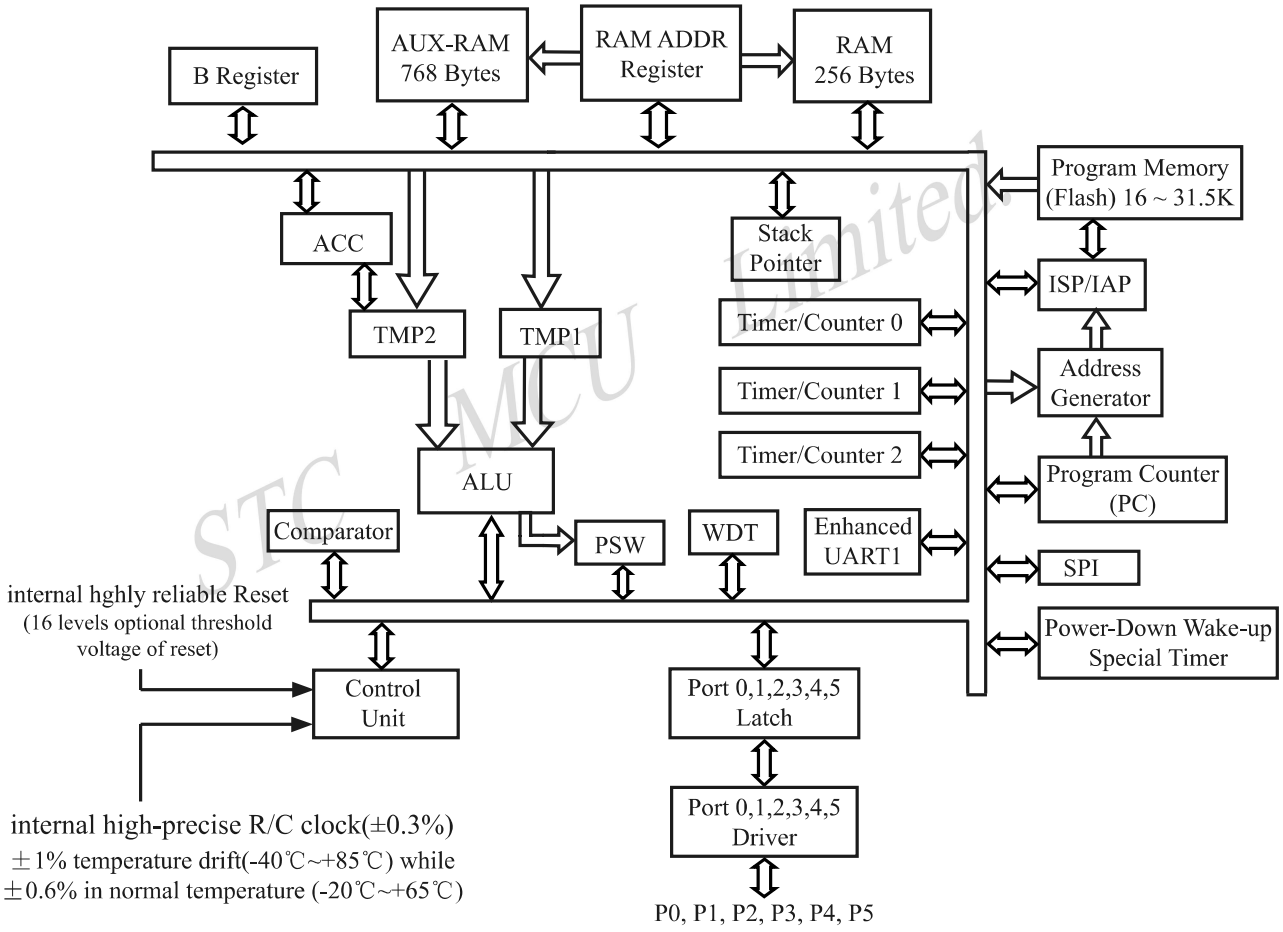
(such as STC15F101W series). However, it is on MCLKO/P5.4 that the Programmable clock output of master clock of other STC15 series MCU including 16-pin or more than 16-pin MCU(such as STC15F2K60S2, STC15W4K32S4 and so on)

- Comparator, which support comparing by external pin CMP+ and CMP- or internal reference voltage and generating output signal (its polarity can be configured) on CMPO pin can be used as 1 channel ADC or brownout detect function.
- One 15 bits Watch-Dog-Timer with 8-bit pre-scaler (one-time-enabled)
- advanced instruction set, which is fully compatible with traditional 8051 MCU, have hardware multiplication / division command.
- 42/38/30/26 common I/O ports are available, their mode is quasi_bidirectional/weak pull-up (traditional 8051 I/O ports mode) after reset, and can be set to four modes: quasi_bidirectional/weak pull-up, strong push-pull/ strong pull-up, input-only/high-impedance and open drain.
  the driving ability of each I/O port can be up to 20mA, but it don't exceed this maximum 120mA that the current of the whole chip of 40-pin or more than 40-pin MCU, while 90mA that the current of the whole chip of 16-pin or more than 16-pin MCU or 32-pin or less than 32-pin MCU.
  If I/O ports are not enough, it can be extended by connecting a 74HC595(reference price: RMB 0.15 yuan). Besides, cascading several chips also can extend to dozens of I/O ports.
- Package : LQFP44(12mm x 12mm), PDIP40, LQFP32(9mm x 9mm),QFN32(5mm x 5mm),SOP28, SKDIP28, TSSOP20 (6.5mm x6.5mm)
- All products are baked 8 hours in high-temperature 175℃ after be packaged, Manufacture guarantee good quality.
- In Keil C development environment, select the Intel 8052 to compiling and only contain < reg51.h > as header file.

STC MCU Limited.

1.7.2 Block diagram of STC15W1K16S series

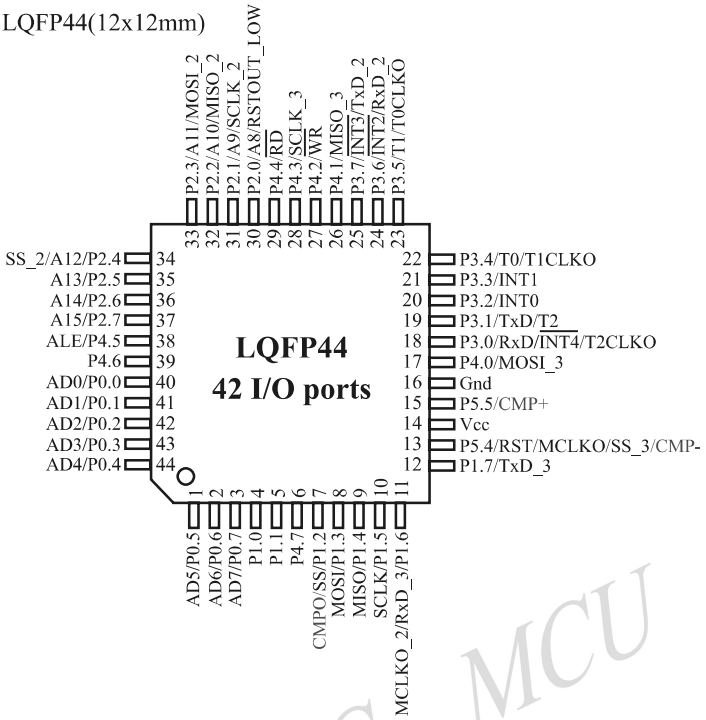
The internal structure of STC15W1K16S series MCU is shown in the block diagram below. STC15W1K16S series MCU includes central processor unit(CPU), program memory (Flash), data memory(SRAM), Timers/ Counters, power-down wake-up Timer, I/O ports, Comparator, Watchdog, high-speed asynchronous serial communication ports---UART, a group of high-speed synchronous serial peripheral interface (SPI), internal high-precise R/C clock, internal hghly reliable Reset and so on. STC15W1K16S series MCU almost includes all of the modules required in data acquisition and control, and can be regarded as an on-chip system (SysTem Chip or SysTem on Chip, abbreviated as STC, this is the name origin of Hongjing technology STC Limited).



STC15W1K16S series Block Diagram

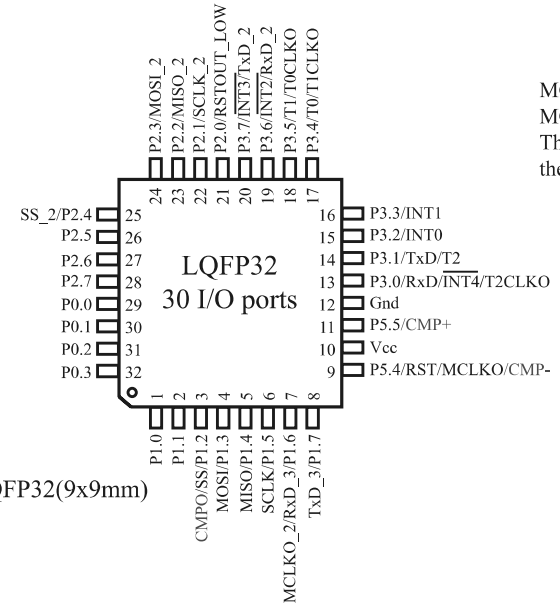
1.7.3 Pin Configurations of STC15W1K16S series MCU

LQFP44(12x12mm)



Note：P0 ports can be multiplexed as Address/Data bus，not as A/D Converter. P0.x/ADx means that P0.x can be used as Address/Data bus in the pin map.

Recommend UART1 on [P3.6/RxD_2, P3.7/TxD_2] or [P1.6/RxD_3/XTAL2, P1.7/TxD_3/XTAL1]



LQFP32(9x9mm)

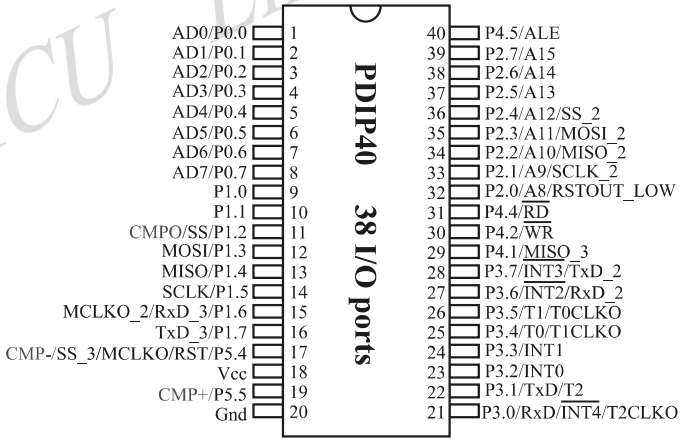
All packages meet EU RoHS standards

T0CLKO refers to the programmable clock output of Timer/Counter 0
(output by dividing the frequency of the internal system clock or the input clock of external pin T0/P3.4);

T1CLKO refers to the programmable clock output of Timer/Counter 1
(output by dividing the frequency of the internal system clock or the input clock of external pin T1/P3.5);

T2CLKO refers to the programmable clock output of Timer/Counter 2
(output by dividing the frequency of the internal system clock or the input clock of external pin T2/P3.1);

In addition to programmable output on the internal system clock, T0CLKO/T1CLKO/T2CLKO also can be used as divider by dividing the frequency of the internal system clock or the input clock of external pin T0/T1/T2.



MCLKO is the output of master clock whose frequency can be divided into MCLK/1, MCLK/2, MCLK/4
The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator. MCLK is the frequency of master clock.

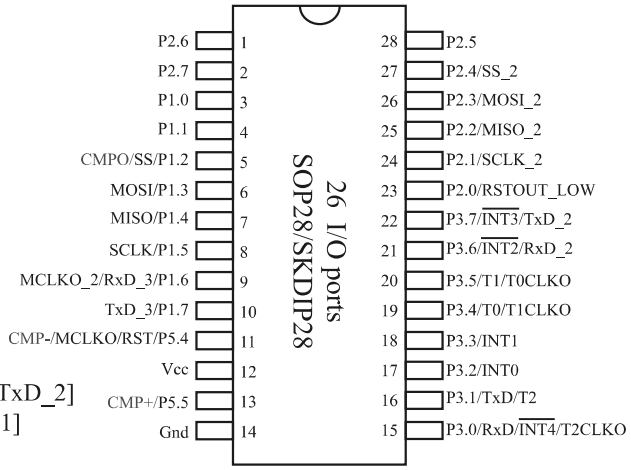
The speed of external programmable clock output of 5V MCU is also not more than 13.5MHz, because the output speed of I/O port of STC15 series 5V MCU is not more than 13.5MHz.

The speed of external programmable clock output of 3.3V MCU is also not more than 8MHz, because the output speed of I/O port of STC15 series 3.3V MCU is not more than 8MHz.

STC MCU Limited.

MCLKO is the output of master clock whose frequency can be divided into MCLK/1, MCLK/2, MCLK/4

The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator. MCLK is the frequency of master clock.



Recommend UART1 on [P3.6/RxD_2, P3.7/TxD_2] or [P1.6/RxD_3/XTAL2, P1.7/TxD_3/XTAL1]

The speed of external programmable clock output of 5V MCU is also not more than 13.5MHz, because the output speed of I/O port of STC15 series 5V MCU is not more than 13.5MHz.

The speed of external programmable clock output of 3.3V MCU is also not more than 8MHz, because the output speed of I/O port of STC15 series 3.3V MCU is not more than 8MHz.

T0CLKO refers to the programmable clock output of Timer/Counter 0
(output by dividing the frequency of the internal system clock or the input clock of external pin T0/P3.4);

T1CLKO refers to the programmable clock output of Timer/Counter 1
(output by dividing the frequency of the internal system clock or the input clock of external pin T1/P3.5);

T2CLKO refers to the programmable clock output of Timer/Counter 2
(output by dividing the frequency of the internal system clock or the input clock of external pin T2/P3.1);

In addition to programmable output on the internal system clock, T0CLKO/T1CLKO/T2CLKO also can be used as divider by dividing the frequency of the internal system clock or the input clock of external pin T0/T1/T2.

STC MCU Limited.

Mnemonic	Add	Name	7	6	5	4	3	2	1	0	Reset Value
AUXR1 P_SW1	A2H	Auxiliary register 1	S1_S1	S1_S0	CCP_S1	CCP_S0	SPI_S1	SPI_S0	0	DPS	00xx,0000
CLK_DIV (PCON2)	97H	Clock Division register	MCKO_S1	MCKO_S0	ADRJ	Tx_Rx	MCLKO_2	CLKS2	CLKS1	CLKS0	0000,0000

UART1/S1 can be switched in 3 groups of pins by selecting the control bits S1_S0 and S1_S1.		
S1_S1	S1_S0	UART1/S1 can be switched between P1 and P3
0	0	UART1/S1 on [P3.0/RxD,P3.1/TxD]
0	1	UART1/S1 on [P3.6/RxD_2,P3.7/TxD_2]
1	0	UART1/S1 on [P1.6/RxD_3/XTAL2,P1.7/TxD_3/XTAL1] when UART1 is on P1, please using internal R/C clock.
1	1	Invalid

Recommed UART1 on [P3.6/RxD_2,P3.7/TxD_2] or [P1.6/RxD_3/XTAL2,P1.7/TxD_3/XTAL1].

Mnemonic	Add	Name	7	6	5	4	3	2	1	0	Reset Value
AUXR1 P_SW1	A2H	Auxiliary register 1	S1_S1	S1_S0	CCP_S1	CCP_S0	SPI_S1	SPI_S0	0	DPS	00xx,0000
CLK_DIV (PCON2)	97H	Clock Division register	MCKO_S1	MCKO_S0	ADRJ	Tx_Rx	MCLKO_2	CLKS2	CLKS1	CLKS0	0000,0000

SPI can be switched in 3 groups of pins by selecting the control bits SPI_S1 and SPI_S0		
SPI_S1	SPI_S0	SPI can be switched in P1, P2 and P4
0	0	SPI on [P1.2/SS, P1.3/MOSI, P1.4/MISO, P1.5/SCLK]
0	1	SPI on [P2.4/SS_2, P2.3/MOSI_2, P2.2/MISO_2, P2.1/SCLK_2]
1	0	SPI on [P5.4/SS_3, P4.0/MOSI_3, P4.1/MISO_3, P4.3/SCLK_3]
1	1	Invalid

DPS：DPTR registers select bit.

0: DPTR0 is selected

1: DPTR1 is selected

MCKO_S1	MCKO_S0	the control bit of master clock output by dividing the frequency (The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator)
0	0	Master clock do not output external clock
0	1	Master clock output external clock，but its frequency do not be divided，and the output clock frequency = MCLK / 1
1	0	Master clock output external clock，but its frequency is divided by 2，and the output clock frequency = MCLK / 2
1	1	Master clock output external clock，but its frequency is divided by 4，and the output clock frequency = MCLK / 4

The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.

MCLK is the frequency of master clock.

STC15W1K16S series MCU output master clock on MCLKO/P5.4

It is on MCLKO/P3.4 that the Programmable clock output of master clock of STC15 series 8-pin MCU (such as STC15F101W series). However, it is on MCLKO/P5.4 that the Programmable clock output of master clock of other STC15 series MCU including 16-pin or more than 16-pin MCU.

MCLKO_2：to select Master Clock output on where

0：Master Clock output on MCLKO/P5.4

1：Master Clock output on MCLKO_2/XTAL2/P1.6

The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.

Tx_Rx：the set bit of relay and broadcast mode of UART1

0：UART1 works on normal mode

1：UART1 works on relay and broadcast mode，that to say output the input level state of RxD port to the outside TxD pin in real time, namely the external output of TxD pin can reflect the input level state of RxD port.

the RxD and TxD of UART1 can be switched in 3 groups of pins: [RxD/P3.0, TxD/P3.1];
[RxD_2/P3.6, TxD_2/P3.7];
[RxD_3/P1.6, TxD_3/P1.7].

STC MCU Limited.

Mnemonic	Add	Name	7	6	5	4	3	2	1	0	Reset Value
CLK_DIV (PCON2)	97H	Clock Division register	MCKO_S1	MCKO_S0	ADRJ	Tx_Rx	MCLKO_2	CLKS2	CLKS1	CLKS0	0000,0000

CLKS2	CLKS1	CLKS0	the control bit of system clock (System clock refers to the master clock that has been divided frequency, which is offered to CPU, UARTs, SPI, Timers, CCP/PWM/PCA and A/D Converter)
0	0	0	Master clock frequency/1, No division
0	0	1	Master clock frequency/2
0	1	0	Master clock frequency/4
0	1	1	Master clock frequency/8
1	0	0	Master clock frequency/16
1	0	1	Master clock frequency/32
1	1	0	Master clock frequency/64
1	1	1	Master clock frequency/128

The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.

STC MCU Limited.

1.7.4 STC15W1K16S series Selection and Price Table

Type 1T 8051 MCU	Operating Voltage (V)	Flash (byte)	SRAM (byte)	UART	SPI	common Timers T0-T2	CCP PCA PWM	Speical Power-down Wake-up Timer	Standard External Interrupts	A/D 8-channel	COMPARATOR	DPTR	EEP ROM	Internal Low-Voltage Detection Interrupt	WDT	Internal High-reliable Reset (with optional threshold voltage)	Internal High-Precise Clock	Output clock and reset signal from MCU	Encryption Download (to protect your code from being intercepted)	RS485 Control	All Packages LQFP44/ PDIP40 LQFP32/ QFN32 SOP28/ SKDIP28 Price of a part of packages(RMB ¥)	
																					LQFP44	SOP28
STC15W1K16S series MCU Selection and Price Table																						
STC15W1K16S	5.5-2.6	16K	1K	1	Y	3	N	Y	5	N	Y	2	13K	Y	Y	16-level	Y	Y	Y	Y	¥3.5	¥3.3
STC15W1K24S	5.5-2.6	24K	1K	1	Y	3	N	Y	5	N	Y	2	5K	Y	Y	16-level	Y	Y	Y	Y	¥3.8	¥3.6
IAP15W1K29S	5.5-2.6	29K	1K	1	Y	3	N	Y	5	N	Y	2	IAP	Y	Y	16-level	Y	Y	Y	Y	¥3.8 The program Flash in user program area can be used as EEPROM.	¥3.6
IRC15W1K16S (Fixed internal 24MHz clock)	5.5-2.6	31.5K	1K	1	Y	3	N	Y	5	N	Y	2	IAP	Y	Y	Fixed	Y	Y	N	N	¥3.8 The program Flash in user program area can be used as EEPROM.	¥3.6

Encryption Download : please burn source code with encryption key onto MCU in the factory. Then, you can make a simple update software just with one "update" button by fisrtly using the fuction "encrytion download" and then "release project" to update yourself code unabled to be intercepted when you need to upgrade your code.

To provide customized IC services

Because the last 7 bytes of the program area is stored mandatorily the contents of only global ID, the program space the user can actually use is 7 bytes smaller than the space shown in the selection table.

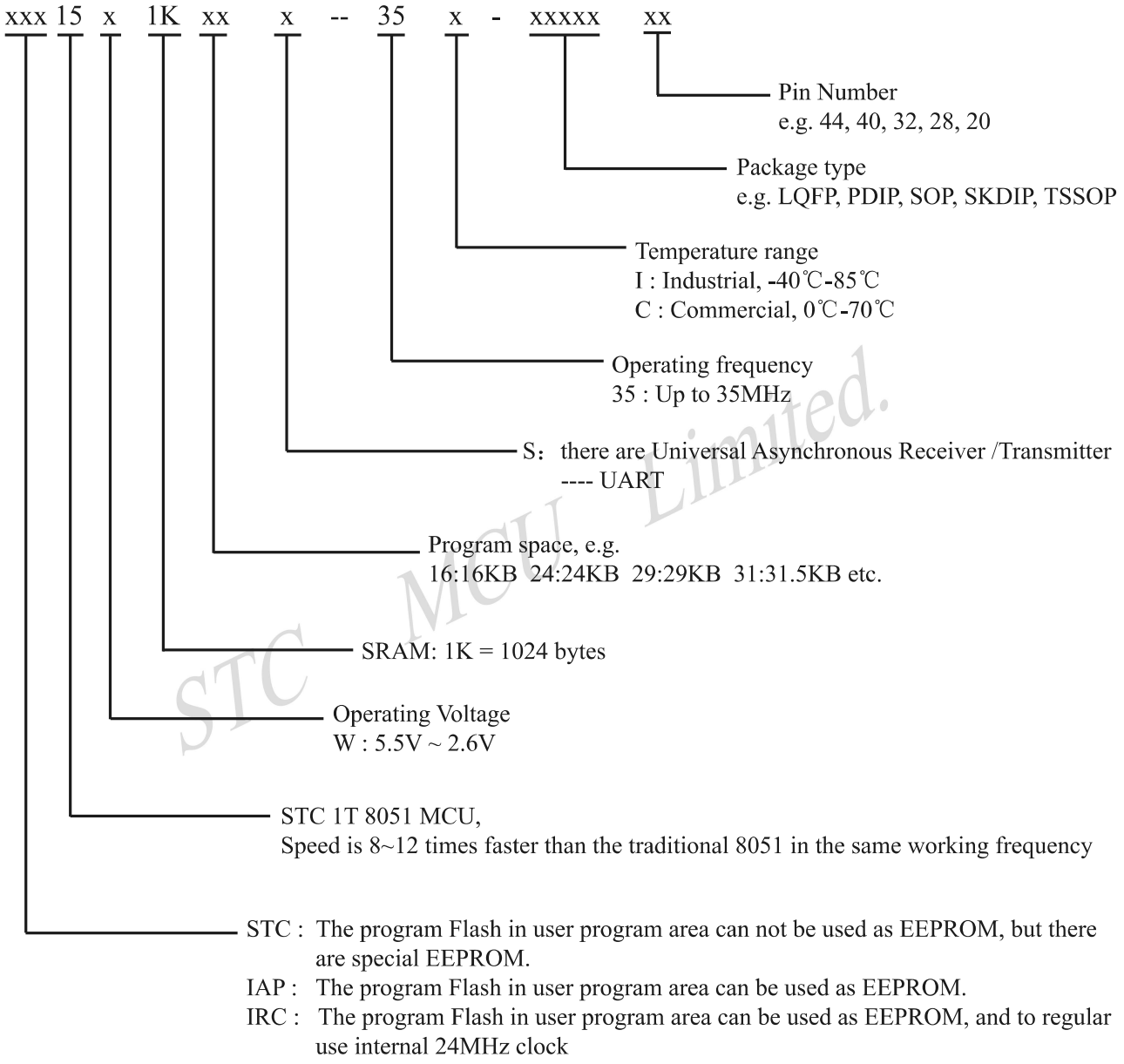
Conclusion : STC15W1K16S series MCU have: Three 16-bit relaodable Timers/Counters that are Timer/Counter 0, Timer/Counter 1 and Timer/Counter 2; 5 external interrupts INT0/INT1/$\overline{\text{INT2}}$/$\overline{\text{INT3}}$/$\overline{\text{INT4}}$; 1 high-speed asynchronous serial port ---- UART; a high-speed synchronous serial peripheral interface ---- SPI; 1 Comparator; 2 data pointers ---- DPTR; external data bus and so on.

STC MCU Limited.

1.7.5 STC15W1K16S series Package and Price Table

Type 1T 8051 MCU	Operating Voltage (V)	Operating Frequency (MHz)	Operating Temprature (I — Industrial)	All Packages Price(RMB ¥) LQFP44 / PDIP40 / LQFP32 / QFN32/SOP28 / SKDIP28 / TSSOP20						
				LQFP44	PDIP40	LQFP32	QFN32	SOP28	SKDIP28	TSSOP20
STC15W1K16S series MCU Package and Price Table										
STC15W1K16S	5.5-2.6	35	-40℃ ~ +85℃	¥3.5	¥4.0	¥3.4		¥3.3	¥3.5	
STC15W1K24S	5.5-2.6	35	-40℃ ~ +85℃	¥3.8	¥4.3	¥3.7		¥3.6	¥3.8	¥3.6
IAP15W1K29S	5.5-2.6	35	-40℃ ~ +85℃	¥3.8	¥4.3	¥3.7	¥3.65	¥3.6	¥3.8	¥3.6
IRC15W1K31S	5.5-2.6	35	-40℃ ~ +85℃	¥3.8	¥4.3	¥3.7		¥3.6	¥3.8	

1.7.6 Naming rules of STC15W1K16S series MCU



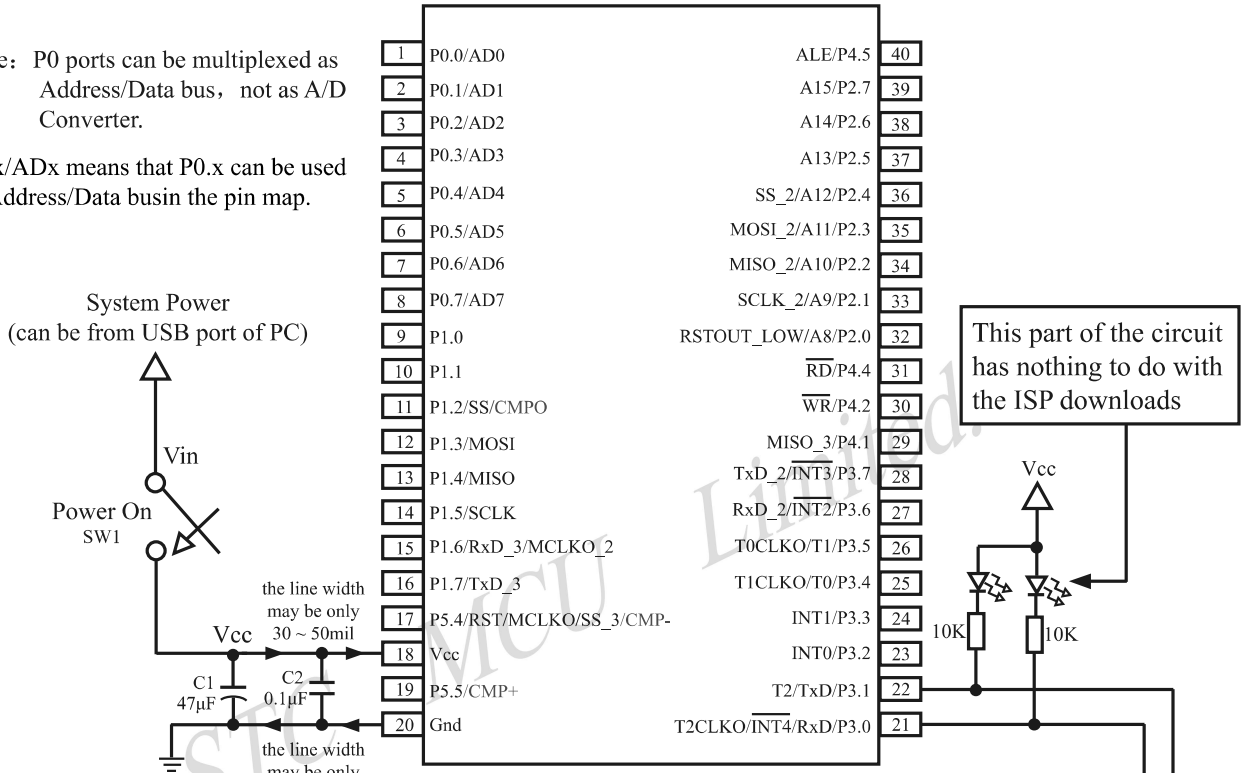
STC MCU Limited.

1.7.7 Application Circuit Diagram for ISP of STC15W1K16S series MCU

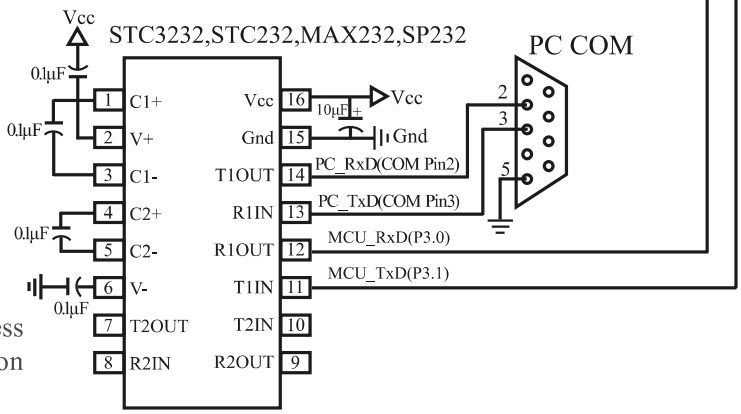
1.7.7.1 Application Circuit Diagram for ISP using RS-232 Converter

Note：P0 ports can be multiplexed as Address/Data bus，not as A/D Converter.

P0.x/ADx means that P0.x can be used as Address/Data busin the pin map.



Circuit diagram for ISP of *STC MCU*, *STC* RS-232 Converter



Please power on the target MCU after press down the button "Download/Program" on STC-ISP.exe when burning code to MCU.

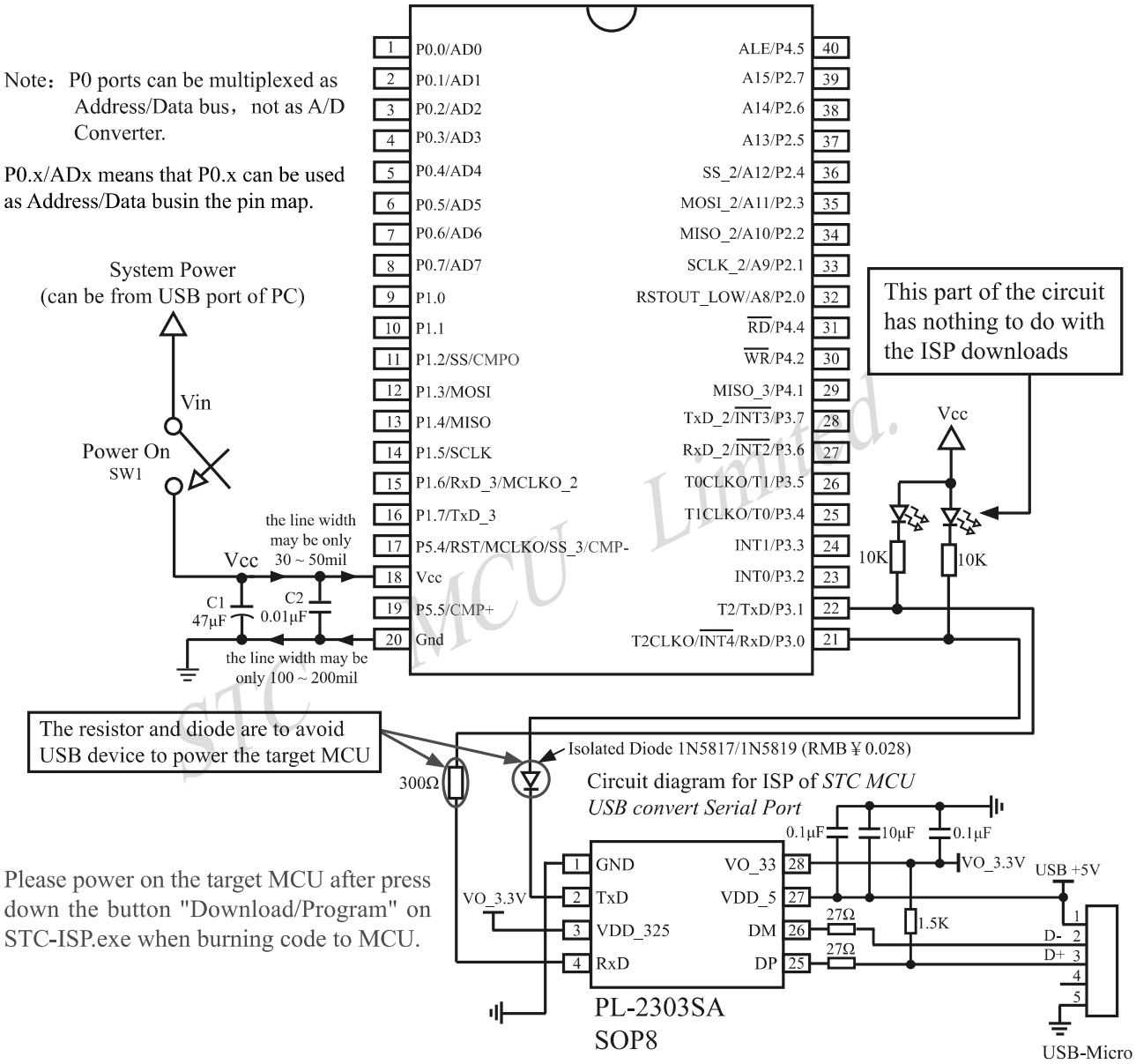
Internal hghly reliable Reset, External reset circuit can be completely removed.

P5.4/RST/MCLKO pin factory defaults to the I/O port, which can be set as RST reset pin(active high) through the STC-ISP programmer.

Internal high-precise R/C clock(±3%), ±1% temperature drift (-40℃~+85℃) while ±0.6% in normal temperature (-20℃~+65℃). External expensive crysal can be completely removed.

Recommend to add decoupling capacitor C1(47μF) and C2(0.1μF) between Vcc and Gnd that can remove power noise and improve the anti-interference ability.

1.7.7.2 Application Circuit Diagram for ISP using USB Chip PL-2303SA to convert Serial Port



Please power on the target MCU after press down the button "Download/Program" on STC-ISP.exe when burning code to MCU.

Internal hghly reliable Reset, External reset circuit can be completely removed.

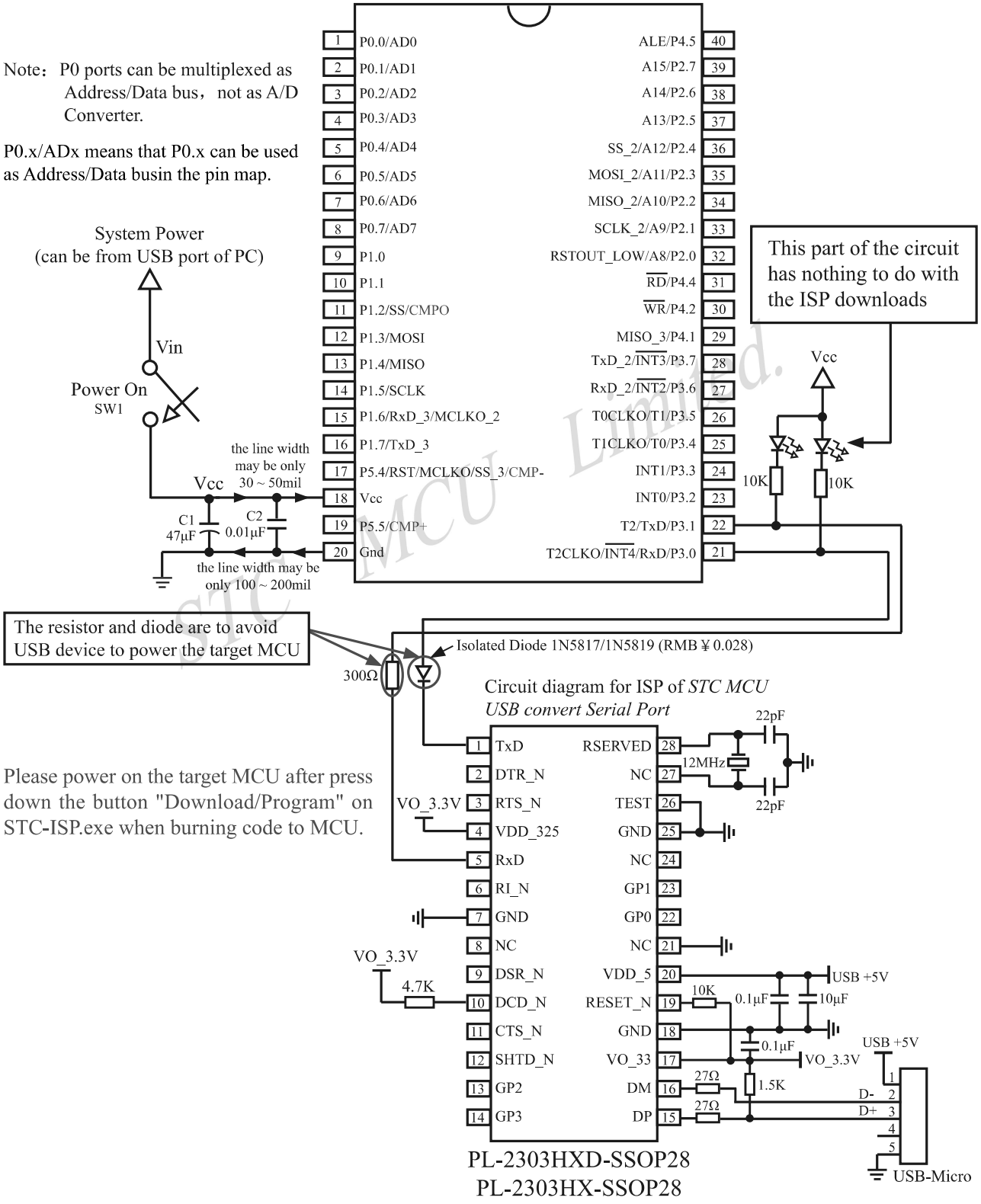
P5.4/RST/MCLKO pin factory defaults to the I/O port, which can be set as RST reset pin(active high) through the STC-ISP programmer.

Internal high-precise R/C clock(±3%), ±1% temperature drift (-40℃~+85℃) while ±0.6% in normal temperature (-20℃~+65℃). External expensive crysal can be completely removed.

Recommend to add decoupling capacitor C1(47μF) and C2(0.1μF) between Vcc and Gnd that can remove power noise and improve the anti-interference ability.

STC MCU Limited.

1.7.7.3 Application Circuit Diagram for ISP using USB Chip PL-2303HXD / PL-2303HX to convert Serial Port



STC MCU Limited.

1.7.8 Pin Descriptions of STC15W1K16S series MCU

MNEMONIC	Pin Number							DESCRIPTION	
	LQFP44	PLCC44	PDIP40	SOP32	LQFP32	SOP28 SKDIP28	TSSOP20		
P0.0/AD0	40	2	1	1	29	-	-	P0.0	common I/O port PORT0[0]
P0.1/AD1	41	3	2	2	30	-	-	P0.1	common I/O port PORT0[1]
P0.2/AD2	42	4	3	3	31	-	-	P0.2	common I/O port PORT0[2]
P0.3/AD3	43	5	4	4	32	-	-	P0.3	common I/O port PORT0[3]
P0.4/AD4	44	6	5	-	-	-	-	P0.4	common I/O port PORT0[4]
P0.5/AD5	1	7	6	-	-	-	-	P0.5	common I/O port PORT0[5]
P0.6/AD5	2	8	7	-	-	-	-	P0.6	common I/O port PORT0[6]
P0.7/AD7	3	9	8	-	-	-	-	P0.7	common I/O port PORT0[7]
P1.0	4	10	9	5	1	3	1	common I/O port PORT1[0]	
P1.1	5	11	10	6	2	4	2	common I/O port PORT1[1]	
P1.2/SS/ CMPO	7	13	11	7	3	5	20	P1.2	common I/O port PORT1[2]
								SS	Slave selection signal of synchronous serial peripheral interface----SPI
								CMPO	The output port of reslut compared by comparator
P1.3/MOSI	8	14	12	8	4	6	19	P1.3	common I/O port PORT1[3]
								MOSI	Master Output Slave Input of SPI
P1.4/MISO	9	15	13	9	5	7	3	P1.4	common I/O port PORT1[4]
								MISO	Master Iutput Slave Onput of SPI
P1.5/SCLK	10	16	14	10	6	8	4	P1.5	common I/O port PORT1[5]
								SCLK	Clock Signal of synchronous serial peripheral interface----SPI
P1.6/RxD_3/ MCLKO_2	11	17	15	11	7	9	5	P1.6	common I/O port PORT1[6]
								RxD_3	Receive Data Port of UART1
								MCLKO_2	Output from the inverting amplifier of internal clock circuit. This pin should be floated when an external oscillator is used.
P1.7/TxD_3	12	18	16	12	8	10	6	P1.7	common I/O port PORT1[7]
								TxD_3	Transit Data Port of UART1
P2.0/ RSTOUT_LOW	30	36	32	25	21	23	-	P2.0	common I/O port PORT2[0]
								RSTOUT_LOW	the pin output low after power-on and during reset, which can be set to output high by software
P2.1/SCLK_2	31	37	33	26	22	24	-	P2.1	common I/O port PORT2[1]
								SCLK_2	Clock Signal of synchronous serial peripheral interface----SPI

STC MCU Limited.

MNEMONIC	Pin Number							DESCRIPTION	
	LQFP44	PLCC44	PDIP40	SOP32	LQFP32	SOP28 SKDIP28	TSSOP20		
P2.2/MISO_2	32	38	34	27	23	25	-	P2.2	common I/O port PORT2[2]
								MISO_2	Master Iutput Slave Onput of SPI
P2.3/MOSI_2	33	39	35	28	24	26	-	P2.3	common I/O port PORT2[3]
								MOSI_2	Master Output Slave Input of SPI
P2.4/SS_2	34	40	36	29	25	27	-	P2.4	common I/O port PORT2[4]
								SS_2	Slave selection signal of synchronous serial peripheral interface----SPI
P2.5	35	41	37	30	26	28	-	common I/O port PORT2[5]	
P2.6	36	42	38	31	27	1	-	common I/O port PORT2[6]	
P2.7	37	43	39	32	28	2	-	common I/O port PORT2[7]	
P3.0/RxD/ $\overline{\text{INT4}}$ /T2CLKO	18	24	21	17	13	15	11	P3.0	common I/O port PORT3[0]
								RxD	Receive Data Port of UART1
								$\overline{\text{INT4}}$	External interrupt 4, which only can be generated on falling edge. /INT4 supports power-down waking-up
								T2CLKO	T2 Clock Output The pin can be configured for T2CLKO by setting INT_CLKO[2] bit /T2CLKO
P3.1/TxD/T2	19	25	22	18	14	16	12	P3.1	common I/O port PORT3[1]
								TxD	Transit Data Port of UART1
								T2	External input of Timer/Counter 2
P3.2/INT0	20	26	23	19	15	17	13	P3.2	common I/O port PORT3[2]
								INT0	External interrupt 0, which both can be generated on rising and falling edge. INT0 only can generate interrupt on falling edge if IT0 (TCON.0) is set to 1. And, INT0 both can generate interrupt on rising and falling edge if IT0 (TCON.0) is set to 0.
P3.3/INT1	21	27	24	20	16	18	14	P3.3	common I/O port PORT3[3]
								INT1	External interrupt 1, which both can be generated on rising and falling edge. INT1 only can generate interrupt on falling edge if IT1 (TCON.2) is set to 1. And, INT1 both can generate interrupt on rising and falling edge if IT1 (TCON.2) is set to 0. INT1 supports power-down waking-up
P3.4/T0/ T1CLKO	22	28	25	21	17	19	15	P3.4	common I/O port PORT3[4]
								T0	External input of Timer/Counter 0
								T1CLKO	T1 Clock Output The pin can be configured for T1CLKO by setting INT_CLKO[1] bit /T1CLKO

STC MCU Limited

MNEMONIC	Pin Number							DESCRIPTION	
	LQFP44	PLCC44	PDIP40	SOP32	LQFP32	SOP28 SKDIP28	TSSOP20		
P3.5/T1/ T0CLKO	23	29	26	22	18	20	16	P3.5	common I/O port PORT3[5]
								T1	External input of Timer/Counter 1
								T0CLKO	T0 Clock Output The pin can be configured for T0CLKO by setting INT_CLKO[0] bit /T0CLKO
P3.6/$\overline{\text{INT2}}$ /RxD_2	24	30	27	23	19	21	17	P3.6	common I/O port PORT3[6]
								$\overline{\text{INT2}}$	External interrupt 2, which only can be generated on falling edge. /INT2 supports power-down waking-up
								RxD_2	Receive Data Port of UART1
P3.7/$\overline{\text{INT3}}$ /TxD_2	25	31	28	24	20	22	18	P3.7	common I/O port PORT3[7]
								$\overline{\text{INT3}}$	External interrupt 3, which only can be generated on falling edge. /INT3 supports power-down waking-up
								TxD_2	Transit Data Port of UART1
P4.0	17	23	-	-	-	-	-	common I/O port PORT4[0]	
P4.1	26	32	29	-	-	-	-	common I/O port PORT4[1]	
P4.2/$\overline{\text{WR}}$	27	33	30	-	-	-	-	P4.2	common I/O port PORT4[2]
								$\overline{\text{WR}}$	Write pulse of external data memory
P4.3	28	34	-	-	-	-	-	common I/O port PORT4[3]	
P4.4/$\overline{\text{RD}}$	29	35	31	-	-	-	-	P4.4	common I/O port PORT4[4]
								$\overline{\text{RD}}$	Read pulse of external data memory
P4.5/ALE	38	44	40	-	-	-	-	P4.5	common I/O port PORT4[5]
								ALE	Address Latch Enable. It is used for external data memory cycles (MOVX)
P4.6	39	1	-	-	-	-	-	common I/O port PORT4[6]	
P4.7	6	12	-	-	-	-	-	common I/O port PORT4[7]	
P5.4/RST/ MCLKO/ CMP-	13	19	17	13	9	11	7	P5.4	common I/O port PORT5[4]
								RST	Reset pin. A high on this pin for at least two machine cycles will reset the device.
								MCLKO	Master clock output; the output frequency can be MCLK/1, MCLK/2 and MCLK/4. The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.
								CMP-	Comparator negative input
P5.5/CMP+	15	21	19	15	11	13	9	P5.5	common I/O port PORT5[5]
								CMP+	Comparator positive input
Vcc	14	20	18	14	10	12	8	The positive pole of power	
Gnd	16	22	20	16	12	14	10	The negative pole of power, Gound	

STC MCU Limited