Second-Stage Primary-Side Regulation Dimmable LED Driver Controller

General Description

The RT7331S is a second-stage dimmable constant current LED driver. It drives the converter in the Quasi-Resonant (QR) mode to achieve the higher efficiency. By using Primary Side Regulation (PSR), the RT7331S controls the output current accurately without a shunt regulator and an opto-coupler at the secondary side, reducing the external component count, the cost, and the volume of the driver board.

The RT7331S is compatible with the analog dimming. The output current can be modulated by the PWM duty ratio or the average level of DIM pin.

The RT7331S embeds comprehensive protection functions for robust designs, including LED open-circuit protection, LED short-circuit protection, output diode short-circuit protection, VDD Under-Voltage Lockout (UVLO), VDD Over-Voltage Protection (VDD OVP), over load protection, input Under-Voltage protection, internal Over-Temperature Protection (OTP), and cycle-by-cycle current limitation.

Features

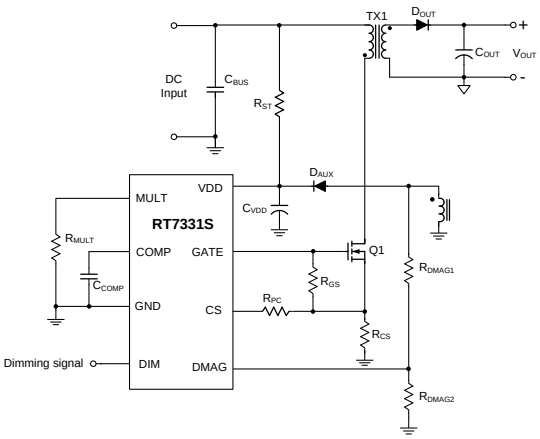
- **Tight LED Current Regulation**
- **Smart CC/CV Mode Control**
- **Wide Dimming Range (1% to 100%)**
- **Quasi-Resonant (QR) Operation**
- **Fast Startup**
- **Adjustable CV Level**
- **Soft Drive for the Better EMI Performance (Source 400mA/ Sink 500mA)**
- **Multiple Protection Features**
  - **LED Open-Circuit Protection**
  - **LED Short-Circuit Protection**
  - **Over Load Protection**
  - **Input Under-Voltage Protection**
  - **Output Diode Short-Circuit Protection**
  - **VDD Under-Voltage Lockout**
  - **VDD Over-Voltage Protection**
  - **Internal OTP**
  - **Cycle-by-Cycle Current Limitation**

Applications

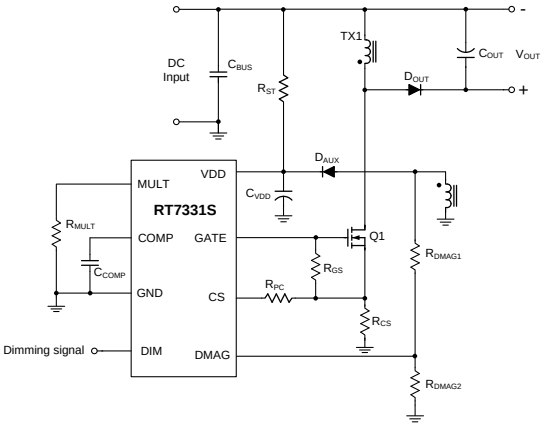
- DC-DC LED Lighting Driver

Simplified Application Circuit

Flyback Application Circuit



Buck-Boost Application Circuit



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Ordering Information

RT7331S □□

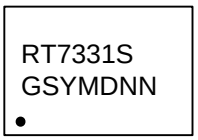
- Package Type
  S : SOP-8
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

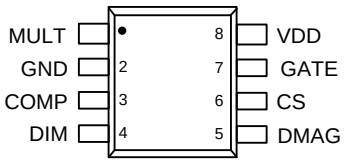
Marking Information



RT7331SGS : Product Number
YMDNN : Date Code

Pin Configuration

(TOP VIEW)



SOP-8

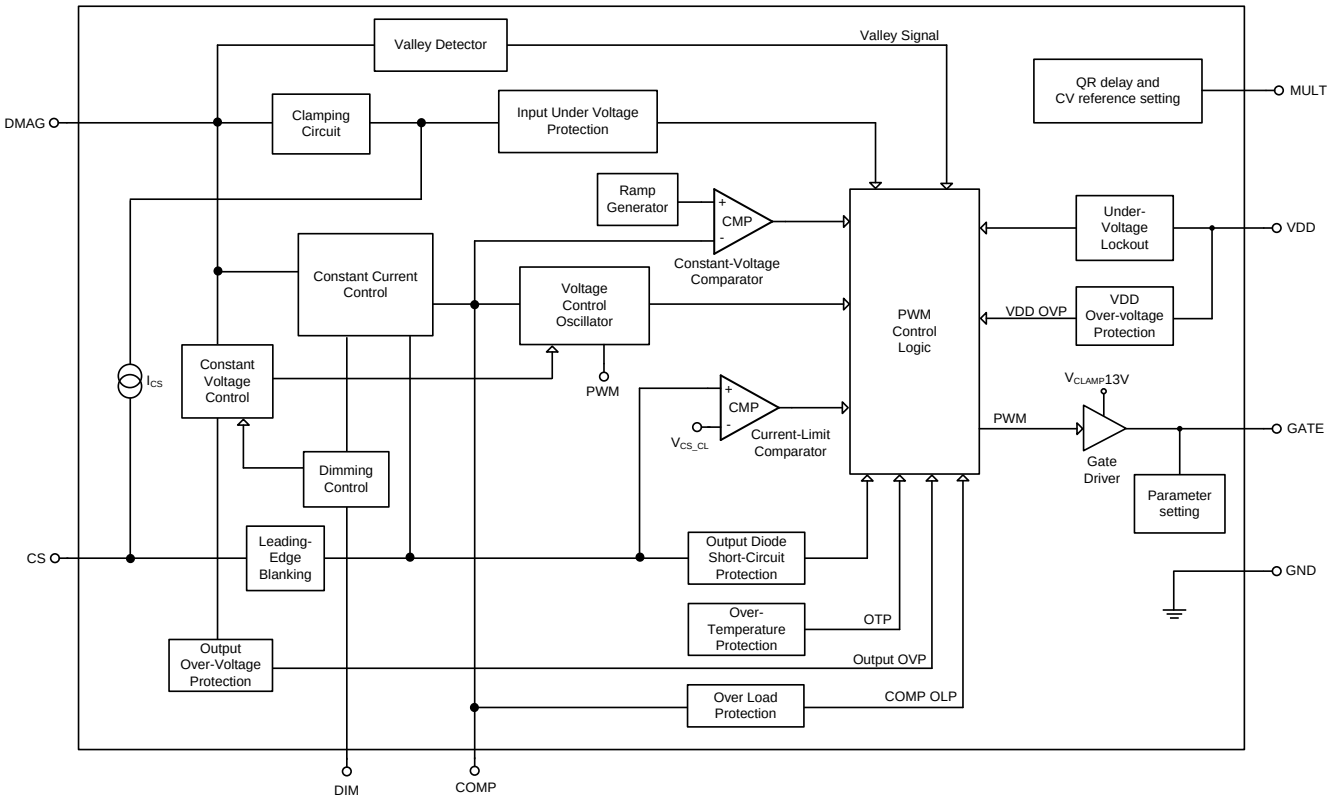
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	MULT	Multi function. Set CV reference voltage and QR delay.
2	GND	Ground of the controller.
3	COMP	Compensation node. Output of the internal trans-conductance amplifier.
4	DIM	Dimming signal input. LED driving current can be modulated by the PWM duty ratio or the average level of this pin.
5	DMAG	Demagnetization pin. To detect the input and the output voltage from the auxiliary winding of the transformer.
6	CS	Current sense input. Connect this pin to the current sense resistor.
7	GATE	Gate driver output for an external power MOSFET. It is recommended to add an external totem pole circuit if the Qg of MOSFET is higher than 60nC.
8	VDD	Supply voltage (V_{DD}) input. The controller will be enabled when V_{DD} exceeds V_{TH_ON} and disabled when V_{DD} is lower than V_{TH_OFF}.

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Functional Block Diagram



Operation

Flyback Control

Figure 1 shows a typical flyback converter with input voltage (V_{IN}).

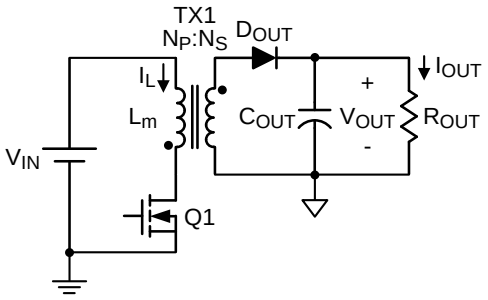


Figure 1. Typical Flyback Converter

The RT7331S needs no shunt regulator and opto-coupler at the secondary side to achieve the output current regulation. Figure 2 shows several key waveforms of a conventional flyback converter in Quasi-Resonant (QR) mode, in which V_{AUX} is the voltage on the auxiliary winding of the transformer.

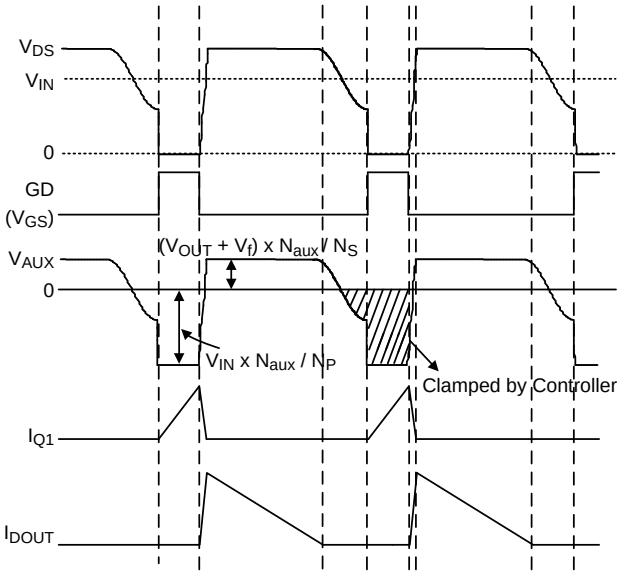


Figure 2. Key Waveforms of a Flyback Converter

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Voltage Clamping Circuit

The RT7331S provides a voltage clamping circuit at DMAG pin since the voltage on the auxiliary winding is negative when the main switch is turned on. The lowest voltage on DMAG pin is clamped near zero to prevent the IC from being damaged by the negative voltage. Meanwhile, the sourcing DMAG current (I_{DMAG}), flowing through the upper resistor (R_{DMAG1}), is sampled and held to be a bus-voltage-related signal for propagation delay compensation. The RT7331S embeds the programmable propagation delay compensation through CS pin. A sourcing current I_{CS} (equal to I_{DMAG} x K_{PC}) applies a voltage offset (I_{CS} x R_{PC}) which is proportional to line voltage on CS to compensate the propagation delay effect. Thus, the output current can be equal at high and low bus voltage.

Quasi-Resonant Operation

Figure 3 illustrates how valley signal triggers PWM. If no valley signal detected for a long time, the next PWM is triggered by a starter circuit at the end of the interval (t_{START}, 127.5μs typ.). A blanking time ($t_{S(MIN)}$, 8.5μs typ.), which starts at the rising edge of the previous PWM signal, limits minimum switching period. When the $t_{S(MIN)}$ interval is on-going, all of valley signals are not allowed to trigger the next PWM signal. After the end of the $t_{S(MIN)}$ interval, the coming valley will trigger the next PWM signal. If one or more valley signals are detected during the $t_{S(MIN)}$ interval and no valley is detected after the end of the $t_{S(MIN)}$ interval, the next PWM signal will be triggered automatically at the end of the $t_{S(MIN)}$ + 5μs (typ.).

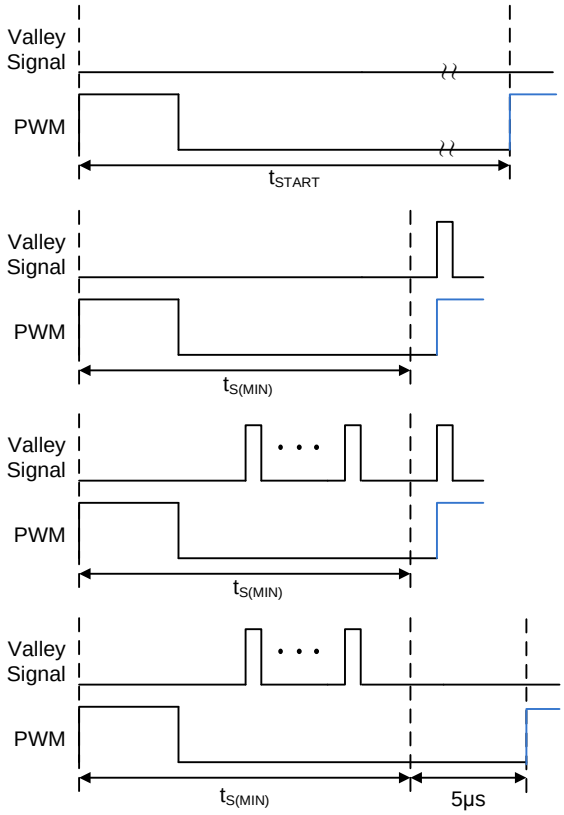


Figure 3. PWM Triggered Method

Dimming Function

The RT7331S features the analog and PWM dimming function.

When the average voltage on the DIM pin (V_{DIM}) is within V_{DIM_EN} and V_{DIM_HIGH}, the regulation factor of the constant current control (K_{CC}) is linearly proportional to V_{DIM}. The suggested PWM high level is 3.3V while the low level is 0V. The frequency of the PWM signal is recommended to be 1.2kHz. The analog and PWM dimming curves are shown in Figure 4. If there exists non-dimming requirement, a pull-high resistor of 1MΩ is needed to connect between DIM and VDD pins.

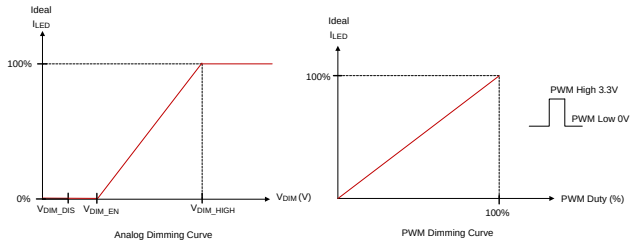


Figure 4. Dimming Curve

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CV Mode

When V_{DIM} is lower than V_{DIM_DIS} for 15ms (typ.), the RT7331S will operate in CV mode. The output voltage is regulated by sensing the auxiliary winding voltage. Furthermore, the CV reference voltage can be selected by the MULT pin resistor R_{MULT}.

Protections

The RT7331S embeds comprehensive protection functions, including LED open-circuit protection, LED short-circuit protection, output diode short-circuit protection, VDD Under-Voltage Lockout (UVLO), VDD Over-Voltage Protection (VDD OVP), over load protection, input under / over voltage protection, internal Over-Temperature Protection (OTP), and cycle-by-cycle current limitation.

VDD pin will sink an extra current (600μA typ.) when protections are triggered except for VDD UVLO and cycle-by-cycle current limitation.

LED Open-Circuit Protection

In an event of output open circuit, the converter will be shut down to prevent being damaged, and it will be auto-restarted when the output is recovered. Once the LED is open-circuit, the output voltage keeps rising, causing the voltage on DMAG pin V_{DMAG} rising accordingly. When the sample-and-hold DMAG voltage exceeds its OV threshold (V_{DMAG_OVP}, 3.8V typ.), output OVP will be activated and the GATE will be forced low to turn off the main switch. If the output is still open-circuit when the converter restarts, the converter will be shut down again.

LED Short-Circuit Protection

The RT7331S implements LED short-circuit protection by DMAG and CS pins. Once the DMAG voltage is lower than 0.5V (typ.) and the current sense voltage V_{CS} exceeds the peak current limitation (V_{CS_CL}) for few cycles, the converter will be shut down to prevent damage. It will be auto-restarted when the output is recovered.

The LED short-circuit protection is masked during the first 30ms (typ.) of power on (VDD > V_{TH_ON}).

Output Diode Short-Circuit Protection

When the output diode is damaged as short-circuit, the transformer will be led to magnetic saturation and the main switch will suffer from a high current stress. To avoid the above situation, an output diode short-circuit protection is built-in. When CS voltage V_{CS} exceeds the threshold (V_{CS_SD} 1 typ.) of the output diode short-circuit protection, the RT7331S will shut down the PWM output (GATE pin) in few cycles to prevent the converter from damage. It will be auto-restarted when the fault condition is recovered.

VDD Under-Voltage Lockout (UVLO) and Over-Voltage Protection (VDD OVP)

The RT7331S will be enabled when VDD voltage (V_{DD}) exceeds rising UVLO threshold (V_{TH_ON}, 20V typ.) and disabled when V_{DD} is lower than falling UVLO threshold (V_{TH_OFF}, 9V typ.).

When V_{DD} exceeds its over-voltage threshold (V_{DD_OVP}, 37V typ.), the PWM output of the RT7331S is shut down. It will be auto-restarted when the VDD is recovered to a normal level.

In order to ensure the VDD voltage can drop to UVLO threshold to reset some protection function, it is recommended to provide the power for the RT7331S VDD from the auxiliary winding of the transformer.

It should be noticed that the start up current I_{ST} must be lower than the discharge current of capacitor C_{VDD}, otherwise VDD may trigger VDD OVP in CV mode or low dim condition. In general, the R_{ST} is suggested to be higher than 700kΩ.

Input Under-Voltage Protection

When VDD exceeds VTH_ON, the RT7331S will entry CV mode. As soon as I_{DMAG} is higher than I_{DMAG_BRI}, the RT7331S will entry normal operation.

Over Load Protection

If the current sense resistor R_{CS} is short-circuit, the COMP voltage will increase and result in over load operation. When V_{COMP} reaches to V_{COMP_OLP} (4.8V typ.) for 70ms (typ.), the main switch will be turned off.

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Internal Over-Temperature Protection (OTP)

The RT7331S provides the internal OTP function to protect the controller itself from suffering the thermal stress and permanent damage. Once the junction temperature is higher than the OTP threshold (T_{OTP_STTH}, 150°C typ.), the controller will shut down until the temperature decreases below 140°C (typ.).

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Absolute Maximum Ratings (Note 1)

- Supply Voltage, VDD ---------- –0.3V to 40V
- Gate Driver Output, GATE ---------- –0.3V to 18V
- Other Pins ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C

  SOP-8 ---------- 0.48W
- Package Thermal Resistance (Note 2)

  SOP-8, θ_{JA} ---------- 206.9°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 11V to 34V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{DD} = 25V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section (VDD)						
VDD OVP Threshold Voltage	V_{DD_OVP}		--	37	--	V
Rising UVLO Threshold Voltage	V_{TH_ON}		--	20	--	V
Falling UVLO Threshold Voltage	V_{TH_OFF}		8	9	10	V
VDD Holdup Mode Entry Point	V_{DD_ET}		--	10.4	--	V
VDD Holdup Mode Ending Point	V_{DD_ED}		--	11	--	V
Start-up Current	I_{DD_ST}	V_{DD} = V_{TH_ON} – 1V	--	12	--	μA
Operating Current	I_{DD_OP}	V_{DD} = 15V, GATE and COMP pin open	--	650	--	μA
DMAG Section (DMAG)						
Lower Clamp Voltage	V_{DMAG_L}	I_{DMAG} = 1mA	--	105	--	mV
DMAG OVP Threshold Voltage	V_{DMAG_OVP}		--	3.8	--	V
Threshold Current of Brown-in Protection	I_{DMAG_BRI}		--	700	--	μA
DMAG Reference Voltage	V_{DMAG_REF}	CV mode, R_{MULT} = 3.5kΩ	--	1.2	--	V
DMAG Threshold Voltage of Soft Start	V_{DMAG_SS}	When V_{DMAG} < V_{DMAG_SS}, soft start	--	0.5	--	V
DMAG Threshold for Output UVP	V_{TH_UVP}	V_{TH_UVP} = V_{DMAG_SS}	--	0.5	--	V
Minimum DMAG Masking Time	$t_{BK(MIN)}$	t_{BK} = 1 + V_{CS_PK} x 2, V_{CS} = 0V	--	1	--	μs

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum DMAG Masking Time	$t_{BK(MAX)}$	t_{BK} = 1 + V_{CS_PK} x 2, V_{CS} = 0.5V	--	2	--	μs
Constant Current Control Section (COMP)						
COMP Over Load Protection Threshold	V_{COMP_OLP}	V_{COMP} rising	--	4.8	--	V
Minimum COMP Voltage	$V_{COMP(MIN)}$		--	0.5	--	V
Maximum Regulated factor for constant-Current Control	$K_{CC(MAX)}$	V_{DIM} = 3V, V_{COMP} = 3V	246.3	250	253.7	mV
Current Sense Section (CS)						
Leading Edge Blanking Time	t_{LEB}	LEB + Propagation Delay	--	400	--	ns
Peak Current Limit at Normal Operation	V_{CL1}	MULT = V_{MLV1} & V_{MLV3}	--	0.4	--	V
	V_{CL2}	MULT = V_{MLV2}	--	0.5	--	V
Peak Current Limit in VDD Holdup and CV Mode	V_{CL_MIN}	CV mode or VDD < V_{DD_ET}	--	0.05	--	V
Peak Current Shutdown Voltage Threshold	V_{CS_SD}		--	1	--	V
Propagation Delay Compensation Factor	K_{PC}	I_{CS} = K_{PC} x I_{DMAG}, I_{DMAG} = −900μA	--	0.022	--	A/A
Gate Driving Section (GATE)						
Rising Time	t_R	V_{DD} = 15V, C_L = 1nF (10% to 90%)	--	160	--	ns
Falling Time	t_F	V_{DD} = 15V, C_L = 1nF (10% to 90%)	--	30	--	ns
Gate Output Clamping Voltage	V_{CLAMP}	V_{DD} = 15V	--	13	--	V
Internal Pull Low Resistor	R_{GATE}	VDD < V_{TH_ON}, before startup	--	60	--	kΩ
Timing Control Section						
Minimum Switching Period	$t_{S(MIN)}$	V_{COMP} > 2V	--	8.5	--	μs
Minimum Switching Period in Green Mode	$t_{S(MIN)_GM}$	V_{COMP} < 0.5V	--	500	--	μs
Start Time During Startup and Normal Operation	t_{START}	V_{COMP} > 2V	--	127.5	--	μs
Max. Start time in Green Mode	t_{START_GM}	V_{COMP} < 0.5V	--	7.5	--	ms
Minimum On Time	$t_{ON(MIN)}$	R_{GS} = 27kΩ	--	600	--	ns
		R_{GS} = 39kΩ/56kΩ	--	500	--	ns
Maximum On Time	$t_{ON(MAX)}$		--	20	--	μs
Dimming Section						
Analog Dimming High Threshold Voltage	V_{DIM_HIGH}		--	2.8	--	V
Analog Dimming Enable Threshold Voltage	V_{DIM_EN}		--	300	--	mV
Analog Dimming Disable Threshold Voltage	V_{DIM_DIS}		--	250	--	mV

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Parameter Setting Section (MULT)						
Detection Sourcing Current	I_{det}	During t_{det}	--	20	--	μA

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity two-layer test board on a JEDEC thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

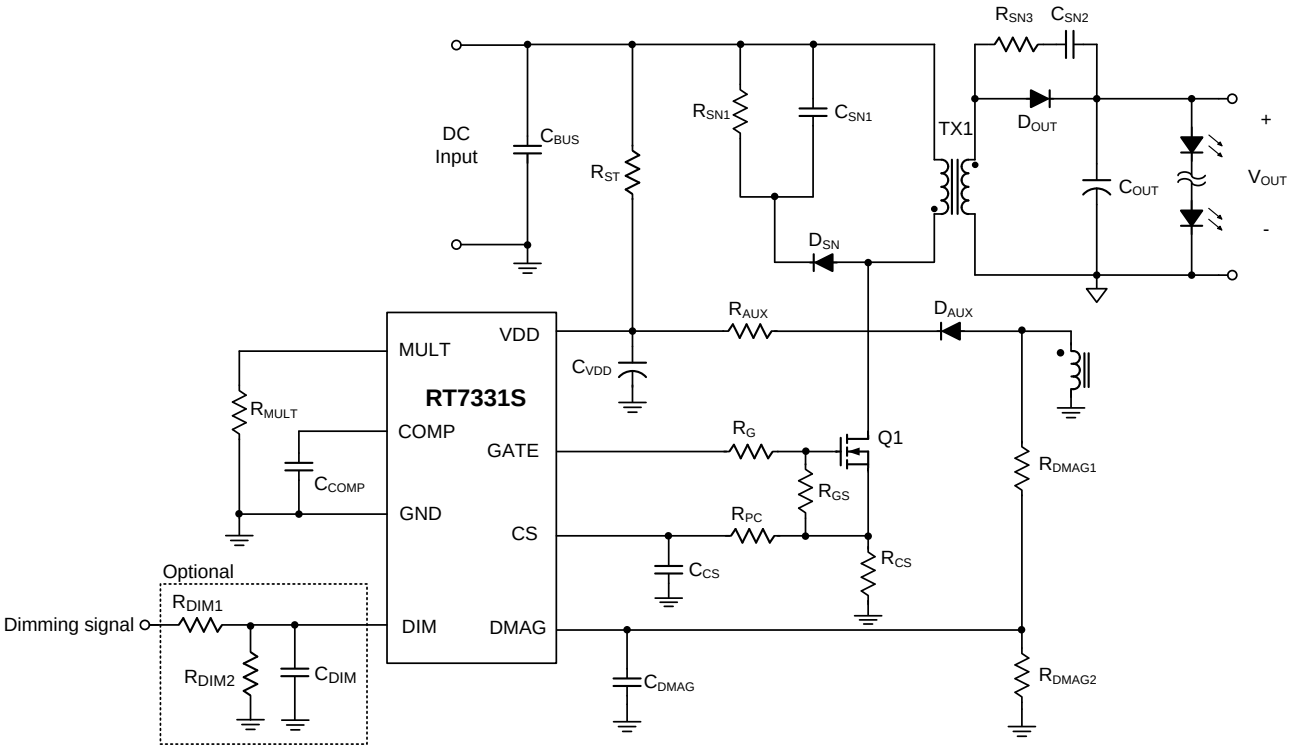
Note 5. Guarantee by design.

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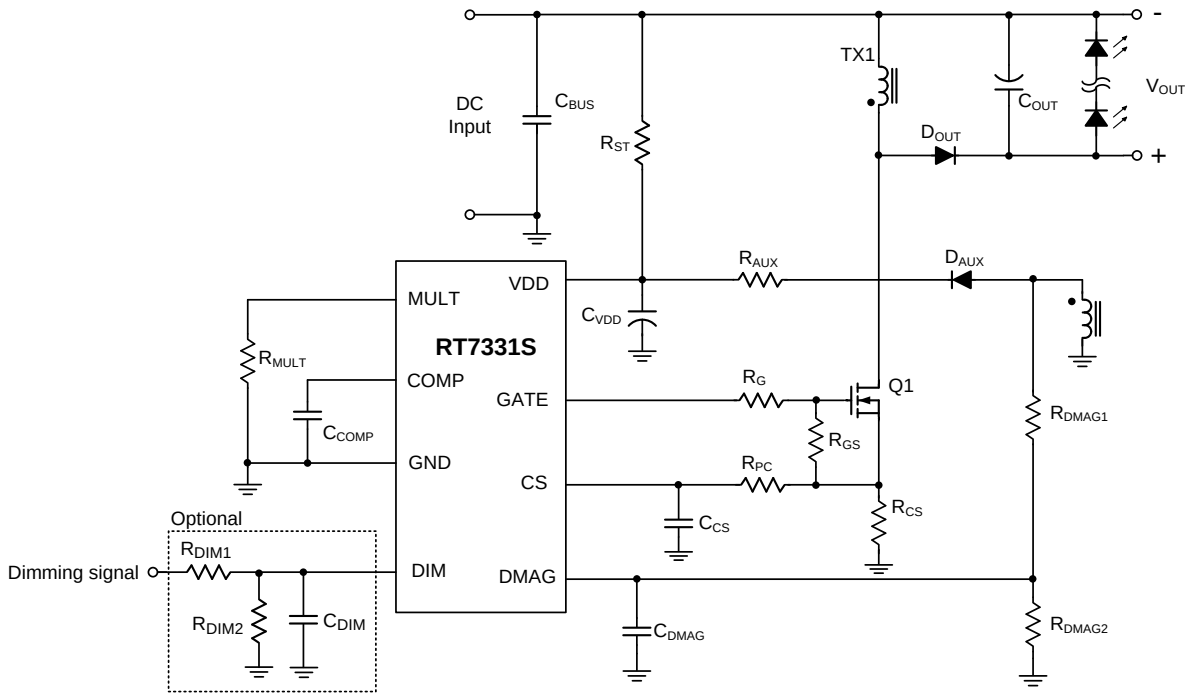
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Typical Application Circuit

Flyback Application Circuit



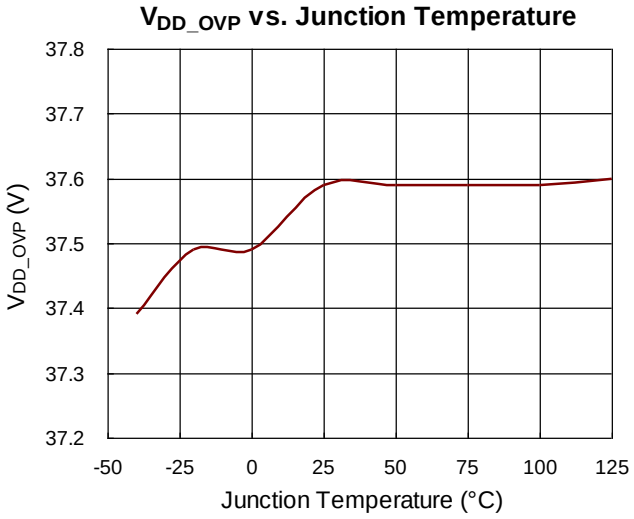
Buck-Boost Application Circuit

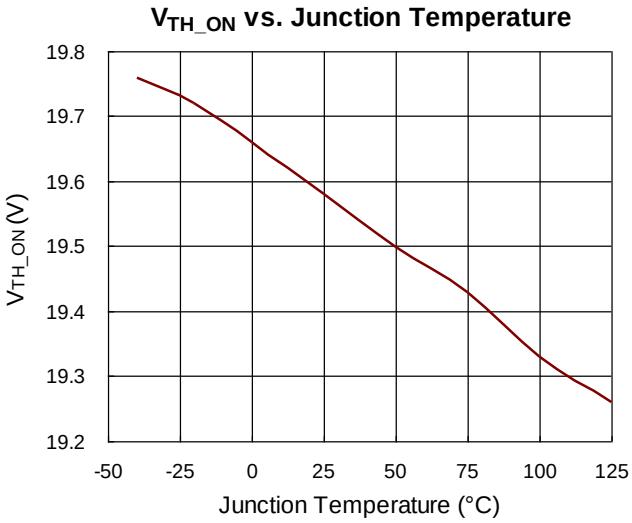


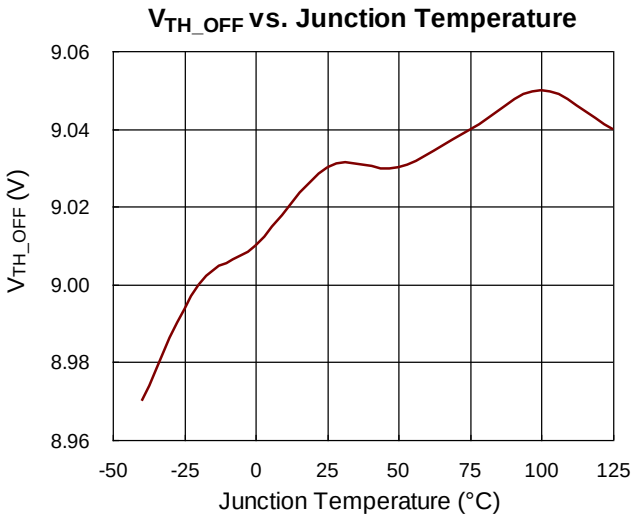
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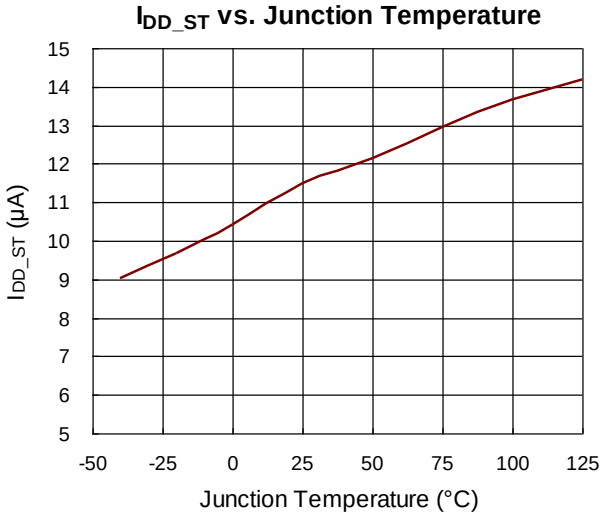
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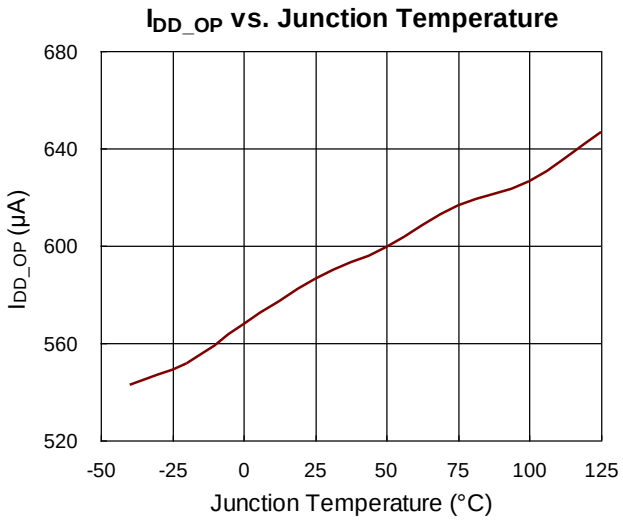
Typical Operating Characteristics

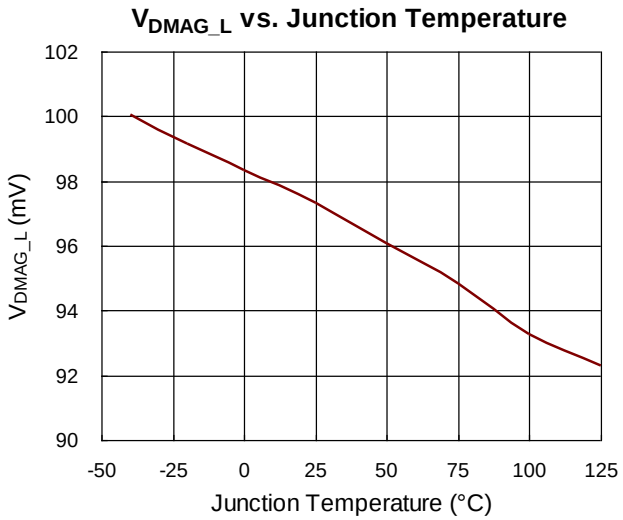








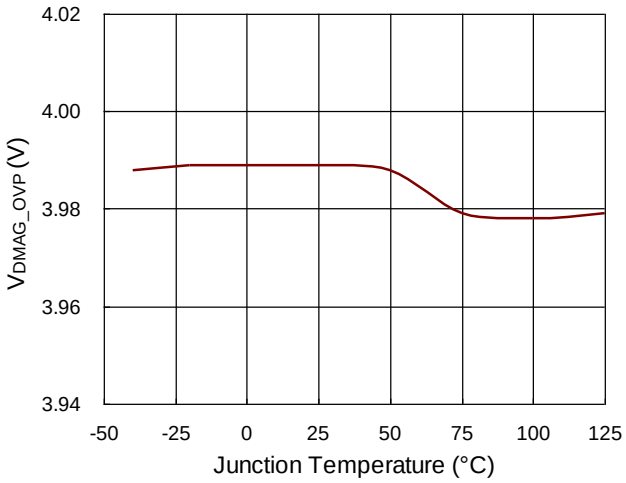




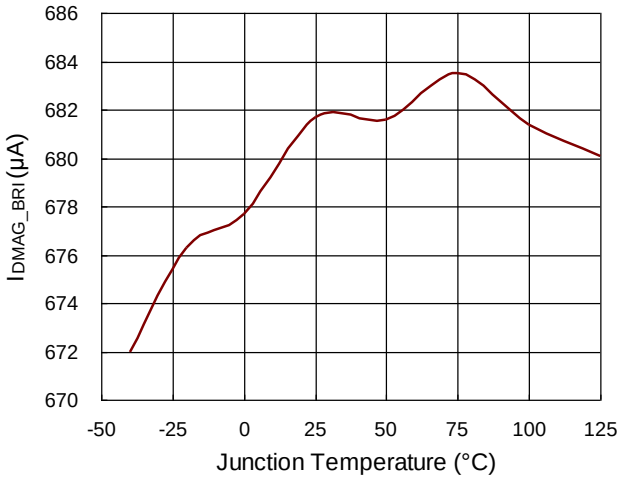
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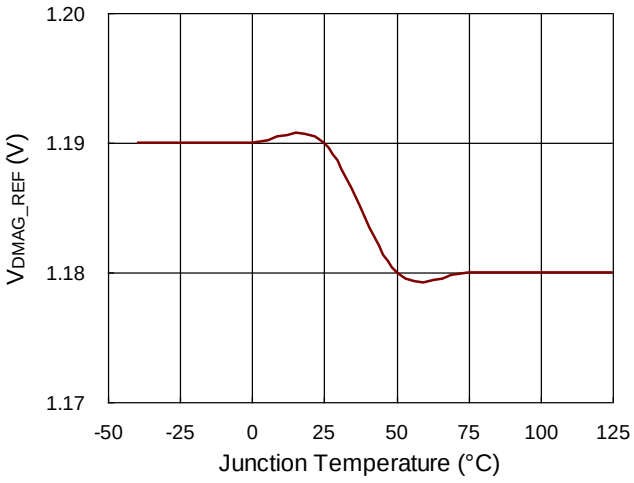
V_{DMAG_OVP} vs. Junction Temperature



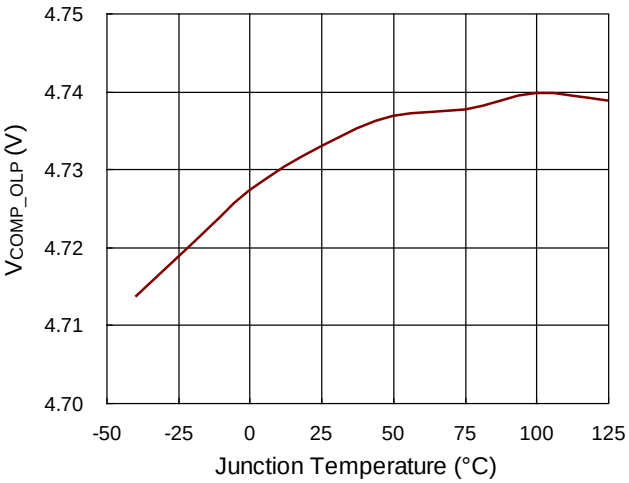
I_{DMAG_BRI} vs. Junction Temperature



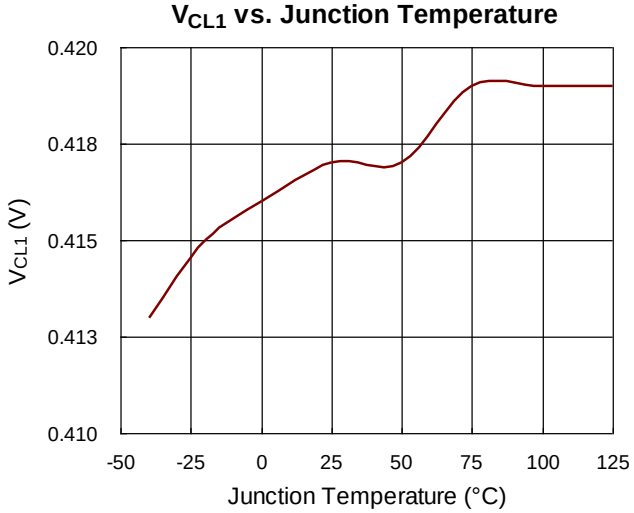
V_{DMAG_REF} vs. Junction Temperature



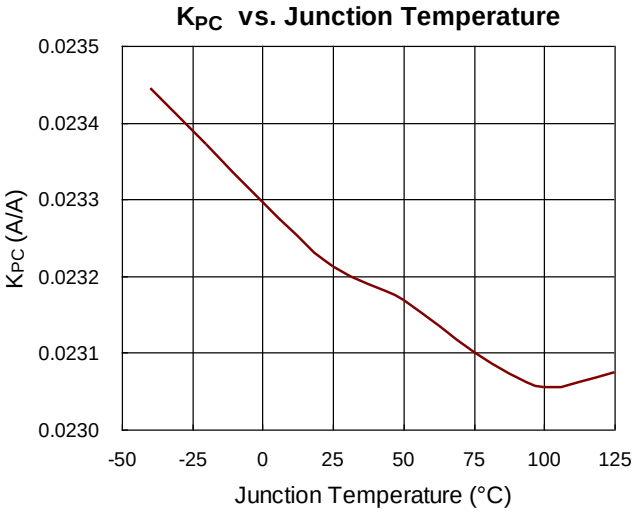
V_{COMP_OLP} vs. Junction Temperature



V_{CL1} vs. Junction Temperature

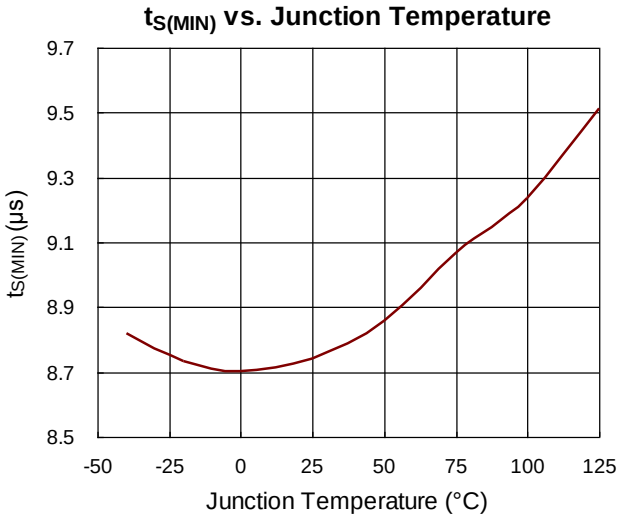


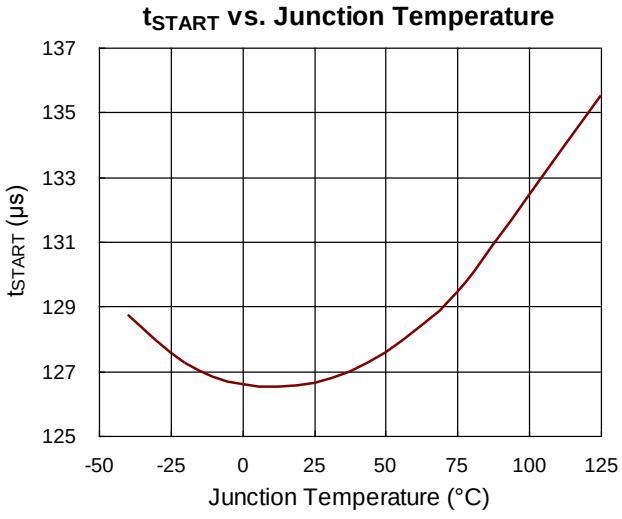
K_{PC} vs. Junction Temperature

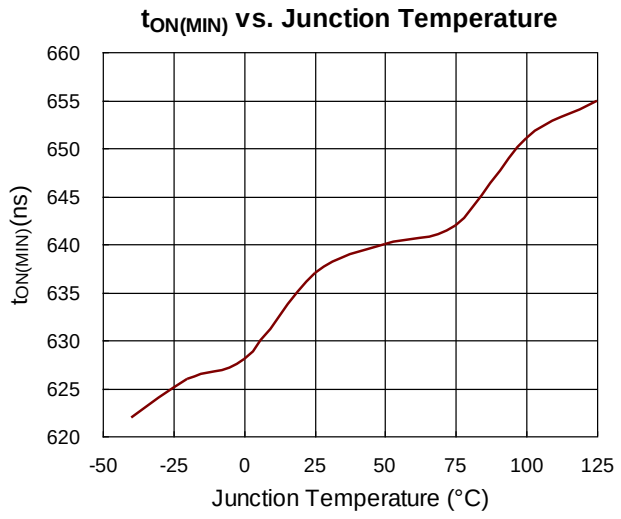


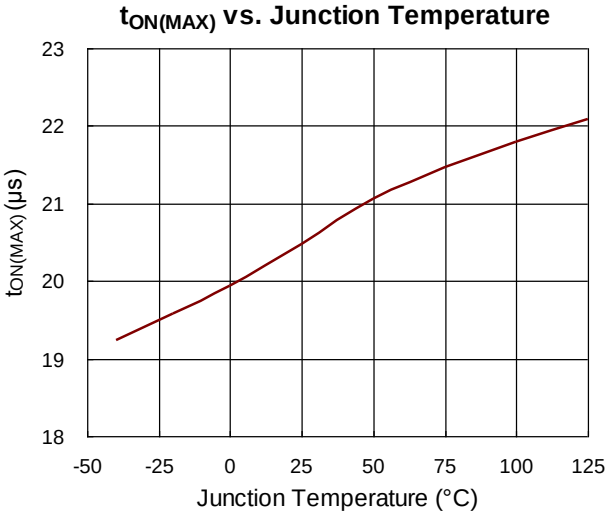
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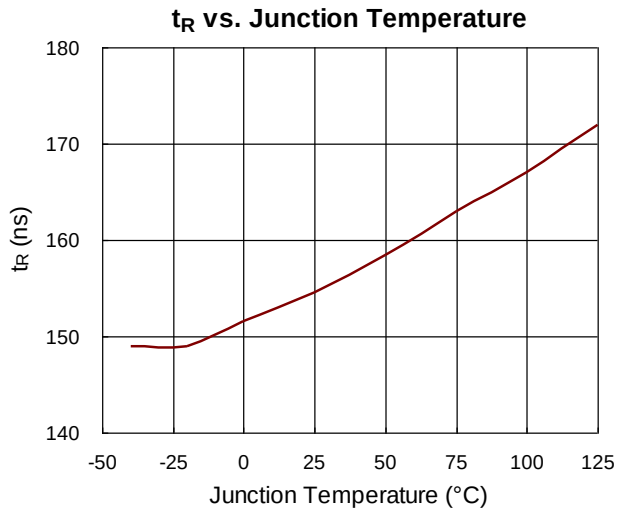
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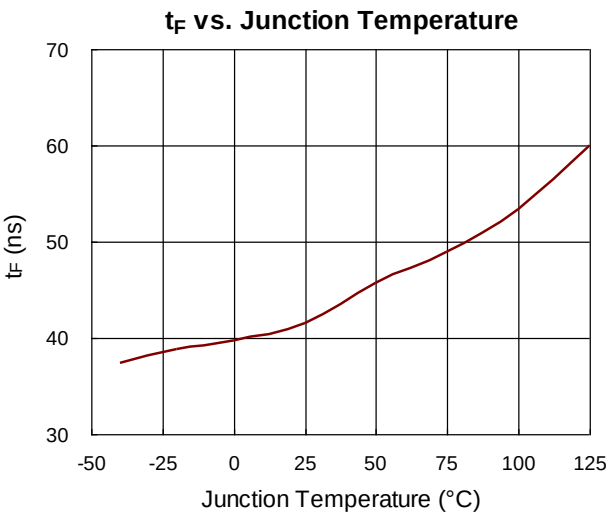






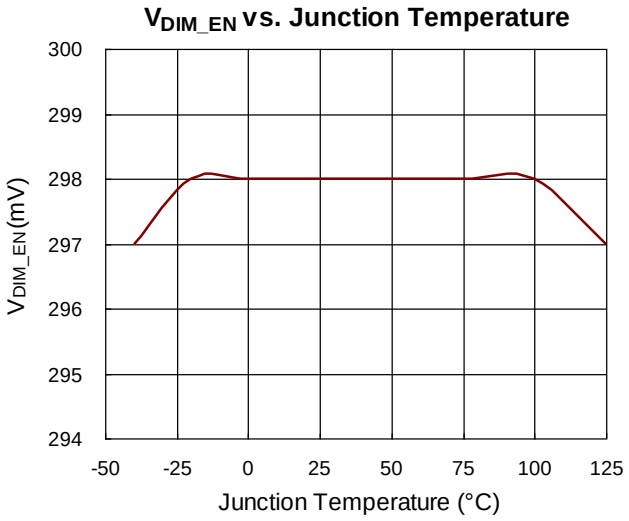


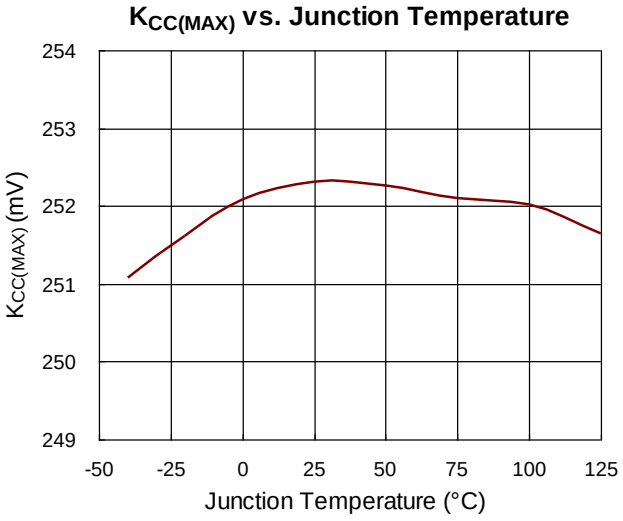


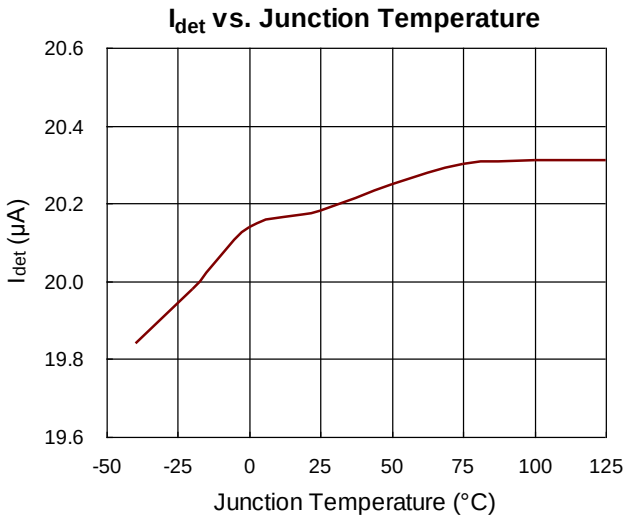


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Application Information

Output Current Setting

Considering the conversion efficiency, the programmed DC level of the average output current ($I_{OUT}(t)$) can be derived as :

$$I_{OUT_CC} = \frac{1}{2} \times \frac{N_P}{N_S} \times \frac{K_{CC}}{R_{CS}} \times CTR_{TX1}$$

$$CTR_{TX1} = \frac{I_{SEC_PK}}{I_{PRI_PK}} \times \frac{N_S}{N_P}$$

in which CTR_{TX1} is the current transfer ratio of the transformer TX1, I_{SEC_PK} is the peak current of the secondary side, and I_{PRI_PK} is the peak current of the primary side. CTR_{TX1} can be estimated to be 0.9. According to the above parameters, current sense resistor R_{CS} can be determined as the following equation :

$$R_{CS} = \frac{1}{2} \times \frac{N_P}{N_S} \times \frac{K_{CC}}{I_{OUT_CC}} \times CTR_{TX1}$$

Propagation Delay Compensation Design

The V_{CS} deviation (ΔV_{CS}) caused by propagation delay effect can be derived as:

$$\Delta V_{CS} = \frac{V_{IN} \cdot t_D \cdot R_{CS}}{L_m},$$

in which t_D is the delay period which includes the propagation delay of the RT7331S and the turn-off transition of the main MOSFET. The sourcing current from CS pin of the RT7331S (I_{CS}) can be expressed as :

$$I_{CS} = K_{PC} \cdot V_{IN} \cdot \frac{N_A}{N_P} \cdot \frac{1}{R_{DMAG1}}$$

where N_A is the turns number of the auxiliary winding.

R_{PC} can be designed by :

$$R_{PC} = \frac{\Delta V_{CS}}{I_{CS}} = \frac{t_D \cdot R_{CS} \cdot R_{DMAG1}}{L_m \cdot K_{PC}} \cdot \frac{N_P}{N_A}$$

CV Reference and QR Delay Setting

After startup, the CV reference voltage and the QR delay is determined by the MULT pin resistor R_{MULT}. The corresponding values of the different R_{MULT} are as follows :

CV Voltage	Current Limit	QR delay = 100ns to 500ns
1.2V	0.4V	R_{MULT} = 3.5kΩ to 17.5kΩ
1.2V	0.5V	R_{MULT} = 24.5kΩ to 122.5kΩ
0.73V	0.4V	R_{MULT} = 171.5kΩ to 857.5kΩ

Provided that the CV reference voltage is chosen as 1.2V (typ.) and the estimated half of the resonant period of the magnetizing inductance L_m and the parasitic capacitance of MOSFET is 100ns, R_{MULT} can be designed as the following equation :

$$R_{MULT} = 3.5k\Omega \times \frac{100ns}{100ns} = 3.5k\Omega \ (typ.)$$

COMP Voltage Design

The COMP voltage, V_{COMP}, can be expressed as follows :

$$V_{COMP} = \frac{V_{set} \times G_{m_ramp} \times t_{on_pk}}{C_{ramp}} + V_D$$

where t_{on_pk} is the peak values at V_{IN_PK}, G_{m_ramp} and C_{ramp} are the fixed parameters in RT7331S and the typical values are : G_{m_ramp} = 2.7μA/V, C_{ramp} = 6.5pF. V_D is the offset of the constant-voltage comparator and its typical value is 2V.

V_{set} can be selected as different voltages by the external Gate-to-Source resistor R_{GS}. The recommended R_{GS} is 22kΩ or 47kΩ, and the corresponding values of V_{set} are 0.5V (typ.) and 0.6V (typ.), respectively. It is recommended to design VCOMP = 2V to 3.5V

Input Under-Voltage Protection Setting

The input voltage is detected by R_{DMAG1}, which is used to set the input UV level (VIN_UVP). Thus, R_{DMAG1} can be determined by the following equation :

$$R_{DMAG1} = V_{IN} \times \frac{N_A}{N_P} \times \frac{1}{I_{DMAG_BRI}}$$

where I_{DMAG_BRI} is the fixed parameters in RT7331S and its typical value is 700μA.

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Output Over-Voltage Protection Setting

Output OVP is achieved by sensing the voltage on the auxiliary winding. It is recommended that output OV level (V_{OUT_OVP}) is set at 120% of nominal output voltage (V_{OUT}). Thus, R_{DMAG1} and R_{DMAG2} can be determined by the equation as :

$$V_{OUT} \times \frac{N_A}{N_S} \times \frac{R_{DMAG2}}{R_{DMAG1} + R_{DMAG2}} \times 120\% = 3.8V(typ.)$$

Adaptive Blanking Time

When the MOSFET is turned off, the leakage inductance of the transformer and parasitic capacitance (C_{OSS}) of the MOSFET induce resonance waveform on the DMAG pin. The resonance waveform may make the controller false trigger the DMAG OVP, and it may cause the controller operate in unstable condition. As load increases, the resonance time also increases. It is recommended to add a 10pF to 47pF bypass capacitor, and it should be as close to DMAG pin as possible. The larger bypass capacitor may cause phase shift on DMAG waveform, so the MOSFET is not turned on at exact valley point.

To avoid the above issue, the RT7331S provides adaptive blanking time (t_{BK}). It varies with the peak voltage of the CS pin (V_{CS_PK}), as shown by the following formula :

t_{BK} = 1μs + V_{CS_PK} x 2μs/V (typ.)

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOP-8 package, the thermal resistance, θ_{JA}, is 206.9°C/W on a standard JEDEC low effective-thermal-conductivity two-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (206.9°C/W) = 0.48W for a SOP-8 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

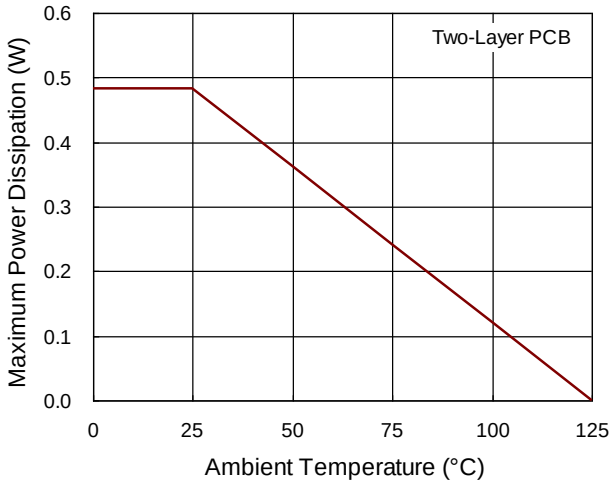


Figure 6. Derating Curve of Maximum Power Dissipation

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Layout Considerations

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when designing a PCB layout for switching power supply :

- The current path(1) from the input capacitor, transformer, MOSFET, RCS returning to input capacitor is a high frequency current loop. The path(2) from GATE pin, MOSFET, RCS returning to the ground of the IC is also a high frequency current loop. They must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially. Besides, the path(3) between MOSFET ground(b) and IC ground(d) is recommended to be as short as possible, too.
- The path(4) from RCD snubber circuit to MOSFET is a high switching loop. Keep it as small as possible.
- The path(5) from the input capacitor to VDD pin is a high voltage loop. Keep a space from path(5) to other low voltage traces.
- It is good for reducing noise, output ripple and EMI issue to separate ground traces of the input capacitor(a), MOSFET(b), auxiliary winding(c) and IC control circuit(d). Finally, connect them together at the input capacitor ground(a). The areas of these ground traces should be kept large.
- To reduce the parasitic trace inductance and EMI, the area of the loop connecting to the secondary winding, the output diode, and the output filter capacitor must be minimized. In addition, the sufficient copper area at the anode and cathode terminal of the output diode can help for heat-sinking. It is recommended to apply the larger area at the quiescent cathode terminal. The large anode area will induce high-frequency radiated EMI.

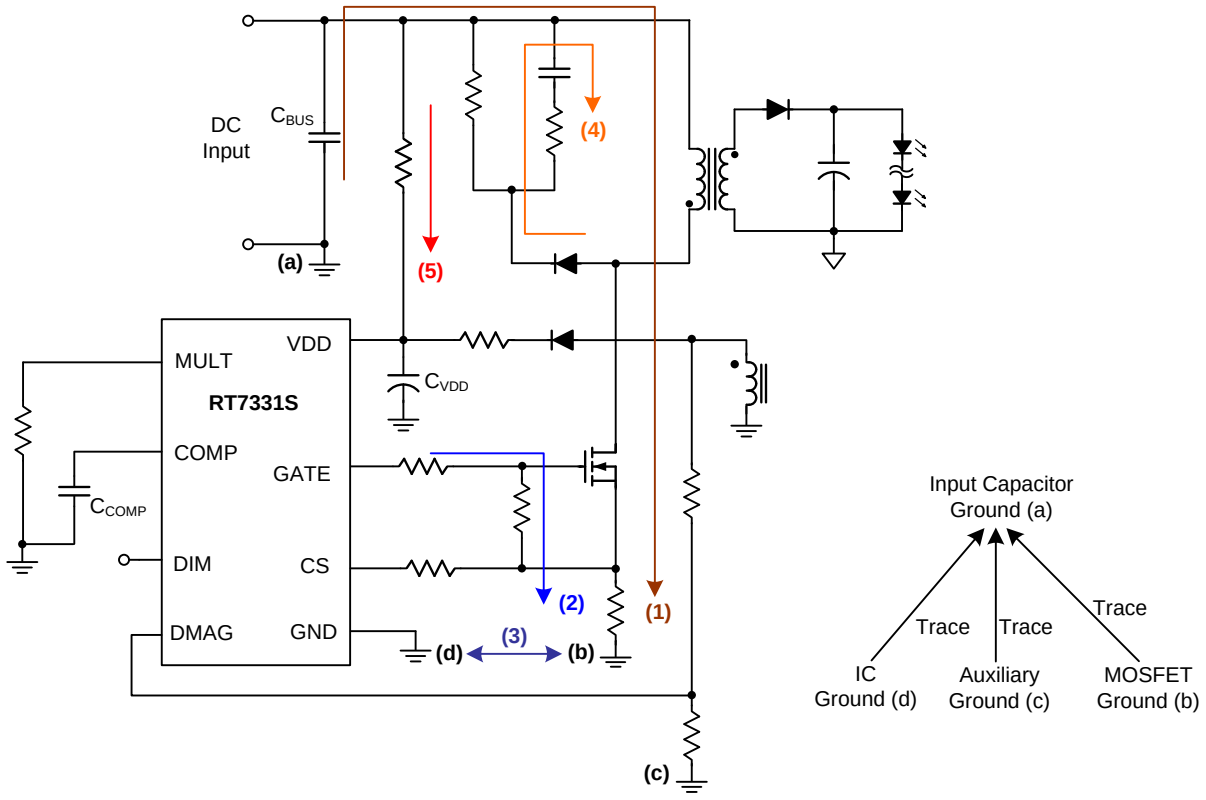


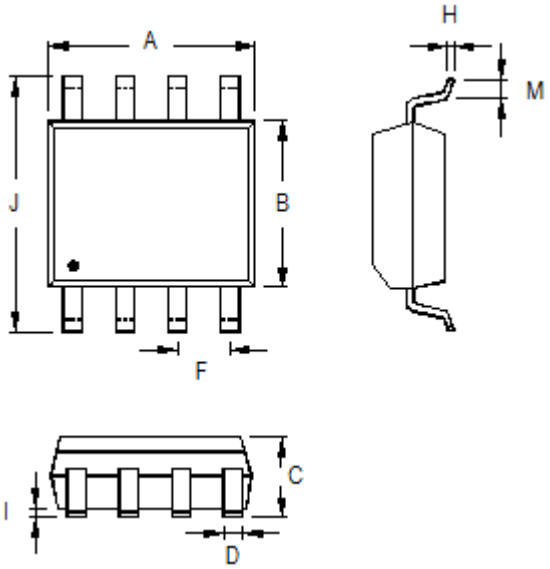
Figure 7.

PCB Layout Guide

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Outline Dimension



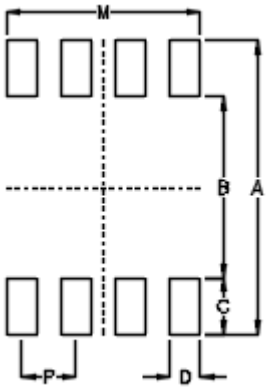
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

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Footprint Information



Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P	A	B	C	D	M	
SOP-8	8	1.27	6.80	4.20	1.30	0.70	4.51	±0.10

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