REV. 1

PRELIMINARY SPECIFICATION

GM76C256/L/LL

32,768x8 BIT STATIC RAM HIGH PERFORMANCE

Description

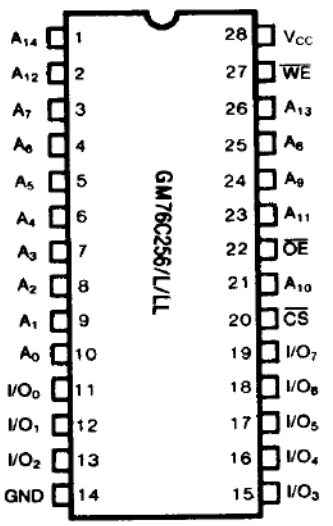
The GM76C256/L/LL is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 60mA (max) at minimum cycle time of 85ns.

When $\overline{CS}$ is a logical high, the device is placed in low power standby mode in which standby current is 2mA (max).

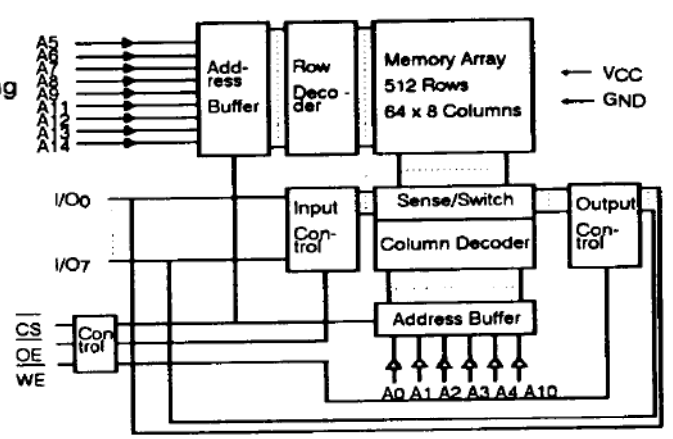
The GM76C256/L/LL has two control inputs. Chip select ($\overline{CS}$) allows for device selection and data retention control, and output enable ($\overline{OE}$) provides fast memory access.

Thus the GM76C256/L/LL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The GM76C256/L/LL is offered in 28 pin DIP (600mil) and SOP (330mil).

Pin Configuration



Block Diagram



Feature

- High Speed : Fast Access and Cycle Time 85/100/120 ns Max.
- Low Power Standby and Low Power Operation ; Stand by : 0.55mW Max. (Low Power Version) Operation : 385mW Max.
- Completely Static RAM : No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible : All Inputs and Outputs
- Standard 28 DIP and SOP
- Capability of Battery Back up Operation

Pin Description

$A_0 \sim A_{14}$	: Address Input
$\overline{WE}$	: Write Enable Input
$\overline{OE}$	: Output Enable Input
$\overline{CS}$	: Chip Select Input
$I/O_0 \sim I/O_7$	: Data Input/Output
V_{CC}	: Power Supply, +5V
GND	: Ground

Absolute Maximum Ratings

Input Voltage	V_{IN}	-0.3 to 7.0V
Supply Voltage	V_{CC}	-0.5 to 7.0V
Supply Voltage Applied to Outputs High Z State (High Z)	V_{CC}	-0.5 to 7.0V
Storage Temperature	T_{STG}	-65 to +150°C
Storage Temperature with Power Supplied	T_{POWER}	-55 to +125°C
Output Current into Output	I_O	10mA

Recommended Operating Condition

$T_A = 0° \sim 70°C$

Supply Voltage	V_{CC}	4.5 to 5.5V
Input High Voltage	V_{IH}	2.2 to 6V
Input Low Voltage	V_{IL}	-0.3 to 0.8V
Data Retention Supply Voltage	V_{DH}	2.0 to 5.5V

* Note: Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect Power Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

DC Electrical Characteristics : (V_{CC} = 5V ±10%, T_A = 0°C ~ 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output High Voltage	V_{CC} = Min I_{OH} = 1.0mA	2.4	-	-	V
V_{OL}	Output Low Voltage	V_{CC} = Min I_{OL} = 2.1mA	-	-	0.4	V
$\lvert I_{LI} \rvert$	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	-2	-	+2	μA
$\lvert I_{LO} \rvert$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}	-2	-	+2	μA
I_{DDS1}	Stand-by Power Supply Current	$\overline{CS}$ = V_{IH}	-	-	2	mA
I_{DDS2}		$\overline{CS}$ ≥ V_{CC} -0.2V GM76C256 GM76C256L GM76C256LL	- - -	- 2 2	1 100 10	mA μA μA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	-	-	45	mA
I_{CC1}	Average Operating Power Supply Current	Min. Cycle, duty = 100%, $I_{I/O}$ = 0mA	-	-	60	mA

Note : V_{CC} = 5V, T_A = 25°C

AC Operating Characteristics : V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C (Note 1, 2, 3)

• Read Cycle

SYMBOL	PARAMETER	GM76C256-85		GM76C256-10		GM76C256-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	85	-	100	-	120	-	ns
t_{AA}	Address Access Time	-	85	-	100	-	120	ns
t_{ACS}	Chip Select Access Time	-	85	-	100	-	120	ns
t_{OE}	Output Enable to Output Valid	-	45	-	50	-	60	ns
t_{OH}	Output Hold from Address Change	5	-	10	-	10	-	ns
t_{CLZ}	Chip Selection to Output in Low Z	10	-	10	-	10	-	ns
t_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
t_{CHZ}	Chip Deselection to Output in High Z	0	30	0	35	0	40	ns
t_{OHZ}	Output Disable to Output in High Z	0	30	0	35	0	40	ns

Notes :

1. t_{OHZ}, t_{CHZ} and t_{WHZ} are tested with C_L = 5pF as in Figure 1b condition is measured ± 500mV from steady state voltage.
2. AC operating conditions assume signal transition times of 5ns or less timing reference levels of 1.5V, input pulse levels of 0.6V to 2.4V and output loading of the specified I_{OL}/I_{OH} and 100pF load capacitance.
3. By given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} for all devices. These parameters are sampled and not 100% tested.

AC Operating Characteristics : V_{CC} = 5V ±10%, T_A = 0°C ~ 70°C

• Write Cycle

SYMBOL	PARAMETER	GM76C256-85		GM76C256-10		GM76C256-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	85	-	100	-	120	-	ns
t_{CW}	Chip Selection to End of Write	75	-	80	-	85	-	ns
t_{AW}	Address Valid to End of Write	75	-	80	-	85	-	ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	60	-	60	-	70	-	ns
t_{WR}	Write Recovery Time	5	-	5	-	5	-	ns
t_{WHZ}	Write to Output in High Z	0	30	0	35	0	40	ns
t_{DW}	Data to Write Time Over-lap	40	-	40	-	50	-	ns
t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
t_{OHZ}	Output Disable to Output in High Z	0	30	0	35	0	40	ns
t_{OW}	Output Active from End of Write	5	-	5	-	5	-	ns

Note : t_{OHZ}, t_{CHZ} and t_{WHZ} are tested with C_L = 5pF as in Figure 1b condition is measured ±500mV from steady state voltage.

AC Test Loads and Waveforms

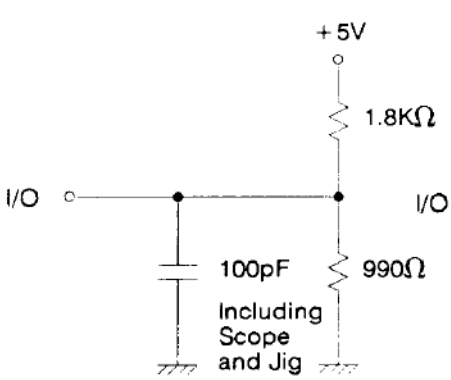


Figure 1a

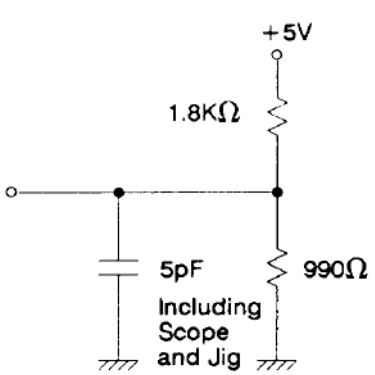


Figure 1b

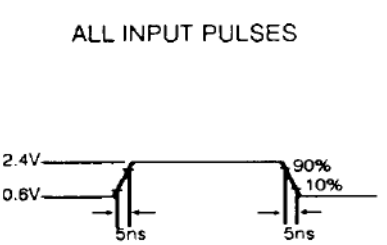
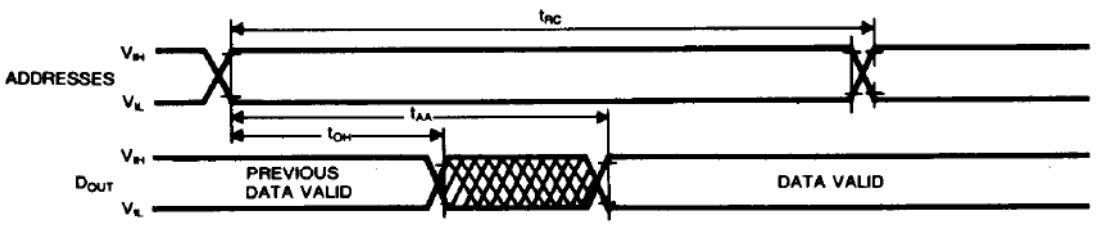


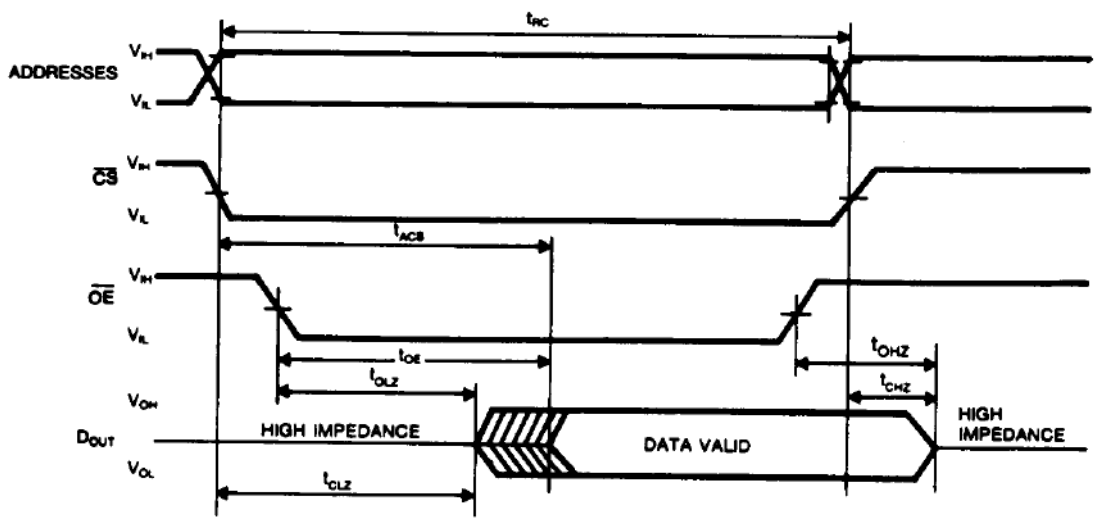
Figure 2

Timing Waveforms

Read Cycle 1 (Notes 1, 2)



Read Cycle 2 (Notes 2, 3)

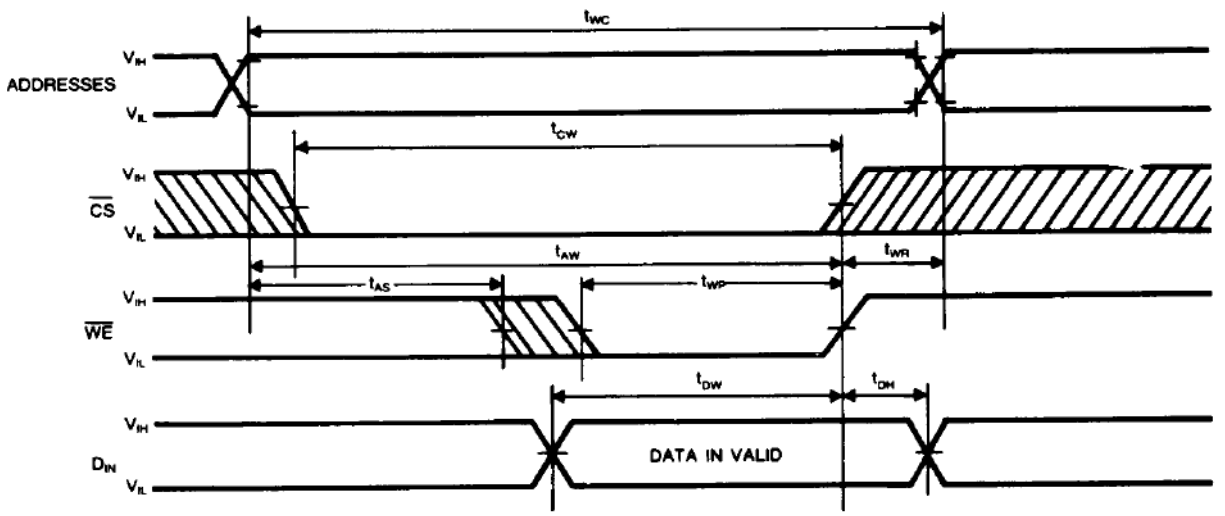


Notes :

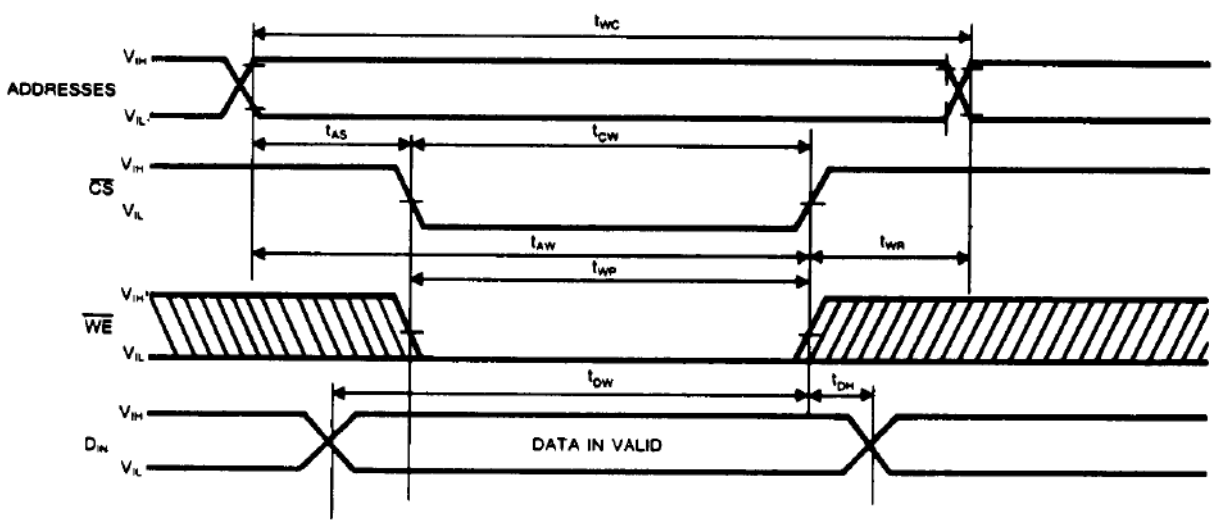
1. Device is continuously selected. $\overline{OE}$, $\overline{CS}$ = V_{IL}
2. Address valid prior to or coincident with $\overline{CE}$ transition low.
3. $\overline{WE}$ is high for read cycle.

Timing Waveforms

Write Cycle 1 ($\overline{WE}$ Controlled) (Note 1, 2)



Write Cycle 2 ($\overline{CS}$ Controlled) (Note 1, 2, 3)



Notes :

1. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. Data I/O is high impedence if $\overline{OE}$ = V_{IH}
3. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ High, the output remains in a high impedance state.

Capacitance

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNIT
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V		6	pF
C_{OUT}	Output Capacitance			8	

Notes : Tested on a sample basis

Data Retention Characteristics : (T_A = 0°~ 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
V_{DH}	Data Retention Supply Voltage	2.0	5.5	V	$\overline{CS} \geq V_{CC}$ -0.2V
I_{DDS3}	Data Retention Current GM76C256	-	50	µA	V_{CC} = 3.0V $\overline{CS} \geq$ 2.8V
	Data Retention Current GM76C256L/LL	-	20		
t_{CDR}	Chip Deselection to Data Retention Mode	0	-	ns	
t_R	Recovery Time	t_{RC}*	-	ns	

Note * : Read Cycle Time

Note ** : If the V_{IH} of $\overline{CS}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{CC} voltage is going down from 4.5V to 2.2V